UCC24612 High-Frequency Multi-Mode Synchronous Rectifier Controller

1 Features

- Secondary-Side Controller Optimized for up to 24-V Systems
- Supporting Active Clamp Fyback, QR, DCM, CCM Flyback and LLC Resonant converter
- High Side or Low Side Synchronous Rectifier
- Up to 1-MHz Operating Frequency
- MOSFET V_{DS} Sensing
- 4-A Sink, 1-A Source Gate-Drive Capability
- Proportion drive for fast turn off at CCM operation
- CCM cycle limit pre-turn off for better CCM support
- Adaptive minimum off time for better noise immunity
- Automatic Light-Load Management
- Synchronous Wake-Up From Sleep and Light-Load Modes
- 16-ns Typical Turnoff Propagation Delay
- 9.5-V Gate Drive Clamp Levels for Minimum Driving Loss

2 Applications

- AC-to-DC Adapters
- Server, Telecom Auxiliary Power Supply
- Telecom DC-to-DC bricks

3 Description

This UCC24612 multi-mode synchronous rectifier controller is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for secondary-side synchronous rectification in high current and high efficiency designs.

The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well, due to compounding of efficiency gains.

Using drain-to-source voltage sensing, the UCC24612 is ideal for Active Clamp Flyback, QR/DCM/CCM Flyback and LLC-resonant power supplies but can also be used with other power architectures. The proportion drive together with the CCM cycle limit pre-turn off design make part operate more robust in CCM operations. The wide VDD voltage range allow UCC24612 to support up to 24-V applications. The 9.5-V gate driver clamping level allows the minimum driving loss.

UCC24612 uses adaptive off time control to improve the noise immunity. This greatly simplifies the design effort and allows the controller be used in wide application and frequency ranges.

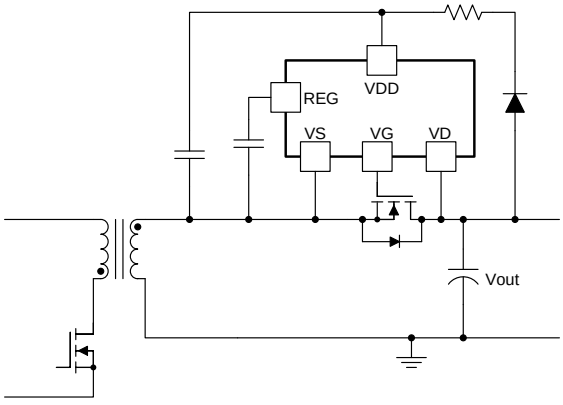
This device is available with SOT23-5 package.

Device Information(1)

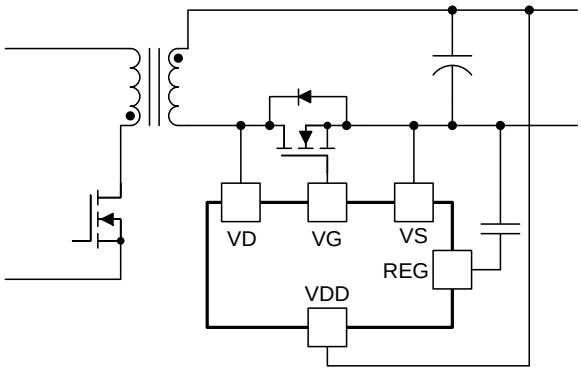
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC24612	SOT23 (5)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Flyback with High-Side SR



Flyback with Low-Side SR



ADVANCE INFORMATION

Table of Contents

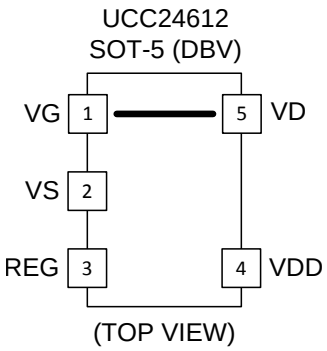
ADVANCE INFORMATION

4 Revision History

DATE	REVISION	NOTES
August 2017	*	Advance Information release.

5 Pin Configuration and Functions

5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REG	3	O	REG is the device's bias pin. An internal linear regulator from VDD to REG generates a well regulated 9.5-V voltage for better bypassing. It is recommend to put 2.2-µF bypass capacitor from REG pin to VS pin.
VD	5	I	MOSFET drain voltage sensing input. Connect this pin to SR MOSFET drain pin. The layout should avoid the VD pin trace sharing the power path to minimize the impacts of parasitic inductor.
VDD	4	I	Internal linear regulator input. Connect this pin to the output voltage when in low side SR configuration. Use R-C-D circuit to generate bias voltage from SR MOSFET drain when using high side SR configuration.
VG	1	O	VG (controlled MOSFET gate drive), connect VG to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The GATE output can achieve >1.5-A peak source current when High and >4-A peak sink current when connected with a large N-channel power MOSFET.
VS	2	-	VS is the internal ground of the UCC24612. It is also used to sense the voltage drop across SR. The layout should avoid the VS pin trace sharing the power path to minimize the impacts of parasitic inductor.

Table 1. Device Comparison

Part Number	Turn on propagation delay	Best suitable Topologies
UCC24612-1	70 ns	CCM/DCM/QR Flyback, Active Clamp Flyback with GaN MOSFET
UCC24612-2	160 ns	LLC, Active Clamp Flyback with Si MOSFET

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	VDD	–0.3	30	V
	VD	–0.7	230	V
	VG	–0.3	V_{REG}	V
	VD for I_{VD} ≤ –10 mA	–1.0	230	V
	REG		12	V
Output current, peak	VG(3) pulsed, t_{PULSE} ≤ 4 ms, duty cycle ≤ 1%		±4	A
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltages more negative than indicated may exist on any listed pin without excess stress or damage to the device if the pin's input current magnitude is limited to less than -10mA.
(3) In normal use, VG is connected to the gate of a power MOSFET through a small resistor. When used this way, VG current is limited by the UCC24612 and no absolute maximum output current considerations are required. The series resistor shall be selected to minimize overshoot and ringing due to series inductance of the VG output and power-MOSFET gate-drive loop. Continuous VG current is subject to the maximum operating junction temperature limitation.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, except pin 5 (1)	±2,000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pin 5 (1)	±1,500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	VDD input voltage	4		28	V
C_{VDD}	VDD bypass capacitor	1			µF
C_{REG}	REG bypass capacitor	1.5	2.2		µF
T_J	Junction temperature	–40		125	°C
f_S	Switching frequency			1000	kHz

6.4 Thermal Information

THERMAL METRIC(1)		UCC24612 DBV (SOT23-5) 5 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *the Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

ADVANCE INFORMATION

6.5 Electrical Characteristics

At VDD = 12 V_{DC}, C_{VG} = 0 pF, C_{REG} = 2.2 µF, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to VS, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
$IVDD_{START}$	VDD current, REG undervoltage	VDD = 4 V, VD = 0 V		120		µA
$IVDD_{RUN}$	VDD current, run	VDD = 12 V		0.95		mA
		VDD = 5 V		0.9		mA
$IVDD_{STBY}$	VDD current, standby mode	VDD = 12 V		390		µA
		VDD = 5 V		320		µA
UNDERVOLTAGE LOCKOUT (UVLO)						
$VREG_{ON}$	REG turnon threshold	Turnon detected by		4.5		V
$VREG_{OFF}$	REG turnoff threshold	Turnoff detected by		4		V
$VREG_{HYST}$	UVLO hysteresis	$VREG_{HYST}$ = $VREG_{ON}$ – $VREG_{OFF}$		0.5		V
MOSFET VOLTAGE SENSING						
V_{THVGON}	GATE turnon threshold	VD falling		-226		mV
$V_{THVGOFF}$	GATE turnoff threshold	VD rising		-10		mV
$V_{THREGLO}$	Low level regulation threshold			-50		mV
$V_{THREGCCM}$	High level regulation threshold for CCM			-150		mV
V_{THARM}	Gate re-arming threshold			0.5		V
I_{VDBIAS}	VD pin bias current	VD = –100 mV		-0.9		µA
GATE DRIVER						
R_{SOURCE}	VG pullup resistance	I_{VG} = –20 mA, VDD = 12 V		5.7		Ω
R_{SINK}	VG pulldown resistance	I_{VG} = 100 mA, VDD = 12 V		0.62		Ω
VG_H	VG clamp level			9.4		V
VG_L	VG output low voltage	I_{VG} = 100 mA, VDD = 12 V		60		mV
V_{OLGUV}	VG output low voltage in UVLO	I_{VG} = 25 mA, VDD = 4 V			0.7	V
IVG_{PU}	Gate driver maximum source current			1		A
IVG_{PD}	Gate driver maximum sink current			4		A
REG SUPPLY						
V_{REG}	REG pin regulation level	VDD = 12 V		9.42		V
$VREG_{LG}$	Load regulation on REG	VDD = 12 V, I_{LOAD_REG}= 10 mA to 0 mA		0.015		V
$VREG_{DO}$	REG drop out on passthrough mode	VDD = 5 V, I_{LOAD_REG}= 10 mA		0.28		V
$IREG_{SC}$	REG short circuit current	VDD = 12 V, VREG = 0 V		5.2		mA
$IREG_{LIM}$	REG current limit	VDD = 12 V, VREG = 8V		42		mA

ADVANCE INFORMATION

6.6 Timing Requirements

At VDD = 12 V_{DC}, C_{VG} = 0 pF, C_{REG} = 2.2 µF, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to VS, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MOSFET VOLTAGE SENSING						
td_{VGON}	Gate turn on propagation delay -1 version	VD moves from 4.7 V to –0.3 V in 5 ns		70		ns
	Gate turn on propagation delay -2 verison	VD moves from 4.7 V to –0.3 V in 5 ns		160		
td_{VGOFF}	Gate turn off propagation delay	VD moves from -0.3 V to 4.7 V in 5 ns		16		ns
MINIMUM ON-TIME						
$t_{ON(min)}$	Minimum SR conduction time	UCC24612 -1		383		ns
		UCC24612 -2		550		ns
Adaptive MINIMUM OFF-TIME						
$tOFF_{ABSMIN}$	Absolute minimum SR off blanking time			350		ns
GATE DRIVER						
t_{r_VG}	VG rise time	10% to 90%, VDD = 12 V, C_{VG} = 6.8 nF		35		ns
t_{f_VG}	VG fall time,	90% to 10%, VDD = 12 V, C_{VG} = 6.8 nF		18		ns
LIGHTLOAD / STANDBY						
t_{STBY_DET}	Standby mode detection time			4.4		ms
f_{SLEEP}	Average frequency entering standby mode			11		kHz
f_{WAKE}	Average frequency coming out of standby mode			14		kHz
PROTECTION						
T_{TSD}	Thermal shut down threshold			165		ºC
T_{HYS}	Thermal shut down recovery hysteresis			15		ºC

ADVANCE INFORMATION

6.7 Typical Characteristics

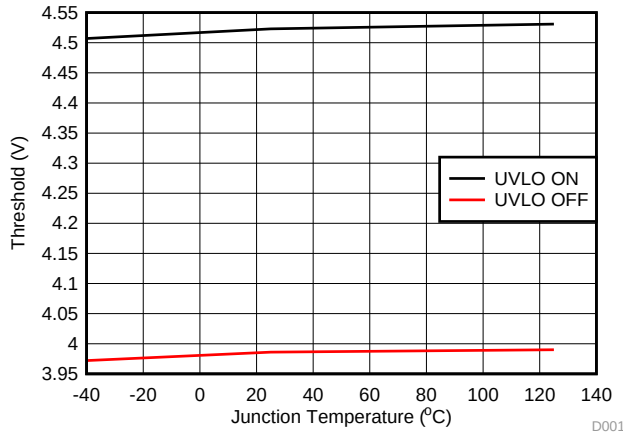


Figure 1. UVLO Threshold Voltage vs. Temperature

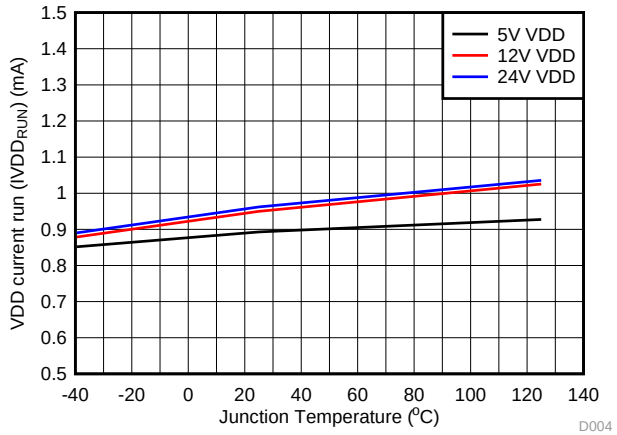


Figure 2. Bias Supply Current vs. Temperature

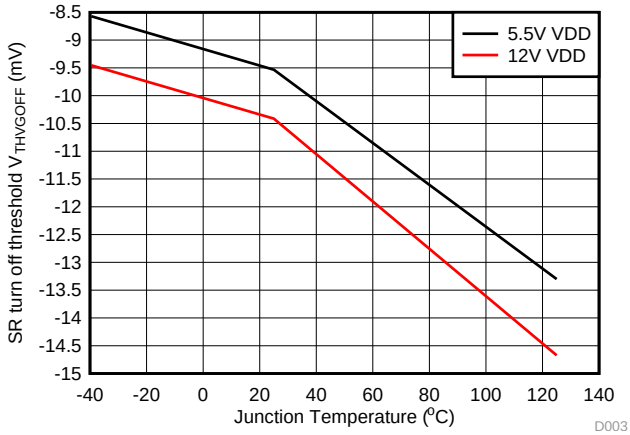


Figure 3. SR Turn Off Threshold Voltages vs. Temperature

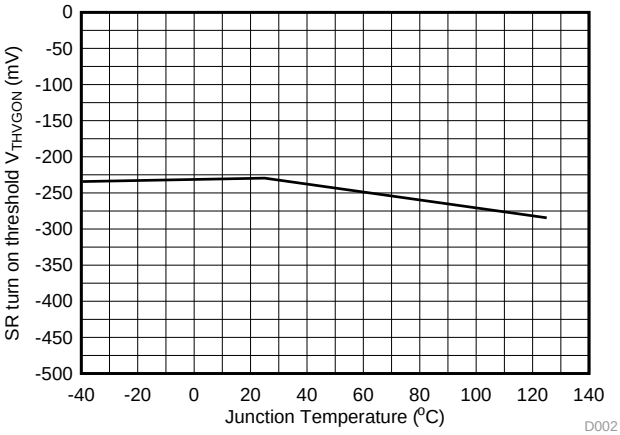


Figure 4. SR Turn On Threshold Voltage vs. Temperature

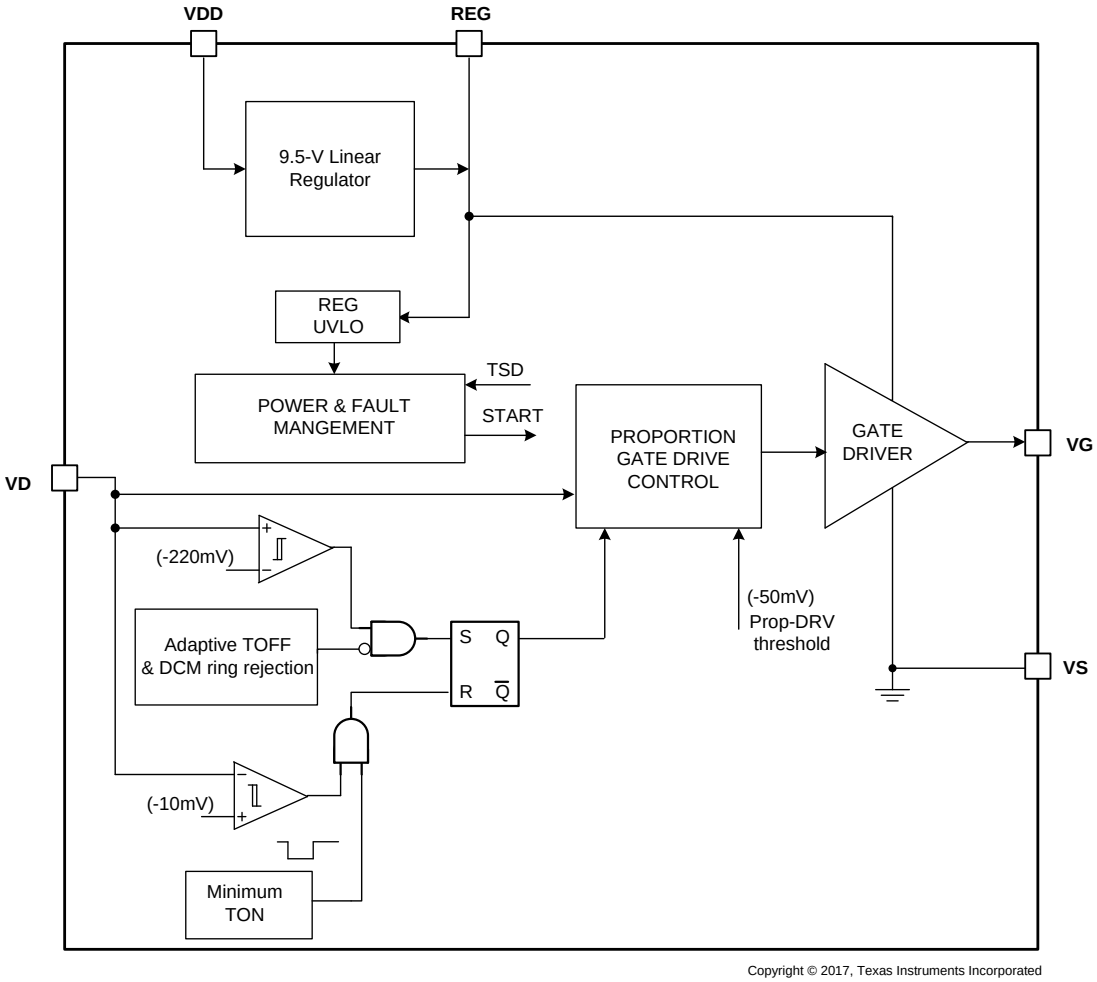
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The UCC24612 synchronous rectifier (SR) controller uses drain-to-source voltage sensing to determine the SR MOSFET conduction interval. The SR MOSFET is turned on when V_{DS} exceeds –200 mV, and is turned off when V_{DS} diminishes to –10 mV. The SR conduction voltage drop is continuously monitored and regulated to minimize the conduction loss while allowing SR to pre-turn off to operate in CCM mode. The extremely fast turn off comparator and driving circuit allows the fast turn off of SR MOSFET, even in CCM condition. Fixed 350-ns minimum on time allows the controller effectively driving the SR operating up to 1-MHz switching frequency. The adaptive minimum off time control simplifies the design, making the controller suitable to be used in wide applications and switching frequencies, while immune to the noises caused by the parasitic ringing. To minimize the standby power, automatic light-load mode disables the GATE pulses when the average switching frequency of the converter becomes lower than 12 kHz. When the load increases such that the average switching frequency becomes above 15 kHz, the controller resumes normal SR operation. The wide VDD range and gate driver clamp makes the controller ideal for wide output voltage range such as USB-PD applications.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Power Management

The UCC24612 synchronous-rectifier (SR) controller is powered from REG pin through the internal linear regulator between VDD pin and REG pin. This configuration allows optimal design the gate driver stage to achieve fast driving speed, low driving loss and higher noise immunity.

In low side configuration, as shown in Figure 5, the UCC24612 is powered from the output voltage directly.

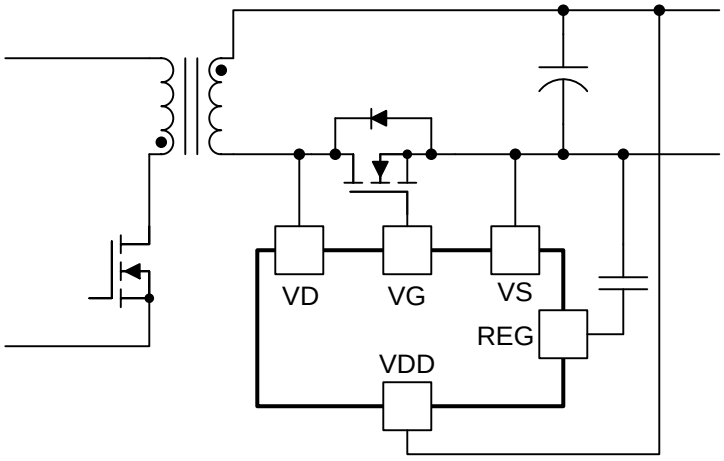


Figure 5. UCC24612 Used in Low Side SR Configuration

During start up, the output voltage rises from 0 V. With the rising of output voltage, the internal linear regulator operates in a passthrough mode, and the REG pin voltage rises together with the output voltage. The UVLO function of UCC24612 monitors the voltage on REG pin instead of VDD pin. Before REG pin voltage becomes above UVLO on threshold, UCC24612 consumes the minimum current of $IVDD_{START}$. Once the REG voltage rises above the UVLO on threshold, the device starts to consume the full operating current and controls the on and off the SR MOSFETs.

When VDD voltage is above ~9.5 V, the internal linear regulator operates in regulator mode. The REG pin is well regulated at 9.5 V. This allows the optimal driving voltage for the SR MOSFET without increasing the gate driver loss. The internal regulator is rated at 10 mA of load regulation capability for higher switching frequency operation. It is required to have sufficient bypass capacitor on REG pin to ensure stable operation of the linear regulator. A 2.2 µF bypass capacitor is recommended.

When VDD voltage is below 9.5 V, the internal linear regulator operates in passthrough mode. Depending on the load current, the regulator has a voltage drop approximately 0.2 V. The UCC24612 continue operates during this mode until the REG pin voltage drops below UVLO turn off level.

A typical time diagram of VDD and REG pin voltage can be found in Figure 6

ADVANCE INFORMATION

Feature Description (continued)

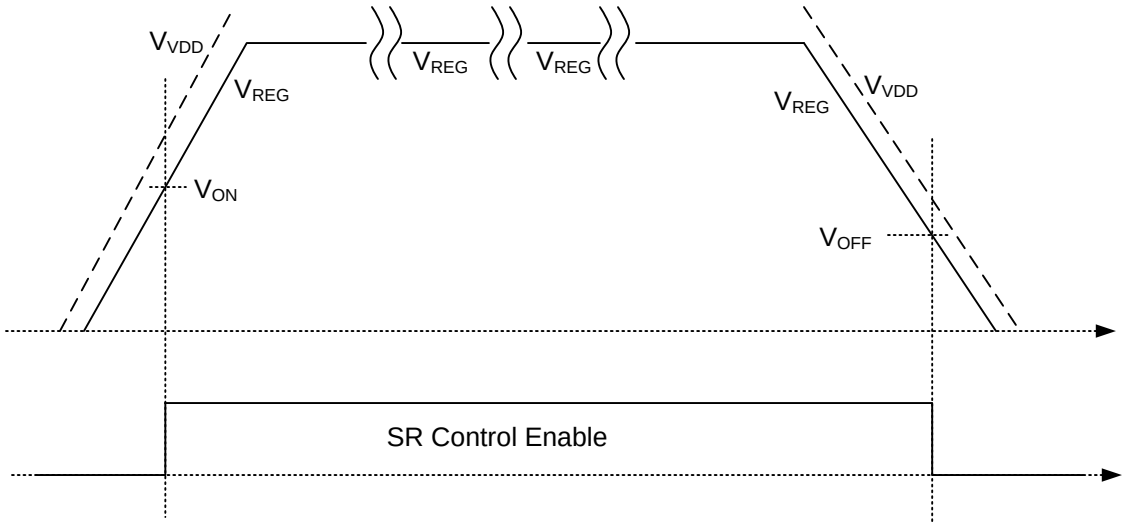


Figure 6. Timing diagram for VDD and REG at low side SR configuration

In some applications, such as USB chargers, the converter is required to deliver the full output current when the output is over loaded and output voltage drops below the regulation level. In 5-V applications, the output voltage could drop too low and not enough to turn on the SR. In this case, the UCC24612 can be power from VDD through a simple external R-C-D circuit. Due to the wide voltage range handling capability, this simple circuit provides the power through SR drain voltage. Even though this method easily powers up the device, this is a very inefficient way of powering up the controller. Other more efficient way would be using the auxiliary winding that able to provide the power during this mode.

Not only during output over load condition, the same powering method can also have to maintain the SR controller operation at high side SR configuration, as shown in Figure 7

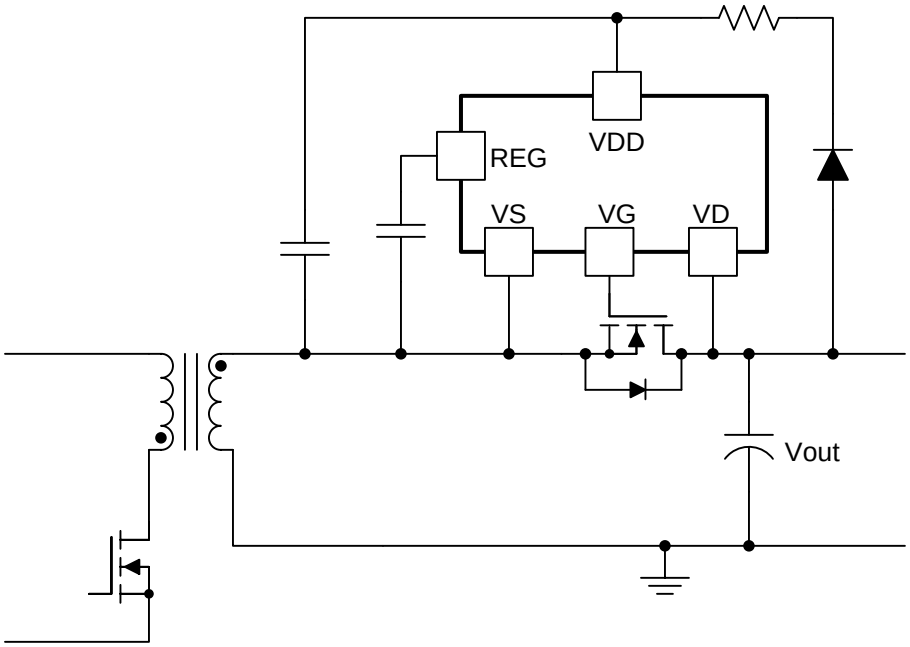


Figure 7. UCC24612 Used in High Side SR Configuration

ADVANCE INFORMATION

Feature Description (continued)

7.3.2 Synchronous Rectifier Control

The UCC24612 SR controller determines the conduction time of the SR-MOSFET by comparing the drain-to-source voltage of the MOSFET against a turnon threshold and a turnoff threshold. The GATE output is driven high when V_{DS} of the MOSFET exceeds Vth_{VGON} and is driven low when V_{DS} decreases below Vth_{VGOFF} as illustrated in Figure 8.

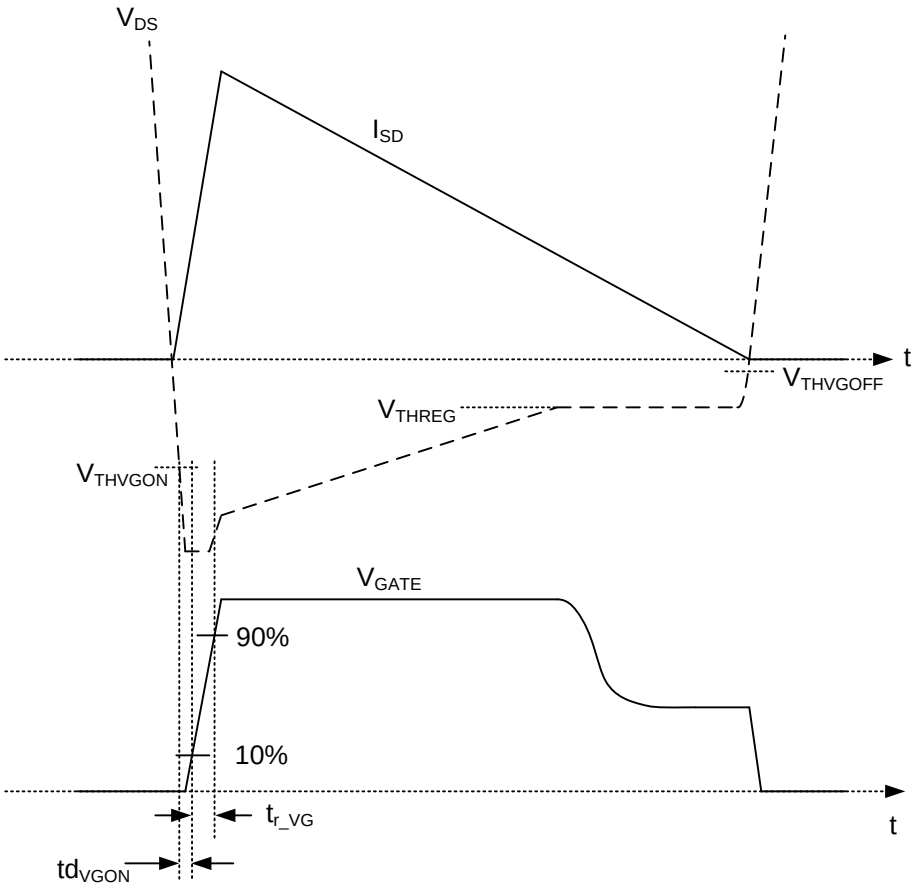


Figure 8. GATE Output With Respect to V_{DS}

NOTE

Because of finite propagation and rise times, the body diode of the SR-MOSFET may conduct briefly after Vth_{VGON} has been exceeded. A waveform similar to that of V_{DS} depicted in Figure 8 can be observed during SR operation in a simple Flyback circuit.

It should be noticed that before SR turns on, there is a small delay caused by the internal comparator delay and the gate driver delay. During the delay time, SR MOSFET body diode is conducting. For Flyback converter, the SR current is at its maximum value during this delay time. It is desired to have the minimum delay. The gate driver design should avoid long turn on delay.

For certain applications, this delay is essential for appropriate operation. In Active Clamp Flyback, especially when the primary side switches are using Si based super junction MOSFET, due to the large nonlinear junction capacitor, the SR often sees a leading spike current, follow by the real conduction current. Normally, a prolonged minimum on time can override this spike to make the circuit operate normally. However, this causes large negative current that transfer the energy from output to the input and reduces the overall converter efficiency. In

Feature Description (continued)

UCC24612, two different versions are created. UCC24612-1, the SR driver with inherent short turn on propagation delay (70 ns typical) can be used with the converter needs shorter delay, such as standard Flyback converter or Active Clamp Flyback covnerter using GaN MOSFET as main switches. UCC24612-2, the SR driver with added 150-ns turn on delay, to further ignore the leading edge spike, can be used with Active Clamp Flyback with Si based super junction MOSFET as the main switch or the LLC covnerters.

When SR body diode is conducting, VD pin becomes negative to VS pin, by a body diode drop. The connection of VD and VS pin should be directly to the SR MOSFET pins, to avoid any overlapping of sensing paths to the power path, minimizing the negative voltage and ringing caused by the parasitic inductors. Low package inductance MOSFETs are preferred to minimize this effect.

Besides the simple comparator, UCC24612 also includes a proportional driver for the SR. For normal SR controller, the SR MOSFET is turn on and off by the full driving voltage. This way, the conduction loss can be minimized. However, this method has couple major drawbacks. The turn off threshold is a fixed value, often, to prevent shoot through, the SR is turned off before current reaches zero. This causes the SR body diode conduction and actually increases the conduction loss. Another issue is associated with the converter operate in continuous conduction mode (CCM) condition. When Flyback converter operates in CCM, the SR current slope (di/dt) at turn off could be as high as 150A/µs. This high current slope could cause large negative current with long propagation delays. Furthermore, the delay caused by discharging SR MOSFET gate voltage to full voltage to its threshold level introduces another delay, this further increases the negative current.

Instead of always turning off the SR MOSFET in full gate driver voltage, UCC24612 reduces its gate driver voltage when the voltage drop across SR drain to source becoming more than -50mV (current approaching zero). During this time, UCC24612 reduces its gate drive voltage and tries to regulate SR voltage drop to -50mV. This brings two major benefits to the application: a) Preventing the SR premature turning off, which causes extra loss associated with body diode conduction and reverse recovery b) Shorter turn off delay since the SR MOSFET gate is already reduced close to threshold level and SR can be turned off with virtually no delay from moving gate voltage.

In certain applications, such as telecom DC/DC bricks, due to the lower input and output voltage, the converter operate in deep CCM mode (low inductor ripple) gives the benefit of less conduction loss. In these applications, the SR turn off current is high and the SR MOFET voltage drop can still be less than the -50-mV threshold. UCC24612 increases -50-mV threshold to -150 mV to force the proportion drive activated and reducing the gate driver voltage for fast turn off. The time to increase the threshold is based on previous cycle SR conduction time. Because the regular proportion drive and the turn off mechanism are kept functional all the time, the UCC24612 can still provide correct SR control even the large SR conduction time change with two switching cycles. The forced proportion drive mechanism can be shown in Figure 9. In Figure 9, the turn on delay was ignored to simplify the illustration.

ADVANCE INFORMATION

Feature Description (continued)

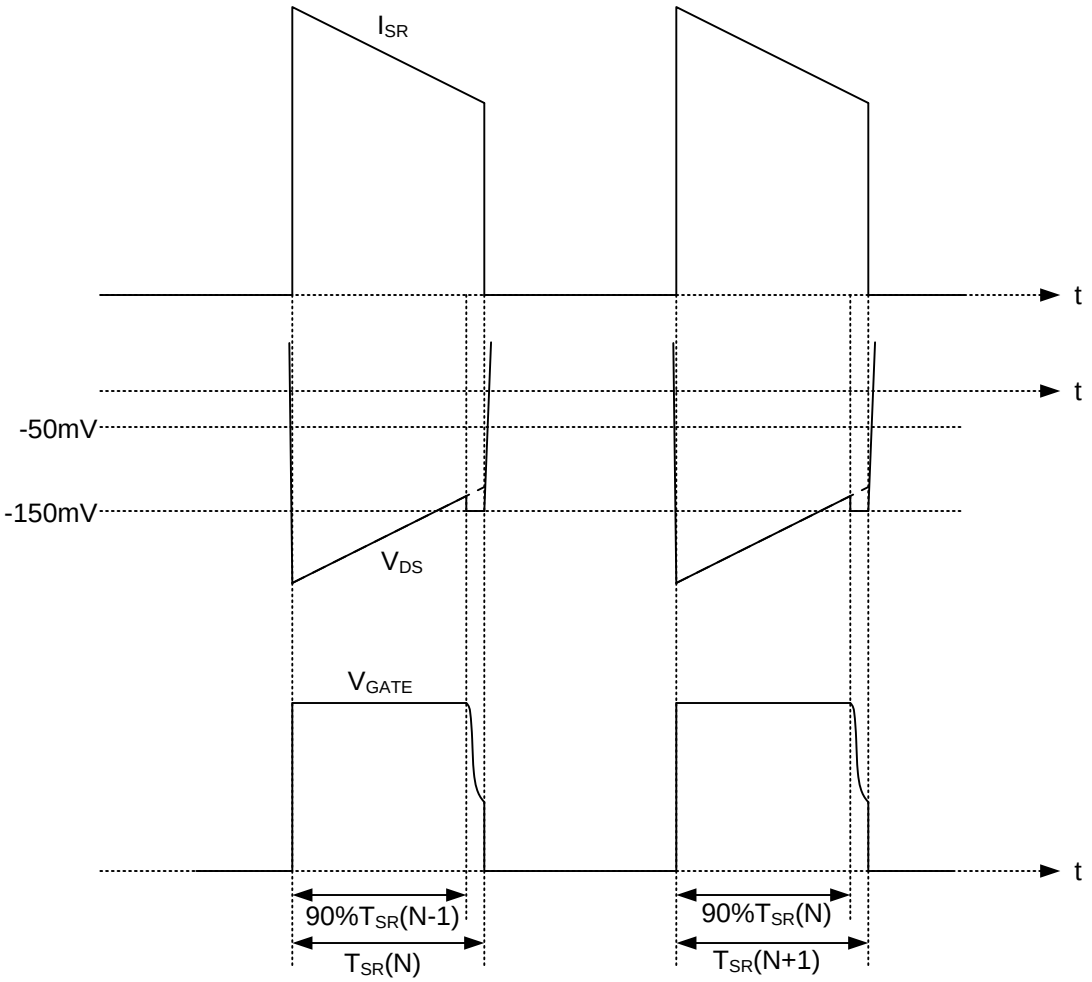


Figure 9. Forced Proportion Drive for Deep CCM Operation

For Flyback converters, the SR current starts from its maximum current and keep reducing. Proportion drive is always enabled at the later part of the SR conduction period. However, for other topologies such as LLC or active clamp Flyback, the SR current start from lower amplitude and then increase to higher amplitude. To prevent the proportion drive gets enabled at beginning of the conduction period, proportion drive is disabled for the first 50% of SR conduction time, based on the previous cycle's SR condition time. This way, the proportion drive is always enabled on the current down slope and minimizes the impact to the conduction loss.

ADVANCE INFORMATION

Feature Description (continued)

7.3.3 Adaptive Blanking Time

In actual power converters, the voltage across SR is often noisy, caused by the parasitic ringing. This parasitic ringing is often associated with the SR turning on and off. Blanking time is used to deal with the parasitic ringing to prevent SR false turn on and off.Figure 10 shows more realistic waveforms and the internal control timing which accommodates them.

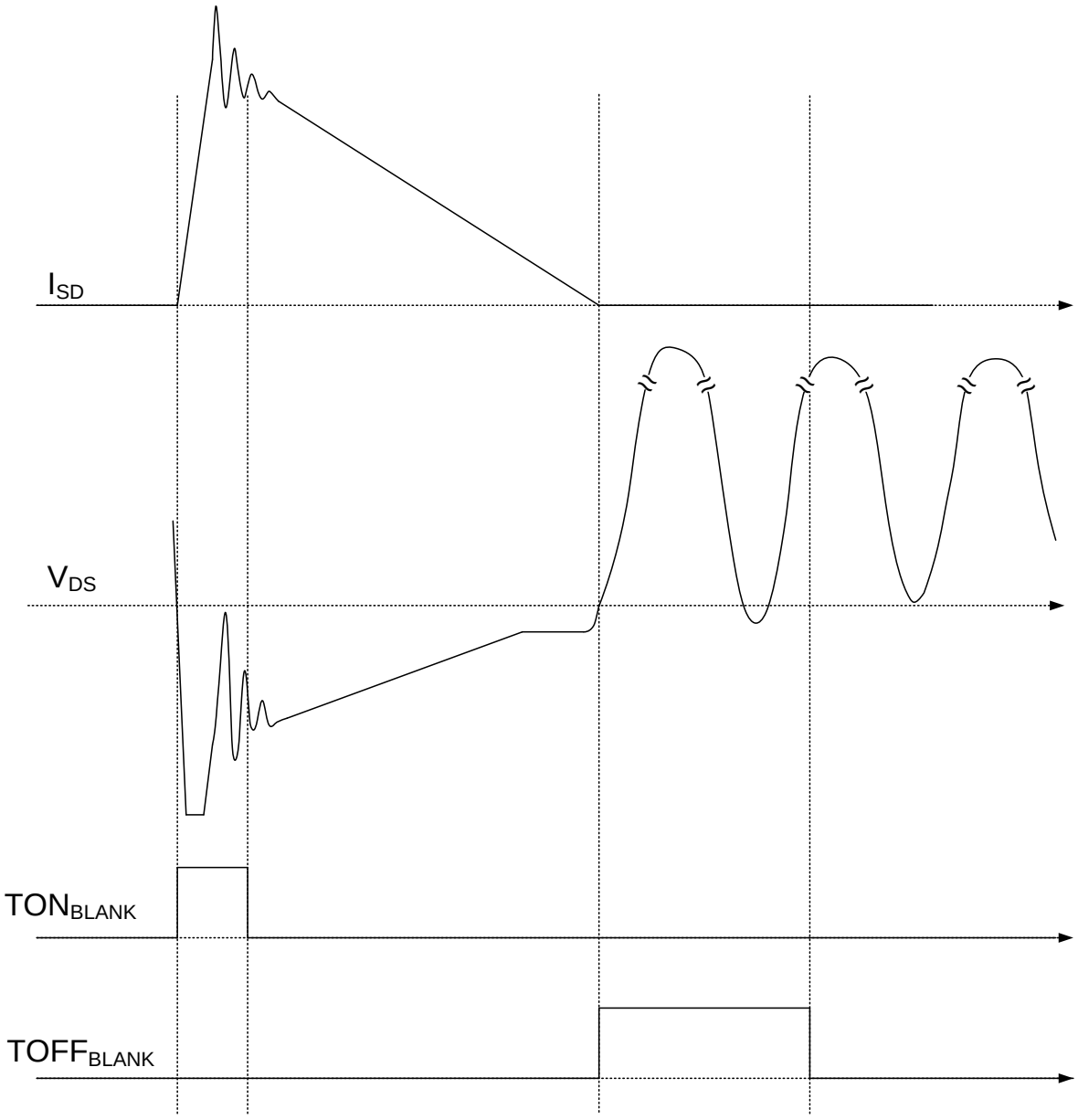


Figure 10. Parasitic Ringing Associated with DCM Operation

Feature Description (continued)

7.3.3.1 On Blanking Timer

Right after SR turn on, the SR is driven fully on. For some topologies, such as Flyback, the SR starts to conduct its maximum current. Due to the parasitic ringing, SR voltage drop might still trip the turn off threshold and prematurely turn off the SR. This is largely caused by the ringing current caused the voltage drop on the package inductor of the SR FET. The ringing voltage can be managed through appropriate snubbering and using low package inductance MOSFET. To further improve the noise immunity, UCC24612 blanks the turn off comparator with a fixed 350-ns minimum on time timer. The SR needs to conduct a minimum of 350 ns regardless its turn off comparator state. The minimum on time allows the UCC24612 used in up to 1 MHz switching frequency, while still maintain the good noise immunity.

7.3.3.2 Off Blanking Timer

When converter operate in discontinuous conduction mode (DCM), after SR turns off, there is large parasitic ringing caused by the inductor and the switch node capacitor. At first couple of ringing cycles, there is a good chance that the drain voltage resonant below the SR turn on threshold. SR could be false turned on at these instances and introduces extra loss and EMI noise.

Due to different switching frequency and power level designs, this parasitic ringing frequency can vary quite a bit. Traditionally, the DCM ringing is blanked by a programmable off blanking timer. It is often called minimum off time. This allows the maximum flexibility of the circuit design and avoid the false triggering. However, there are couple limitations associated with the method. Firstly, the program pin can force the device using higher pin count package, this increases the overall cost and difficulty of layout. Secondly, the fixed off blanking timer might not work well for the entire line and load conditions. For example, for a quasi-resonant (QR) Flyback, in the light load mode, it enters DCM operation. In this case, the off blanking timer like to be long to avoid the DCM ringing causing SR false turning on. However, at high input voltage, when the converter operates in the QR mode, the primary side MOSFET conduction time is quite short, the long minimum off time might cut into the conduction time of the SR, introduce extra conduction loss.

In UCC24612, instead of a fixed off blanking timer, adaptive off blanking timer is used to blank the parasitic ringing and avoid false turn on of the SR. The off blanking timer $TOFF_{blank}$is determined by three values, the absolute minimum off banking time of 350 ns ($tOFF_{ABSMIN}$), the recorded DCM ring cycle time t_{DCM} and previous cycle's SR off time t_{OFF}.

UCC24612 sets up the off blanking timer based on previous cycle's SR off time. By choose 70% of previous switching cycle's SR off time, the off blanking timer is maximized to prevent any false triggering.

However, the off blanking timer minimum value is clamped by the 350-ns absolute minimum value and recorded DCM ringing cycle.

After SR turn off, if the off blanking time is not sufficient, the SR could be turned on again by a DCM ring. Because of the DCM ring, SR's conduction time is limited by the minimum on time. By looking at the SR conduction time, UCC24612 is able to determine the conduction is a real SR conduction or false turn on triggered by the DCM ring. Once the false turn on is captured, the time duration between SR turn off and the SR false turn on is recorded as the DCM ring cycle. For the next switching cycle, the off blanking timer is clamped to 2.2 times of the recorded DCM ring cycle. This adaptive off blanking timer allows UCC24612 achieving the noise immunity without a dedicated program pin.

Feature Description (continued)

For some conditions, such as mentioned earlier, the off blanking timer suitable for the DCM condition might be too long for the high line QR operation. In this case, the off blanking timer clamp needs to be reset to the correct value. UCC24612 continue monitors SR body diode conduction time during minimum off time. If the body diode conduction time is longer than the minimum on time, this means the minimum off time clamp setting is too long and needs to be reduced. UCC24612 reset the minimum off time clamping to allow full conduction of the SR. The adaptive minimum off time schemes are illustrated in Figure 11.

If for any reason the off blanking time expires after the SR body diode conduction, the SR turning on is skipped for the switching cycle. This is because when the SR conducts, it conducts with a minimum on time, if the blanking time expires at the end of the SR conduction time and converter operates in the CCM condition, there is a good chance to cause shoot through the endanger the converter.

The off blanking time also has a maximum value of 4.3 µs.

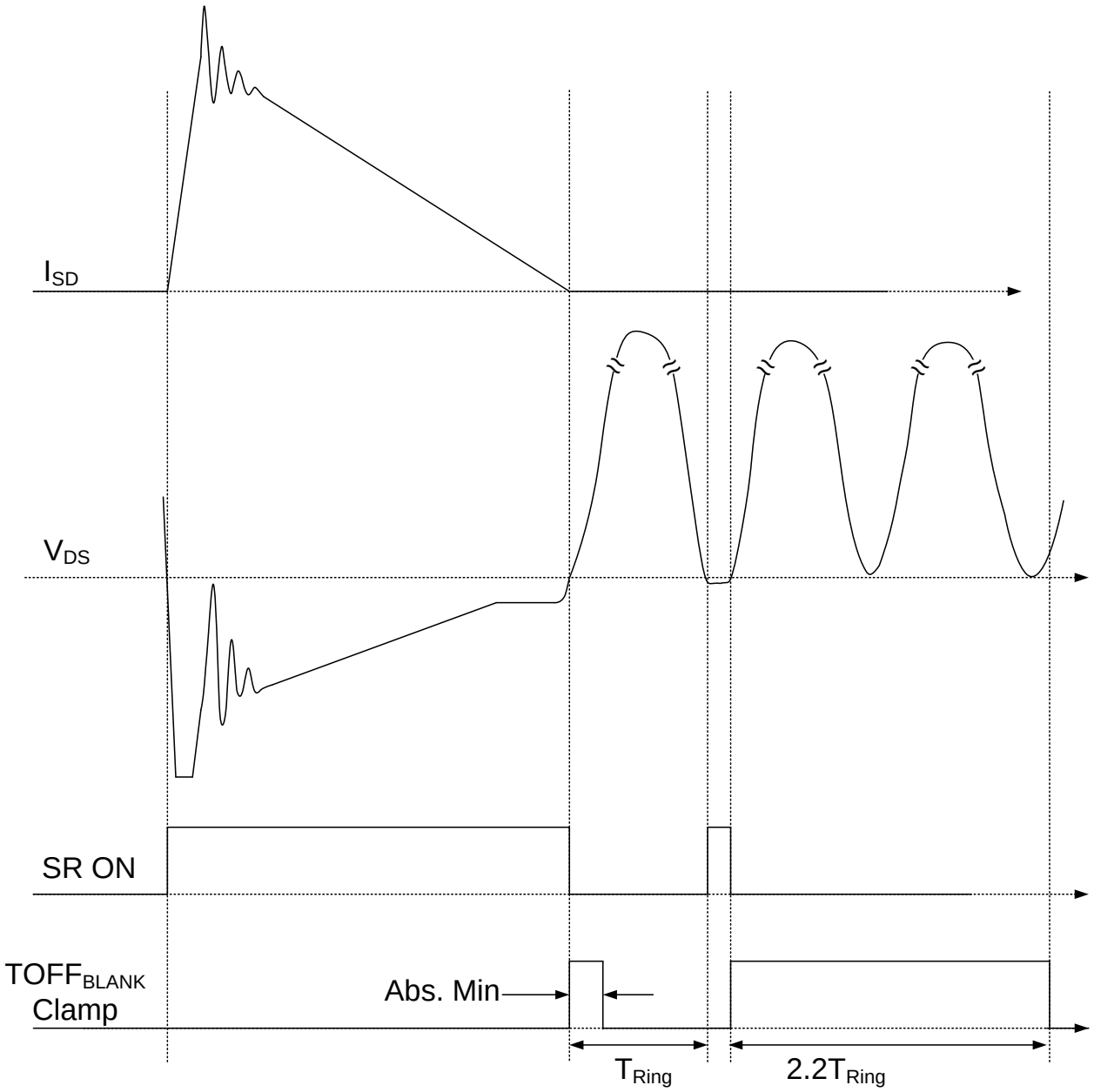


Figure 11. Adaptive Off-Time Blanking

ADVANCE INFORMATION

Feature Description (continued)

7.3.3.3 SR Turn ON Re-arm

The VG output may only turn on when the controller has been armed for the switching cycle. The controller is armed for each successive SR cycle only after $TOFF_{BLANK}$ expires after VD pin voltage rises 500 mV above VS pin.

7.3.4 Gate Voltage Clamping

With the wide VDD voltage range capability, UCC24612 clamps the gate driver voltage on a maximum level of 9.5 V to allow fast driving speed, low driving loss and compatible with different MOSFETs. The 9.5-V level is chosen to minimize the conduction loss for the non-logic level MOSFET.

The gate driver voltage clamp is achieved through the regulated REG pin voltage. When VDD voltage above 9.5 V, the linear regulator regulates the REG pin voltage to be 9.5 V, which is also the power supply of the gate driver stage. This way, the MOSFET gate is well clamped at 9.5 V, regardless how high the VDD voltage is. When the VDD voltage is getting close to or below the programmed REG pin regulation voltage, UCC24612 can no long regulate the REG pin voltage. Instead, it enters a passthrough mode that the REG pin voltage follows the VDD pin voltage. During this time, the gate driver voltage is lower than its programmed value but still provides the SR driving capability. The UCC24612 is disabled once the REG pin voltage drops below its UVLO level.

7.3.5 Standby Mode

With the more stringent industrial standard such as Department of Energy (DoE) level VI, the external power supplies are expected to maintain very low standby power at no load condition. It is essential for the SR controller entering the low power standby mode to help save the standby power.

During standby mode, the power converter loss allocation is quite different comparing with heavy load. At heavier load, both conduction loss and switching loss are quite high. However, at light load, the conduction loss becomes insignificant and switching loss dominates the loss. To help improve the standby power, modern power supply controllers often enters burst mode to save the switching loss. Furthermore, in each burst switching cycle, the energy delivered is maximized to minimize the number of switching cycle needed and further reduces the switching loss.

Traditionally, the SR controller monitors the SR conduction time to distinguish the normal operation mode or the standby mode. This criterion is no longer suitable for the modern power supply controller designed for delivering minimum standby power.

Instead, in UCC24612, a frequency based standby mode detection is used. UCC24612 continuously monitors the average switching frequency of the SR. Once average switching frequency of SR drops below 12 kHz, the UCC24612 enters the standby mode and reduces its current consumption to I_{STB}. During standby mode, the SR switching cycle is continuously monitored. Once the average switching frequency is more than 16 kHz within 4 ms, the SR operation is enabled again. UCC24612 ignores the first SR switching cycle after coming out of standby mode to make sure the SR isn't turned on in the middle of the switching cycle.

7.4 Device Functional Modes

7.4.1 UVLO Mode

UCC24612 uses REG pin voltage to detect UVLO instead of VDD pin voltage. When the REG voltage to the device has not yet reached the V_{TH_ON} threshold, or has fallen below the UVLO threshold V_{TH_OFF}, the device operates in the low-power UVLO mode. In this mode, most internal functions are disabled and ICC current is typically much less than 100 µA. If the REG pin is above 2 V, there is active pull down from VG to VS to prevent SR turning on by noise. When the REG pin voltage is less than 2 V, there is a weak pull down from VG to VS and this also prevents the noise turning on SR MOSFET. The device exits UVLO mode when REG increases above the V_{TH_ON} threshold.

7.4.2 Standby Mode

Standby mode is a low-power operating mode to help achieve low standby power for the entire power supply. UCC24612 detects the operation frequency of SR MOSFET and enters or exists the standby mode operation automatically. REG current reduces to I_{STB} level. During standby mode, majority of the SR control functions are disabled, except the switching frequency monitoring and the active pull down on the gate driver.

7.4.3 Run Mode

Run mode is the normal operating mode of the controller when not in UVLO mode, or standby mode. In this mode, REG current is higher because all internal control and timing functions are operating and the GATE output is driving the controlled MOSFET for synchronous rectification. REG current is the sum of I_{RUN} plus the average current necessary to drive the load on the VG output. The VG voltage is automatically adjusted based on the SR MOSFET drain to source voltage.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

UCC24612 synchronous rectifier controller is designed to control the SR MOSFET to replace lossy diode rectifier in various topologies, such as Active Clamp Flyback, Flyback operating in DCM, QR and CCM mode, as well as LLC resonant converter to improve the efficiency.

8.2 Typical Application

The following application information is applied to the UCC24612 Evaluation Module (EVM), which is used as a rectifier stage in a 20V, 60W DCM Flyback design. The controller used in this design was a UCC28740 secondary side regulated, variable-frequency flyback controller that had a maximum switching frequency of roughly 85 kHz. Please refer to the UCC28740 data sheet for further details.

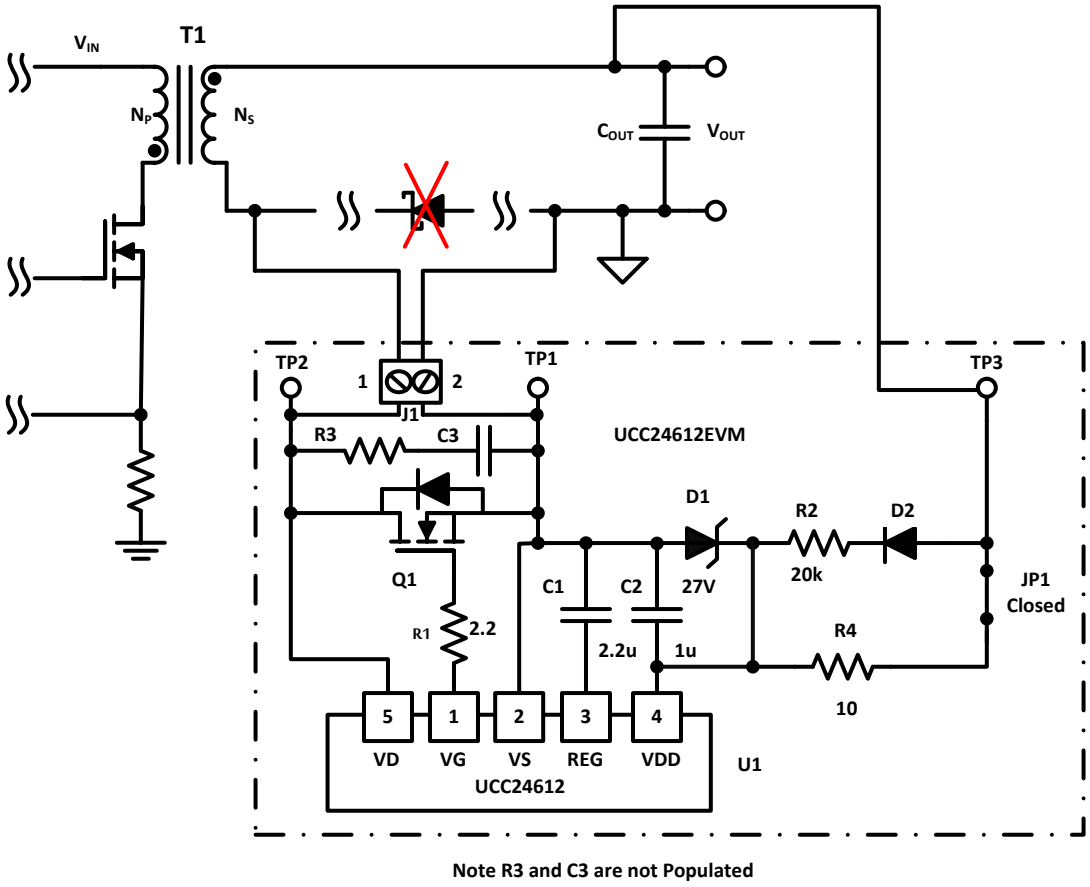


Figure 12. UCC24612 Typical Application Example

ADVANCE INFORMATION

Typical Application (continued)

8.2.1 Design Requirements

Table 2. 60W DCM Flyback Design Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		85		265	V_{RMS}
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage, average	V_{IN} = 85 V_{RMS} to 265 V_{RMS}, I_{OUT} = 0 A to 3 A	19	20	21	V
I_{OUT}	Output current	V_{IN} = 85 V_{RMS} to 265 V_{RMS}	0		3	A

ADVANCE INFORMATION

8.2.2 Detailed Design Procedure

8.2.2.1 SR MOSFET Selection

UCC24612 can be paired with the appropriate MOSFET to replace the diode rectifier on the existing designs and demonstrate the conduction loss reduction. The SR MOSFET selection should consider the tradeoff between the cost and performance. Lower on state resistance gives lower conduction loss, while it hurts the efficiency at light load. Due to the implementation of proportional gate drive, the benefit of lower on state resistance gets diminishing return. It is recommended to keep the proportional gate drive to kick in less than 50% of the full load SR conduction time.

The MOSFET breakdown voltage should be higher than the maximum voltage the SR MOSFET sees under maximum input voltage.

In this EVM, a 150-V, 19-mΩ MOSFET was used to get a balance between the cost and performance

8.2.2.2 Bypass Capacitor Selection

UCC24612 needs sufficient external bypass capacitor to allow internal regulator operate correctly. Referring to the power supply recommendation section, a 2.2-µF 15-V ceramic capacitor was chosen as the bypass capacitor on REG pin. For the VDD pin, it is normally powered by output voltage and there are plenty of capacitor there. A 0.1-µF ceramic capacitor is still recommended to be placed close to the IC to provide high frequency current.

8.2.2.3 Snubber design

It is required for the user to setup snubber components C3 and R3 to get the best performance when using the UCC24612EVM.

To setup these components will require knowing the flyback transformers secondary leakage inductance (Lslk) and measuring the secondary resonant ring frequency (fr) in circuit. It is recommended that the SR is not engaged while doing this. TP3 should be disconnected from the flyback converter to ensure FET Q1 is turned off while setting up the snubber.

The secondary winding capacitance (Cs) then needs to be calculated based on the following equation. Please note for a transformer with a secondary winding leakage inductance of 3.8 uH and a ring frequency of 2 MHz, the parasitic capacitance would be 1.7 nF.

$$Cs = \frac{1}{(2 \times \pi \times f_r)^2 \times Lslk} = \frac{1}{(2 \times \pi \times 2MHz)^2 \times 3.8uH} = 1.7nF \quad (1)$$

Based on the calculated Cs, Lslk and fr the snubber resistor R3 can be set to critically dampen the ringing on the secondary, which requires setting the Q of the circuit equal to 1.

$$R3 = \frac{1}{Q}\sqrt{\frac{Lslk}{Cs}} = \frac{1}{1}\sqrt{\frac{3.8uH}{1.7nF}} \approx 47\ ohm \quad (2)$$

Capacitor C3 is used to limit the time the snubber resistor is applied to the aux winding during the switching cycle. It is recommended to set the snubber capacitor C3 with the following equation based on the flyback converters switching frequency (fSW). For a flyback converter switching at 85 kHz in the example would require a C3 of roughly 497 pF.

$$C3 = \frac{0.01}{5 \times fsw \times R3} = \frac{0.01}{5 \times 85kHz \times 47.3ohm} \approx 497pF \quad (3)$$

Please note that the calculations for R3 and C3 are just starting points and should be adjusted based on individual preference, performance and efficiency requirements.

8.2.2.4 High-Side Operation

To use the UCC24612EVM to replace a high-side rectifier requires removing jumper JP1 and connecting the EVM as shown in Figure 13. Please note that the EVM comes with a default filtering resistor (R2) of 20 kΩ. However, resistor R2 needs to be adjusted based on your individual application.

ADVANCE INFORMATION

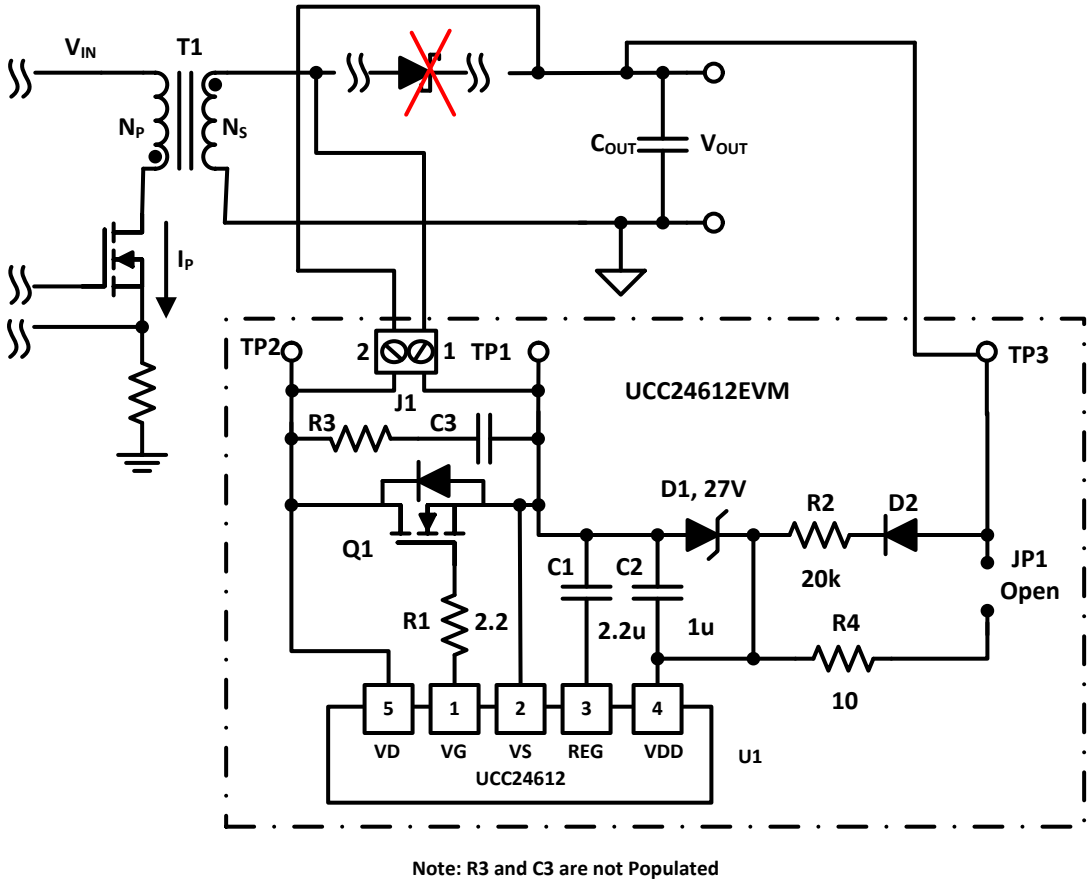


Figure 13. UCC24612-1EVM Used in High-Side Rectifier Application

If the magnitude of voltage across TP1 and TP2 is less than 28 V please remove R2 that is populated on the EVM (20 kΩ) and set R2 to 0 to 10 ohms and remove 27-V Zener diode D1 from the board.

If TP2 to TP1 is greater than 28 V use resistor R2 to setup an averaging filter to lower the DC voltage applied to VD.

The RC filter formed by C2 and R2 requires setting the filter pole frequency to a hundredth of the converter's maximum switching frequency. In this example the converter's maximum switching frequency (f_{SW}) was 85 kHz. Please note the switching frequency will vary based on design and preference.

$$R2 > \frac{1}{2\pi \times C1 \times \frac{f_{SW}}{100}} = \frac{1}{2\pi \times 1uF \times \frac{85kHz}{100}} \approx 187ohm \quad (4)$$

When the RC filter circuit is used, to engage the gate driver properly it is recommended that the VD voltage applied be between 4 V to 27 V to provide enough energy and voltage to the gate driver. This range can be determined in a fixed frequency flyback converter with the following equations. Variable D_{MAX} in the maximum duty cycle of the converter and D_{MIN} is the minimum duty cycle of the converter. Variable N_P is the flyback transformer's primary (T1) number of turns and N_S is the transformers secondary number of turns. Please refer to Figure 13 for details.

Maximum VDD voltage ($V_{VDD(MAX)}$):

$$V_{VDD(MAX)} = \left(V_{OUT} + V_{IN(MAX)} \times \frac{N_S}{N_P}\right) \times D_{MAX} = \left(20V + 375V \times \frac{1}{13}\right) \times 0.5 = 24.4V \quad (5)$$

Minimum VDD voltage ($V_{VDD(MIN)}$):

$$V_{VDD(MIN)} = \left(V_{OUT} + V_{IN(MIN)} \times \frac{N_S}{N_P}\right) \times D_{MIN} = \left(20V + 72V \times \frac{1}{13}\right) \times 0.36 = 9.2V \quad (6)$$

ADVANCE INFORMATION

8.2.3 Application Curves

The UCC24612EVM was used in a synchronous rectifier in both a high side and low side application in an offline (VIN = 85 V to 265 V RMS), 20-V (VOUT), 60-W application. The controller used in this design was a UCC28740 secondary side regulated, variable-frequency flyback controller that had a maximum switching frequency of roughly 85 kHz. Please refer to the UCC28740 data sheet for further details.

8.2.3.1 Steady State Testing Low Side

- Snubber Components, R2 = 1.02 kΩ, R3 = 51.1Ω , C3 = 470 pF
- CH1 = VG, CH2 = Q1 drain (TP2), CH3 = VOUT Voltage Ripple (TP3)

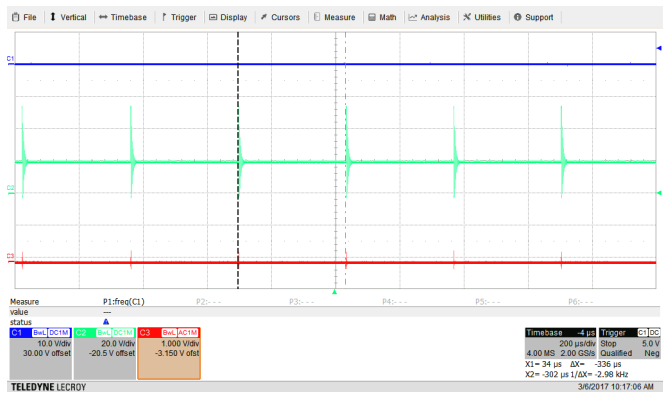


Figure 14. 85-V_{AC}, 0-A Load

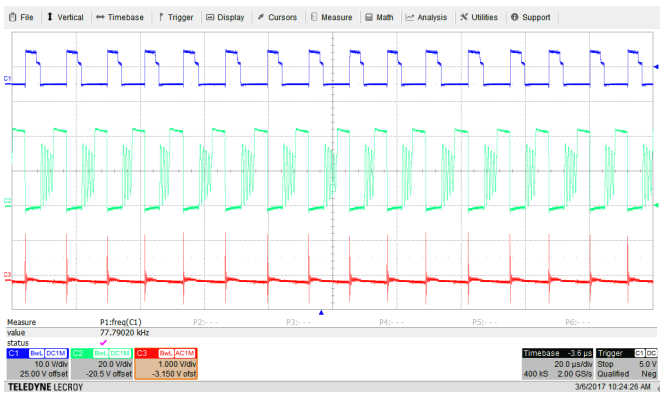


Figure 15. 85-V_{AC}, 3-A Load

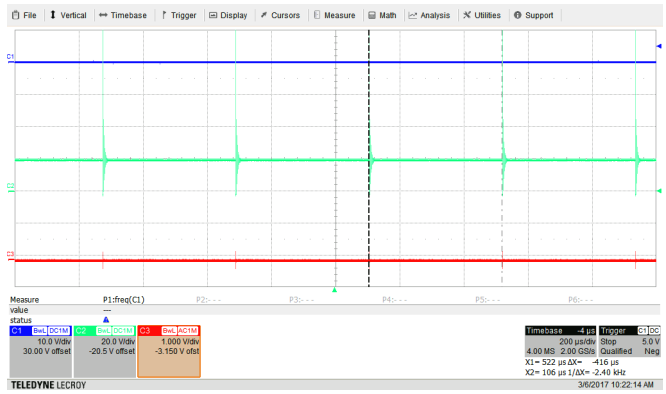


Figure 16. 265-V_{AC}, 0-A Load

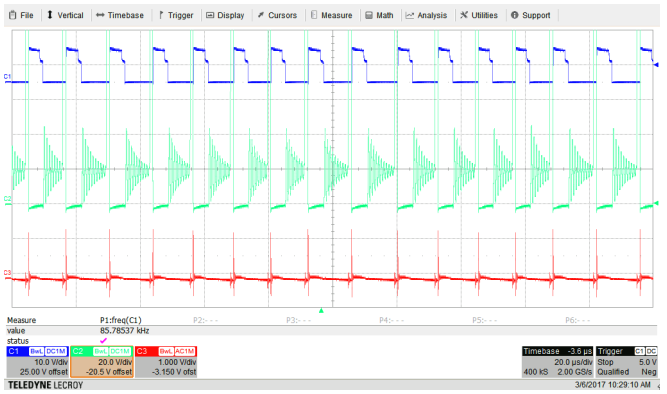


Figure 17. 265-V_{AC}, 3-A Load

8.2.3.2 Steady State Testing High Side

- Snubber Components, R2 = 1.02 kΩ, R3 = 51.1 Ω , C3 = 470 pF
- CH1 = VG, CH2 = Q1 drain (TP2), CH3 = VOUT Voltage Ripple (TP3)

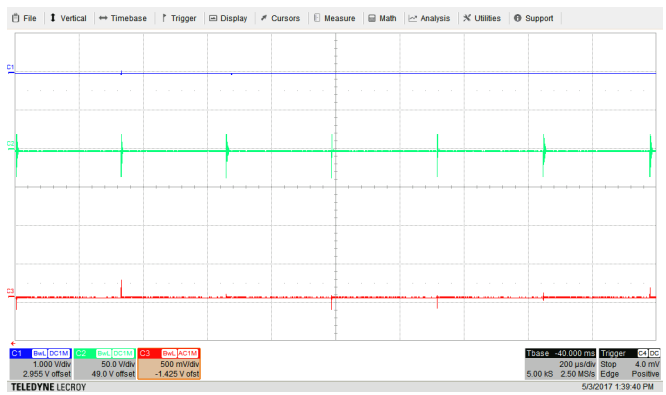


Figure 18. 85-V_{AC}, 0-A Load

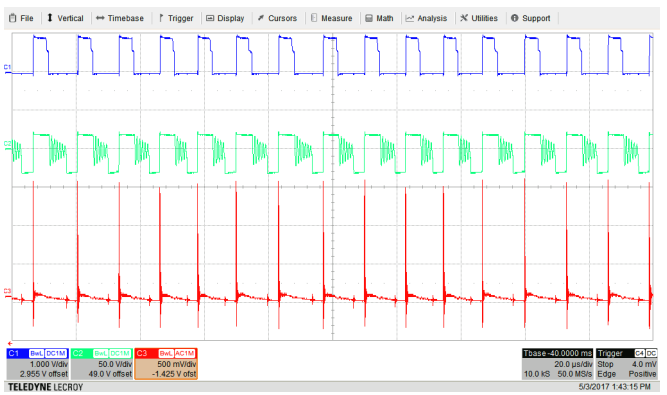


Figure 19. 85-V_{AC}, 3-A Load

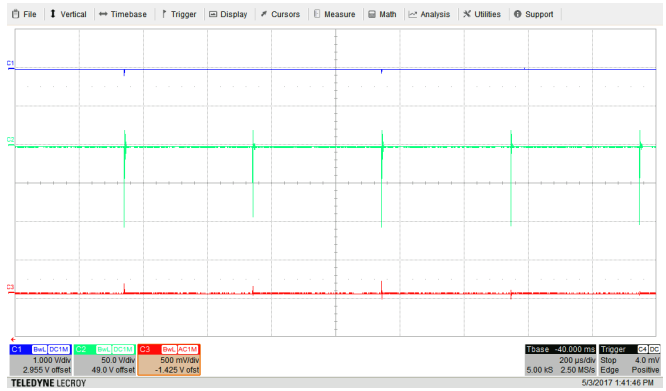


Figure 20. 265-V_{AC}. 0-A Load

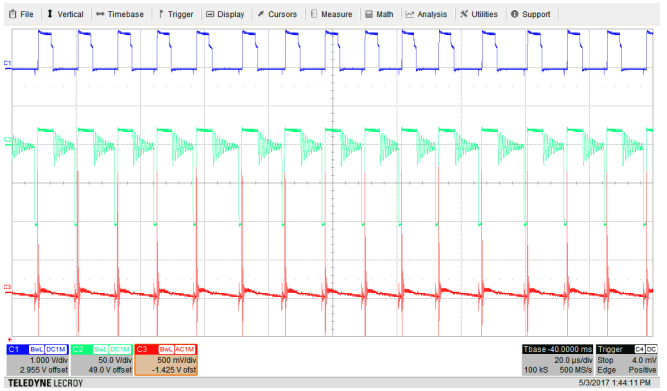


Figure 21. 265-V_{AC}, 3-A Load

ADVANCE INFORMATION

9 Power Supply Recommendations

UCC24612 internal circuits are powered from REG pin only. There is an internal LDO between VDD pin and REG pin to provide a well regulated REG pin voltage when VDD voltage is above 9.5 V. This allows the device to have better bypassing and better gate driver performance.

It is important to keep the sufficient bypass cap on REG pin. A minimum of 1-µF bypass capacitor is required. When the gate charge current is higher than 5mA, it is required to have at least 2.2-µF bypass capacitor on REG pin.

VDD pin is the main power source of the device. The voltage on VDD pin should be kept between 4.5 V and 28 V for normal operation. Referring to the electric spec table for the tolerances on the REG pin UVLO and OFF levels.

When UCC24612 is used in low side SR application, VDD can be directly tied to the output voltage, if the output voltage is between 5 V to 24 V.

When the UCC24612 is used in high side SR configuration, VDD can be powered through three different ways, according to the trade off between cost, and performance.

a. Power the device through secondary side auxiliary winding
b. Power the device through simple R-C filter
c. Power the device through depletion mode FET

By using the secondary side auxiliary winding, UCC24612 is equivalently powered by the output voltage because of the transformer coupling effect. This provides the best efficiency solution. However, this solution is often limited by the transformer construction and cost constrains.

The UCC24612 can be powered by using a diode and RC filter on VDD pin. This allows the device to get power from SR drain voltage. Due to the wide range of VD voltage variation (for example, VD voltage is the sum of reflected input voltage and output voltage in Flyback converter), this might or might not work for some applications. However, this provides a simple and low cost solution.

A more universal solution without changing the transformer is to provide the VDD through SR drain using a diode and depletion mode MOSFET. This allows a well regulated VDD voltage through out the entire operation range of the converter. Even though it still hurts the efficiency because the device is powered up from a high voltage source, this provides a simple solution without changing the transformer design.

The three different configurations are summarized in Figure 22, Figure 23 and Figure 24

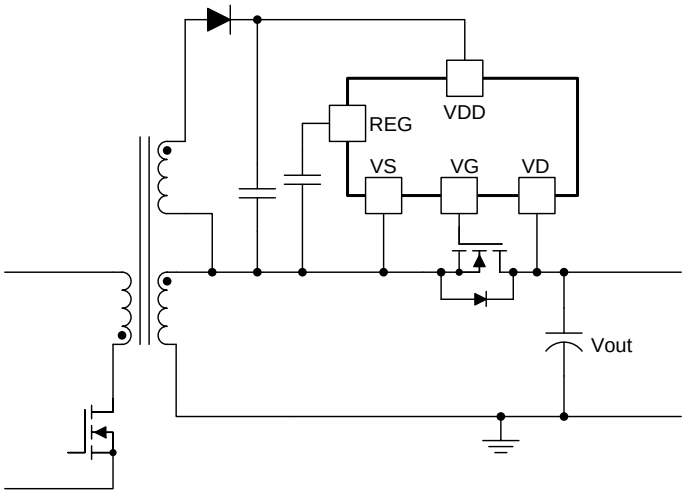


Figure 22. Power UCC24612 Using Auxiliary Winding

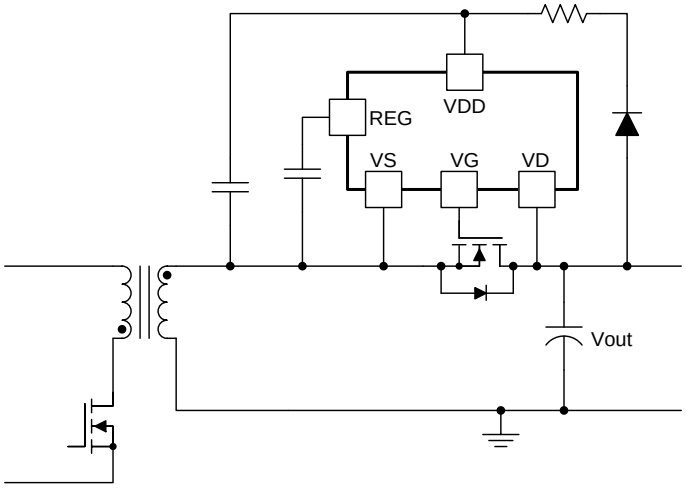


Figure 23. Power UCC24612 Using R-C-D

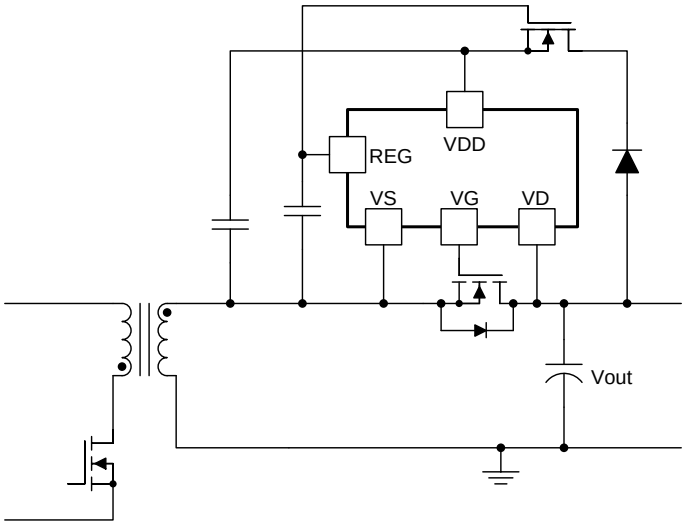


Figure 24. Powering UCC24612 Using Depletion Mode MOSFET

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

The printed circuit board (PCB) requires conscientious layout to minimize current loop areas and track lengths, especially when using single-sided PCBs.

- Place a ceramic MLCC bypass capacitor as close as possible to VCC and GND.
- Avoid connecting VD and VS sense points at locations where stray inductance is added to the SR MOSFET package inductance, as this will tend to turn off the SR prematurely.
- Run a track from the VD pin directly to the MOSFET drain pad to avoid sensing voltage across the stray inductance in the SR drain current path.
- Run a track from the VS pin directly to the MOSFET source pad to avoid sensing voltage across the stray inductance in the SR source current path. Because this trace shares both the gate driver path and the MOSFET voltage sensing path, it is recommended to make this trace as short as possible.
- Run parallel tracks from GATE and GND to the SR MOSFET. Include a series gate resistance to dampen ringing.

10.2 Layout Example

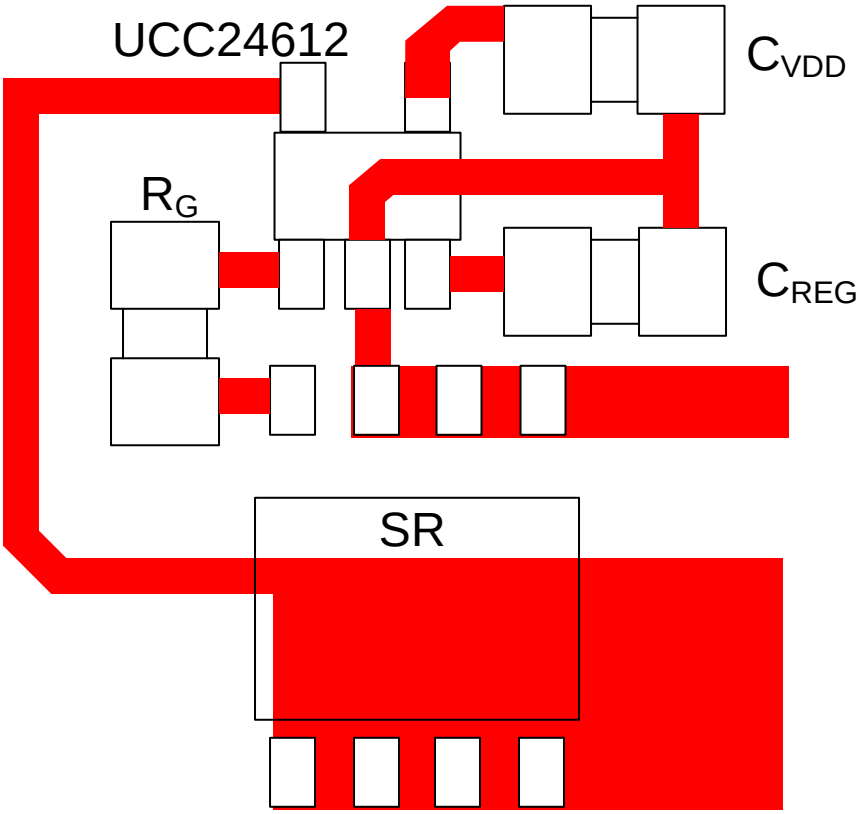


Figure 25. PCB Layout for Driving an SR with SO-8 Package

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
UCC24612DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650
UCC24612DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	U650

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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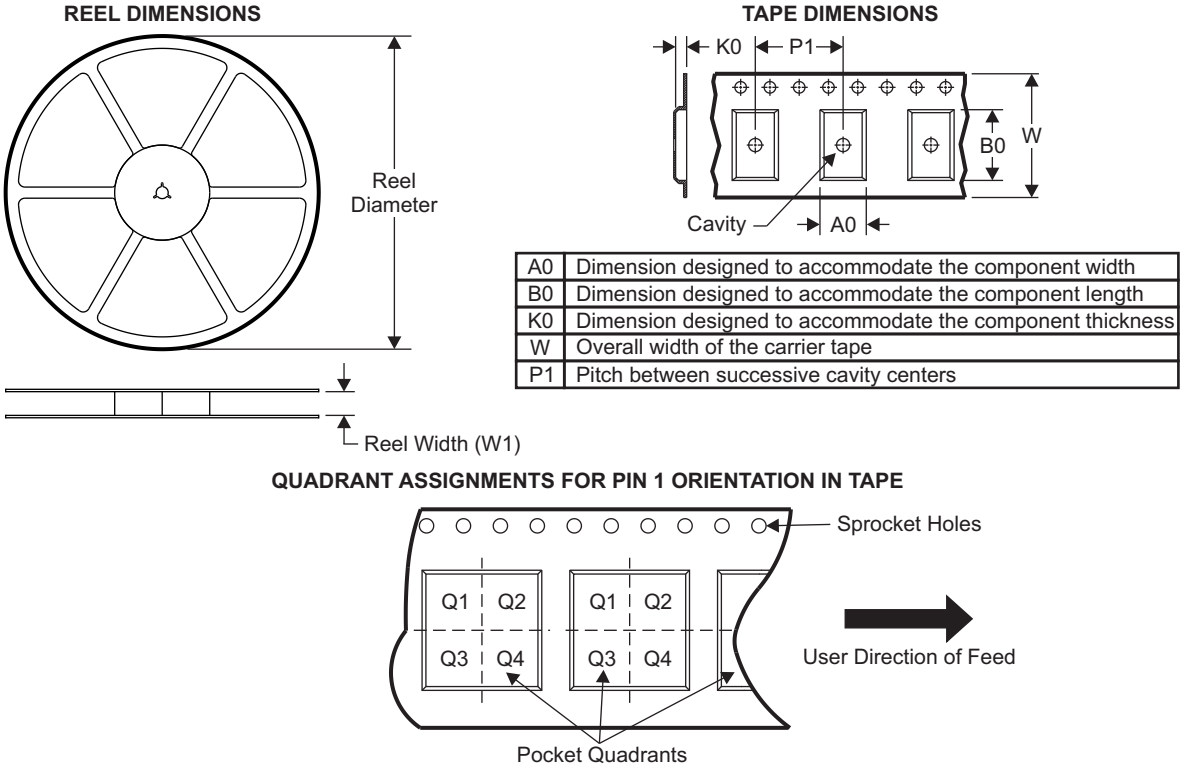
ADVANCE INFORMATION

12.1.2 Tape and Reel Information

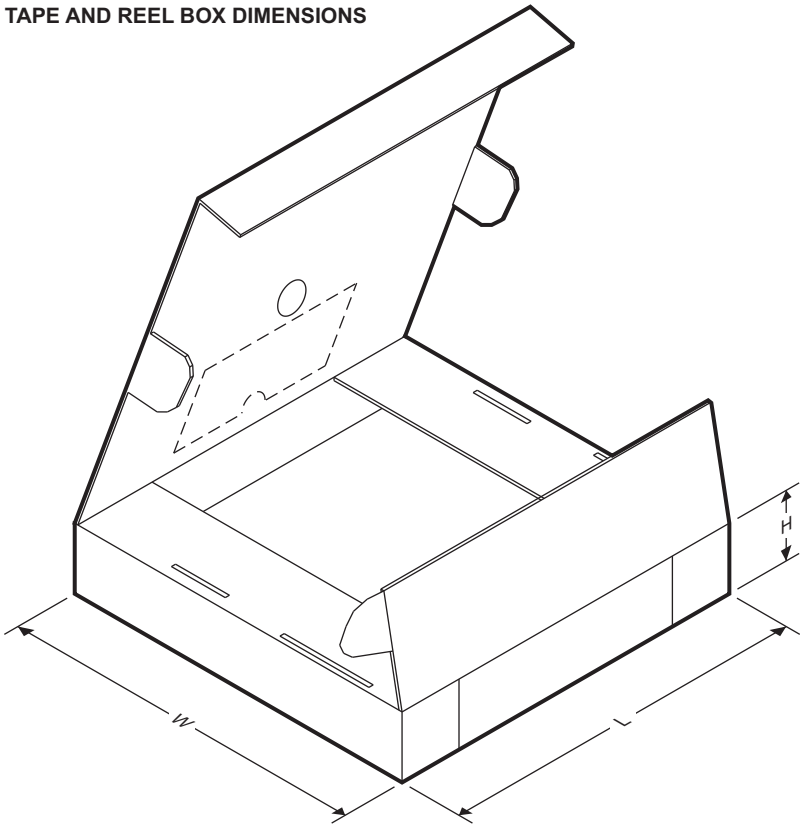


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC24612DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC24612DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS

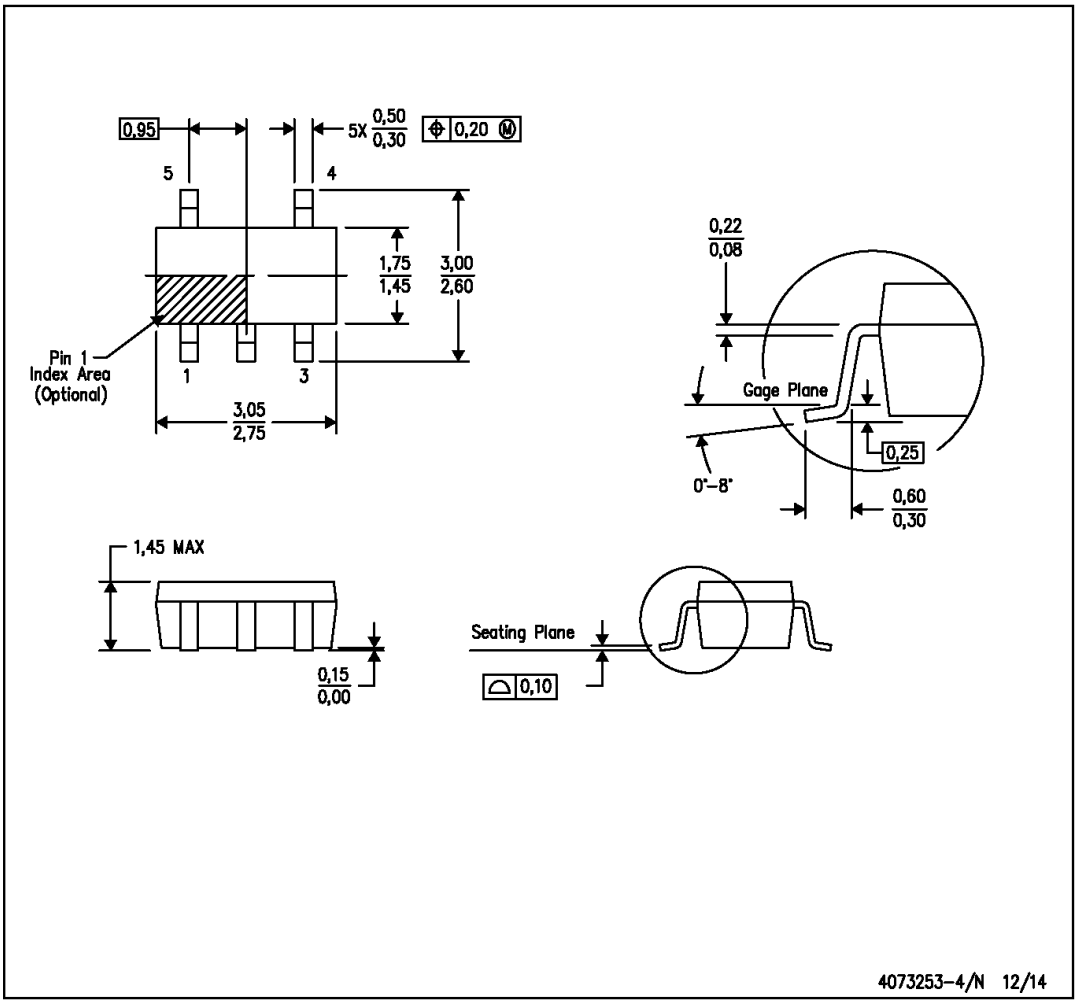


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC24612DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
UCC24612DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

ADVANCE INFORMATION

MECHANICAL DATA

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

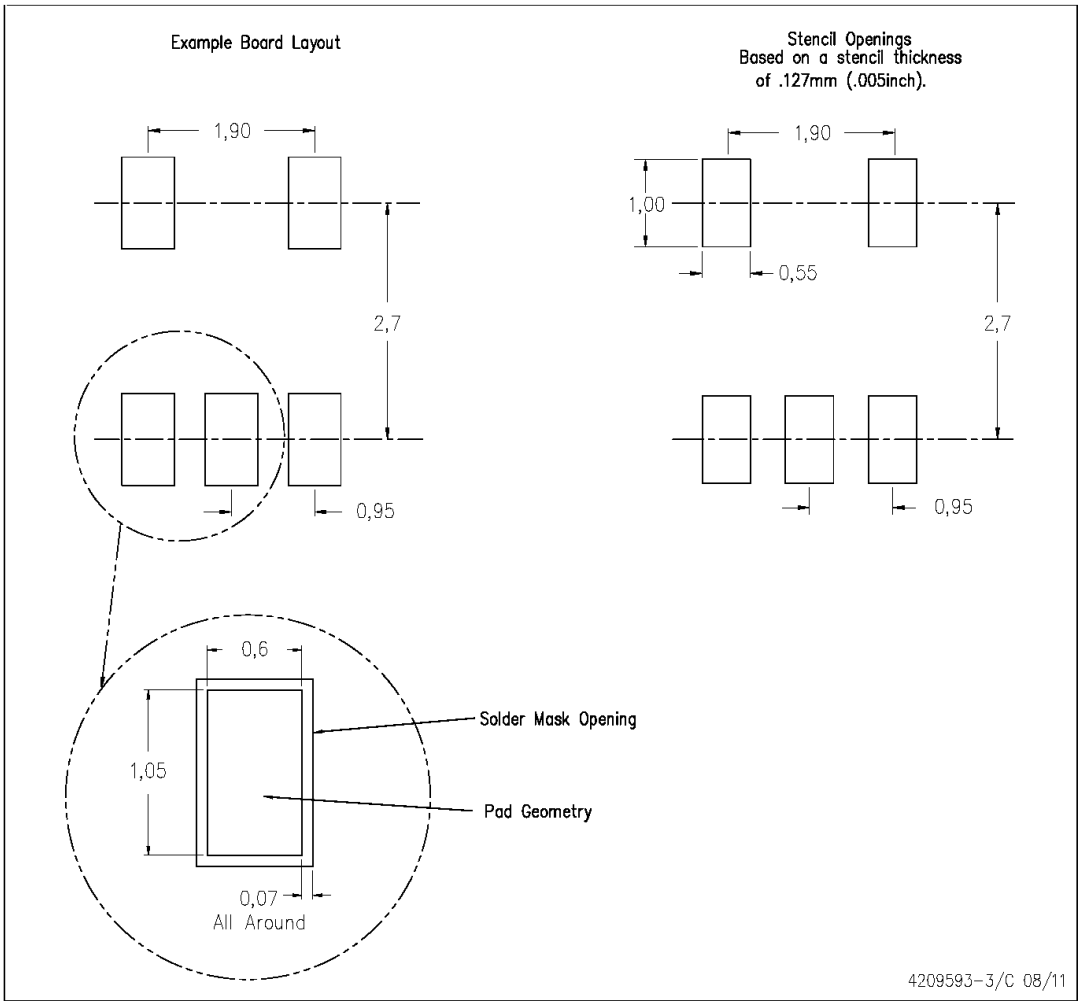


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

ADVANCE INFORMATION

LAND PATTERN DATA

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUC24612-1DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PUC24612-2DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
UCC24612-1DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
UCC24612-1DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
UCC24612-2DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
UCC24612-2DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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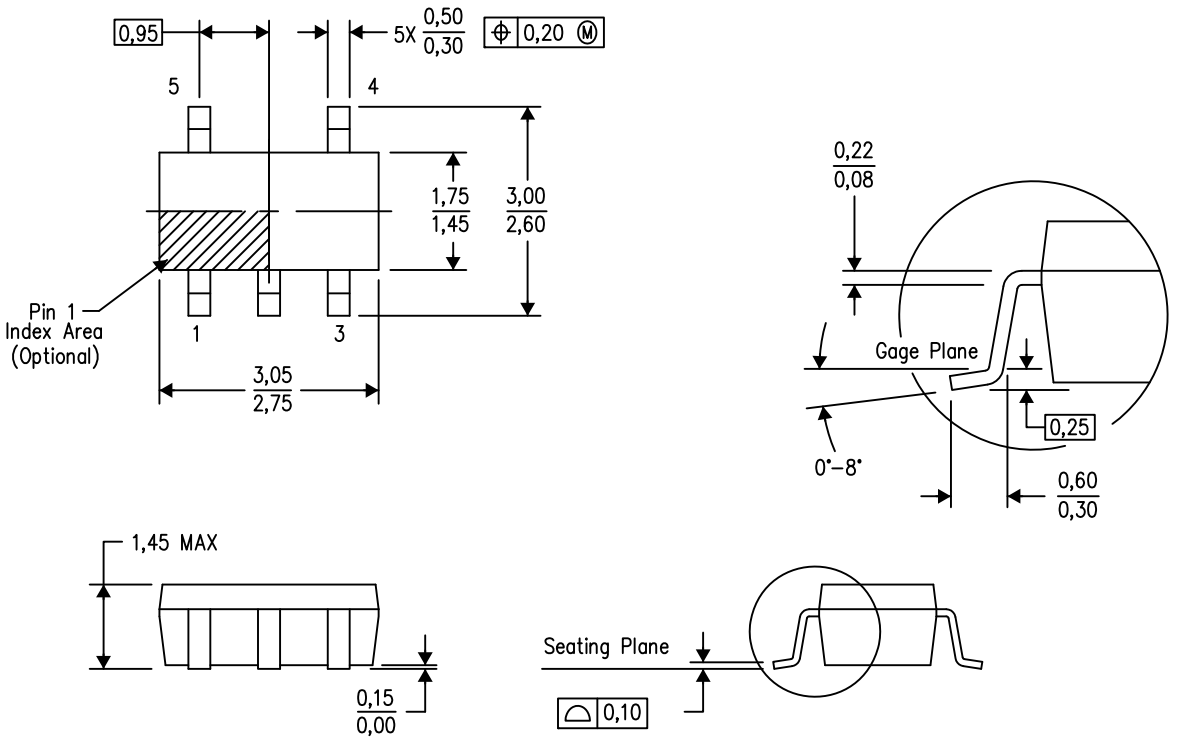
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

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