

**CONTROL CIRCUIT FOR FAST SWITCHING TRANSISTORS**

- DIRECT DRIVE OF THE SWITCHING TRANSISTOR
- SELF REGULATED POSITIVE BASE CURRENT (1 A max)
- NEGATIVE BASE CURRENT ENSURING FAST TURN-OFF (3 A max)
- THE OUTPUT CURRENT CAN BE INCREASED BY MEANS OF ONE (or more) EXTERNAL TRANSISTOR(S)
- MINIMUM CONDUCTING TIME (or no conduction) TO ALLOW THE DISCHARGE OF A RDC NETWORK
- PROTECTION AGAINST SATURATION FAILURE OF THE POWER TRANSISTOR DURING CONDUCTING PERIOD, WITH ADJUSTABLE DETECTION THRESHOLD
- INSTANTANEOUS-COLLECTOR CURRENT LIMITATION
- POSITIVE SUPPLY ( $V_{CC}$ ) MONITORING
- NEGATIVE SUPPLY MONITORING WITH ADJUSTABLE THRESHOLD

- ON-CHIP THERMAL PROTECTION
- PROGRAMMABLE MAXIMUM ON TIME
- TTL AND CMOS COMPATIBLE INPUT
- CAN BE DRIVEN WITH ALTERNATE PULSES
- ADJUSTABLE DELAY BETWEEN THE RISING EDGE OF THE INPUT SIGNAL AND THE BEGINNING OF THE POSITIVE BASE DRIVE

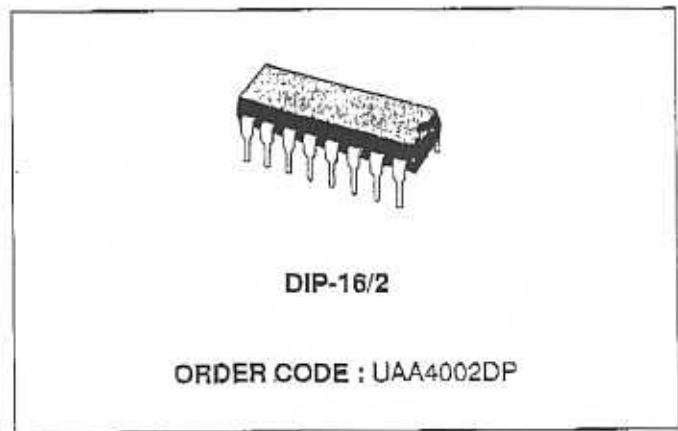
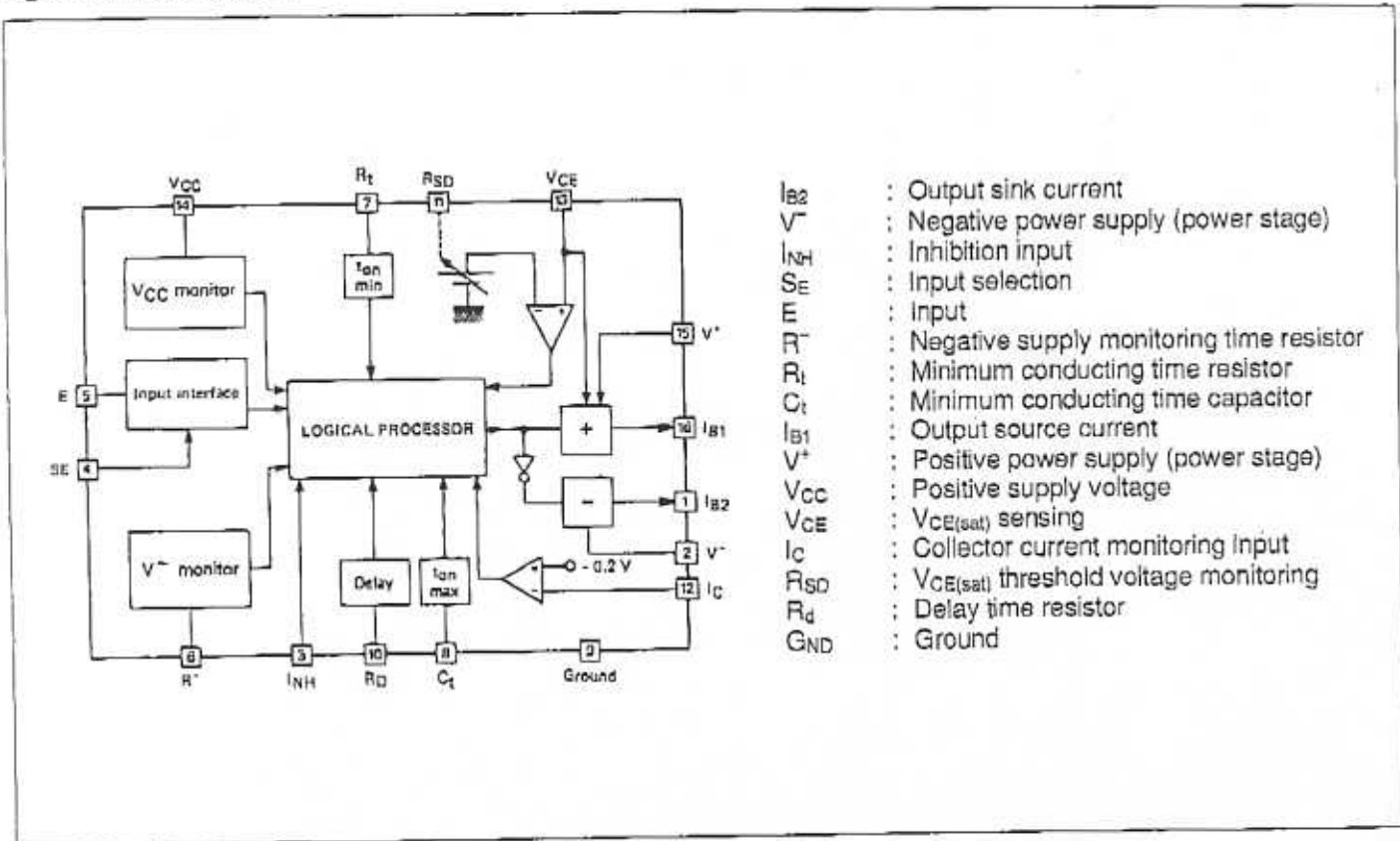


Figure 1: Block Diagram

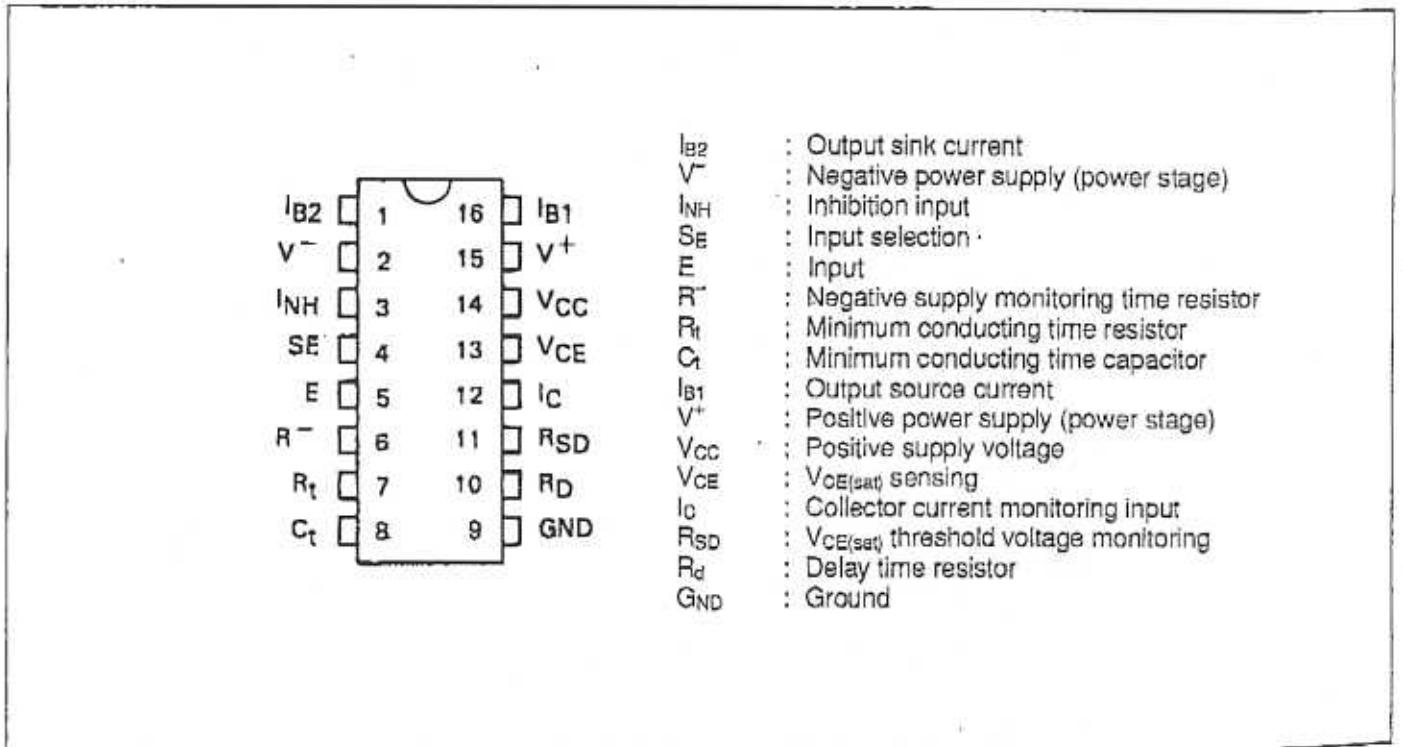


**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	+ 15	V
$V^+$	Positive Supply Voltage (power stage)	+ 15	V
$V^-$	Negative Supply Voltage (power stage)	- 10	V
$V^+ - V^-$	Voltage between Pins 15 and 2	+ 18	V
$I_{B1}$	Positive Output Current	+ 1.5	A
$I_{B2}$	Negative Output Current	- 3.5	A
$I_C$	Current into Input $I_C$ (internal protection diodes)	$\pm 5$	mA
-	Minimum Value of Resistors $R_t$ and $R_D$	5	k $\Omega$
-	Voltage between Input and $V^-$	+ 18	V
$T_j$	Junction Temperature Range	- 40 to + 150	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	- 40 to + 150	$^{\circ}C$

Note : 1. Pin 2 ( $V^-$ ) should not be left open.

**PIN CONNECTION (top view)**



**THERMAL DATA**

$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	80	$^{\circ}C/W$
---------------	---	----	---------------

## ELECTRICAL CHARACTERISTICS

 $T_{amb} = +25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = +10\text{ V}$ ,  $V^{-} = -5\text{ V}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	7	—	14	V
—	Positive Supply Voltage Monitoring Threshold	—	7	—	V
$I_{CC}$	Supply Current	—	12	—	mA
$V^{+}$	Positive Supply Voltage (power stage)	4	—	14	V
$V^{-}$	Negative Supply Voltage (power stage)	-1	—	-9	V
$V_I$	Threshold of Input $I_C$	0.160	0.2	0.240	V
$I_I$	Current into Input $I_C$	—	5	20	$\mu\text{A}$
$R_I$	Value of Resistor $R_I$ ( $R_I$ between pin 7 and ground)	10	47	200	$\text{k}\Omega$
$R_D$	Value of Resistor $R_D$ ( $R_D$ between pin 10 and ground)	20	—	200	$\text{k}\Omega$
$I_{B1}$	Positive Output Current ( $V_{(15)} - V_{(16)} = +2\text{ V}$ )	0.5	—	—	A
$I_{B1(\text{peak})}$	Positive Output Current (peak value)	1	—	—	A
$I_{B2}$	Negative Output Current ( $V_{(1)} - V_{(2)} = +4\text{ V}$ )	3	—	—	A
$V_{SD}$	Comparator $V_{CE}$ Threshold Voltage	1	—	5.6	V
—	High Level on Input E ( $V_{(5)} - V^{-} < +18\text{ V}$ )	2	—	$V_{CC}$	V
—	Low Level on Input E (input SE not connected)	$V^{-}$	—	0.8	V
—	Low Level on Input E ( $ V^{-}  > 2.5\text{ V}$ , input SE tied to ground)	$V^{-}$	—	-2	V
—	Current into Input E ( $V_{(5)} = 0\text{ V}$ )	—	10	50	$\mu\text{A}$
—	Input SE Left Open	—	0.2	0.3	mA
—	Input SE Grounded	—	—	—	—
—	Low Level on Input $I_{NH}$	0	—	0.8	V
—	High Level on Input $I_{NH}$	2	—	$V_{CC}$	V
$t_{on(\text{min})}$	Time Constant $t_{on}$ min ( $R_I$ between pin 7 and ground)	0.06 $R_I$ ( $\text{k}\Omega$ )			$\mu\text{s}$
$t_d$	Delay between Input Pulse and Rise of Output Current ( $R_D$ between pin 10 and ground)	0.05 $R_D$ ( $\text{k}\Omega$ )			$\mu\text{s}$
—	Propagation between Input Pulse and Rise of Output Current	0.3			$\mu\text{s}$
$V_{SD}$	Desaturation Threshold ( $R_{SD}$ between pin 11 and ground)	$10 \times \frac{R_{SD}}{R_I}$			V
$R^{-}$	$V^{-}$ min Detection Resistor Value ( $R^{-}$ between pin 6 and $V^{-}$ )	$\frac{R_I}{2} \left( 1 + \frac{V^{-} \text{ min}}{5} \right)$			$\Omega$
$t_{on(\text{max})}$	Time Constant $t_{on}$ max ( $C_I$ between pin 8 and ground)	2 $R_I C_I$			s
—	Thermal Shut Down	150			$^{\circ}\text{C}$

## APPLICATION INFORMATION

The coexistence of a power circuit handling high voltages and currents, and a control circuit carrying low amplitude signals, does not represent any special difficulty provided that a few simple rules are observed.

Positive and negative supply voltages of the integrated circuit must be carefully filtered by means of capacitors located very close to the device.

The device itself must be situated close to the power transistor, using short connections.

The control circuit ground (pin 9) and the power circuit ground (emitter of the power transistor) must be linked by a single connection, as short as possible and of adequate cross-section.

A ground plane on the printed circuit board may be favourable in noisy environments. With regards to upper switches of a bridge configuration, the auxiliary supplies of the integrated circuit must have a low parasitic capacitor with respect to the ground potential. In the same way, the isolated components

driving the UAA4002 (optocoupler or pulse transformer) must have also a low parasitic capacitor in order to reduce  $dv/dt$  phenomenons and to avoid risks of reswitching or conduction cut-off.

If a free-wheel diode is connected in parallel with the power transistor (which is generally the case in

bridge systems), a diode (1N4148) must be connected between pin 13 and ground (cathode on pin 13 and anode on ground) in order to limit the negative voltage applied to this pin during the conduction of the free-wheel diode.

**CIRCUIT DESCRIPTION** (see block diagram figure 1)

**INPUT INTERFACE E AND SE INPUT**

It translates the input signal into the logic levels required by the internal processor.

It also includes a RS flip-flop for the pulse mode operation.

**FAULT DETECTORS**

- Power transistor collector current limiting ( $I_c$  input)

The collector current of the power transistor is measured by means of a shunt connected in the negative return of the power supply. As a result the current rather than the emitter current, since the base

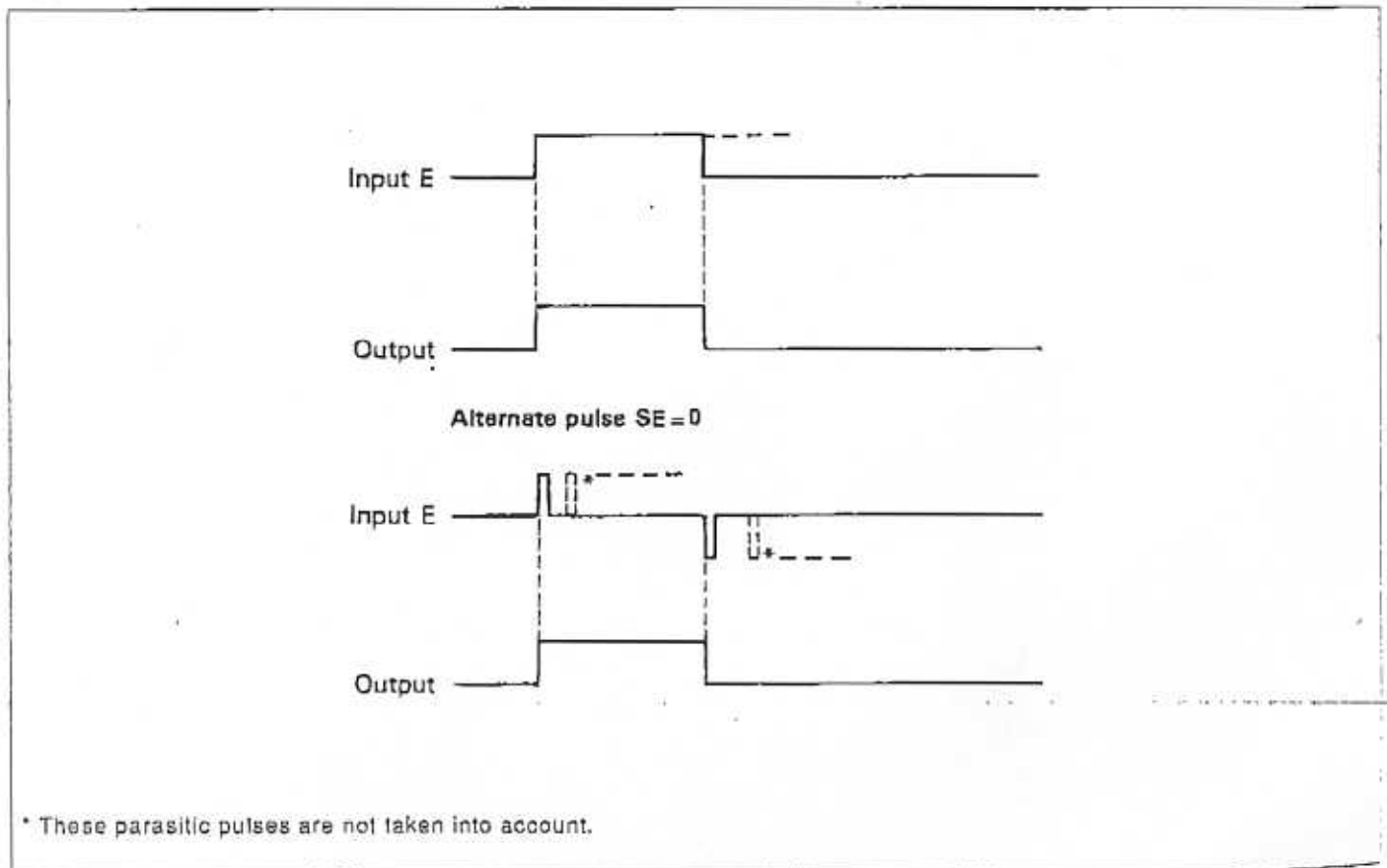
current of the switching does not flow through the shunt.

A voltage below - 0.2 V on input  $I_c$  causes comparator to change state. This information is transmitted to the logic unit, which blocks the output pulses from the circuit until the next positive transition of the input signal.

If the voltage across the measuring shunt exceeds 0.2 V for the required limiting current value, a voltage divider bridge may be used (see application note NA031A).

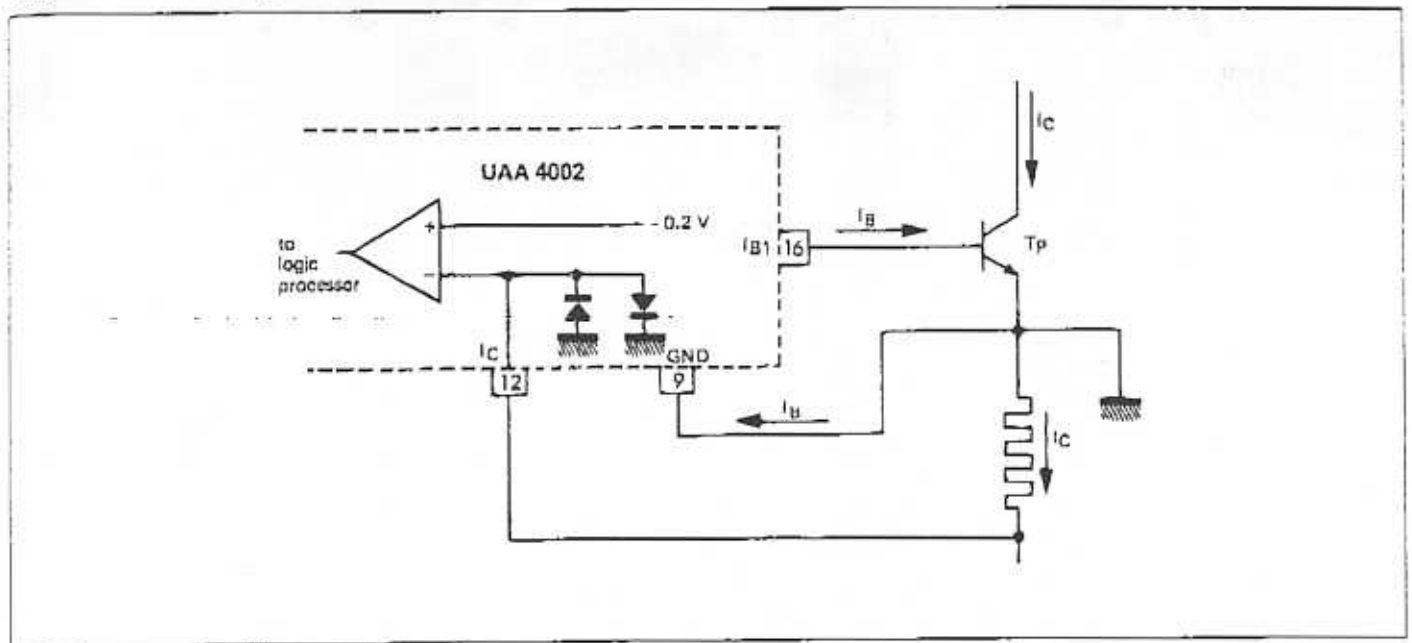
If input  $I_c$  not used, it must be connected directly to ground.

Figure 2 : Level Mode SE = 1.



Note : Pulse duration > 100ns.

Figure 3 : Switching Transistor Collector Current Measurement.



- Protection against desaturation of the power transistor.

A comparator monitors continuously during the conduction that the collector voltage on the switching transistor remains lower than the preset value.

The preset value  $V_{RSD}$  (see figure 4) is given by :

$$R_{SD} = 5 \text{ V} \times 2 \frac{R_{SD}}{R_t}$$

Current  $I$  set by external resistor  $R_t$  is :

$$I \text{ (mA)} = \frac{5 \text{ (V)}}{R_t \text{ (k)}}$$

Without resistor  $R_{SD}$ , the threshold is set internally at + 5.6 V.

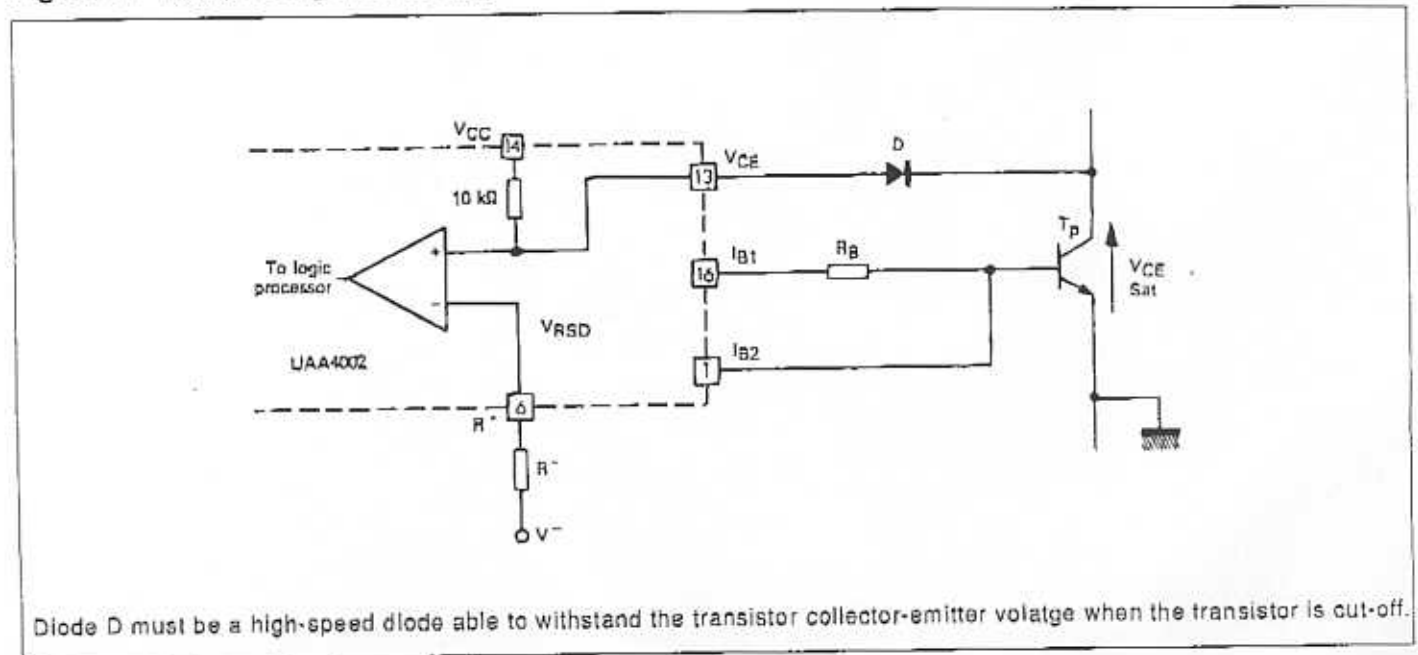
In case of overstep, the information is transmitted to the logic unit, which turns the output off until the next positive edge of the input signal.

To enable the switching transistor collector emitter voltage to fall when conduction begins, the protection function against desaturation is disabled during  $t_{on \text{ min}}$  (see application note NA031A).

This protection is disabled by connecting pin  $R_{SD}$  directly to  $V$ .

(FOR THRESHOLD EXCEEDING 5.5 V SEE NA031EA).

Figure 4 :  $V_{CEsat}$  Voltage Monitoring.



Diode D must be a high-speed diode able to withstand the transistor collector-emitter voltage when the transistor is cut-off.

**SUPPLY DEFECT**

- Negative supply (R input, see figure 4).

It is possible to disable the output pulses if the negative supply voltage V is insufficient to guarantee the switching of the power transistor (optional).

(FOR USING WITHOUT NEGATIVE POWER SUPPLY SEE NA031A)

For this a resistor R is tied between pin 6 and the negative supply.

A current 2 I flows into it, and the threshold of the detector is + 5 V on pin 6.

Thus giving the relationship :

$$\frac{5 + V- \text{ min}}{R-} = 2 \times \frac{5}{R_t} \quad R- = \frac{R_t}{2} \left( 1 + \frac{V- \text{ min}}{5} \right)$$

This function can be disabled by tying pin 6 to ground.

- Positive supply (Vcc input)

An internal comparator ensures that there is no output voltage if positive supply Vcc is less than + 7 V. This threshold is not adjustable.

- Inhibition (INH input)

The action of the inhibition input is shown in the diagram below.

This input is CMOS and TTL compatible. If not used, it must be connected directly to ground.

- Thermal protection

The UAA4002 is protected against excessive overheating by a thermal cut-out which automatically cuts off the output pulses if the chip temperature exceeds + 150 °C. The interruption is stored for a complete conduction period, but the output pulses reappear as soon as the chip temperature falls below the limiting temperature value.

**TIME CONSTANTS**

- Minimum conducting time (Rt input)

To enable the capacitor of the switching aid network associated with power transistor to discharge completely, the logic processor ensures that the integrated circuit output pulse has a minimum duration  $t_{on \text{ min}}$ . To be effective, this must be at least four times the time constant of the RDC network.

The value of  $t_{on \text{ min}}$  is programmed by a resistor  $R_t$

Typically  $t_{on \text{ min}} \text{ (s)} = 0.06 \times R_t \text{ (k)}$

The usable range of values for  $t_{on \text{ min}}$  is between 1 and 12 s.

Resistor  $R_t$  has a key role in the operation of the UAA4002 integrated circuit. It sets the value of a bias current internal to the circuit :

$$I \text{ (mA)} = \frac{5}{R_t \text{ (k)}}$$

$t_{on \text{ min}}$  embodies a priority function : no other security function can stop the conduction during  $t_{on \text{ min}}$ .

The  $t_{on \text{ min}}$  function cannot be disabled.

- Maximum conducting time (Rt and Ct inputs)

At the start of each conduction period the capacitor  $C_t$  is loaded by a constant current  $I/2$ , where I is the current through resistor  $R_t$  ( $I = 5/R_t$ ). When the voltage across  $C_t$  reaches + 5 V the conduction is stopped. The value of  $t_{on \text{ max}}$  is thus given by the equation :

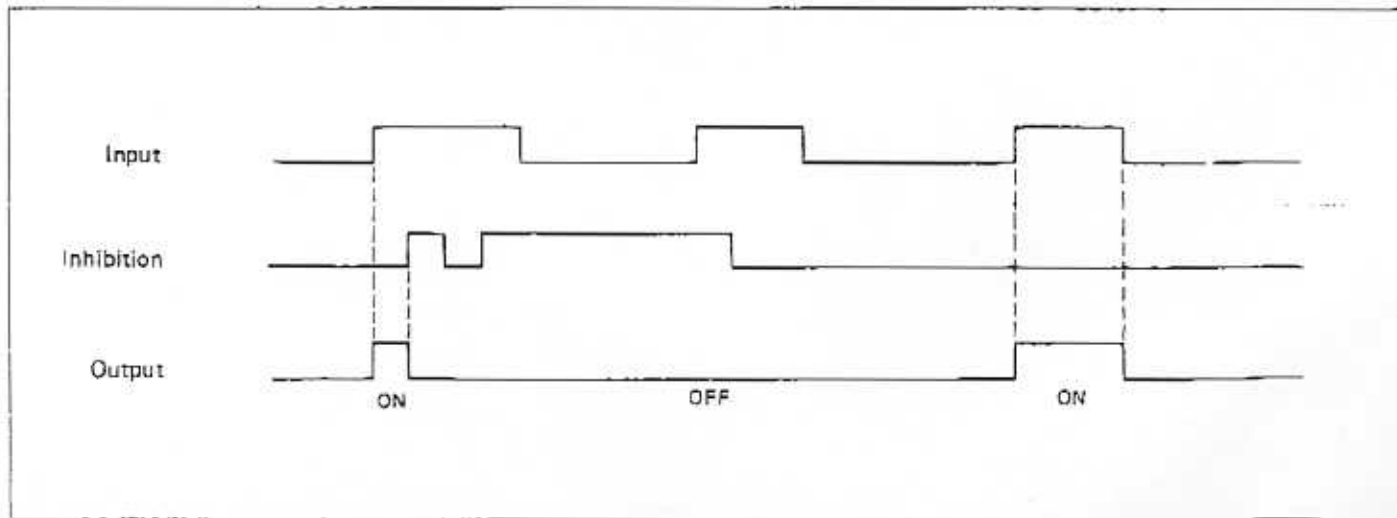
$$t_{on \text{ max}} \text{ (s)} = 2 \times R_t \text{ (k)} \times C_t \text{ (nF)}$$

If the  $t_{on \text{ max}}$  function is not to be used, it is only necessary to replace capacitor  $C_t$  with a short-circuit.

- Time delay function

A constant time delay may be implemented between the rising edge of the control pulse and the begin-

Figure 5.



ring of the conduction pulse at the circuit output = (1 to 20  $\mu$ s by using resistor  $R_D$ ,  $t_d$  ( $\mu$ s) = 0.05  $R_D$  ( $k\Omega$ ).

**LOGIC PROCESSOR**

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

Figure 6.

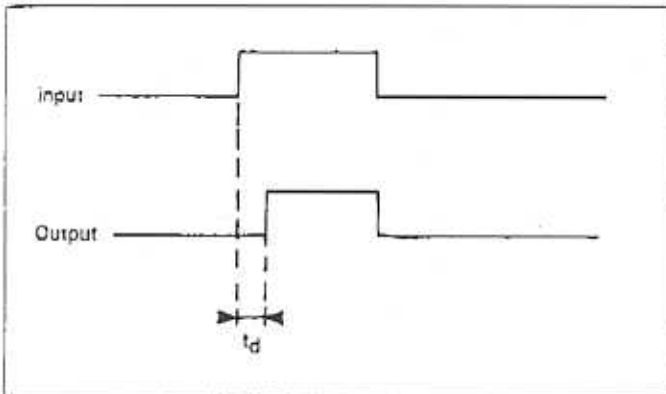
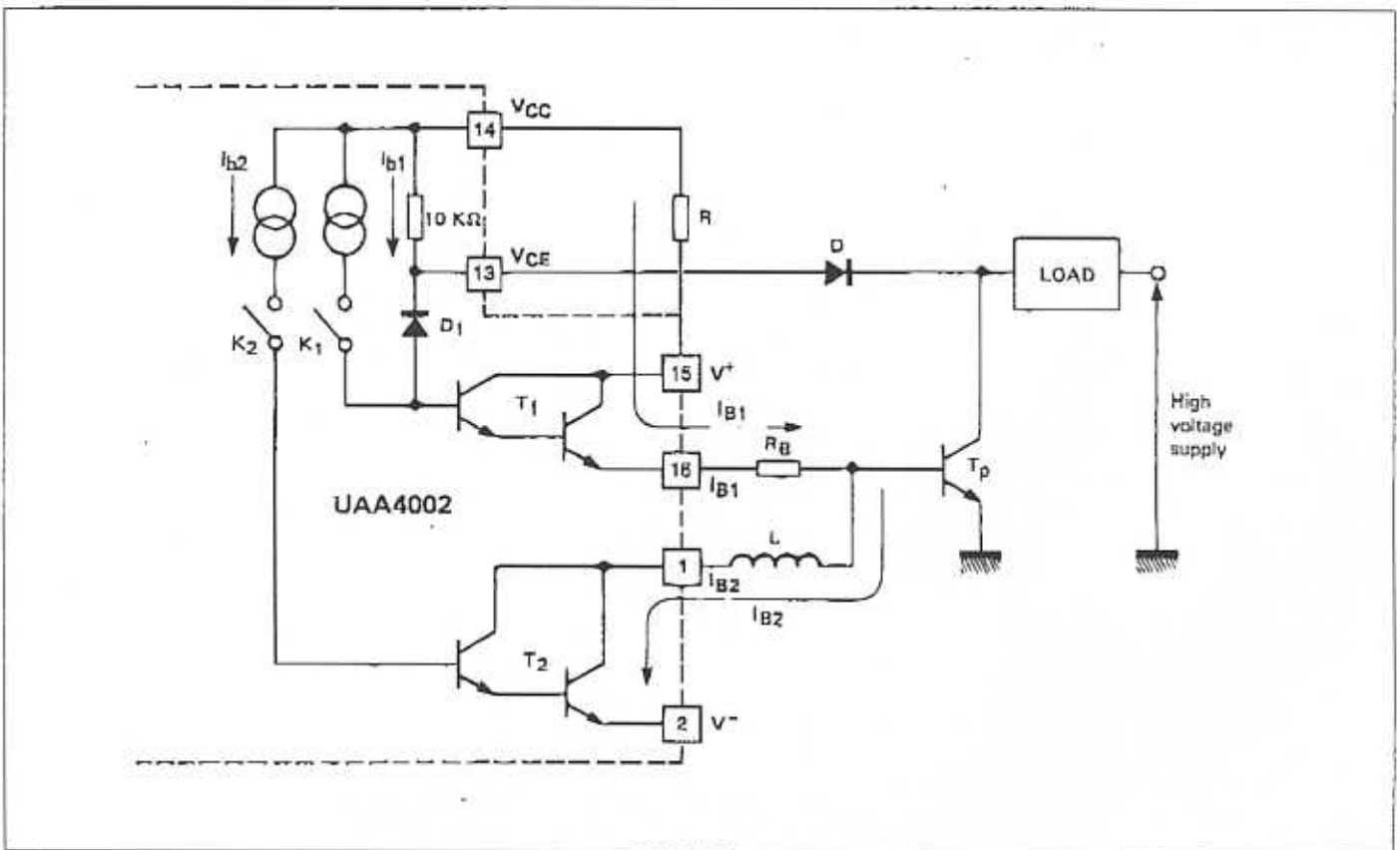


Figure 7.



- No double pulsing within a period : the occurrence of a defect is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum output pulse width is set at a given value  $t_{on\ min}$ .

**OUTPUT STAGE :  $V^+$ ,  $V^-$ ,  $I_{B1}$ ,  $I_{B2}$ , INPUTS**

■ Introduction

The highly sophisticated output stage of the UAA4002 offers high performance in terms of switching transistor control.

Its principal features are as follows :

- the switching transistor is direct driven
- the transistor remains in a quasi-saturated state, whence reduced storage time
- control power is limited to the strict minimum
- it is easy to use

This stage is in fact in two parts, a positive driver stage which turns on the transistor and a negative driver stage which turns off the transistor.

■ Power transistor conduction

The maximum value of the positive base current is determined by the limitation resistor R ( $I_{B1} = 1 \text{ A}$ ). A regulation loop is used to keep  $T_P$  in a quasi-saturation mode : the more  $T_P$  becomes saturated, the more diode D will shunt an important part of the drive current  $I_{B1}$ , through diode  $D_1$ .  $R_B$  is a low value resistor (about 1  $\Omega$ ) which helps to stabilize the regulation loop.

Voltage  $V_{CE}$  across transistor Q is :

$$V_{CE} (V) = V_{BE} (V) + R_B (\Omega) I_{B1} (A)$$

If the required drive current is greater than 0.5 A, one external NPN transistor may be added.

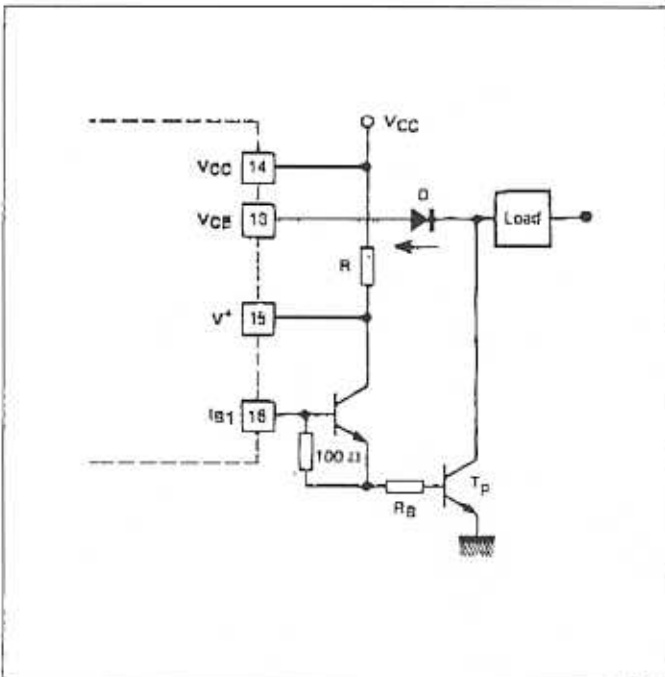
In this case :

$$V_{CE} (V) = 2 V_{BE} (V) + R_B (\Omega) I_{B1} (A)$$

■ Turn-off switching of power transistors

The closing of contact  $K_2$  (figure 10) causes Darlington  $T_2$  to conduct. The negative supply voltage is applied to the base of transistor  $T_P$  and a high negative base current  $I_{B2}$  flows, permitting the rapid evacuation of charges stored in the base-emitter junction of transistor  $T_P$ .

Figure 8.



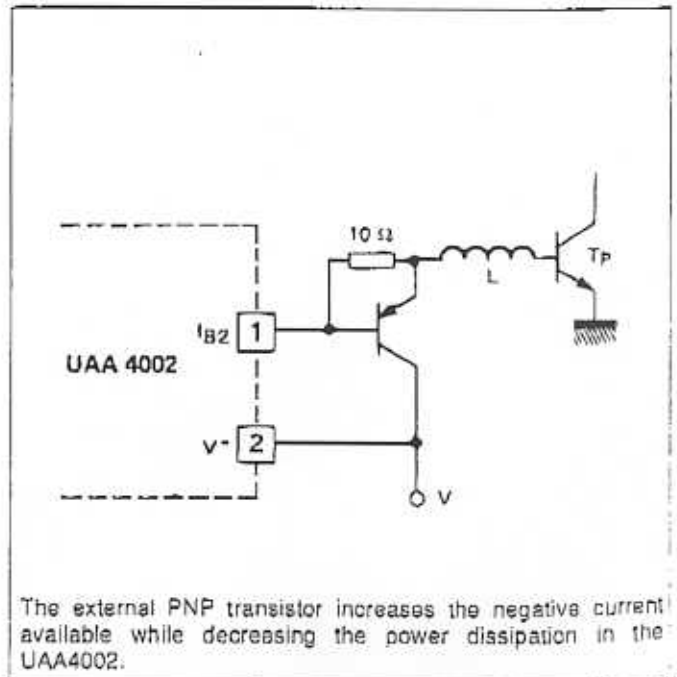
A low-value inductor L may be required between the base of transistor  $T_P$  and the  $I_{B2}$  output of the UAA4002, so as to limit the gradient  $dI_{B2}/dt$  (see "The Power Transistor in its Environment" published by the Discrete Semiconductors Division of Thomson-CSF). In many cases, this inductor is not required.

The Darlington  $T_2$  can carry a maximum current of 3 A. The corresponding saturation voltage is typically 3 V. Like the positive stage, this stage is designed for easy augmentation of the available output current by the addition of one or more external transistors.

■ Typical inductive load waveforms

When conduction begins, the base current assumes a high value briefly and then reverts to zero. This base current spike permits rapid switching on of the power transistor. The base current value is then that required for quasi-saturation of the transistor. The base current curve is generally curved upward, due to the decreased gain of the power transistor with increased collector current.

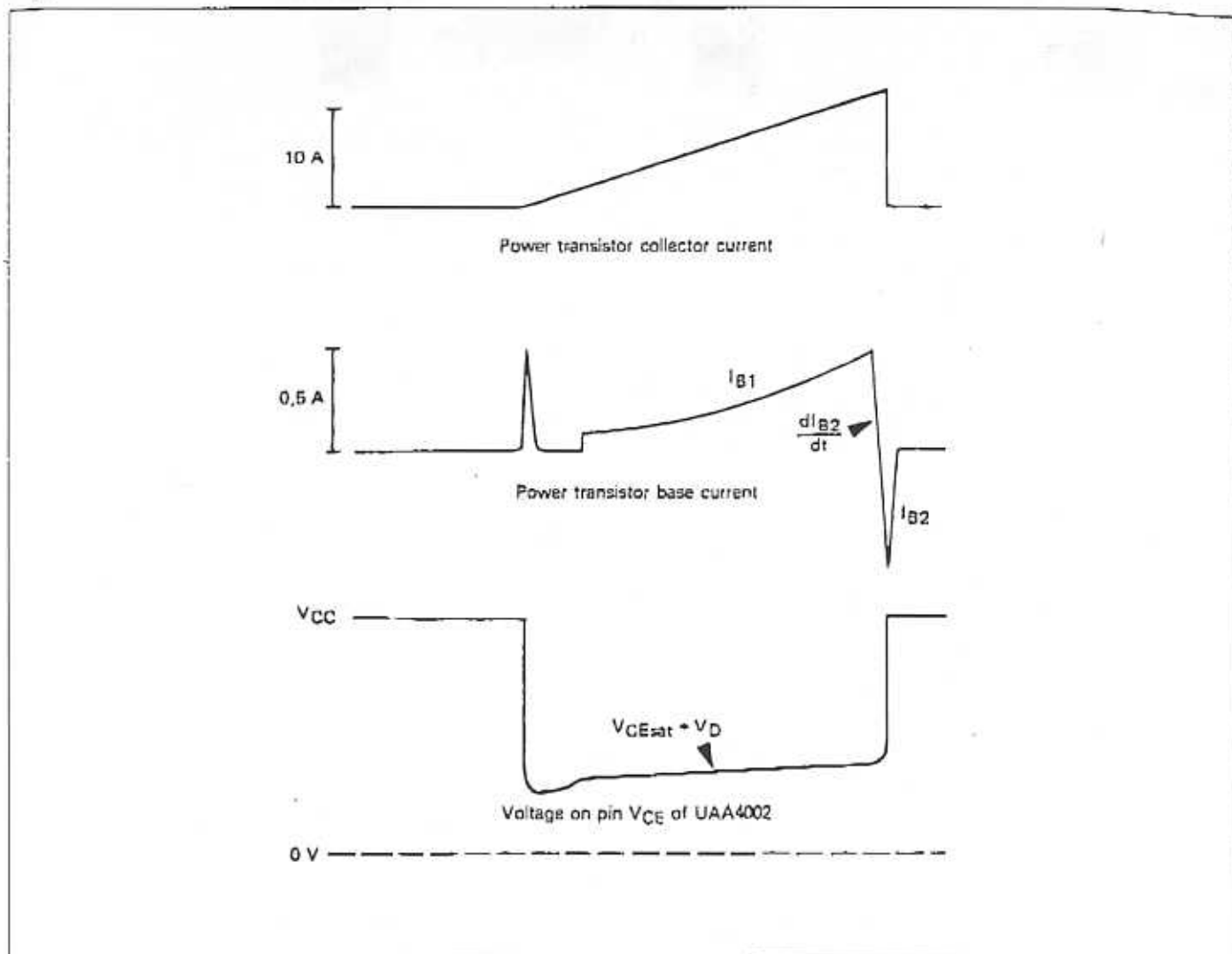
Figure 9.



The external PNP transistor increases the negative current available while decreasing the power dissipation in the UAA4002.



Figure 10.



### CONTROL OF MOS POWER TRANSISTORS

Ideally, MOS power transistors should be voltage-controlled. In practice, in order to benefit from the high speed typical of this type of transistor it is necessary to charge and discharge the spurious input capacitance at high speed, so that high currents flow. By virtue of the high current capability of its output stages, the UAA4002 is particularly suitable for controlling MOS power transistors.

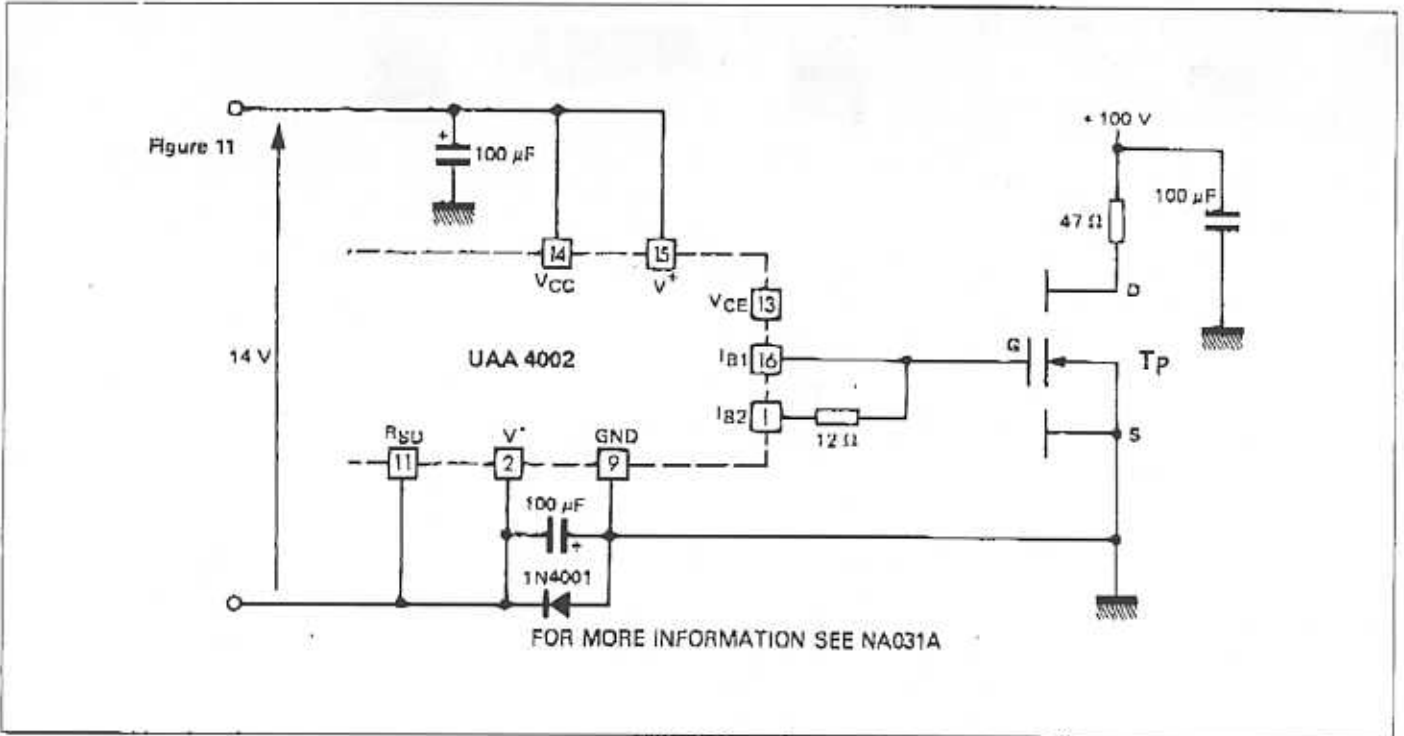
The output of the positive stage is connected directly to the gate of the MOS transistor, to switch it into conduction very fast. The negative stage controls the turning off of the MOS transistor, by discharging the gate capacitance of the transistor. There is no need for a high negative supply voltage, and the ar-

angement described in the previous section is therefore used.

In this circuit the UAA4002 is used in a completely conventional manner, in "level" control mode.

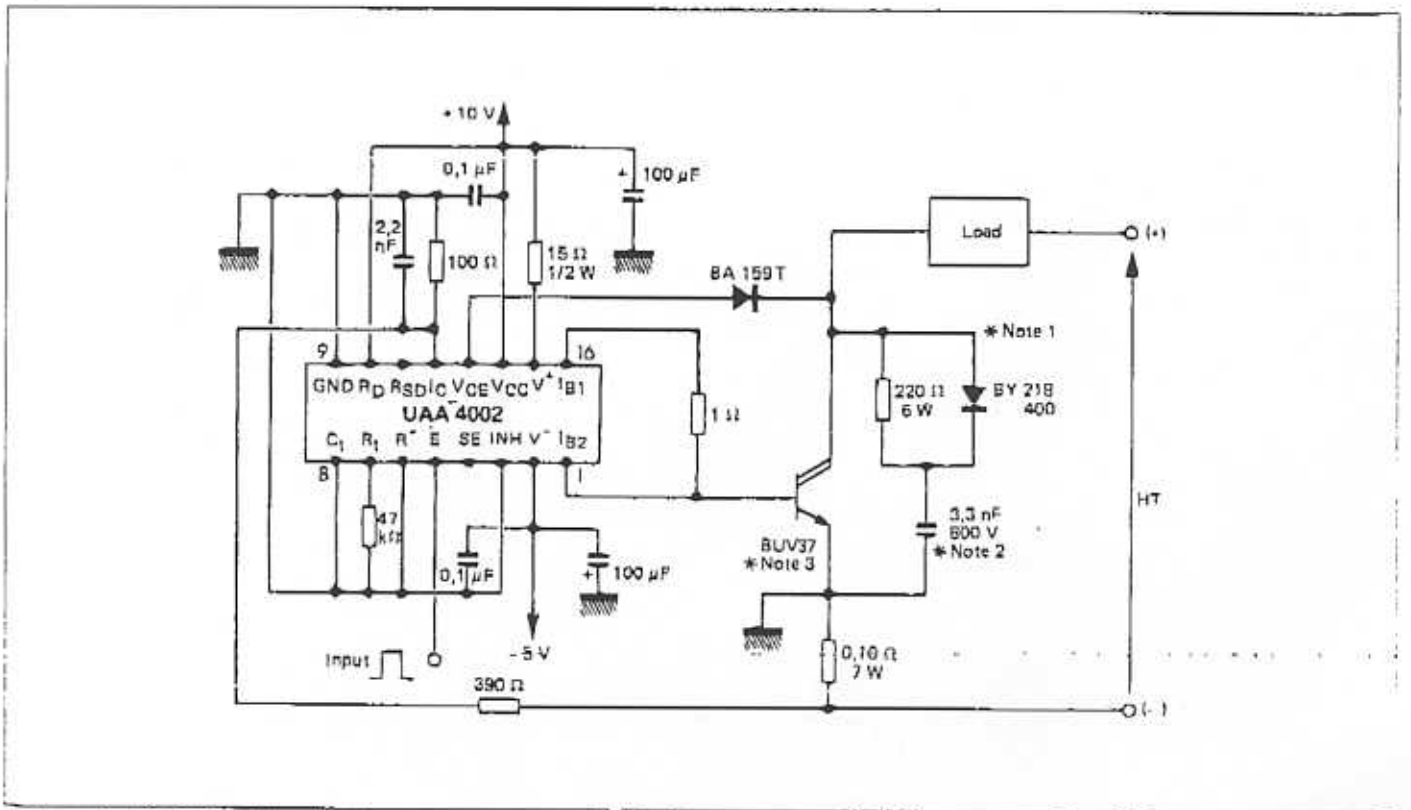
The time constant  $t_{on\ min}$  is set at 2.8 s, which is four times the time constant of the snubber network associated with the BUV37 transistor. The positive output stage of the UAA4002 is connected to the  $V_{CC}$  rail through a 15 resistor. The maximum base current is approximately 0.45 A. The collector current is measured using a 0.10 shunt, and is limited to 10 A. The BUV37 Darlington for which the specified value of  $I_{C(sat)}$  is 12 A, is thus operated with a considerable safety margin.

Figure 11.



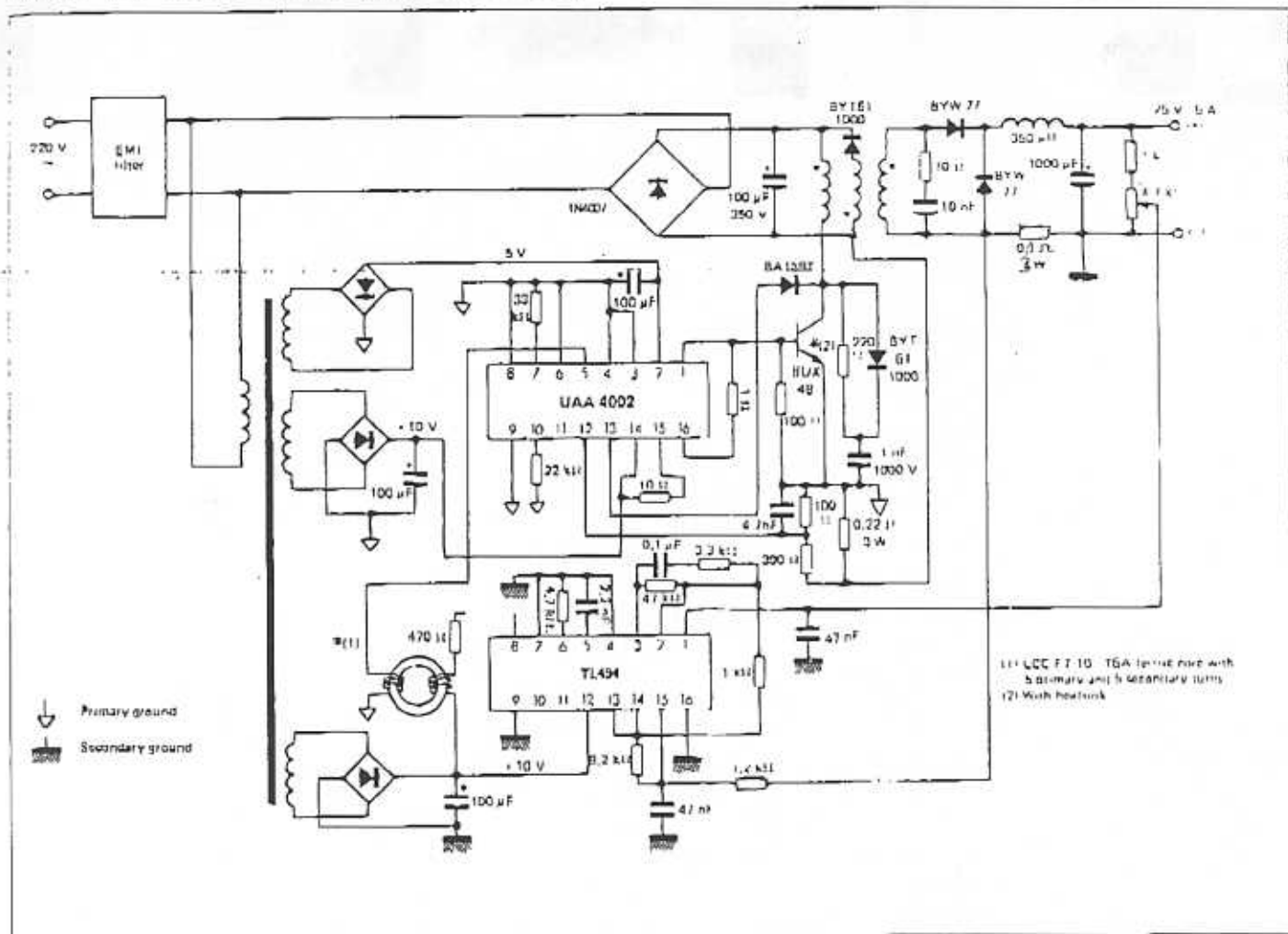
TYPICAL APPLICATIONS

Figure 12 : 8 A, 400 V switch.



- Notes :
1. Switching aid network.
  2. Polypropylene capacitor.
  3. With heatsink,  $R_{HT} < 3.5 \text{ } ^\circ\text{W}$ .

Figure 13 : 150 W Forward Type Power Supply.



**Performance**

- Output voltage stability :  
 For an input voltage varying from 190 to 245 V, the maximum relative variation in the output voltage is 0.7 % at nominal operating conditions.  
 ( $V_{OUT} = 25 \text{ V}$ ,  $I_{OUT} = 6 \text{ A}$ ).  
 For a variation in the load from 0 to 100 % the relative variation in the output voltage is 1.3 %.  
 For a variation in the load from 10 to 100 % ( $I_{OUT} = 0.6 \text{ to } 6 \text{ A}$ ), the relative variation in the output voltage is 0.4 %.
- Efficiency 80 % under nominal operating conditions.
- Behaviour on overload :  
 The power supply is fully protected against overloads and short-circuits, the output current being limited to 7 A.

Figure 14 : Capacitor Type Half Bridge Symmetrical Converter.

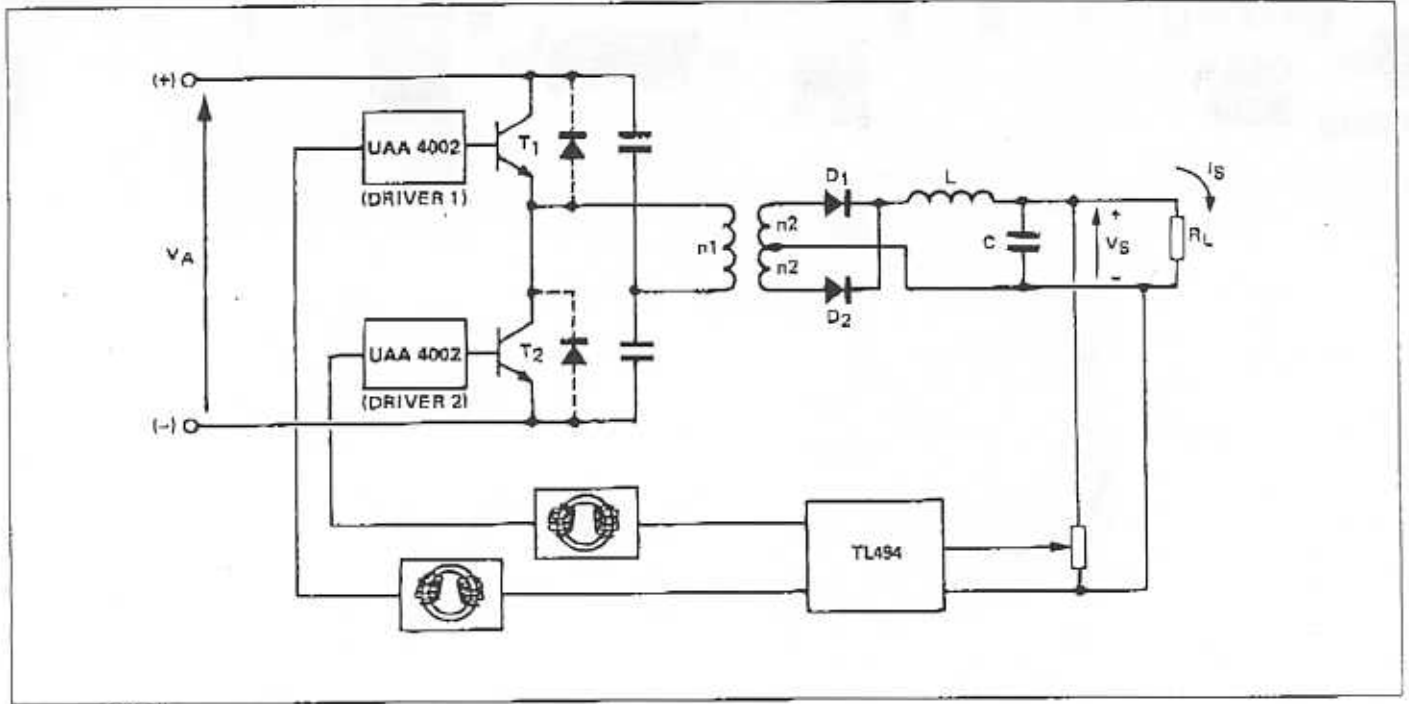


Figure 15 : 200 A, 700 V Switch.

