



Features

- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier (P_{out} typically 26.5 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF typically 1.8 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components

Electrostatic sensitive device.
Observe precautions for handling.



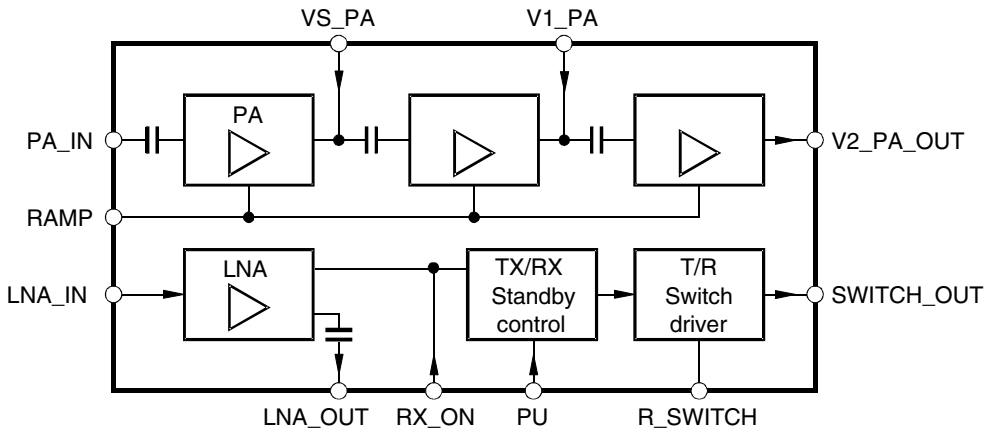
DECT SiGe Front End IC with High PAE

U7006B

Description

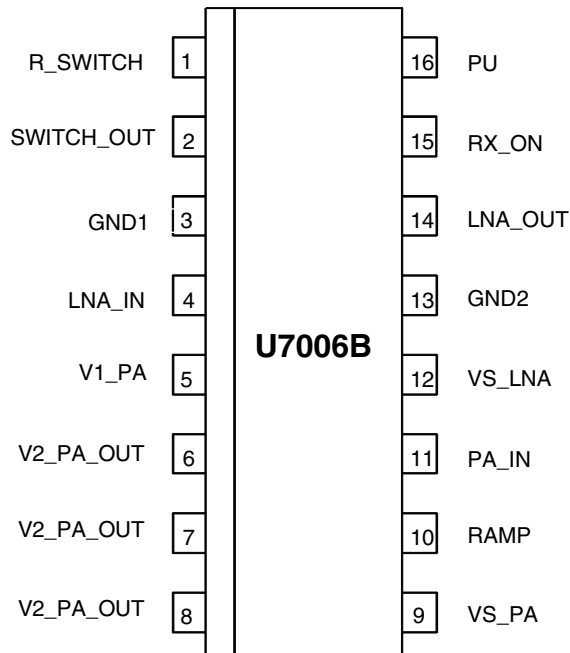
The U7006B is a monolithic SiGe transmit/receive front end IC with power amplifier, 50- Ω internal matching, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT. Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning PSSO16



Pin Description

Pin	Symbol	Function
1	R_SWITCH	Resistor to GND sets the PIN diode current
2	SWITCH_OUT	Switched current output for PIN diode
3	GND1	Ground
4	LNA_IN	Low-noise amplifier input
5	V1_PA	Inductor to power supply for power amplifier
6	V2_PA-OUT	Inductor to power supply and matching network for power amplifier output
7		
8		
9	VS_PA	Supply voltage for power amplifier
10	RAMP	Power-ramping control input
11	PA_IN	Power amplifier input
12	VS_LNA	Supply-voltage input for low-noise amplifier
13	GND2	Ground
14	LNA_OUT	Low-noise amplifier output
15	RX_ON	RX active high
16	PU	Power-up active high

Absolute Maximum Ratings

All voltages refer to GND (Pins 3 and slug), ESD protection according to ESD-S5.2-1994, Class M1.

Parameters	Symbol	Value	Unit
Supply voltage; pins 6, 10, 13 and 16 (no RF)	V_S	5	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
Input power PA, Pin 11	P_{inPA}	+10	dBm
Input power LNA, Pin 4	P_{inLNA}	-5	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	30	K/W

Operating Range

All voltages refer to GND (Pins 3, 13 and slug). The following table represents the sum of all supply currents depending on the TX/RX mode. Power supply points are VS_LNA, VS_PA, V1_PA, V2_PA_OUT.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage pins 5, 6, 7, 8 and 9	V_S	2.7	3	4.6	V
Supply voltage pin 12	V_S	2.7	3.6	4.6	V
Supply current TX	I_S		350		mA
RX	I_S		8		mA
Standby current PU = 0	I_S		10		µA
Ambient temperature	T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3\text{ V}$, $T_{amb} = 25^\circ\text{C}$, CW mode

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier ⁽¹⁾						
Supply voltage	Pins 5, 6, 7, 8 and 9	V_S	2.7	3	4.6	V
Supply current	TX	I_{S_TX}		350		mA
Supply current	RX (PA off)	I_{S_RX}			10	µA
Standby current	Standby	$I_{S_standby}$			10	µA
Frequency range	TX	f	1.88		1.94	GHz
Power gain	TX, pin 11 to pins 6, 7, 8	G_p		28		dB
Gain-control range	TX	ΔG_p		48		dB
Ramping voltage	TX, power gain (max), pin 10	$V_{RAMP\ max}$		2.1		V
Ramping current	TX, power gain (max), pin 10	I_{RAMP}		0.5	2.0	mA
Power-added efficiency	TX	PAE		40		%

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: TBD
 2. With external matching network (see Figure 13)
 3. Low-noise amplifier shall be unconditionally stable

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_S = 3\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, CW mode

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Saturated output power	TX, referred to pins 6, 7, 8 $V_S = 3.6\text{ V}$	P_{sat}		26.5		dBm
Input matching ⁽²⁾	TX, pin 11	VSWRin		< 2:1		
Output matching ⁽²⁾	TX, pins 6, 7, 8	VSWRout		< 2:1		
Harmonics at P 1dB	TX, pins 6, 7, 8	2 fo 3 fo		-30		dBc
Maximum input power	Pin 11	P_{inPA}		10		dBm
Stability (non harmonic emission)	TX, pin 10 $P_{\text{in}} = 2\text{ dBm}$, $V_{\text{RAMP}} = 2\text{ V}$ VSWRout < 10:1 (all phases)			-60		dBc
T/R Switch Driver (Currently Programmed by External Resistor from R_SWITCH to GND)						
Switch-out current output	Standby, pin 2	$I_{\text{S_O_standby}}$			2	μA
	RX	$I_{\text{S_O_RX}}$			2	μA
	TX at 100 Ω	$I_{\text{S_O_100}}$		1		mA
	TX at 1.2 k Ω	$I_{\text{S_O_1k2}}$		3		mA
	TX at 33 k Ω	$I_{\text{S_O_33k}}$		10		mA
Low-noise Amplifier ⁽³⁾						
Supply voltage	All, pin 12	V_S	2.7	3.6	4.6	V
Supply current	RX	I_S		8		mA
Supply current (LNA and control logic)	TX (control logic active), pin 12	I_S		300		μA
Standby current	Standby, pin 12	I_S		1	10	μA
Frequency range	RX	f	1.88		1.94	GHz
Power gain	RX, pin 4 to pin 14	Gp	17	19		dB
Noise figure	RX	NF		1.8	2.0	dB
Gain compression	RX, refer to pin 14	P1dB		-7		dBm
3rd-order input interception point	RX	IIP3		-15		dBm
Input matching	RX	VSWRin		< 2:1		
Output matching	RX	VSWRin		< 2:1		
Logic Input Levels (RX_ON, PU)						
High input level	= 1, pins 5 and 16	V_{iH}	2.4		V_S	V
Low input level	= 0	V_{iL}	0		0.5	V
High input current	= 1	I_{iH}		40		μA
Low input current	= 0	I_{iL}		0		μA

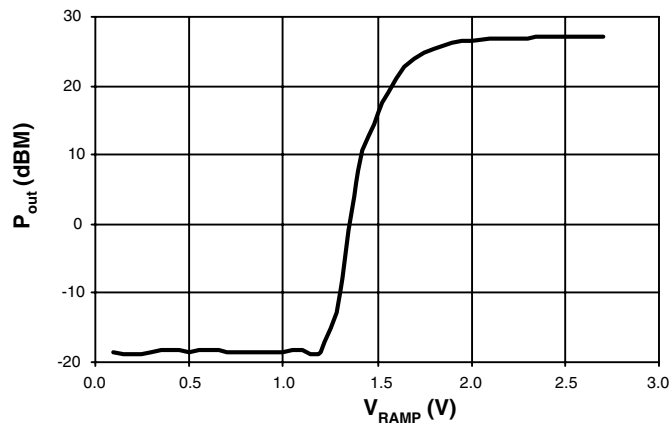
- Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: TBD
2. With external matching network (see Figure 13)
3. Low-noise amplifier shall be unconditionally stable

Control Logic

Table 1. Control Logic for LNA and T/R Switch Driver

Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

Figure 3. Output Power versus Ramp Voltage



Input/Output Circuits

Figure 4. Input Circuit PA_IN/VS_PA

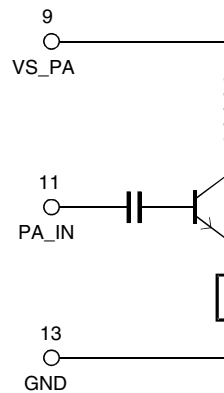


Figure 5. Input Circuit RAMP/VS_PA

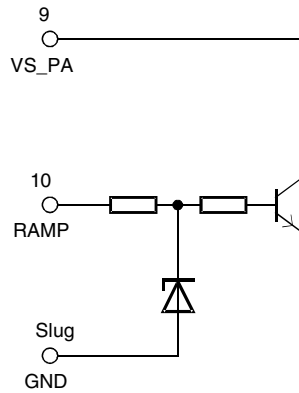


Figure 6. Input Circuit V1_PA

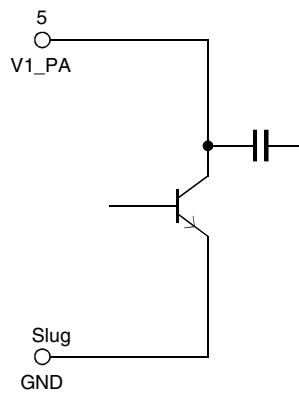


Figure 7. Input/Output Circuit V2_PA

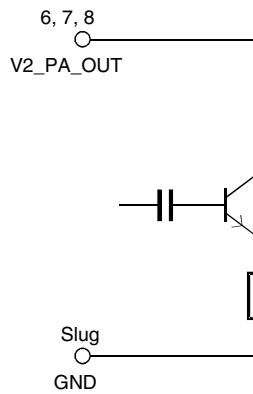


Figure 8. Input Circuit LNA_IN/VS_LNA

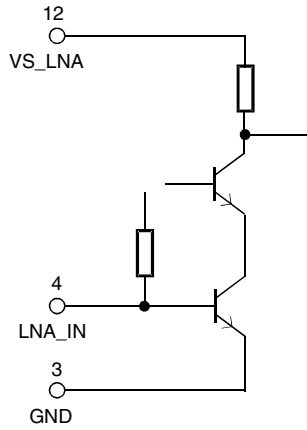


Figure 9. Output Circuit LNA_OUT

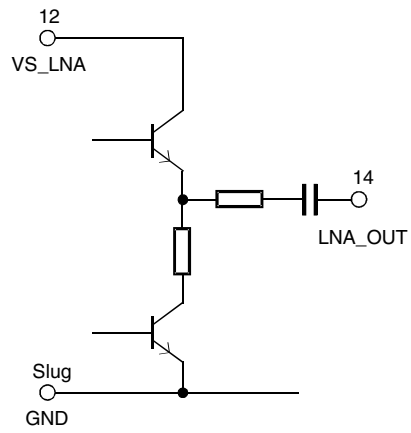


Figure 10. Input Circuit SWITCH_OUT/R_SWITCH

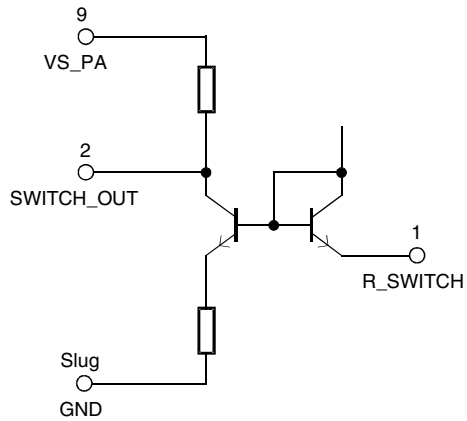


Figure 11. Input Circuit RX_ON

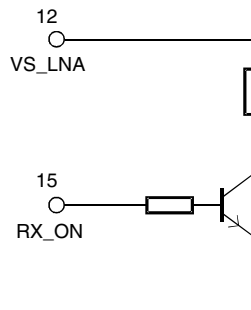
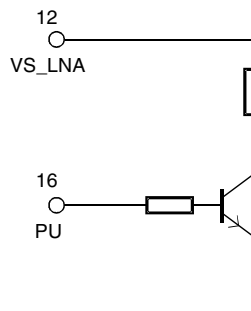


Figure 12. Input Circuit PU



Typical Application Circuit

Figure 13. Typical Schematic

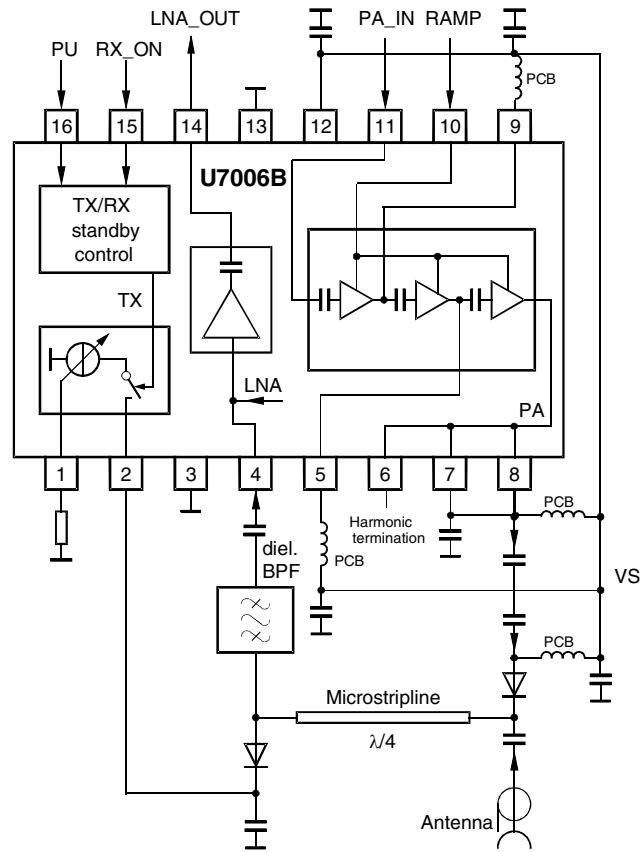


Figure 14. U7006B Application Board Schematic

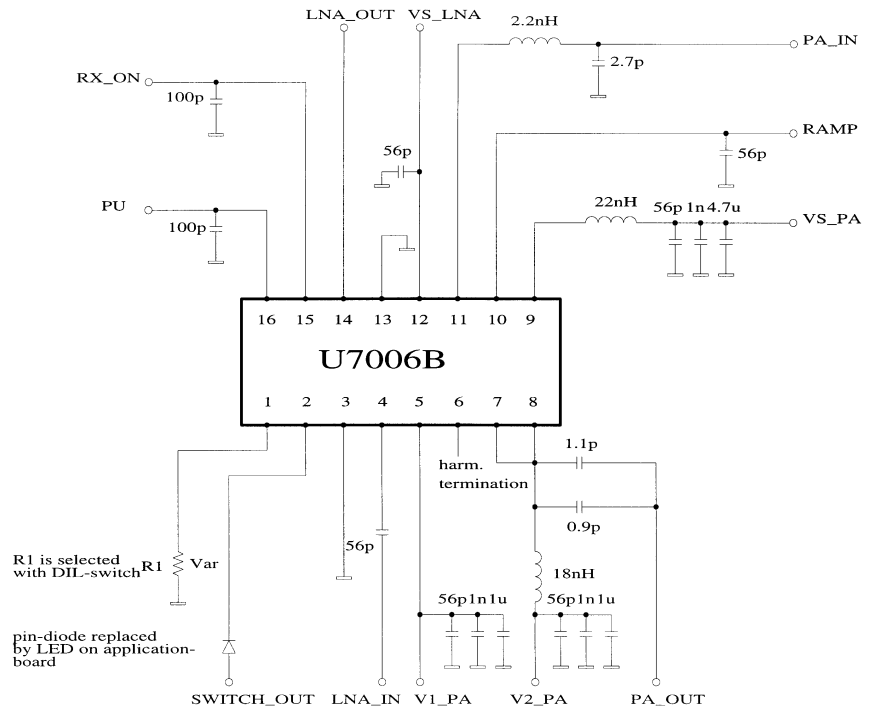
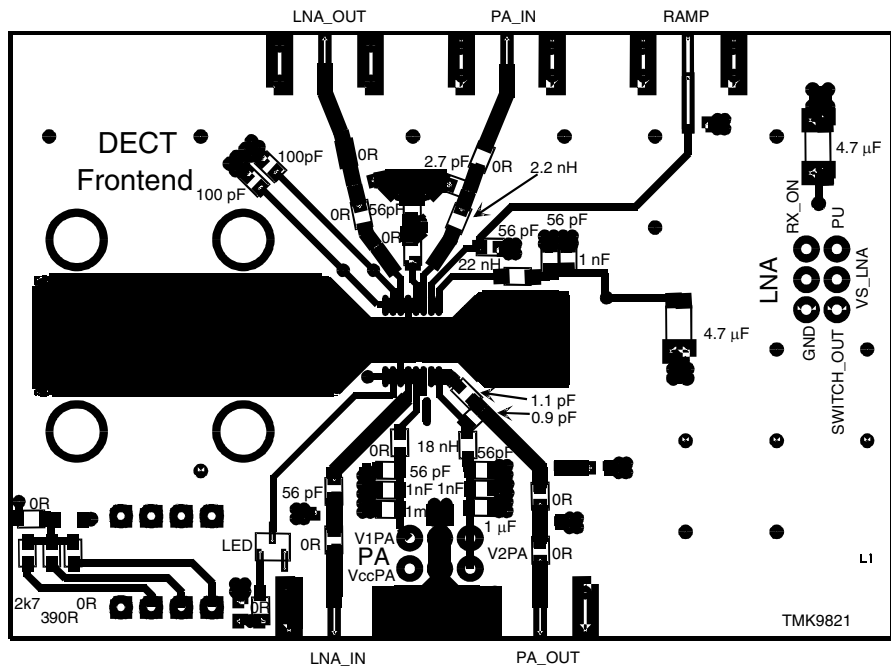


Figure 15. U7006B Application Board Layout



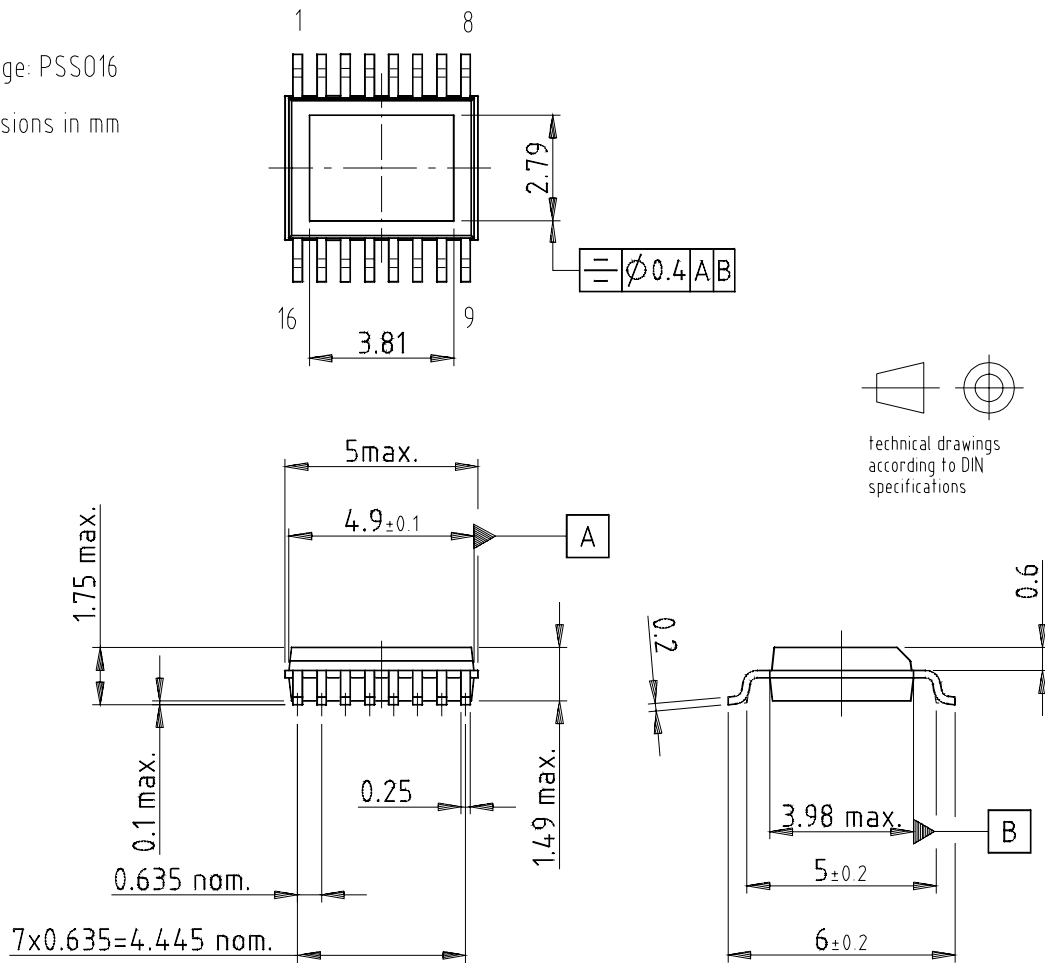
Ordering Information

Extended Type Number	Package	Remarks
U7006B-MLB	PSSO16	Tube
U7006B-MLBG3	PSSO16	Taped and reeled

Package Information

Package: PSSO16

Dimensions in mm



Drawing-No.: 6.543-5067.01-4

Issue: 3; 08.08.00



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

Disclaimer: Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

© Atmel Corporation 2003. All rights reserved.

Atmel® and combinations thereof are the registered trademarks of Atmel Corporation or its subsidiaries.

Other terms and product names may be the trademarks of others.



Printed on recycled paper.