TEXAS INSTRUMENTS

TUSB214 USB 2.0 High Speed Signal Conditioner with BC1.2 CDP

1 Features

- Compatible with USB 2.0, OTG 2.0 and BC 1.2
- Pin strap or I²C configurable
- BC1.2 Charging Downstream Port (CDP) controller
- Support for LS, FS, HS signaling
- Ultra-low USB Disconnect and Shutdown Power Consumption
- Selectable Signal Gain Via Daisy Chain Device for High Loss Applications
- D1P/M and D2P/M Interchangeable and Host/Device Agnostic
- Supports up to 5m pre-channel or 2m post-channel Cable Length
  - Four Selectable AC Boost Settings Via External Pulldown Resistor
  - DC Boost Along With AC Boost for Best Signal Integrity

2 Applications

- Notebooks
- Desktops
- Docking Stations
- Tablets
- Cell Phones
- Active Cable, Cable Extenders
- Backplane
- Televisions

3 Description

The TUSB214 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel.

TUSB214 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals. LS and FS signal characteristics are unaffected by the TUSB214 while HS signals are compensated.

Programmable signal AC boost and DC boost permits fine tuning device performance to optimize High Speed signals at the connector. This helps to pass USB High Speed electrical compliance tests.

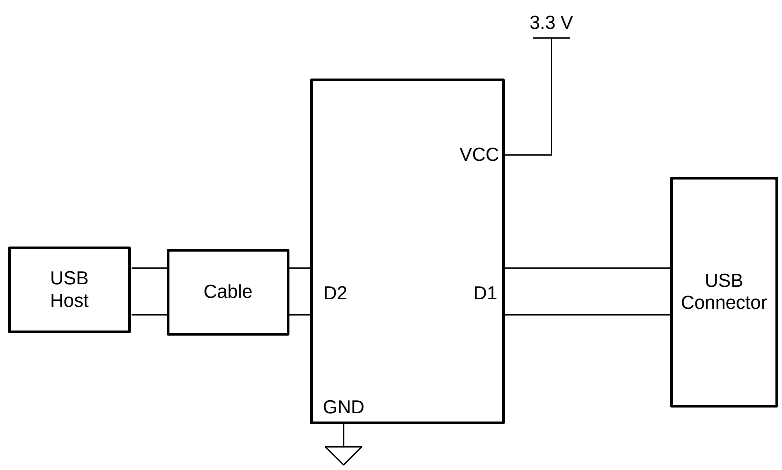
In addition, TUSB214 is compatible with the USB On-The-Go (OTG) and Battery Charging (BC) protocols. The TUSB214 provides BC1.2 Charging Downstream Port (CDP) controller for applications in which USB host or hub do not have this support.

Device Information [(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB214 TUSB214I	X2QFN (12)	1.60 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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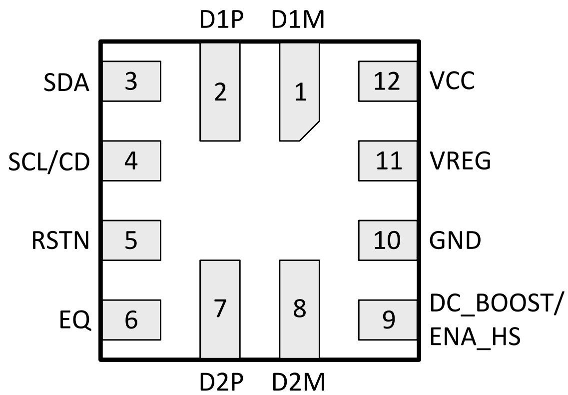
4 Revision History

DATE	REVISION	NOTES
August 2017	*	Initial release.

5 Pin Configuration and Functions

RWB Package
12 Pin (X2QFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
D1M	1	I/O	N/A	USB High Speed negative port..
D1P	2	I/O	N/A	USB High Speed positive port.
SDA(1)	3	I/O	RSTN asserted: 500 kΩ PD	I2C Mode: Bidirectional I2C data pin [I2C address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
SCL(1)/CD	4	I/O	RSTN asserted: 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
RSTN	5	I	500 kΩ PU	Device disable/enable. Low – Device is at reset and in shutdown, and High – Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
EQ	6	I	N/A	USB High Speed AC boost select via external pull down resistor. Sampled upon de-assertion of RSTN. Does not recognize real time adjustments. Auto selects max AC Boost when left floating.
D2P	7	I/O	N/A	USB High Speed positive port.
D2M	8	I/O	N/A	USB High Speed negative port.
DC_BOOST(2)/ ENA_HS	9	I/O		In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal DC_BOOST. USB High Speed DC signal boost selection. H (pin is pulled high) – 80 mV M (pin is left floating) – 60 mV L (pin is pulled low) – 40 mV After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].
GND	10	P	N/A	Ground
VREG	11	O	N/A	1.8-V LDO output. Only enabled when operating in High Speed mode. Requires 0.1-µF external capacitor to GND to stabilize the core.
VCC	12	P	N/A	Supply power

(1) Pull-up resistors for SDA and SCL pins in I^2C mode should be 2 kΩ (5%). If both SDA and SCL are pulled up at reset the device enters into I^2C mode.
(2) Pull-down and pull-up (to 3.3 V) resistors for DC_BOOST pins must be between 22 kΩ to 47 kΩ in non I^2C mode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply Voltage Range	VCC	-0.3	3.8	V
Voltage Range on I/O pins	DxP, DxM, RSTN, EQ, SCL, SDA, DC_BOOST, VREG	-0.3	3.8	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
T_A	Ambient temperature	TUSB214	0		70	°C
		TUSB214I	-40		85	°C
T_J	Junction temperature	TUSB214	0		85	°C
		TUSB214I	-40		105	°C

6.4 Thermal Information

THERMAL METRIC[1]		TUSB214	UNIT
		RWB (VQFN)	
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High-speed active curent	USB channel = HS mode; 480 Mbps traffic; V_{CC} = 3.3V; V_{CC} supply stable; DC Boost = 60 mV		22	30	mA
I_{IDLE_HS}	High-speed idle current	USB channel = HS mode; no traffic; V_{CC} = 3.3V; V_{CC} supply stable; DC Boost = 60 mV		14	22	mA
$I_{SUSPEND\_HS}$	High-speed suspend current	USB channel = HS suspend mode; V_{CC} = 3.3V; V_{CC} supply stable		0.55	1.5	mA
I_{FS_LS}	Full/Low speed current	USB channel = FS mode or LS mode; V_{CC} = 3.3V		0.6	1.5	mA
$I_{DISCONNECT}$	Disconnect current	Host side application; No device attachment; V_{CC} = 3.3V		0.7	1.5	mA
I_{RSTN}	Disable current	RSTN driven low; V_{CC} supply stable; V_{CC} = 3.3V		13	80	µA
I_{LKG_FS}	Pin fail-safe leakage current for SDA, SCL, DC_BOOST, DxP/N, RSTN	V_{CC} = 0 V; Pin at 3.6 V			40	µA
RSTN						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High-level input current	V_{IH} = 3.6 V	-4		4	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	-11		11	µA
EQ						
R_{EQ}	External pull-down resistor on EQ pin.	AC Boost Level 0			160	Ω
		AC Boost Level 1	1.4		2	kΩ
		AC Boost Level 2	3.7		3.9	kΩ
		AC Boost Level 3	6			kΩ
CD, ENA_HS						
V_{OH}	High-level output voltage	I_O = -50µA	2.4			V
V_{OL}	Low-level output voltage	I_O = 50µA			0.4	V
SCL, SDA						
C_{I2CBUS}	I2C Bus capacitance		4		150	pF
DC_BOOST						
V_{IH}	High-level input voltage		2.4		3.6	V
V_{IM}	Mid-level input voltage			1.6		V
V_{IL}	Low-level input voltage		0		0.4	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with LCR meter and device powered down. 1 MHz sinusoid, 30 mVpp ripple		2.4		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{BR_DXX}	DxP/M Bit Rate	USB channel = HS mode; 480 Mbps traffic; VCC supply stable			480.24	Mbps
t_{RISE_DXX}	DxP/M rise time		100			ps
t_{FALL_DXX}	DxP/M fall time		100			ps
$t_{RSTN\_PULSE\_WIDTH}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven	V_{CC} = 3.0 V; Refer to Figure 1	20			µs
t_{STABLE}	VCC stable before RSTN de-assertion	Refer to Figure 1	100			µs
t_{VCC_RAMP}	VCC ramp time		0.2		100	ms

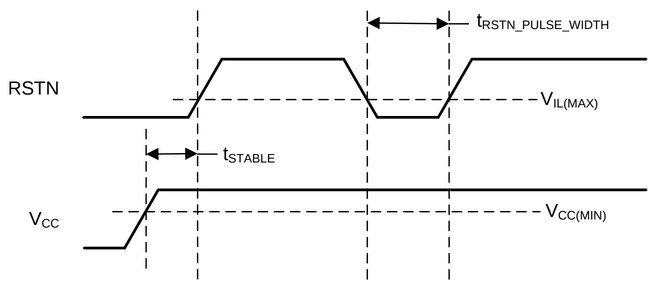


Figure 1. Power On and Reset Timing

6.7 Typical Characteristics

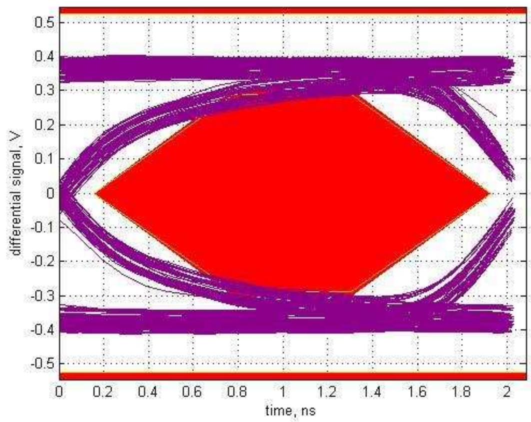


Figure 2. USB2.0 HS Eye Diagram, Host far-end with 2m cable post-channel loss without TUSB214

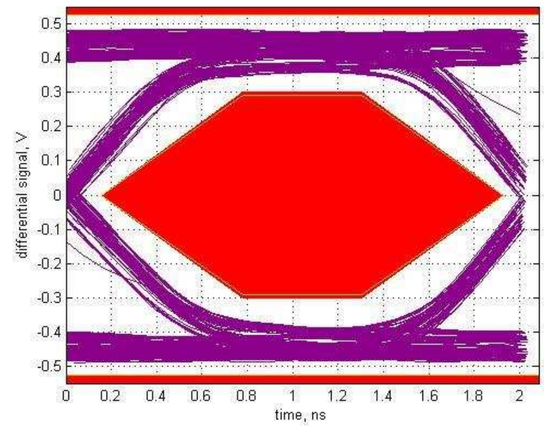


Figure 3. USB 2.0 HS Eye Diagram, Host far-end with 2m cable post-channel loss with TUSB214

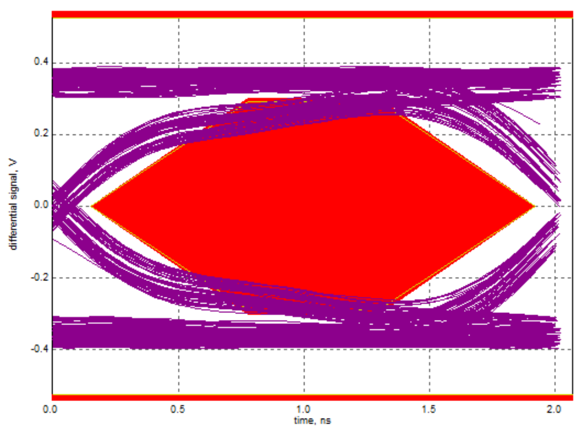


Figure 4. USB2.0 HS Eye Diagram, Host far-end with 5m cable pre-channel loss without TUSB214

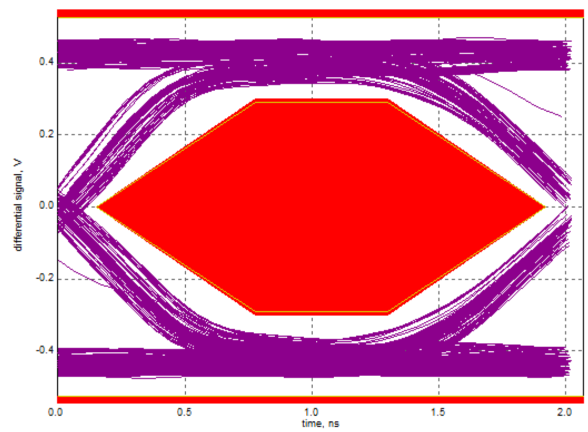


Figure 5. USB2.0 HS Eye Diagram, Host far-end with 5m cable pre-channel loss with TUSB214

7 Detailed Description

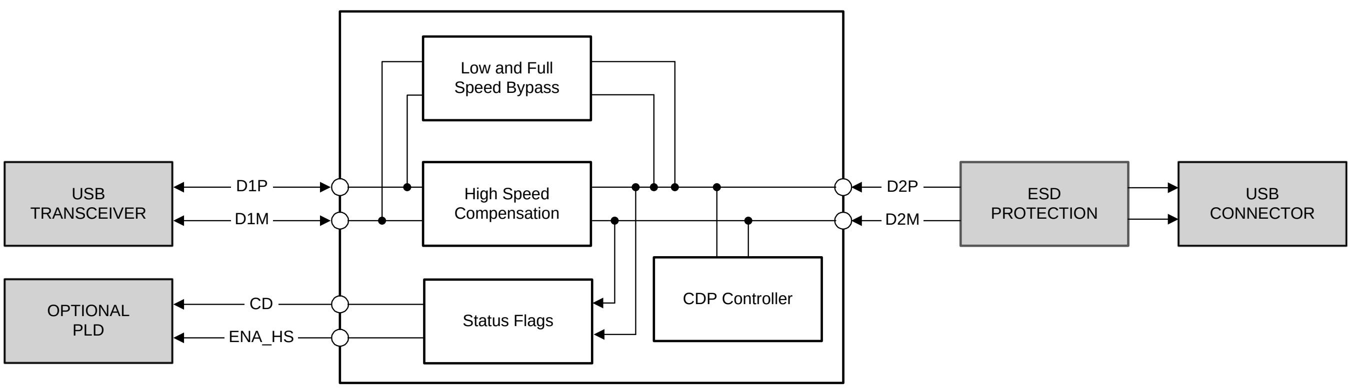
7.1 Overview

The TUSB214 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB214 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications. The TUSB214 includes a USB BC Charging Downstream Port (CDP) controller.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals helping to pass USB HS electrical compliance tests at the connector. Additional DC boost configurable by three level input DC_BOOST helps overcoming the cable losses.

The footprint of TUSB214 allows a board layout using this device such that it does not break the continuity of the DP/DM signal traces. This permits risk free system design of a complete USB channel with flexible use of one or multiple TUSB214 devices as needed for optimal signal integrity. This allows system designers to plan for this device and use it only if signal integrity analysis and/or lab measurements sow a need. If such a need is not warranted, the device can be left unpopulated without any board rework.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EQ

The EQ pin of the TUSB214 is used to configure the AC boost of the device. The four levels are set through different values of an external pulldown resistor at this pin.

7.3.2 DC BOOST

The DC_BOOST pin of the TUSB214 is a tri-level pin, used to set the DC gain of the device according to Table 1.

Table 1. DC Boost Settings

DC BOOST SETTING VIA PIN STRAP	
DC_BOOST	DC Boost Setting (mV)
V_{IL}	40
V_{IM}	60
V_{IH}	80

7.3.3 BC1.2 CDP Support

The TUSB214 main function is a signal conditioner offering the AC/DC Boost features to the incoming DP/DM signals. For applications in which USB host or hub does not provide USB BC charging downstream port (CDP) functionality, the TUSB214 can perform this task.

7.4 Device Functional Modes

7.4.1 Low Speed (LS) Mode

TUSB214 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high.

7.4.2 Full Speed (FS) Mode

TUSB214 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high.

7.4.3 High Speed (HS) Mode

TUSB214 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the DC_BOOST pin and the external pulldown resistance on its EQ pin. CD pin is asserted high.

7.4.4 Shutdown Mode

TUSB214 is disabled when its RSTN pin is asserted low. In shutdown mode the USB channel is still fully operational, but there is neither signal compensation nor any indication from the CD pin as to the status of the channel.

7.4.5 I^2C Mode

TUSB215 supports 100 kHz I^2C for device configuration, status readback and test purposes. This controller is enabled after SCL and SDA pins are sampled high shortly after de-assertion of RSTN. In this mode, the register as described in Table 2 can be accessed by I^2C read/write transaction to 7-bit slave address 0x2C. It is necessary to set CFG_ACTIVE bit and reset it to zero after making changes to the EQ and DC Boost level registers to restart the state machine.

NOTE

All registers or fields in Table 2 which are not specifically mentioned are considered reserved. The default value of these reserved registers or fields must not be changed. It is suggested to perform a read-modify-write operation to maintain the default value of the reserved fields.

Table 2. Register definition

Offset	Bit(s)	Name	Type	Default	Description
0x01	6:4	ACB_LVL	RW	XXX (Sampled from EQ pin at reset)	Sets the level of AC Boost 000 : Level 0 AC Boost programmed [MIN] 001 : Level 1 AC Boost programmed 011 : Level 2 AC Boost programmed 111 : Level 3 AC Boost programmed [MAX]
0x03	0	CFG_ACTIVE	RW	1b	Configuration mode 0 : Normal mode. State machine enabled. 1 : Configuration mode: State machine disabled. After reset, if I2C mode is true (SCL and SDA are both pulled high) it is maintained until it is cleared by an I2C write, but, if I2C mode is not true, it is cleared automatically.

Device Functional Modes (continued)

Table 2. Register definition (continued)

Offset	Bit(s)	Name	Type	Default	Description
0x0E	2:0	DCB_LVL	RW	XXX (Sampled from DC_BOOST pin at reset)	Sets the level of DC Boost 011 : 40mV (DC_Boost = L) 101 : 60mV (DC_Boost = M, default) 111 : 80mV (DC_Boost = H)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The primary purpose of the TUSB214 is to re-store the signal integrity of a USB High Speed channel up to the USB receptacle. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB214 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB214 to control other blocks on the customer platform if so desired. Also, TUSB214 can be used as a CDP controller.

8.2 Typical Application

A typical application is shown in Figure 6. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. If desired, the orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

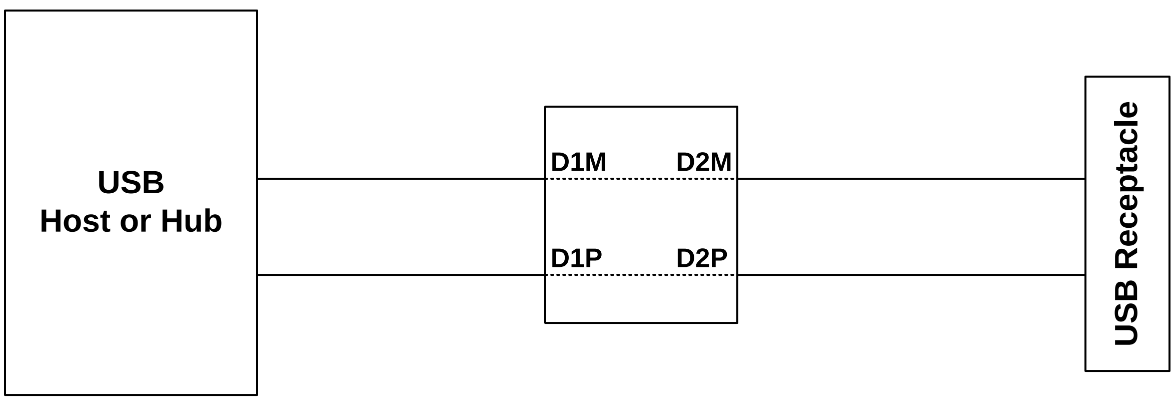


Figure 6. Typical Application

8.2.1 Design Requirements

For this design example, use parameters shown in the table below.

Table 3. Design Parameters

PARAMETER			VALUE
VCC (3.0V to 3.6V)			3.3V
I^2C support required in system (Yes/No)			No
AC Boost	R_{EQ}	Level	AC Boost Level 2: R_{EQ} = 3.83K
	0-ohms	0	
	1.69k +/- 1%	1	
	3.83k +/- 1%	2	
	DNI	3	

Typical Application (continued)

Table 3. Design Parameters (continued)

PARAMETER				VALUE
DC Boost	R_{DC1}	R_{DC2}	Level	Mid DC Level: R_{DC1} = DNI R_{DC2} = DNI
	22k - 47k ohms	Do Not Install (DNI)	40mV Low DC Boost	
	DNI	DNI	60mV Mid DC Boost	
	DNI	22k - 47k ohms	80mV High DC Boost	

8.2.2 Detailed Design Procedure

TUSB214 requires a valid reset signal as described in the power supply recommendations section. The capacitor at RSTN pin is not required if a microcontroller drives the RSTN pin according to recommendations.

VREG pin is the internal LDO output that requires a 0.1-µF external capacitor to GND to stabilize the core.

The ideal AC/DC Boost setting is dependent upon the signal chain loss characteristics of the target platform. The general recommendation is to start with AC Boost level 0, and then increment to AC Boost level 1, etc. when needed. Same applies to the DC boost setting where it is recommended to plan for the required pad to change boost settings.

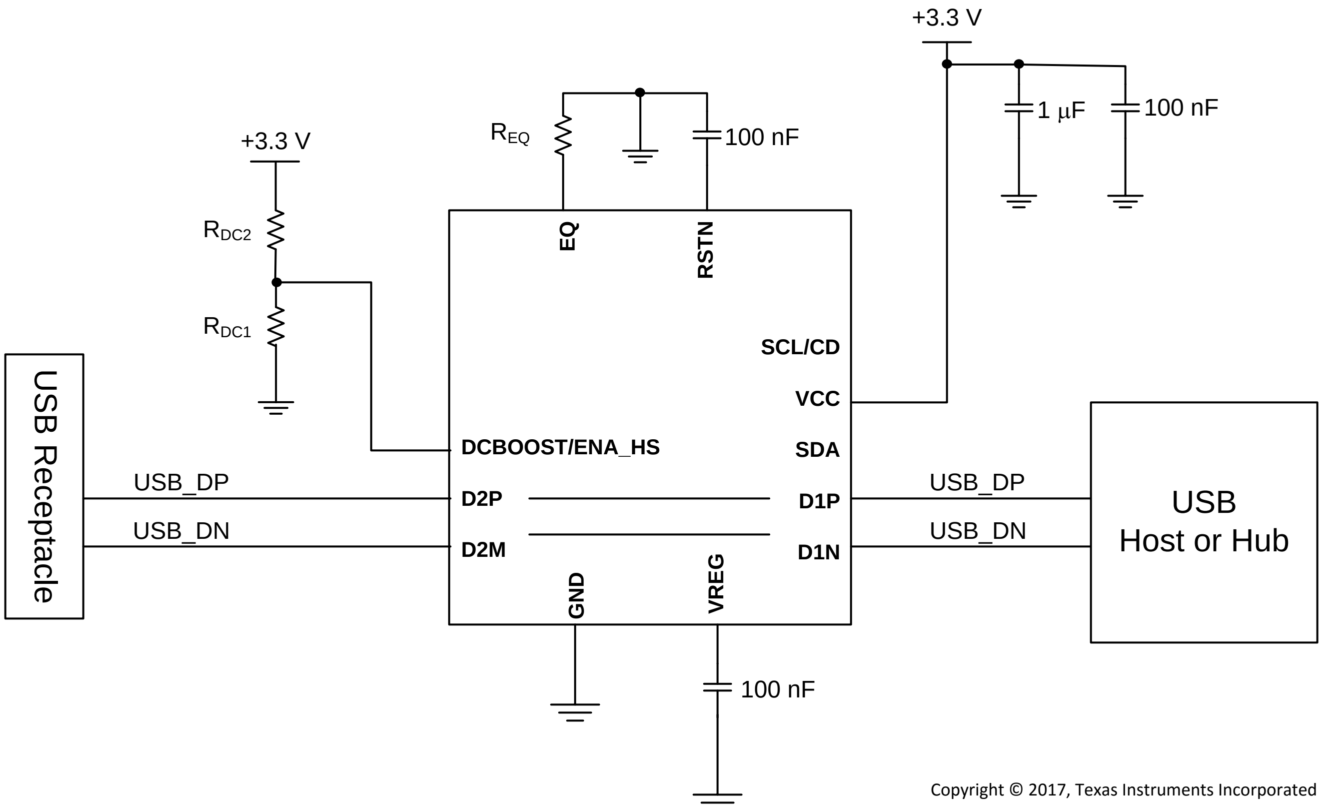
In order for the TUSB214 to recognize any change to the AC or DC boost settings, the RSTN pin must be toggled. This is because the EQ and DC_BOOST pins are latched on power up and the pins are ignored thereafter.

Further D1P has to be shorted to D2P and D1M shorted to D2M on the board for correct functionality of the device.

Placement of the device is also dependent on the application goal. Table 4 summarizes our recommendations.

Table 4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB214 PLACEMENT
Pass USB Near End Mask	Close to measurement point
Pass USB Far End Eye Mask	Close to USB PHY
Cascade multiple TUSB214 to improve device enumeration	Midway between each USB interconnect



D2P must be shorted to D1P on PCB.

D2N must be shorted to D1N on PCB.

Figure 7. Reference Schematic

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

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NOTE

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the 'Electricals' section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB214 to the desired AC and DC boost settings.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB214
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB214
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB214 with different AC and DC boost settings.

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB214 to the desired AC and DC boost settings.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB214

3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB214. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB214 with different AC and DC boost settings.

8.2.3 Application Curves

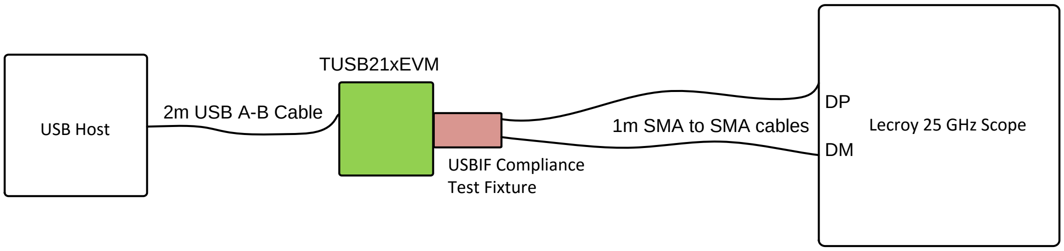

Figure 8. Eye Diagram Bench Setup

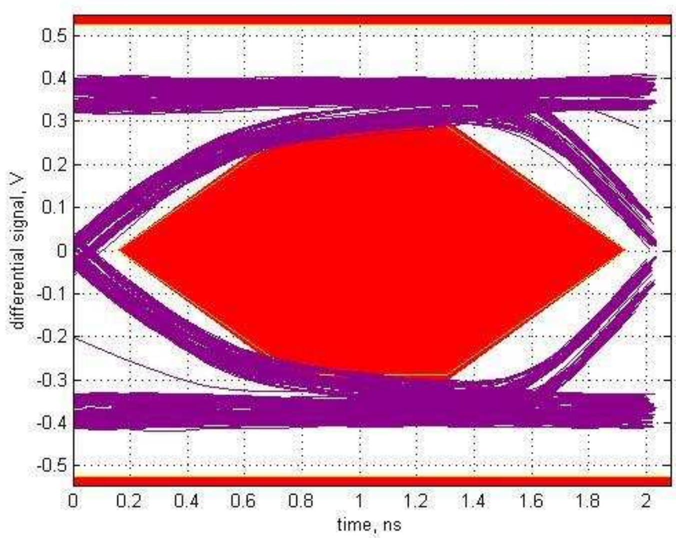

Figure 9. No TUSB214

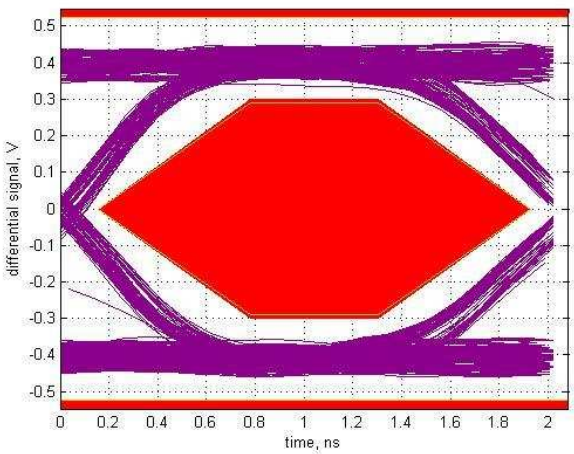

Figure 10. Low DC Boost, AC Boost Level 0

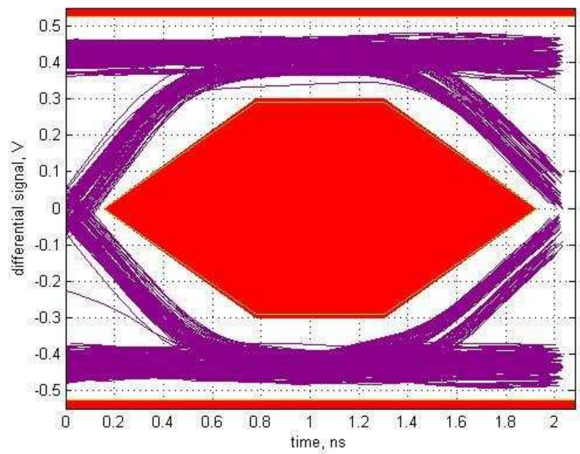

Figure 11. Mid DC Boost, AC Boost Level 0

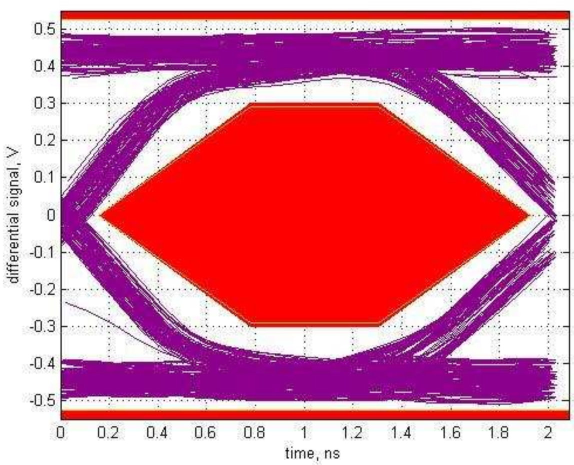

Figure 12. High DC Boost, AC Boost Level 0

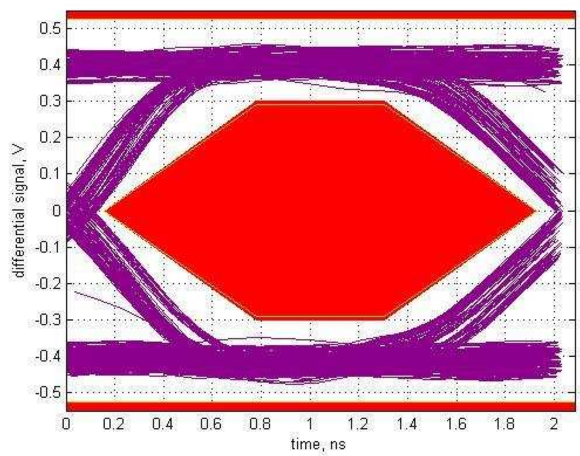

Figure 13. Low DC Boost, AC Boost Level 1

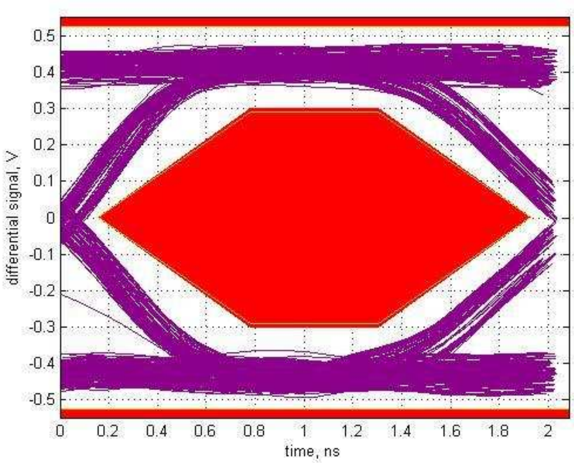

Figure 14. Mid DC Boost, AC Boost Level 1

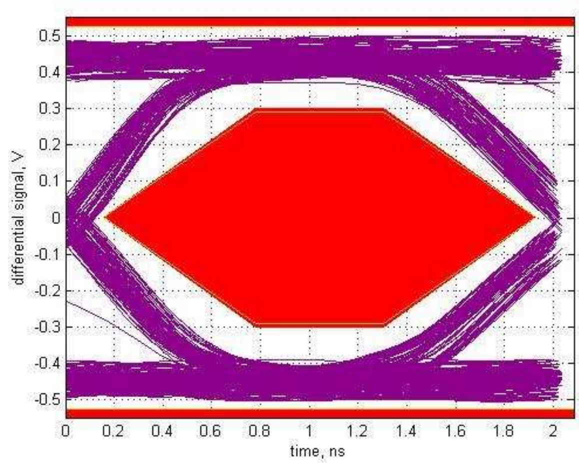

Figure 15. High DC Boost, AC Boost Level 1

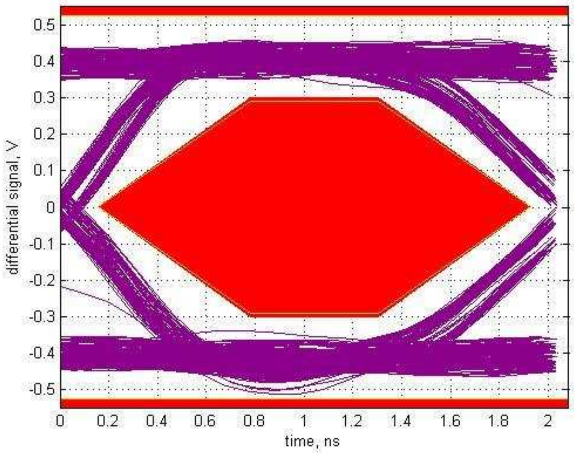

Figure 16. Low DC Boost, AC Boost Level 2

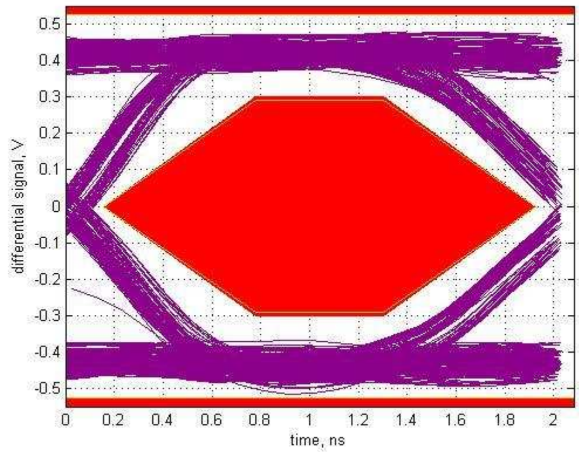

Figure 17. Mid DC Boost, AC Boost Level 2

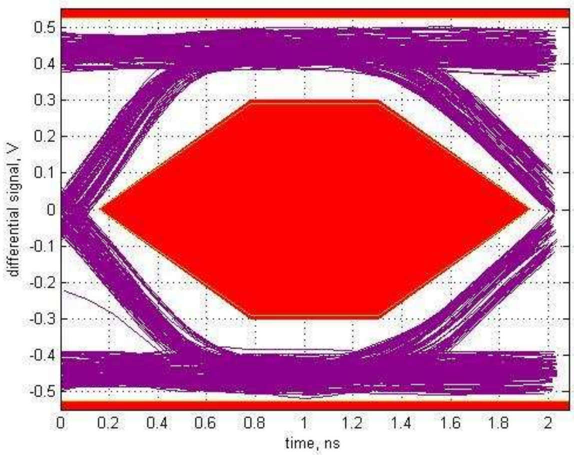

Figure 18. High DC Boost, AC Boost Level 2

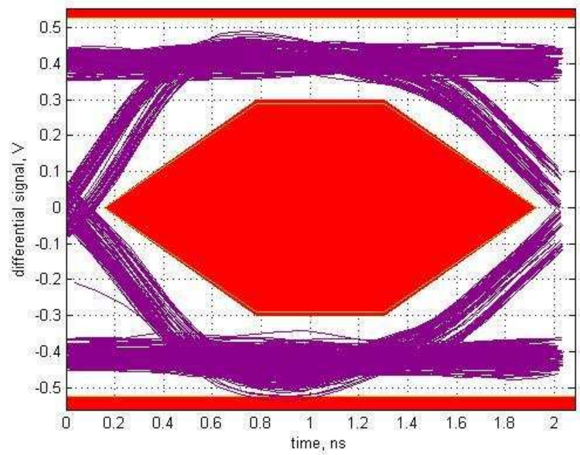

Figure 19. Low DC Boost, AC Boost Level 3

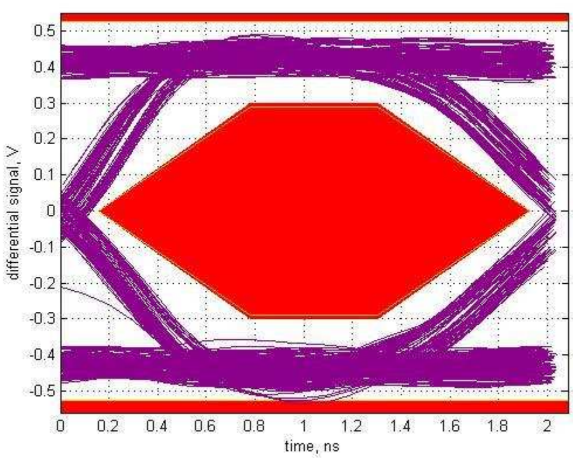

Figure 20. Mid DC Boost, AC Boost Level 3

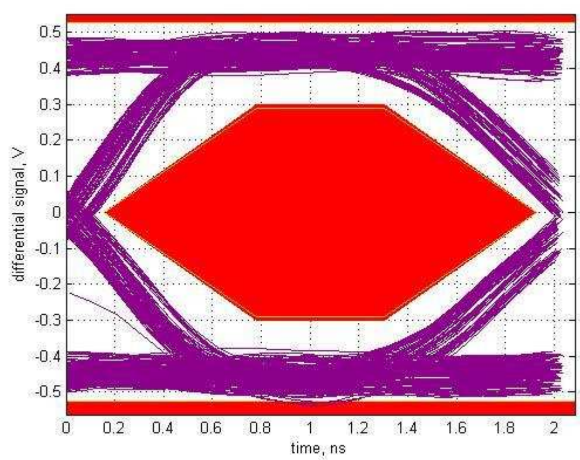

Figure 21. High DC Boost, AC Boost Level 3

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 3 V or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

$$[\text{Ramp Time x } 5] \div [500\ \text{k}\Omega] \tag{1}$$

10 Layout

10.1 Layout Guidelines

The USB signal trace must not be broken when placing TUSB214. Thus, even with the TUSB214 powered down, or not populated, the USB link is still fully operational. To avoid the need for signal vias, it is highly recommend to route the High Speed traces directly underneath the TUSB214 package, as illustrated in the PCB land pattern shown in Figure 22.

Although the land pattern shown below has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. It is recommended to maintain 90 Ω differential routing underneath the device.

All dimensions are in millimetres (mm).

10.2 Layout Example

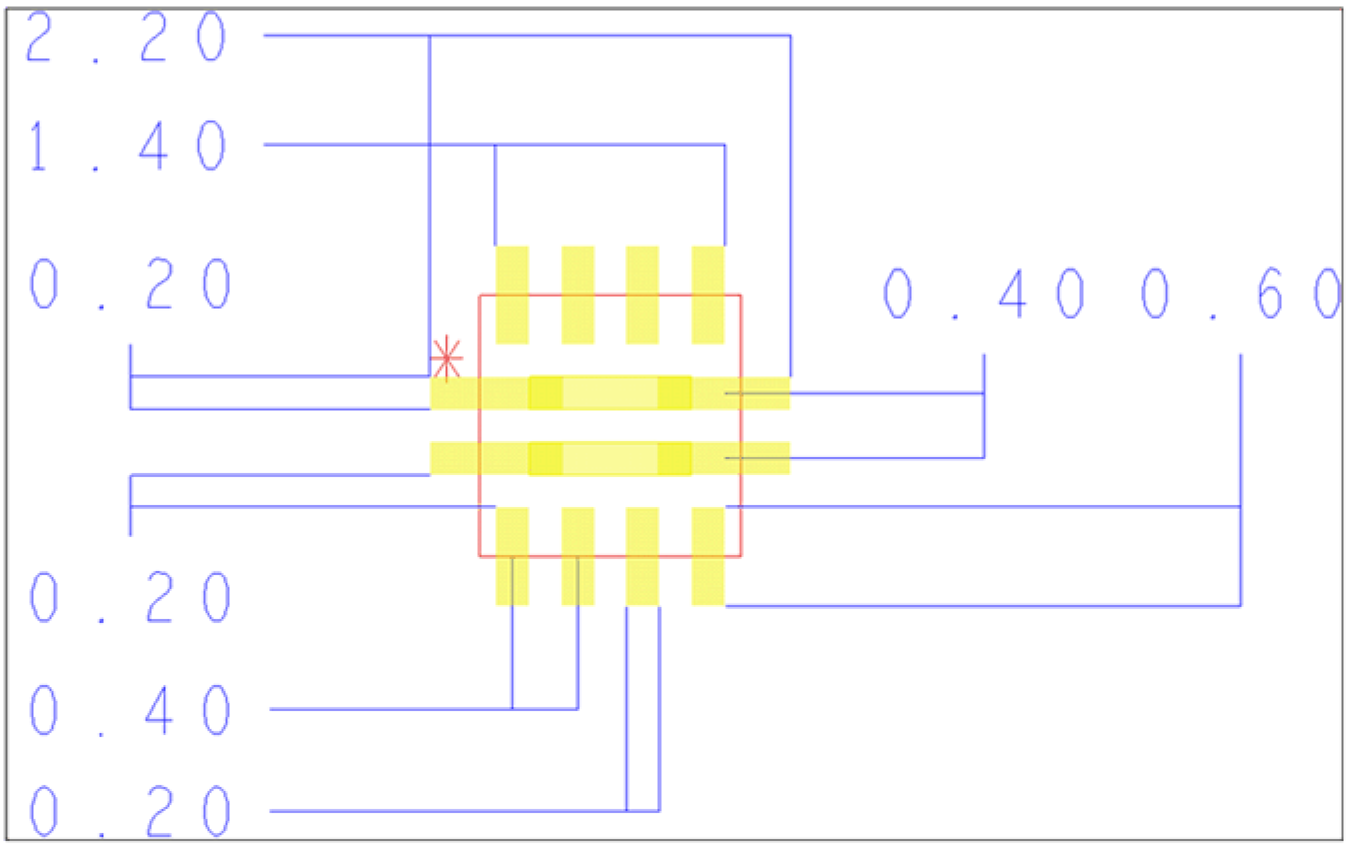

Figure 22. DP and DM Routing Underneath Device Package

11 Device and Documentation Support

11.1 Documentation Support

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB214IRWBR	PREVIEW	X2QFN	RWB	12	3000	TBD	Call TI	Call TI	-40 to 85		
TUSB214IRWBT	PREVIEW	X2QFN	RWB	12	250	TBD	Call TI	Call TI	-40 to 85		
TUSB214RWBR	PREVIEW	X2QFN	RWB	12	3000	TBD	Call TI	Call TI	0 to 70		
TUSB214RWBT	PREVIEW	X2QFN	RWB	12	250	TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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