TSV991, TSV992, TSV994, TSV991A, TSV992A, TSV994A

Rail-to-rail input/output 20 MHz GBP operational amplifiers

Datasheet — production data

Features

- Low input offset voltage: 1.5 mV max (A grade)
- Rail-to-rail input and output
- Wide bandwidth 20 MHz
- Stable for gain ≥ 4 or ≤ -3
- Low power consumption: 820 µA typ
- High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- Low input bias current, 1 pA typ
- ESD internal protection ≥ 5 kV

Related products

- See TSV91 series for unity-gain stable amplifiers

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning and active filtering
- Medical instrumentation
- Automotive applications

Description

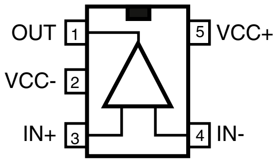
The TSV991, TSV992 and TSV994 family of single, dual, and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

These devices feature an excellent speed/power consumption ratio, offering a 20 MHz gain-bandwidth, stable for gains above 4 (100 pF capacitive load), while consuming only 1.1 mA maximum at 5 V. They also feature an ultra-low input bias current.

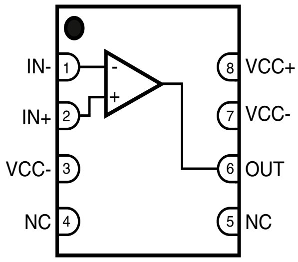
These characteristics make the TSV99x family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Pin connections (top view)

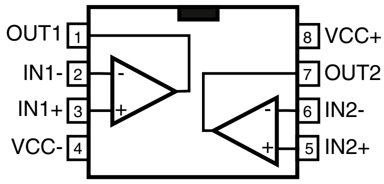
SOT23-5



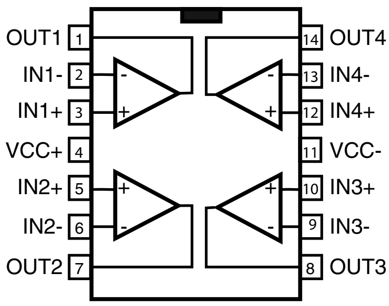
DFN8 2x2



MiniSO-8, SO-8



SO-14, TSSOP14



Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{id}	Differential input voltage (2)	$\pm V_{CC}$	V
V_{in}	Input voltage(3)	V_{CC-} -0.2 to V_{CC+} +0.2	V
I_{in}	Input current(4)	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(5)(6) DFN8 2x2 SOT23-5 SO-8 MiniSO-8 SO-14 TSSOP14	 57 250 125 190 103 100	°C/W
R_{thjc}	Thermal resistance junction to case SOT23-5 SO-8 MiniSO-8 SO-14 TSSOP14	 81 40 39 31 32	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: Human body model(7)	5	kV
	MM: Machine model(8)	400	V
	CDM: Charged device model(9) SOT23-5, SO-8, MiniSO-8 DFN8 2x2 TSSOP14 SO-14	 1500 1500 750 500	V
	Latch-up immunity	200	mA

1. Value with respect to V_{DD} pin.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC}-V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: 200 pF charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.1 to V_{CC+} +0.1	V
T_{op}	Operating free air temperature range	-40 to +125	°C

2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +2.5 V, V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, with R_L connected to $V_{CC}/2$, full temperature range (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV99x	T_{op} = 25° C		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage TSV99xA	T_{op} = 25° C			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current(2) ($V_{out} = V_{CC}/2$)	T_{op} = 25° C		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current(2) ($V_{out} = V_{CC}/2$)	T_{op} = 25° C		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 2.5 V, V_{out} = 1.25 V, T_{op} = 25° C	58	75		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.5 V to 2 V, T_{op} = 25° C	80	89		
		$T_{min} < T_{op} < T_{max}$	75			
V_{CC}-V_{OH}	High level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$		15	40	mV
		R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$		15	40	
		R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$		45	150	
I_{out}	I_{sink}	V_o = 2.5 V, T_{op} = 25° C	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	V_o = 0 V, T = 25° C	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$, $T_{min} < T_{op} < T_{max}$		0.78	1.1	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25° C		20		MHz
Gain	Minimum gain for stability	Phase margin = 45°, R_f = 10kΩ, R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25° C				V/V
		Positive gain configuration		4		
		Negative gain configuration		-3		
SR	Slew rate	R_L = 2kΩ, C_L = 100 pF, T_{op} = 25° C		10		V/μs

Table 3. Electrical characteristics at V_{CC+} = +2.5 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, with R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	f = 10 kHz, T_{op} = 25° C		21		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion	G = -3, f = 1 kHz, R_L = 2 kΩ, Bw = 22 kHz, V_{icm} = V_{CC}/2, V_{out} = 2 V_{pp}, T_{op} = 25° C		0.0025		%

1. All parameter limits at temperatures other than 25° C are guaranteed by correlation.
2. Guaranteed by design.

Table 4. Electrical characteristics at V_{CC+} = +3.3 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, with R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV99x	T_{op} = 25° C		0.1	4.5	mV
		$T_{min} < T_{op} < T_{max}$			7.5	
	Offset voltage TSV99xA	T_{op} = 25° C			1.5	
		$T_{min} < T_{op} < T_{max}$			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		-	2	-	μV/°C
I_{io}	Input offset current(2) (V_{out} = V_{CC}/2)	T_{op} = 25° C		1	10	pA
		$T_{min} < T_{op} < T_{max}$			100	
I_{ib}	Input bias current(2) (V_{out} = V_{CC}/2)	T_{op} = 25° C		1	10	
		$T_{min} < T_{op} < T_{max}$			100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V, T_{op} = 25° C	60	78		dB
		$T_{min} < T_{op} < T_{max}$	55			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V, T=25° C	80	90		
		$T_{min} < T_{op} < T_{max}$	75			
V_{CC}- V_{OH}	High level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$		15	40	mV
		R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$ R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$	-	15 45	40 150	
I_{out}	I_{sink}	V_o = 3.3 V, T_{op} = 25° C	18	32		mA
		$T_{min} < T_{op} < T_{max}$	16			
	I_{source}	V_o = 0 V, T_{op} = 25° C	18	35		
		$T_{min} < T_{op} < T_{max}$	16			
I_{CC}	Supply current (per operator)	No load, V_{out} = V_{CC}/2, $T_{min} < T_{op} < T_{max}$		0.8	1.1	

Table 4. Electrical characteristics at V_{CC+} = +3.3 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, with R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25° C		20		MHz
Gain	Minimum gain for stability	Phase margin = 45°, R_f = 10kΩ, R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25° C Positive gain configuration Negative gain configuration		 4 -3		V/V
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25° C		10		V/μs
e_n	Equivalent input noise voltage	f = 10 kHz, T_{op} = 25° C		21		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion	G = -3, f = 1 kHz, R_L = 2 kΩ, Bw = 22 kHz, V_{icm} = V_{CC}/2, V_{out} = 2.8 V_{pp}, T_{op} = 25° C		0.0018		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Guaranteed by design.

Table 5. Electrical characteristics at V_{CC+} = +5 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV99x	T_{op} = 25° C		0.1	4.5	mV
		T_{min} < T_{op} < T_{max}			7.5	
	Offset voltage TSV99xA	T_{op} = 25° C			1.5	
		T_{min} < T_{op} < T_{max}			3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		-	2	-	μV/°C
I_{io}	Input offset current(2) (V_{out} = V_{CC}/2)	T_{op} = 25° C		1	10	pA
		T_{min} < T_{op} < T_{max}			100	
I_{ib}	Input bias current(2) (V_{out} = V_{CC}/2)	T_{op} = 25° C		1	10	
		T_{min} < T_{op} < T_{max}			100	
CMR	Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V, T_{op} = 25° C	62	82		dB
		T_{min} < T_{op} < T_{max}	57			
SVR	Supply voltage rejection ratio, 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{CC} = 2.5 to 5 V	70	86		
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V, T = 25° C	80	91		
		T_{min} < T_{op} < T_{max}	75			

Table 5. Electrical characteristics at V_{CC+} = +5 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, R_L connected to V_{CC}/2, full temperature range (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}- V_{OH}	High level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$		15	40	mV
		R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$		45	150	
V_{OL}	Low level output voltage	R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$		15	40	
		R_L = 600 Ω, $T_{min} < T_{op} < T_{max}$		45	150	
I_{out}	I_{sink}	V_o = 5 V, T_{op} = 25° C	18	32		mA
		$T_{min} < T_{amb} < T_{max}$	16			
	I_{source}	V_o = 0 V, T_{op} = 25° C	18	35		
		$T_{min} < T_{amb} < T_{max}$	16			
I_{CC}	Supply current (per operator)	No load, V_{out} = 2.5 V, $T_{min} < T_{op} < T_{max}$		0.82	1.1	mA
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz, T_{op} = 25° C		20		MHz
Gain	Minimum gain for stability	Phase margin = 45°, R_f = 10kΩ, R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25° C Positive gain configuration Negative gain configuration		 4 -3		V/V
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, T_{op} = 25° C		10		V/μs
e_n	Equivalent input noise voltage	f = 10 kHz, T_{op} = 25° C		21		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion	G = -3, f = 1 kHz, R_L = 2 kΩ, Bw = 22 kHz, V_{icm} = V_{CC}/2, V_{out} = 4.4 V_{pp}, T_{op} = 25° C		0.0014		%

1. All parameter limits at temperatures other than 25°C are guaranteed by correlation.
2. Guaranteed by design.

Figure 1. Input offset voltage distribution at T = 25° C

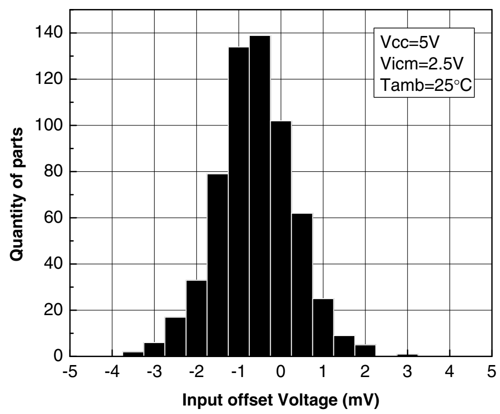


Figure 2. Input offset voltage distribution at T = 125° C

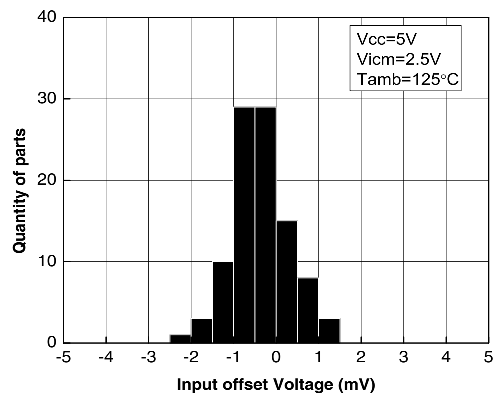


Figure 3. Supply current vs. input common mode voltage at V_{CC} = 2.5 V

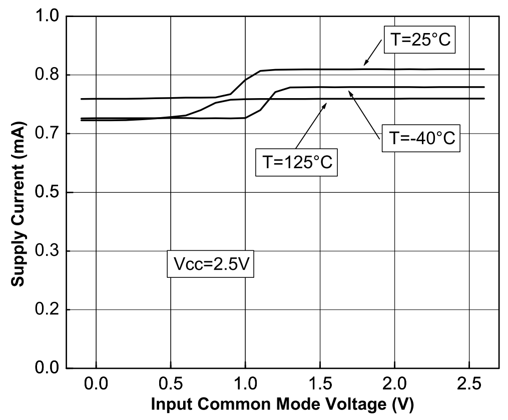


Figure 4. Supply current vs. input common mode voltage at V_{CC} = 5 V

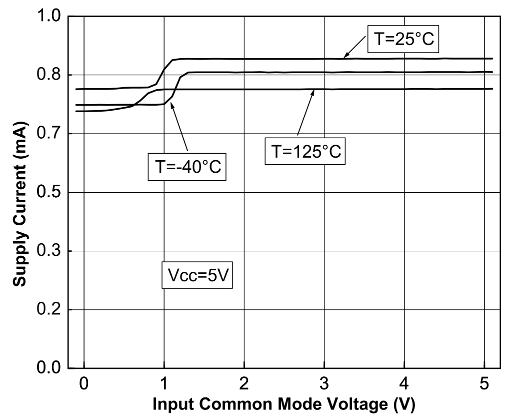


Figure 5. Output current vs. output voltage at V_{CC} = 2.5 V

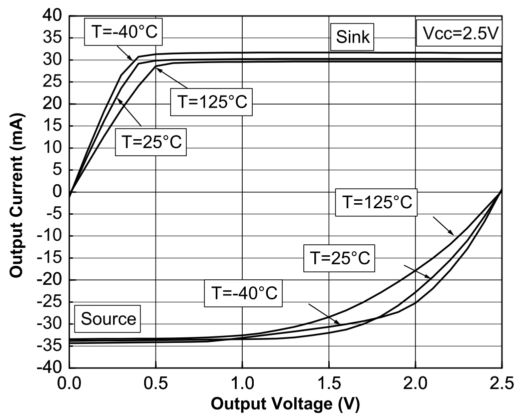


Figure 6. Output current vs. output voltage at V_{CC} = 5 V

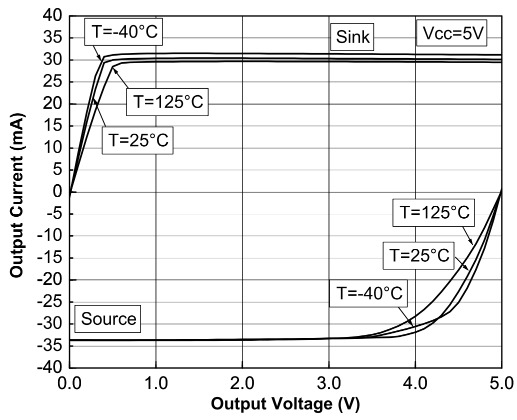


Figure 7. Voltage gain and phase vs frequency at V_{CC} = 5 V and V_{icm} = 0.5 V

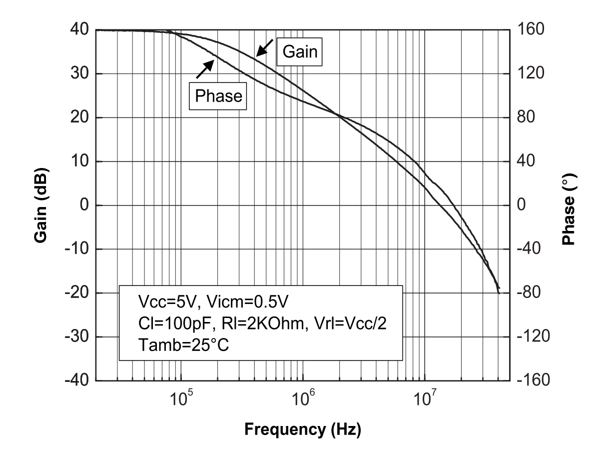


Figure 8. Voltage gain and phase vs frequency at V_{CC} = 5 V and V_{icm} = 2.5 V

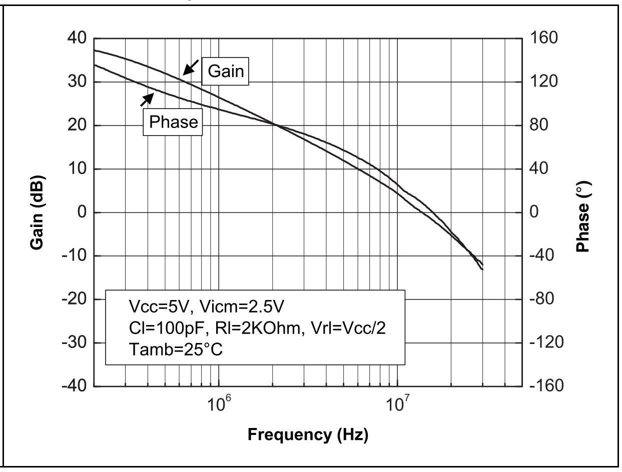


Figure 9. Positive slew rate

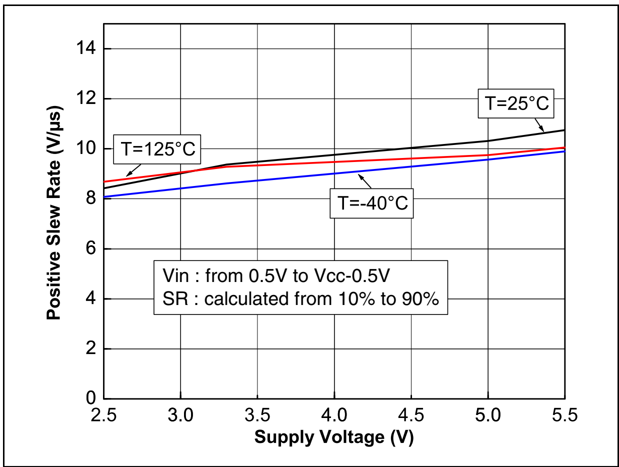


Figure 10. Negative slew rate

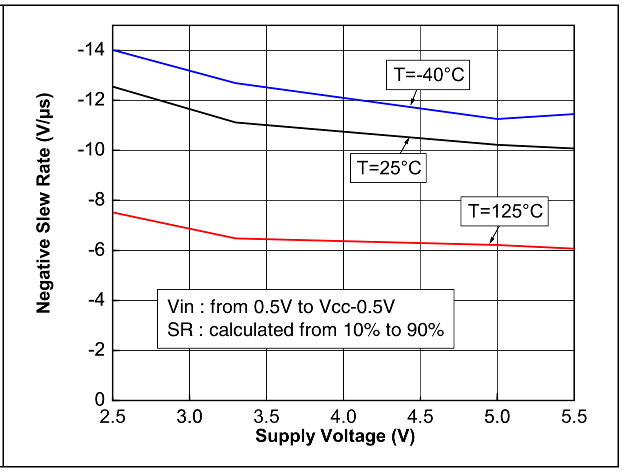


Figure 11. Distortion + noise vs. frequency

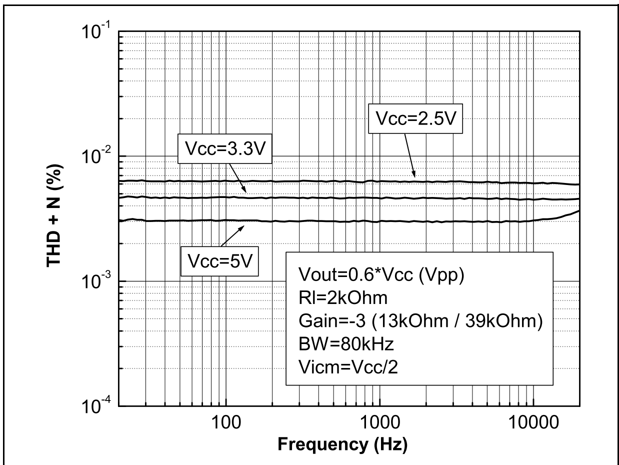


Figure 12. Distortion + noise vs. output voltage

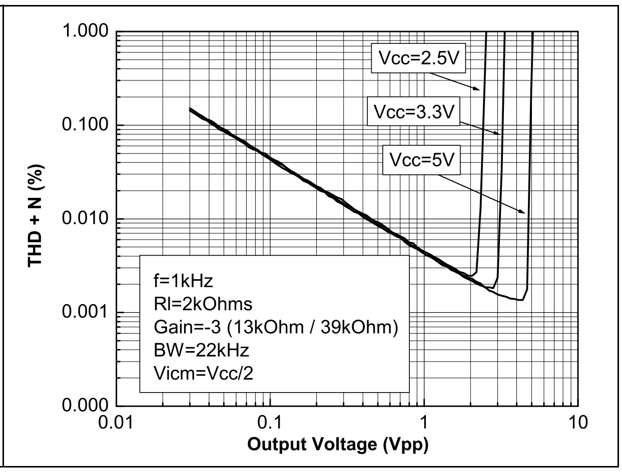


Figure 13. Noise vs. frequency

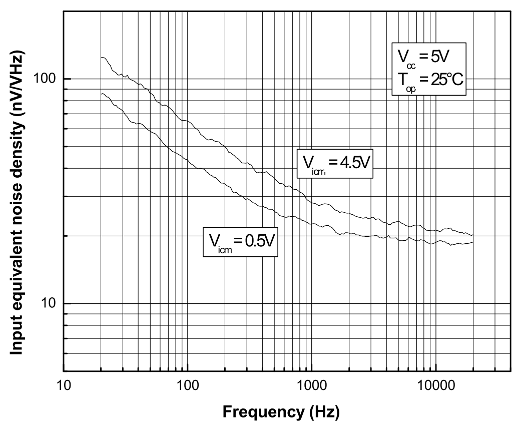
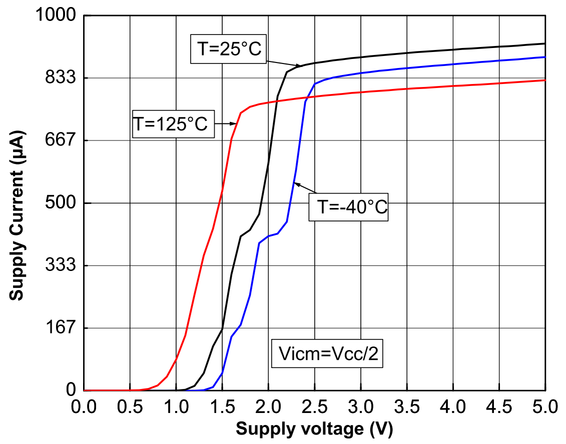


Figure 14. Supply current vs. supply voltage



3 Application information

3.1 Driving resistive and capacitive loads

These products are low-voltage, low-power operational amplifiers optimized to drive rather large resistive loads above 2 kΩ.

TSV99x products are not unity gain stable. To ensure proper stability they must be used in a gain configuration, with a minimum gain of -3 or +4.

However, they can be used in a “follower“ configuration by adding a small, in-series resistor at the output, which drastically improves the stability of the device (*Figure 15* shows the recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on the bench and simulated with the simulation model.

Figure 15. In-series resistor vs. capacitive load when TSV99x used in follower configuration

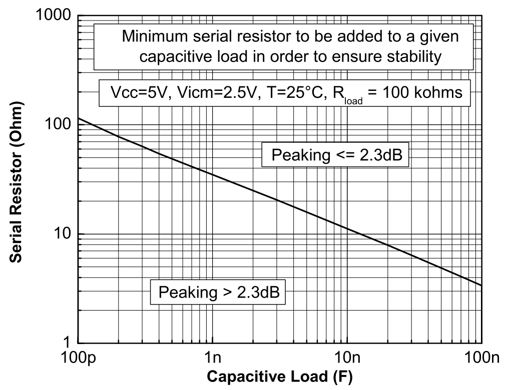
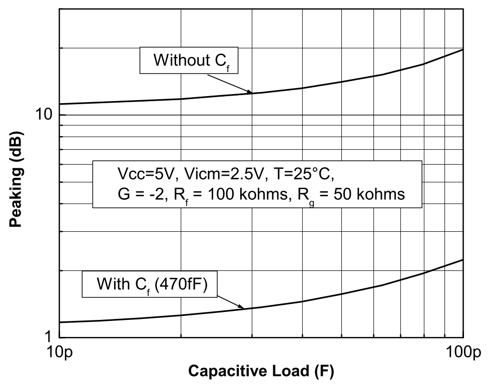


Figure 16. Peaking versus capacitive load, with or without feedback capacitor in inverting gain configuration



Another way to improve stability and reduce peaking is to add a capacitor in parallel with the feedback resistor. As shown in *Figure 16*, the feedback capacitor drastically reduces the peaking versus capacitive load (inverting gain configuration, gain = -2).

3.2 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

3.3 Macromodel

An accurate macromodel of the TSV99x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV99x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *however, it does not replace on-board measurements*.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 SOT23-5 package information

Figure 17. SOT23-5 package mechanical drawing

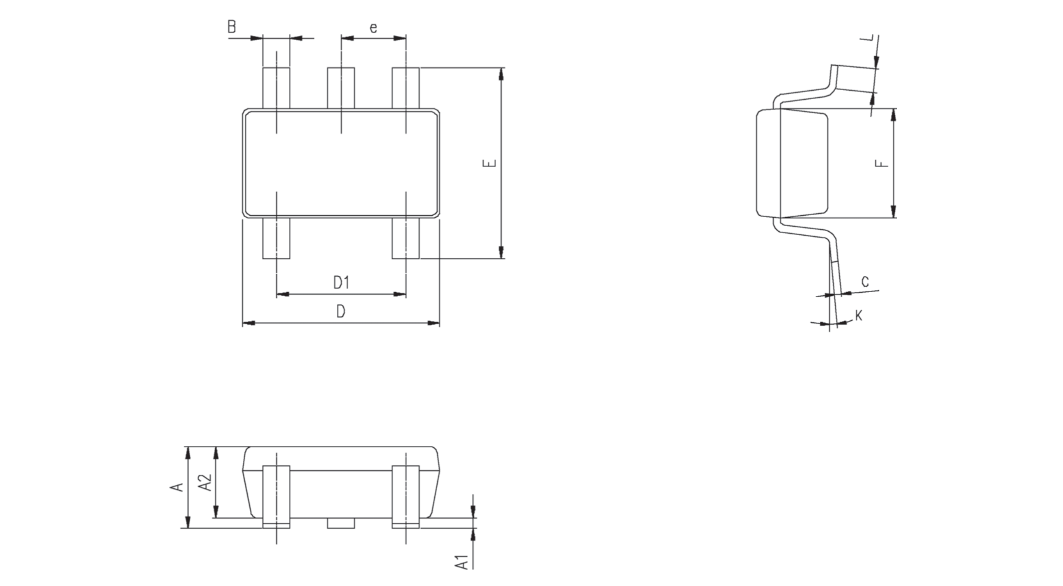


Table 6. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

4.2 DFN8 2x2 package information

Figure 18. DFN8 2x2 package mechanical drawing

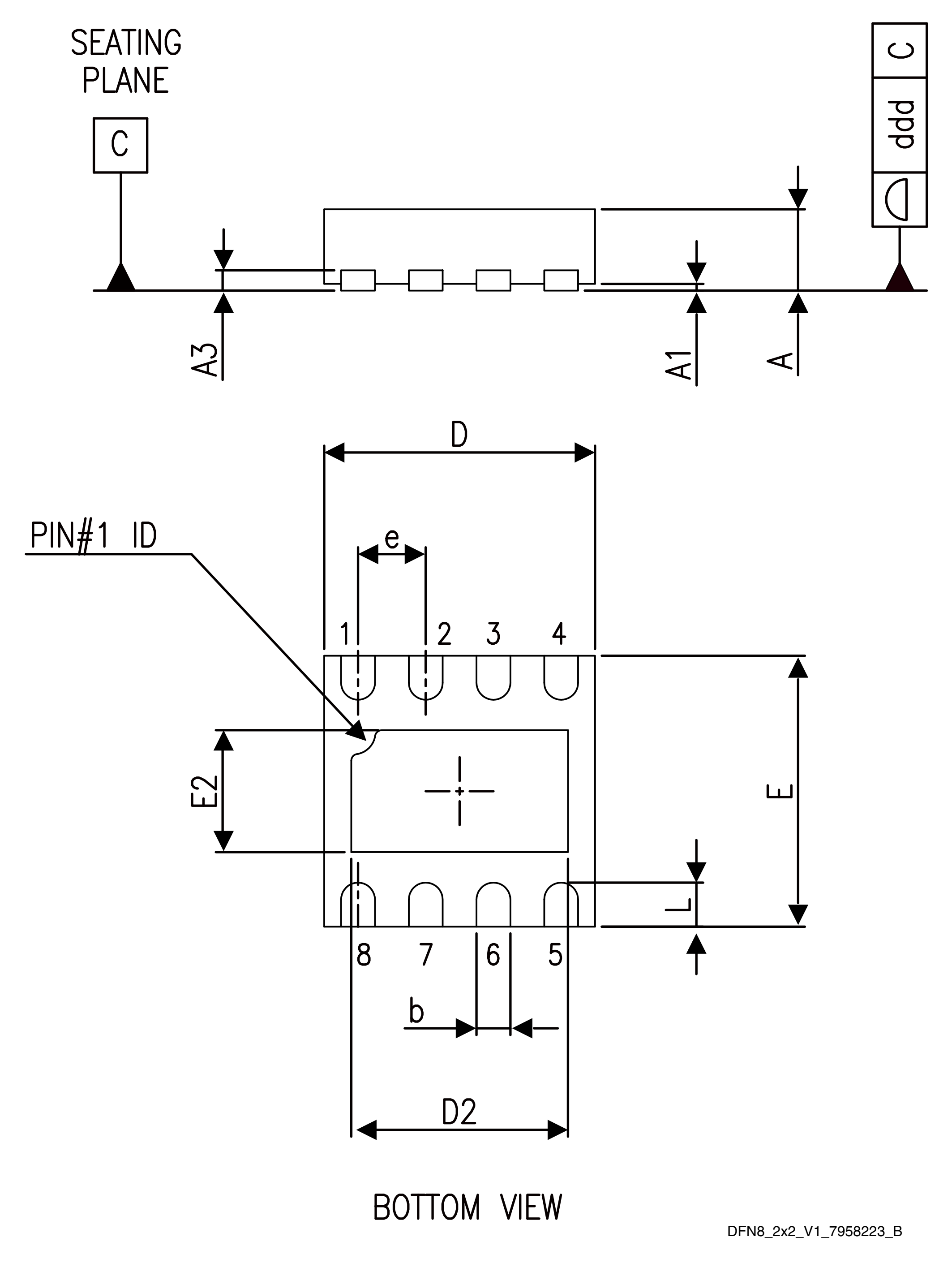
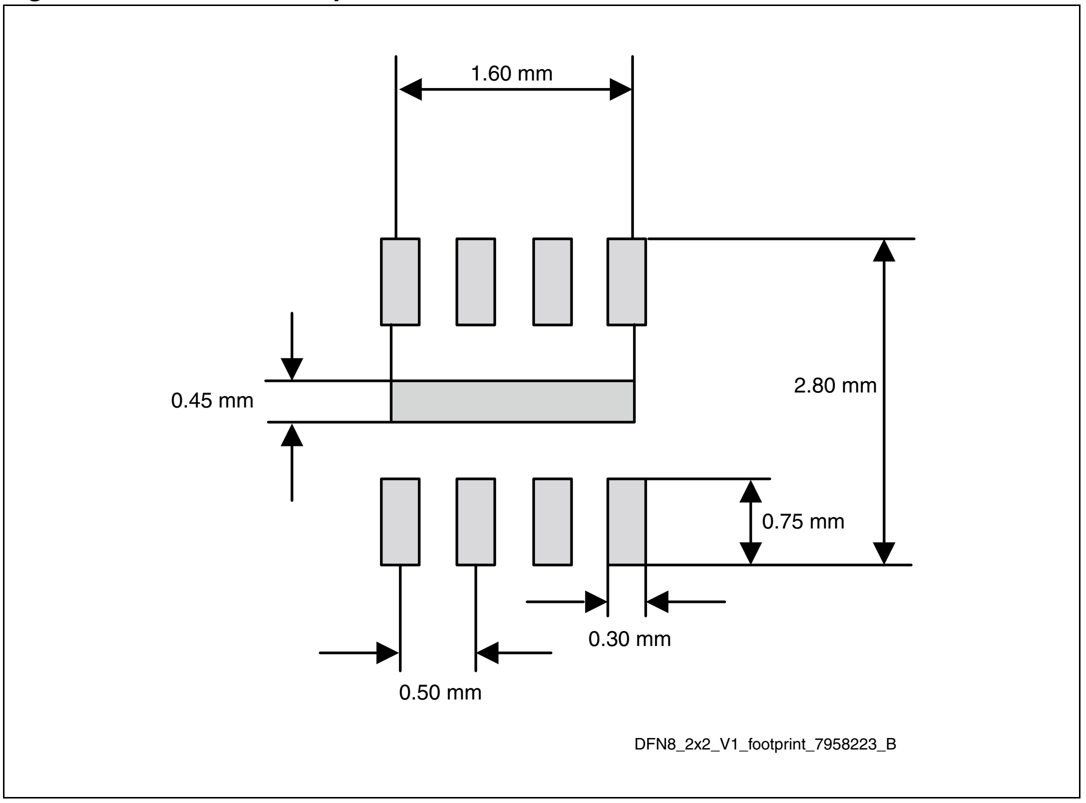


Table 7. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003

1. Values in inches are rounded to three decimal digits.

Figure 19. DFN8 2x2 footprint recommendation



4.3 MiniSO-8 package information

Figure 20. MiniSO-8 package mechanical drawing

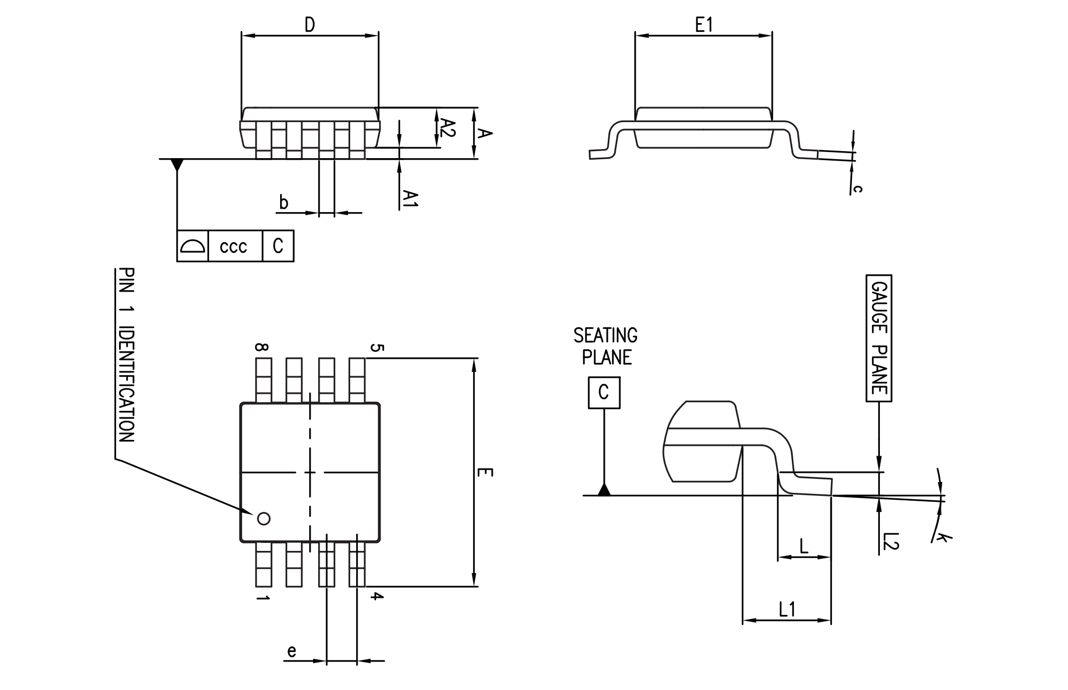


Table 8. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

4.4 SO-8 package information

Figure 21. SO-8 package mechanical drawing

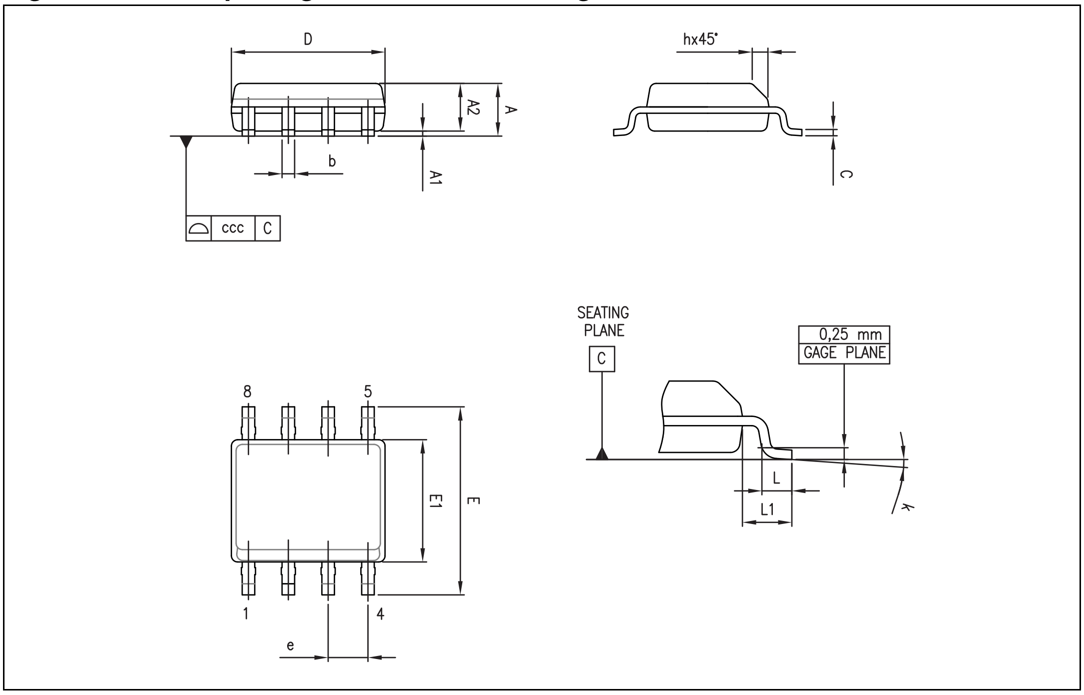


Table 9. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

4.5 TSSOP14 package information

Figure 22. TSSOP14 package mechanical drawing

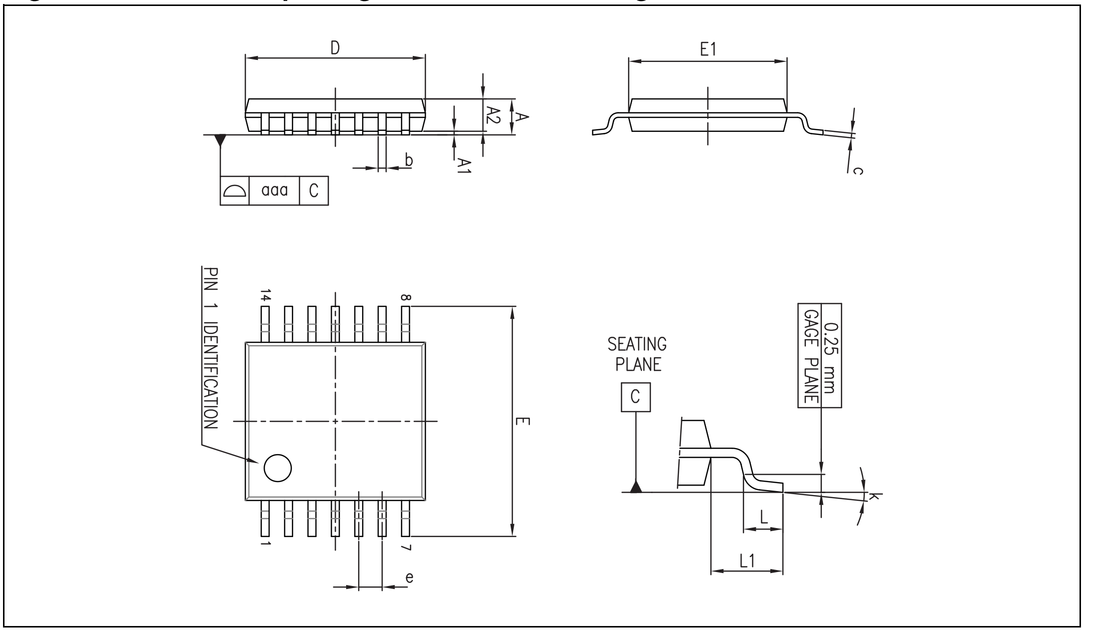


Table 10. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

4.6 SO-14 package information

Figure 23. SO-14 package mechanical drawing

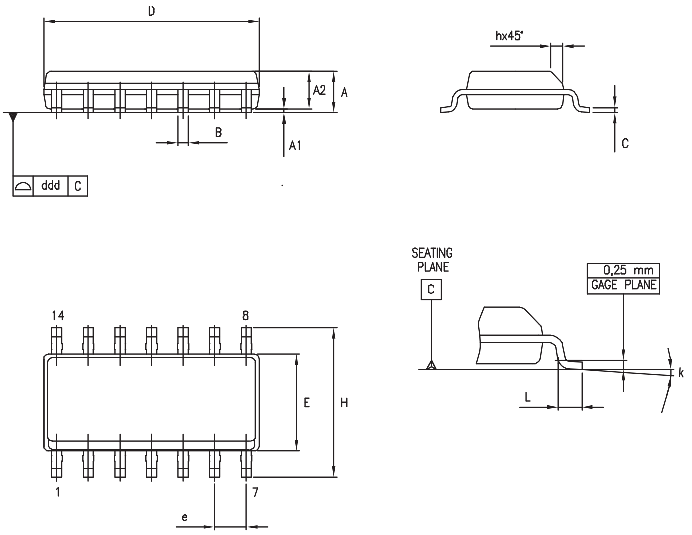


Table 11. SO-14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

5 Ordering information

Table 12. Order codes[1]

Order code	Temperature range	Package	Packing	Marking
TSV991ILT	-40° C to +125° C	SOT23-5	Tape & reel	K130
TSV991AILT				K129
TSV991IQ2T		DFN8 2x2		K1E
TSV992IST		MiniSO-8		K132
TSV992AIST				K135
TSV992ID TSV992IDT		SO-8	Tube Tape & reel	V992I
TSV992AID TSV992AIDT			Tube Tape & reel	V992AI
TSV994IPT		TSSOP14	Tape & reel	V994I
TSV994AIPT				V994AI
TSV994ID TSV994IDT		SO-14[1]	Tube Tape & reel	V994I
TSV994AID TSV994AIDT			Tube Tape & reel	V994AI
TSV991IYLT[2]	-40° C to +125° C Automotive grade	SOT23-5	Tape & reel	K149
TSV991AIYLT[2]				K150
TSV992IYDT[2]		SO-8	Tape & reel	V992IY
TSV992AIYDT[2]			Tape & reel	V992AY
TSV992IYST[2]		MiniSO-8	Tape & reel	K149
TSV992AIYST[2]				K150
TSV994IYDT[2]		SO-14[1]	Tape & reel	V994IY
TSV994AIYDT[2]			Tape & reel	V994AY
TSV994IYPT[2]		TSSOP14	Tape & reel	V994IY
TSV994AIYPT[2]				V994AY

1. All packages are Moisture Sensitivity Level 1 as per Jedec J-STD-020-C, except SO-14 which is Jedec level 3.
2. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
31-Jul-2006	1	Preliminary data release for product under development.
07-Nov-2006	2	Final version of datasheet.
12-Dec-2006	3	Noise and distortion figures added.
07-Jun-2007	4	ESD tolerance modified for SO-14, CDM in *Table 1: Absolute maximum ratings*. Automotive grade commercial products added in *Table 12: Order codes*. Note about SO-14 added in *Table 12: Order codes*. Limits in temperature added in *Section 2: Electrical characteristics*.
11-Feb-2008	5	Corrected MiniSO-8 package information. Corrected footnote for automotive grade order codes in order code table. Improved presentation of package information.
25-May-2009	6	Added input current information in table *Table 1: Absolute maximum ratings*. Added *Chapter 3: Application information*. Updated all packages in *Chapter 4: Package information*. Added new order codes: TSV991IYLT, TSV991AIYLT, TSV992IYST, TSV992AIYST, TSV994IYPT, TSV994AIYPT in *Table 12: Order codes*.
19-Oct-2009	7	Added A versions of devices in title on cover page. Added parameters for full temperature range in *Table 3*, *Table 4*, *Table 5*. Removed *gain margin* and *phase margin* parameters in *Table 3*, *Table 4* and *Table 5*. These parameters have been replaced by the *gain* parameter (minimum gain for stability). Added *Figure 14* and *Figure 16*.
14-Jan-2010	8	Added parameters for full temperature range in *Table 3*, *Table 4* and *Table 5*. Modified *Note 2* relative to automotive grade in *Table 12: Order codes*.
22-Oct-2012	9	Document status changed to production data. Modified gain value in *Features* and *Description*. Added DFN8 2x2 pin connection diagram. *Table 1: Absolute maximum ratings*: added package DFN8 2x2 to rows R_{thja} and ESD. *Table 3*, *Table 4*, and *Table 5*: replaced “DV_{io}” with $\Delta V_{io}/\Delta T$; modified “Gain” and “THD+N” conditions and typical values. *Figure 7* and *Figure 8*: added arrows indicating “Gain” and ‘Phase”.

Table 13. Document revision history

Date	Revision	Changes
22-Oct-2012	9 cont'd	*Figure 11* and *Figure 12*: updated. Added *Figure 18: DFN8 2x2 package mechanical drawing* and *Figure 19: DFN8 2x2 footprint recommendation*. *Table 12: Order codes*: updated automotive grade qualification and added order code of DFN8 package.