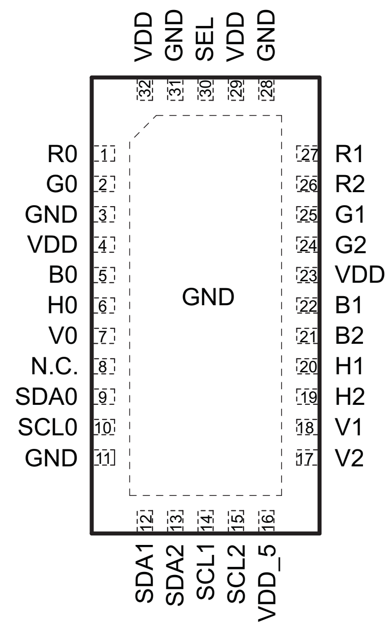
7-CHANNEL, 1:2 VIDEO SWITCH WITH INTEGRATED LEVEL SHIFTERS

Check for Samples: TS3V713EL

FEATURES

- **Supports 7-channel VGA Signals (R, G, B, H_{SYNC}, V_{SYNC}, DDC CLK, and DDC DAT)**
- **Operating Voltage**
  - **V_{DD} = 3.3 V ±10%**
  - **V_{DD_5} = 5 V ±10%**
- **High Bandwidth of 1.3 GHz (–3 dB)**
- **R, G, B Switches**
  - **R_{ON} = 4 Ω (Typ.)**
  - **C_{ON} = 8 pF (Typ.)**
- **Integrated Level Shifting Buffers for H_{SYNC} and V_{SYNC} Channels**
- **Voltage Clamping NMOS Switches for SCL and SDA Channels**
- **ESD Performance (Pins 12–15, 17–22, 24–27)**
  - **±2-kV Contact Discharge (IEC61000-4-2)**
  - **8 kV Human Body Model (JESD22-A114E)**
- **ESD Performance (All Pins)**
  - **4 kV Human Body Model (JESD22-A114E)**
- **32-Pin Quad Flat Pack No-Lead (QFN) Package**

RTG PACKAGE (TOP VIEW)



The exposed center pad must be connected to GND.

APPLICATIONS

- **Notebook Computers**
- **Docking Stations**
- **KVM Switches**

DESCRIPTION/ORDERING INFORMATION

The TS3V713EL is a high bandwidth, 7-channel video multiplexer/demultiplexer for switching between a single VGA source and one of two end points. The device is designed for ensuring video signal integrity and minimizing video signal attenuation by providing high bandwidth of 1.3 GHz.

The TS3V713EL has integrated level shifting buffers for the H_{SYNC} and V_{SYNC} signals which provide voltage level translation between 3.3V and 5V logic. The SCL and SDA lines use NMOS switches which clamp the output voltage to 1 V below V_{DD}.

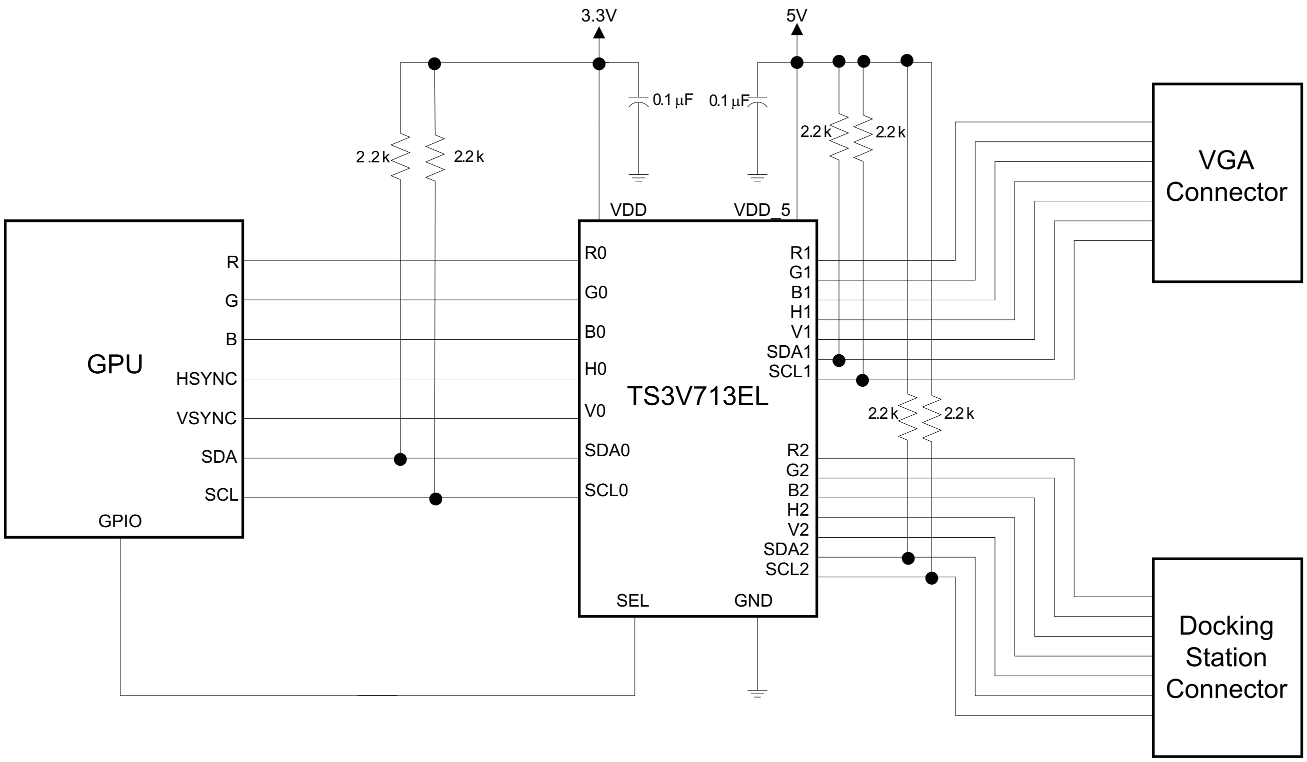
The video signals are protected against ESD with integrated diodes to V_{DD} and GND that support levels up to ±2 kV Contact Discharge (IEC61000-4-2) and 8 kV Human Body Model (JESD22-A114E).

ORDERING INFORMATION(1)

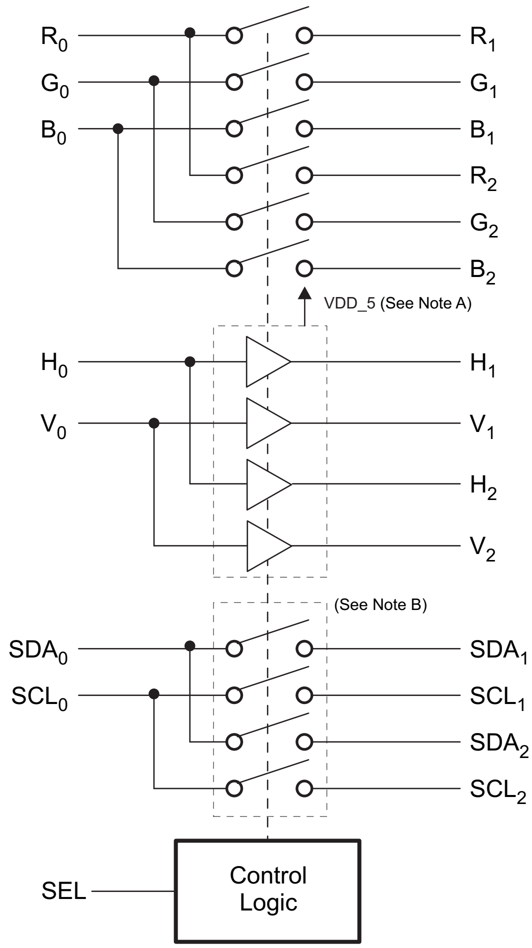
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RTG	Tape and reel	TS3V713ELRTGR	TF713EL

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

TYPICAL APPLICATION DIAGRAM



LOGIC DIAGRAM



A. Supply for H_{SYNC} and V_{SYNC} translators

B. Output clamped to V_{DD} – 1 V

FUNCTION TABLE

SEL	FUNCTION	
	R_0, G_0, B_0, H_0, V_0, SCL_0, SDA_0	**Hi-Z**
L	R_1, G_1, B_1, H_1, V_1, SCL_1, SDA_1	R_2, G_2, B_2, H_2, V_2, SCL_2, SDA_2
H	R_2, G_2, B_2, H_2, V_2, SCL_2, SDA_2	R_1, G_1, B_1, H_1, V_1, SCL_1, SDA_1

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	4.6	V
V_{DD_5}			–0.5	6.5	
$V_{I/O}$	Analog voltage range[2][3]	R, G, B, SCL, SDA	–0.5	V_{DD} + 0.5	V
V_{IN}	Digital input voltage range[2][3]	SEL, H, V	–0.5	6.5	V
$I_{I/OK}$	Analog port diode current	$V_{I/O}$ < 0 V		–50	mA
I_{IK}	Digital input clamp current	V_{IN} < 0 V		–50	mA
$I_{I/O}$	ON-state switch current	R, G, B, SCL, SDA	–128	128	mA
I_{DD}	Continuous current through V_{DD} or GND		–100	100	mA
I_{GND}					
θ_{JA}	Package thermal impedance[4]	RTG package[4]		39.2	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-1.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{DD}	Supply voltage		3	3.6	V
V_{DD_5}	Supply voltage for H and V channels		4.5	5.5	V
V_{IN}	Digital control input voltage	SEL, H, V	0	5.5	V
V_{IH}	High-level control input voltage	SEL, H, V	2		V
V_{IL}	Low-level control input voltage	SEL, H, V		0.8	V
I_{OH}	High-level output current	H, V		–8	mA
I_{OL}	Low-level output current	H, V		8	mA
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS(1)

over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V, V_{DD_5} = 5 V ±0.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS				MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	SEL, H, V	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	I_{IN} = –18 mA				–0.8	–1.2	V
r_{ON}	ON-state resistance	R, G, B	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	0 V ≤ $V_{I/O}$ ≤ V_{DD},	$I_{I/O}$ = –40 mA			3	6	Ω
		SCL, SDA						4	8	
$r_{ON(flat)}$	ON-state resistance flatness(3)	R, G, B	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	$V_{I/O}$ = 1.5 V and V_{DD},	$I_{I/O}$ = –40 mA			0.2	1	Ω
Δr_{ON}	ON-state resistance match between channels(4)	R, G, B	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	0 V ≤ $V_{I/O}$ ≤ V_{DD},	$I_{I/O}$ = –40 mA			0.2	1	Ω
I_{IH}	Digital input high leakage current	SEL, H, V	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	V_{IN} = V_{DD}					±1	µA
I_{IL}	Digital input low leakage current	SEL, H, V	V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	V_{IN} = GND					±1	µA
I_{OFF}	Leakage under power off conditions	All outputs	V_{DD} = 0 V, V_{DD_5} = 0 V,	$V_{I/O}$ = 0 to 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
C_{IN}	Digital input capacitance	SEL, H, V	f = 10 MHz	V_{IN} = 0,				4		pF
C_{OFF}	Switch OFF capacitance	R, G, B	f = 10 MHz	$V_{I/O}$ = 0 V,	Output open,	Switch OFF		2.5		pF
		SCL, SDA						2.3		
C_{ON}	Switch ON capacitance	R, G, B	f = 10 MHz	$V_{I/O}$ = 0 V,	Output open,	Switch ON		8		pF
		SCL, SDA						8.2		
V_{OH}	High-level output voltage	H, V	V_{IN} = V_{IH},	I_{OH} = –8 mA			3.8			V
V_{OL}	Low-level output voltage	H, V	V_{IN} = V_{IH},	I_{OL} = 8 mA					0.5	V
V_{HYST}	Voltage hysteresis	H, V						200	300	mV
I_{DD}	V_{DD} supply current		V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	V_{IN} = V_{DD} or GND,	$I_{I/O}$ = 0 mA,			200	500	µA
I_{DD_5}	V_{DD_5} supply current		V_{DD} = 3.6 V, V_{DD_5} = 5.5 V,	V_{IN} = V_{DD} or GND,	$I_{I/O}$ = 0 mA,				50	µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3V, V_{DD_5} = 5V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center port to any other ports.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V, V_{DD_5} = 5 V ±0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{pd} (1)	R_0,G_0, B_0	R_1, G_1, B_1 or R_2, G_2, B_2		0.25		ns
	SCL_0, SDA_0	SCL_1, SDA_1 or SCL_2, SDA_2		0.25		
	H0,V0	H1, V1 or H2, V2		3	7	
t_{PHZ}, t_{PLZ} (2)	SEL	R_1, G_1, B_1, SCL_1, SDA_1 or R_2, G_2, B_2, SCL_2, SDA_2	0.5		11	ns
	SEL	H_1, V_1 or H_2, V_2	0.5		13	
t_{PZH}, t_{PZL} (3)	SEL	R_1, G_1, B_1, SCL_1, SDA_1 or R_2, G_2, B_2, SCL_2, SDA_2	0.5		11	ns
	SEL	H_1, V_1 or H_2, V_2	0.5		13	
$t_{sk(o)}$ (4)	R, G, B			0.05	0.1	ns
$t_{sk(p)}$ (5)	R, G, B			0.05	0.1	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) Line disable time: SEL to input and output; also called "SEL to Switch Turn Off Time."
(3) Line enable time: SEL to input and output; also called "SEL to Switch Turn On Time."
(4) Output skew between center channel to any other channel.
(5) Skew between opposite transitions of the same output. $|t_{PHL} – t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V, V_{DD_5} = 5 V ±0.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP (1)	UNIT
X_{TALK}	R, G, B	R_L = 50 Ω	f = 250 MHz	–50	dB
O_{IRR}	R, G, B	R_L = 50 Ω	f = 250 MHz	–40	dB
BW	R, G, B	R_L = 50 Ω	Switch ON	1.3	GHz

(1) All typical values are at V_{DD} = 3.3 V, V_{DD_5} = 5 V (unless otherwise noted)

TYPICAL CHARACTERISTICS

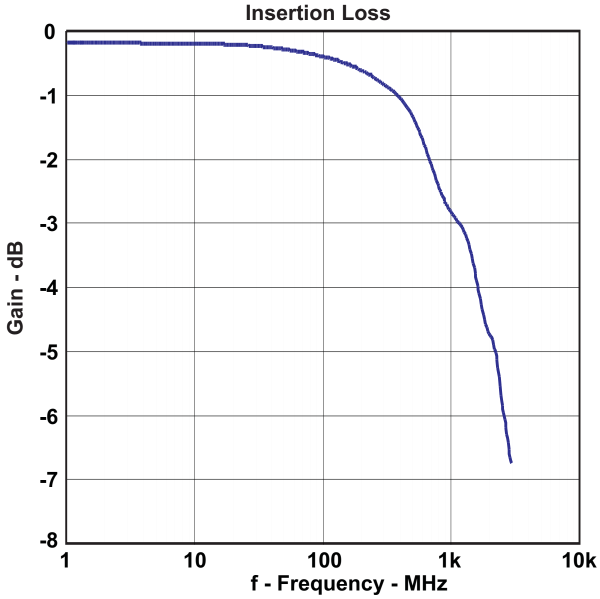


Figure 1. Gain vs Frequency

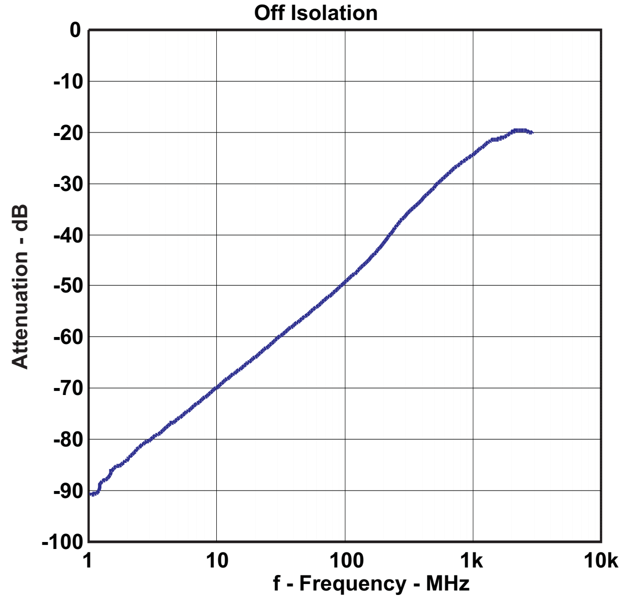


Figure 2. Off Isolation vs Frequency

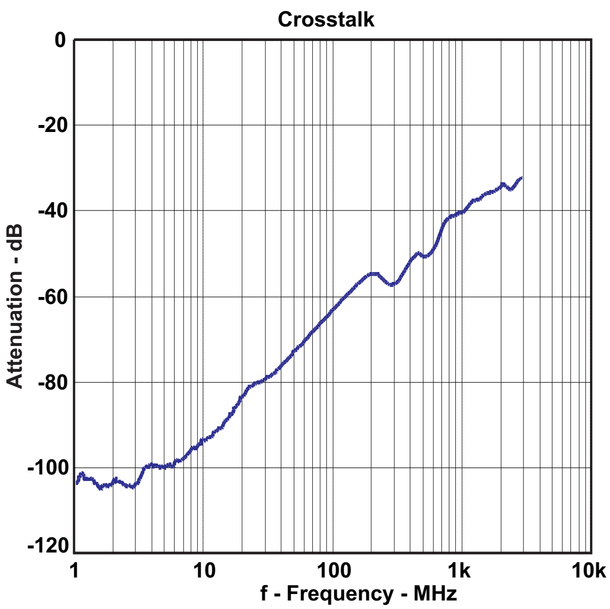


Figure 3. Crosstalk vs Frequency

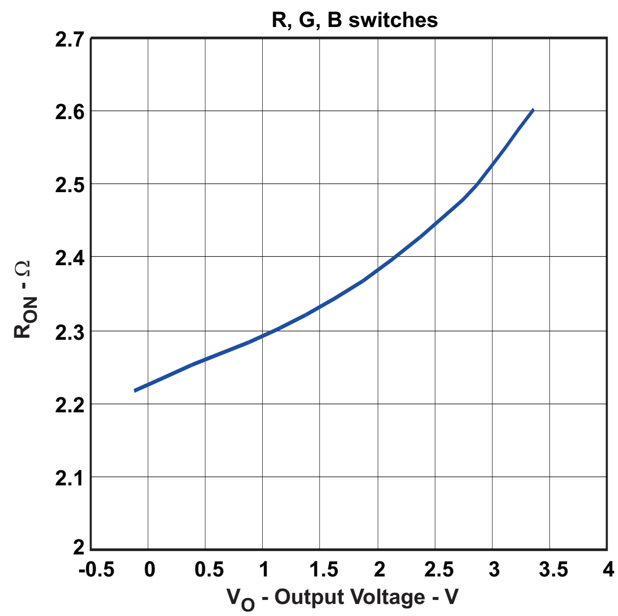


Figure 4. R_{ON} vs V_O

TYPICAL CHARACTERISTICS (continued)

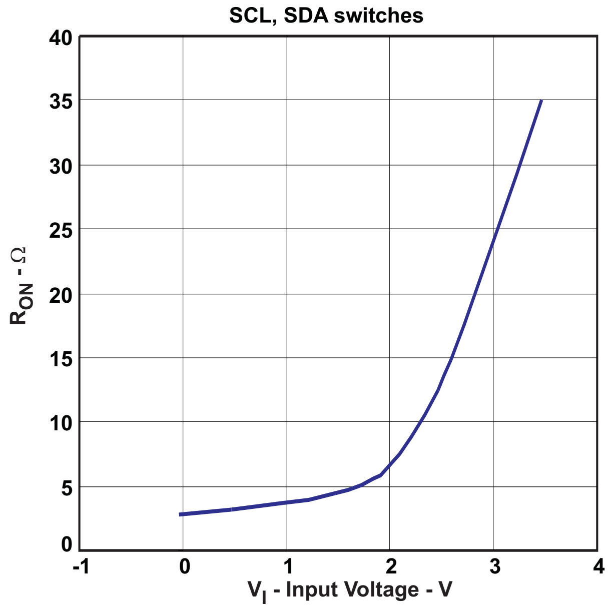


Figure 5. R_{ON} vs V_I

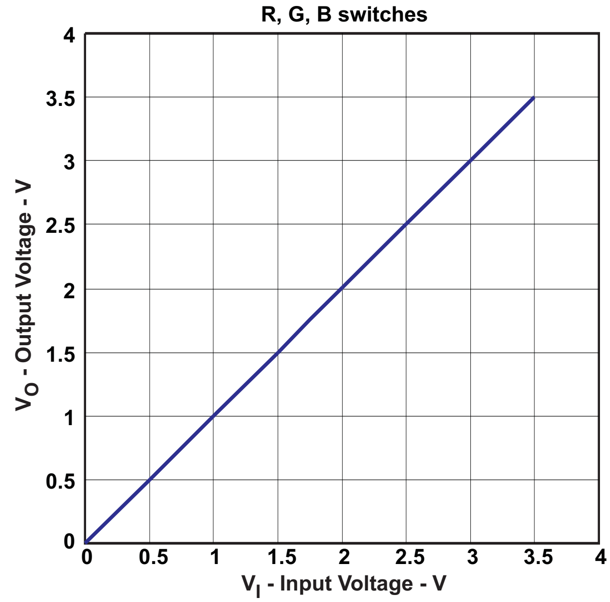


Figure 6. V_O vs V_I

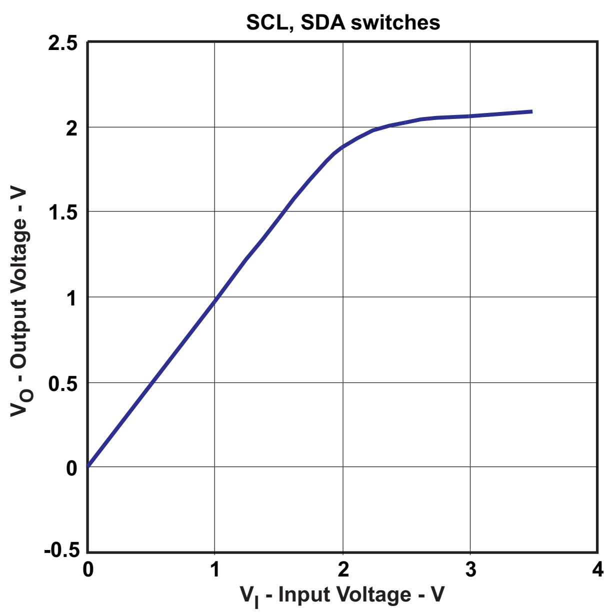


Figure 7. V_O vs V_I

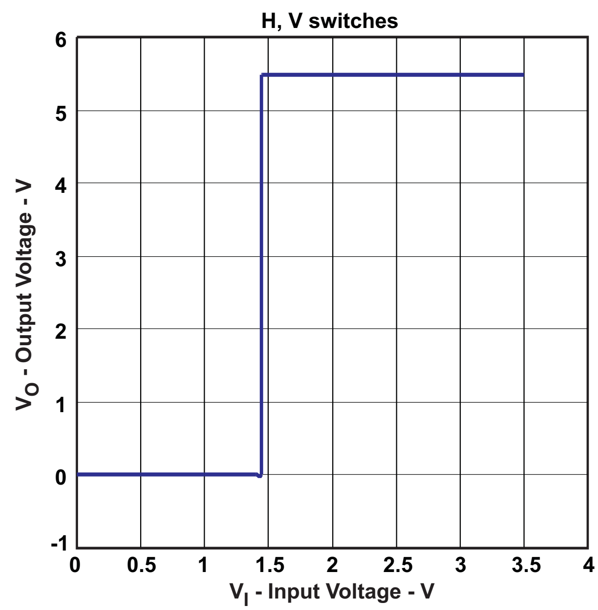
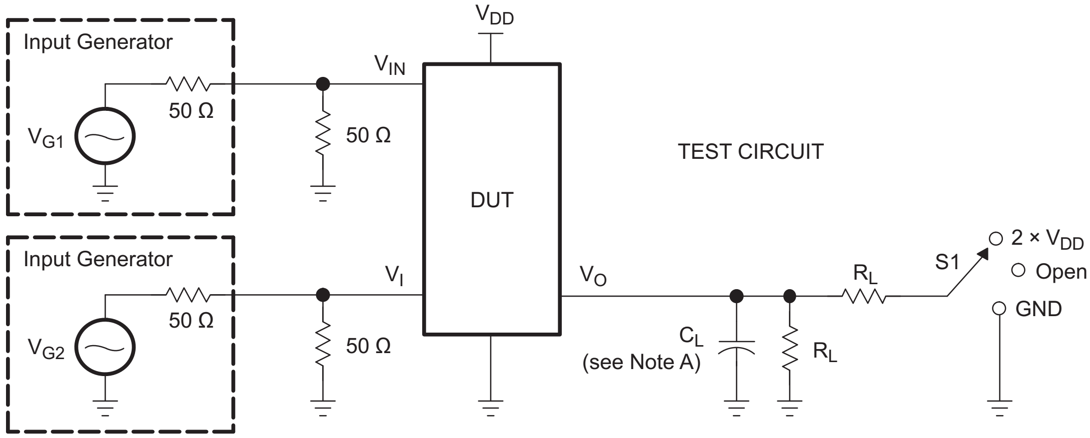


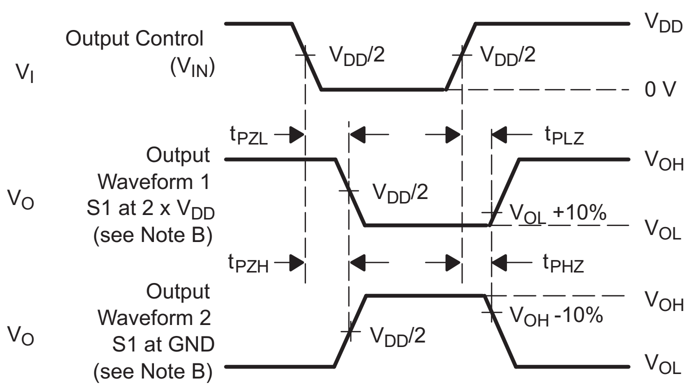
Figure 8. V_O vs V_I

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{DD_5}	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	5 V± 0.5 V	3.3 V± 0.3 V	2 × V_{DD}	200 Ω or 1 kΩ*	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V± 0.5 V	3.3 V± 0.3 V	GND		V_{DD}	10 pF	0.3 V

*R_L = 200 Ω applies to all switch outputs
R_L = 1 kΩ applies to all buffer outputs

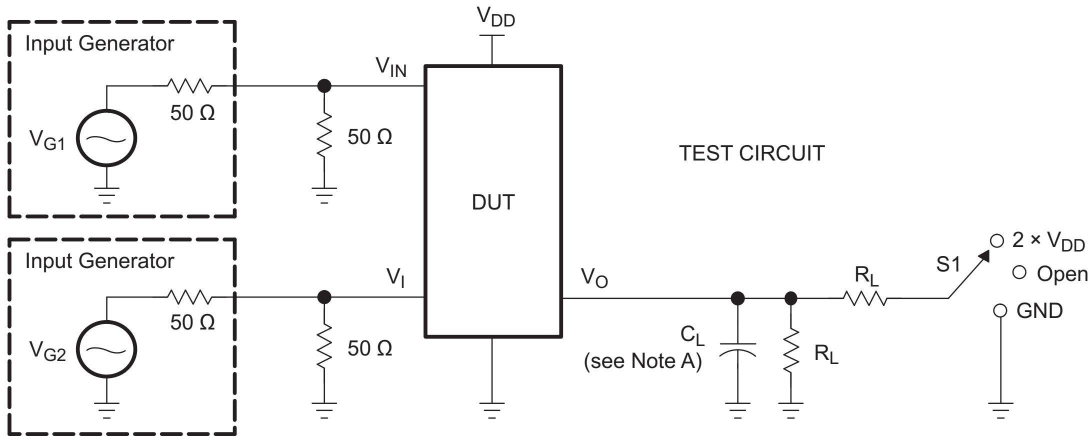


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

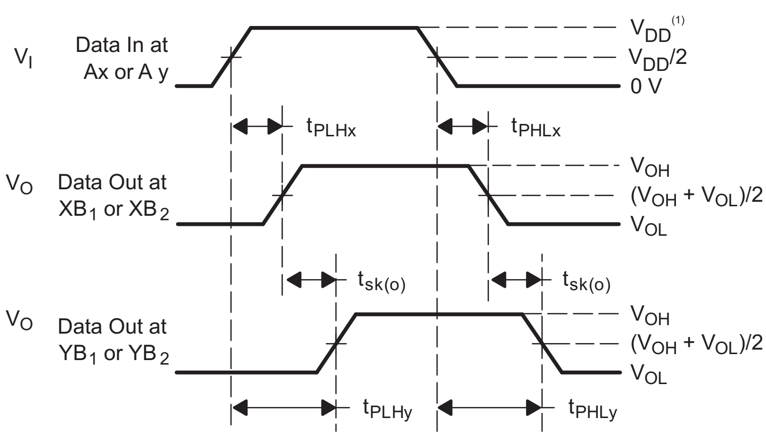
Figure 9. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (Propagation Delay and Skew)



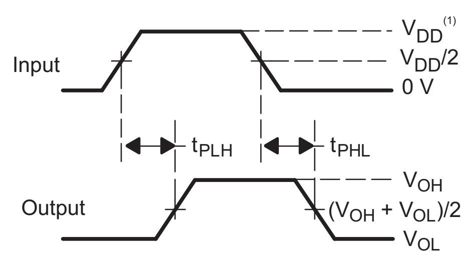
TEST	V_{DD}	V_{DD_5}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	5 V ± 0.5 V	Open	200 Ω* or 1 kΩ	V_{DD} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	5 V ± 0.5 V	Open		V_{DD} or GND	10 pF

*R_L = 200 Ω applies to all switch outputs
R_L = 1 kΩ applies to all buffer outputs



$t_{sk(o)} = t_{PLHy} - t_{PLHx}$ or $t_{PHLy} - t_{PHLx}$

VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



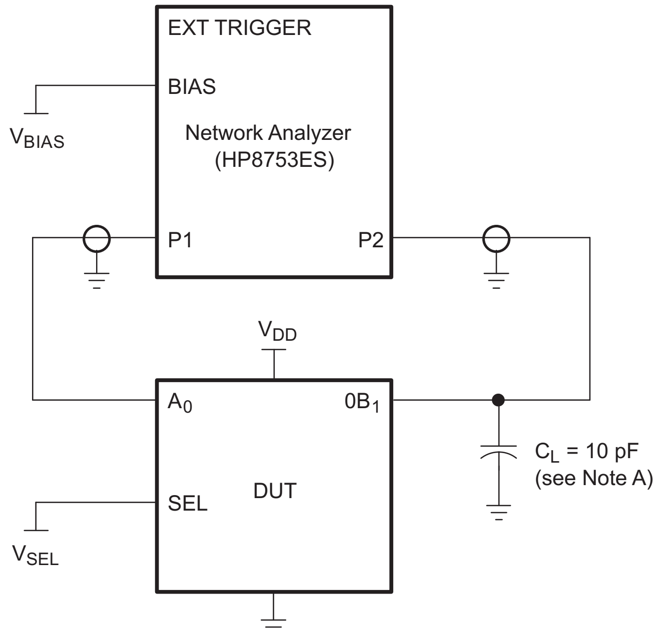
$t_{sk(p)} = t_{PHL} - t_{PLH}$

VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
(1) 2 V ± 0.2 V for SCL, SDA

Figure 10. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

Figure 11. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4

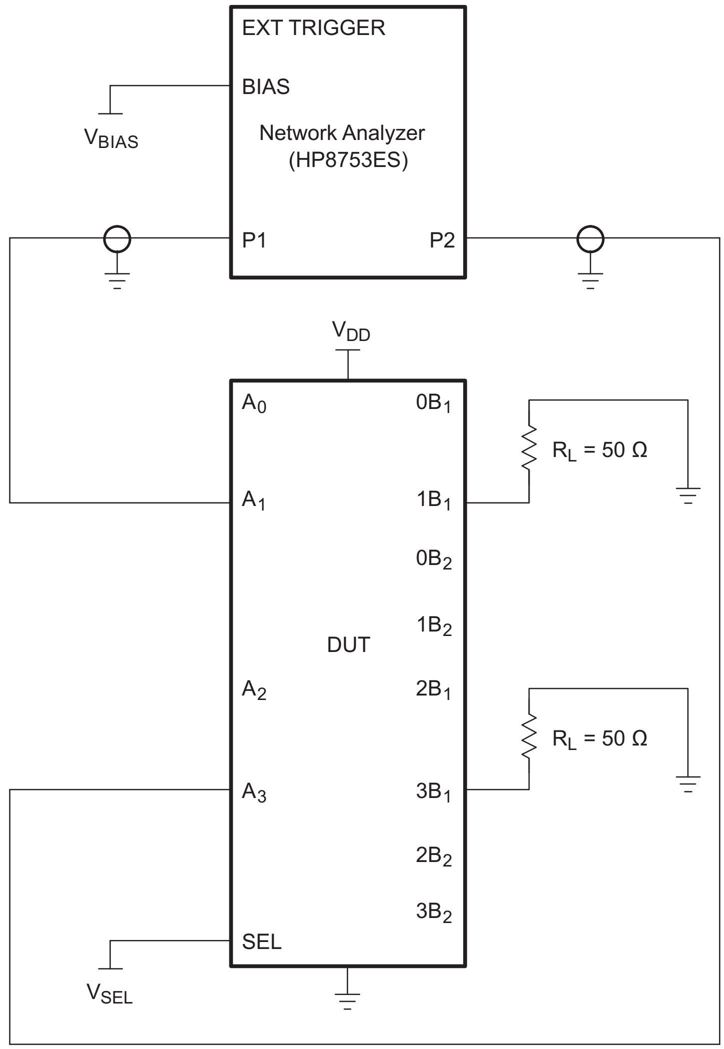
RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3 . All unused analog input (A) ports are connected to GND, and the output (B) ports are left open.

HP8753ES Setup

Average = 4

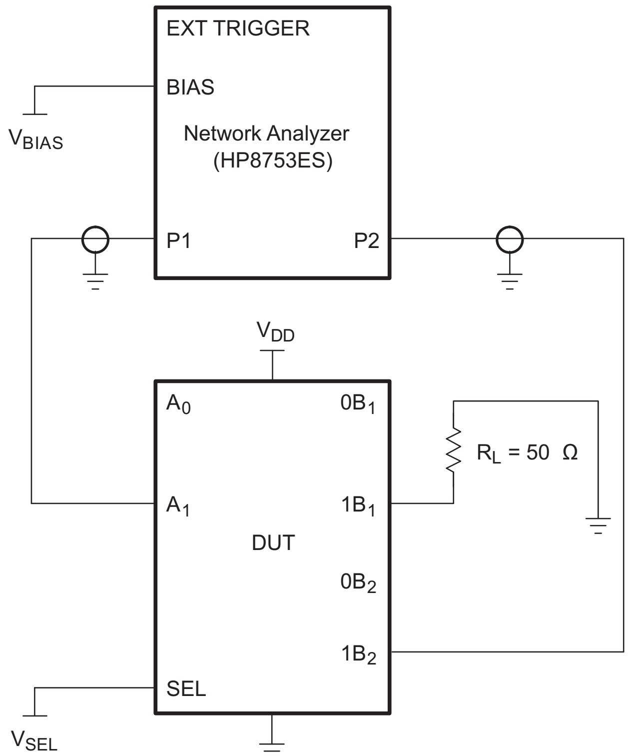
RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 13. Test Circuit for Off Isolation (O_{IRR})

Off isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_s is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to GND, and the output (B) ports are left open.

HP8753ES Setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS3V713ELRTGR	ACTIVE	WQFN	RTG	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

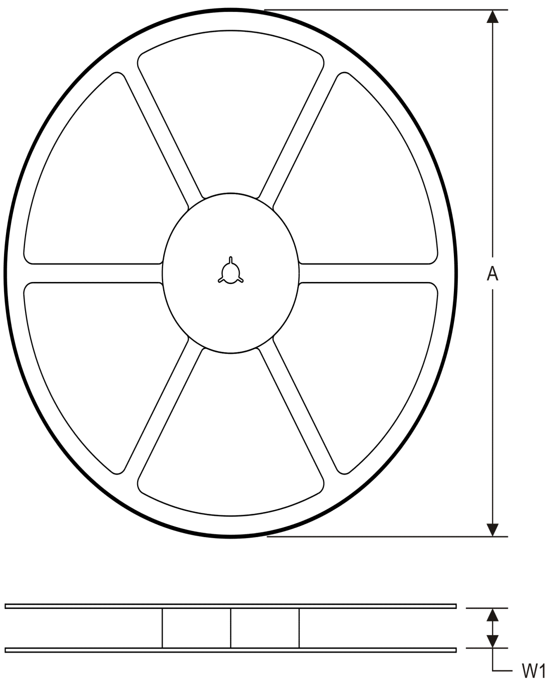
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

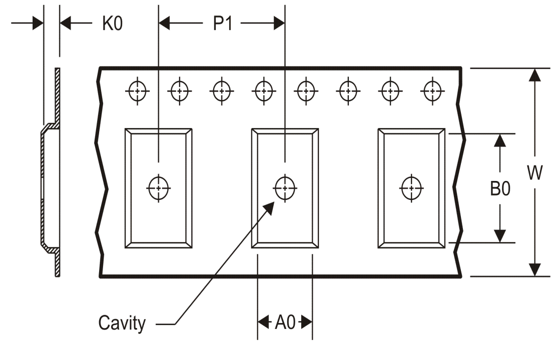
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



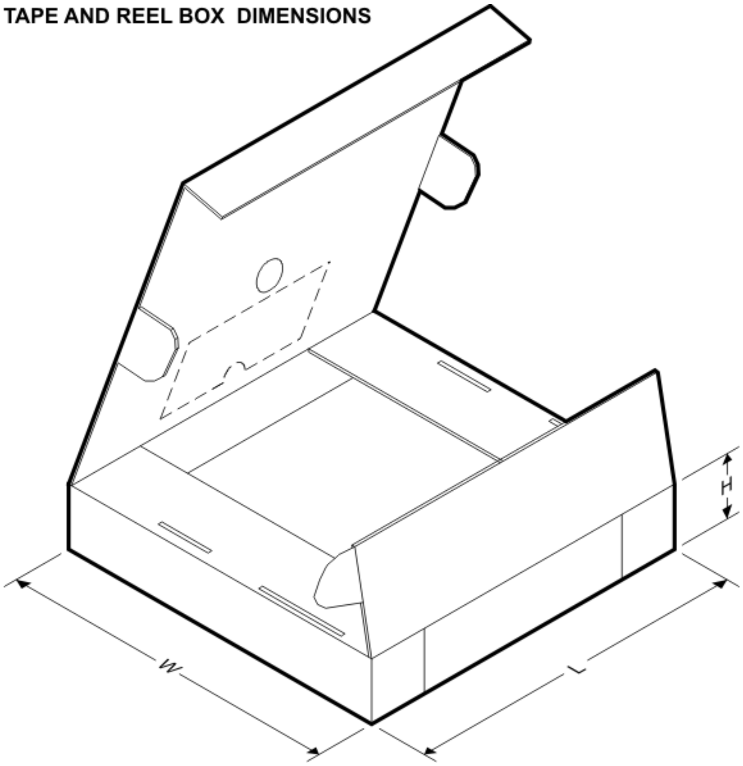
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3V713ELRTGR	WQFN	RTG	32	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1

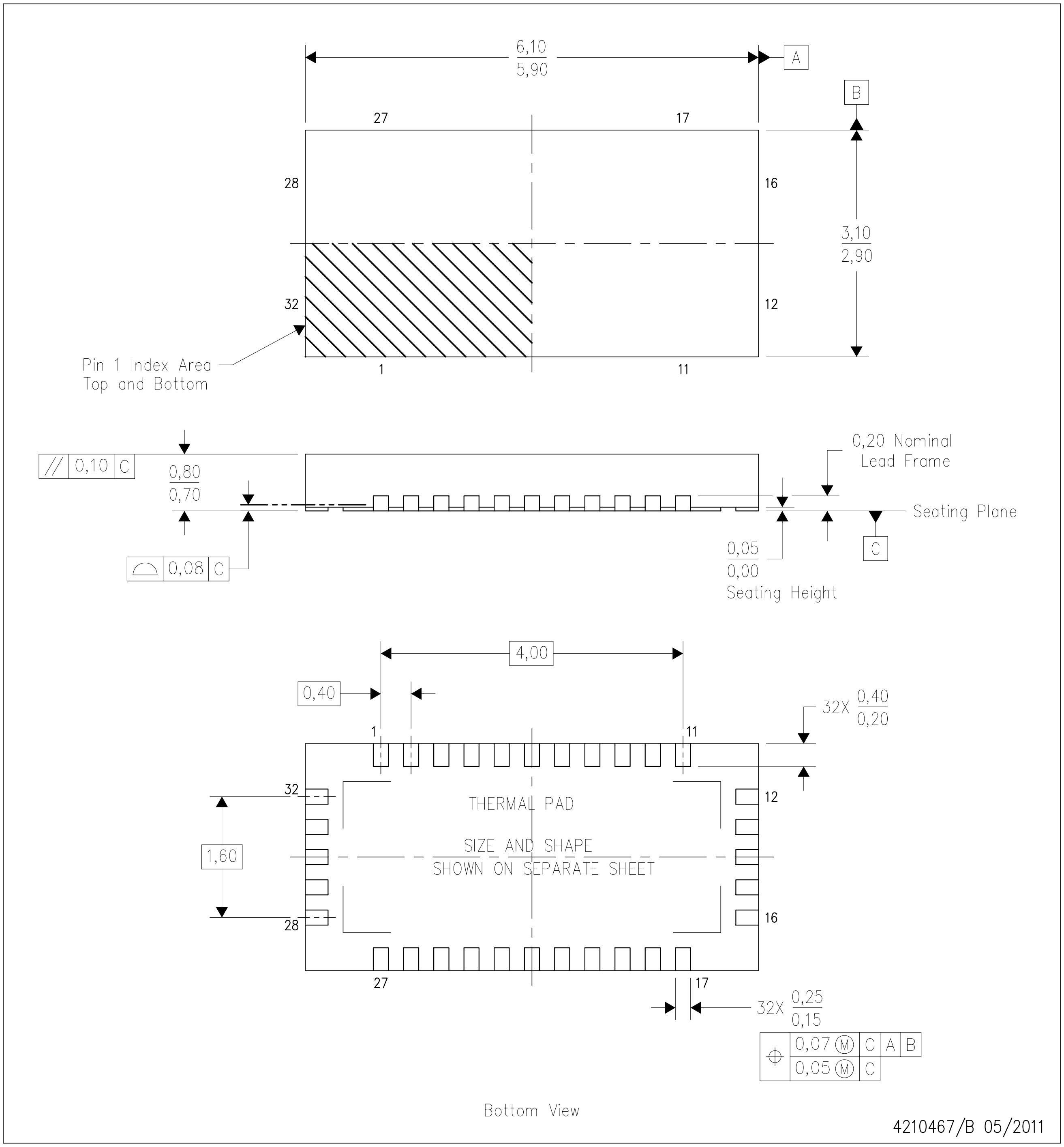
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3V713ELRTGR	WQFN	RTG	32	3000	367.0	367.0	38.0

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Reference JEDEC MO–220.

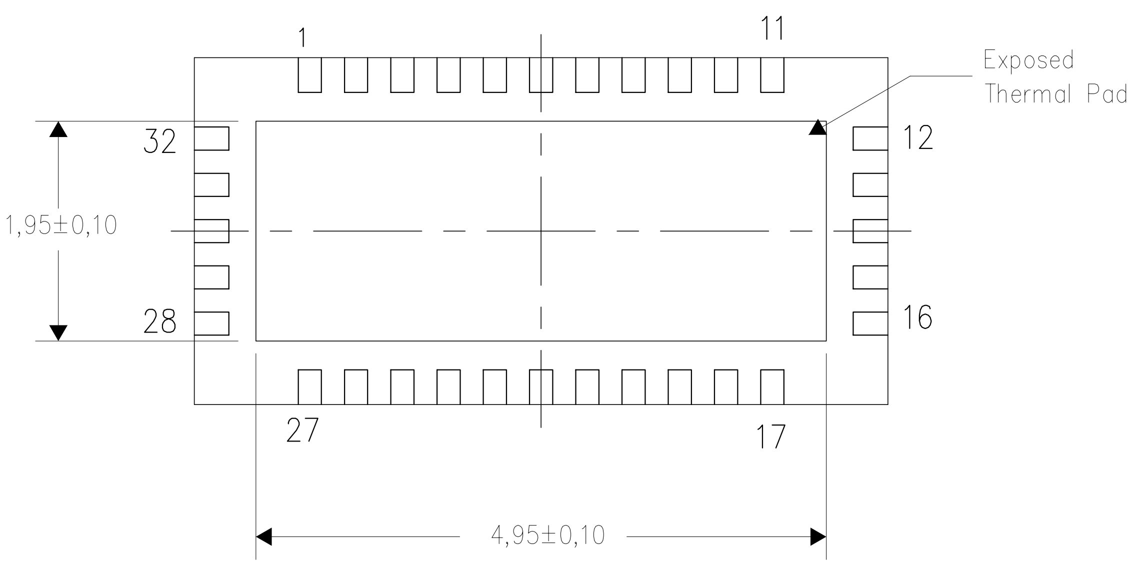
RTG (R-PWQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



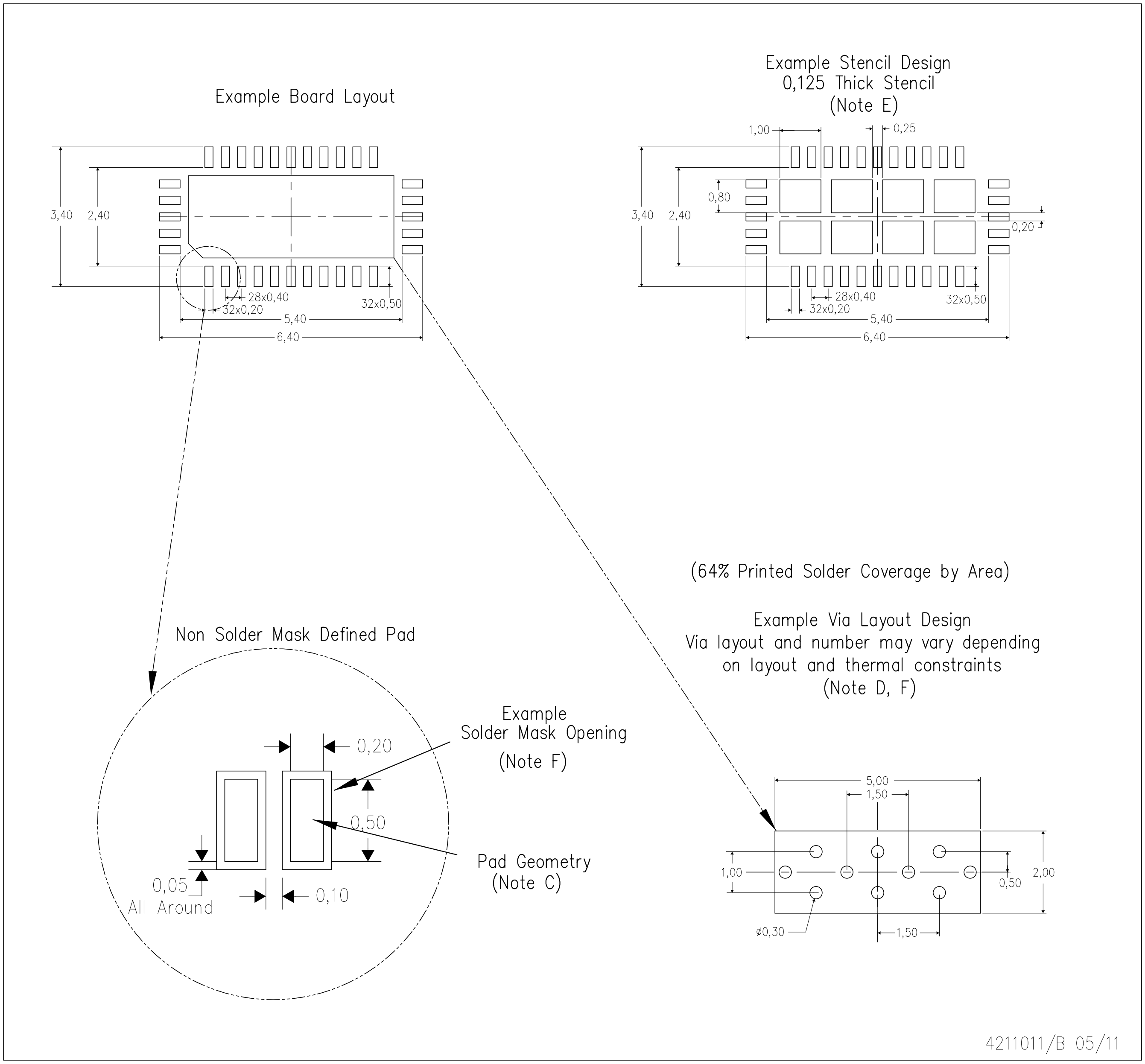
Bottom View

Exposed Thermal Pad Dimensions

4210534/C 05/11

NOTE: All linear dimensions are in millimeters

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265