



TS1851-TS1852-TS1854

1.8V input/output rail-to-rail
Low power operational amplifiers

Features

- Operates at $V_{CC} = 1.8V$ to $6V$
- Rail-to-rail input and output
- Extended V_{icm} ($V_{DD} - 0.2V$ to $V_{CC} + 0.2V$)
- Low supply current ($120\mu A$)
- Gain bandwidth product ($480kHz$)
- High unity gain stability (able to drive $500pF$)
- ESD tolerance ($2kV$)
- Latch-up immunity
- Available in SOT23-5 micropackage

Applications

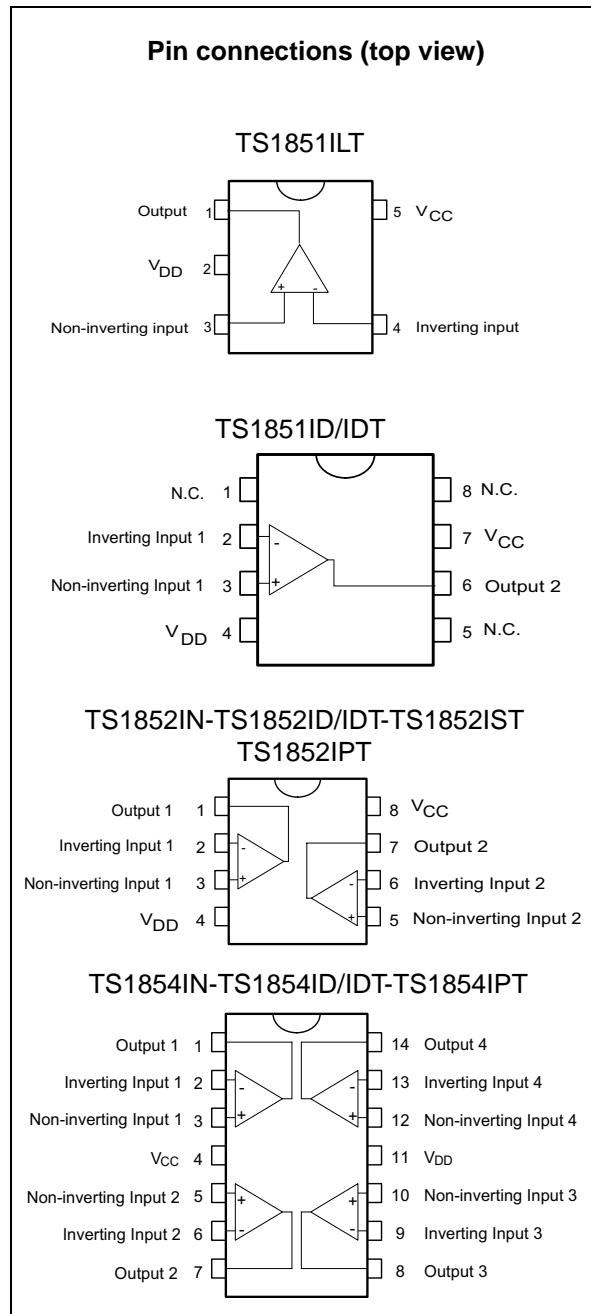
- Two-cell battery-powered systems
- Battery-powered electronic equipment
- Cordless phones
- Cellular phones
- Laptops
- PDAs

Description

The TS185x (single, dual and quad) are operational amplifiers able to operate with voltages as low as $1.8V$. They feature both input and output rail-to-rail ($1.71 @ V_{CC} = 1.8V$, $R_L = 2k\Omega$), $120\mu A$ current consumption and $480kHz$ gain bandwidth product.

With such a low consumption and a sufficient GBP for many applications, this op-amp is very well-suited for all kinds of battery-supplied and portable equipment applications.

The TS1851 is housed in the space-saving 5-pin SOT23-5 package which simplifies the board design (outside dimensions are $2.8mm \times 2.9mm$).



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1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	7	V
V_{id}	Differential input voltage ⁽²⁾	±1	V
V_i	Input voltage	$V_{dd} - 0.3$ to $V_{CC} + 0.3$	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient ⁽³⁾		°C/W
	SOT23-5	250	
	DIP8	85	
	DIP14	66	
	miniSO-8	190	
	SO-8	125	
	SO-14	103	
R_{thjc}	Thermal resistance junction to case		°C/W
	SOT23-5	81	
	DIP8	41	
	DIP14	33	
	miniSO-8	39	
	SO-8	40	
	SO-14	31	
ESD	HBM: human body model ⁽⁴⁾	2	kV
	MM: machine model ⁽⁵⁾	200	V
	CDM: charged device model ⁽⁶⁾	1.5	kV
	Lead temperature (soldering, 10sec)	250	°C
	Output short-circuit duration	see note ⁽⁷⁾	

1. All voltage values, except differential voltage are with respect to network terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If $V_{id} > \pm 1V$, the maximum input current must not exceed $\pm 1mA$. When $V_{id} > \pm 1V$, add an input series resistor to limit input current.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
4. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
5. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
6. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
7. Short-circuits from the output to V_{CC} can cause excessive heating. The maximum output current is approximately 48mA, independent of the magnitude of V_{CC} . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

2 Operating conditions

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 6	V
V_{icm}	Common mode input voltage range $T_{op} = 25^{\circ}\text{C}$, $1.8 \leq V_{CC} \leq 6\text{V}$ $T_{min} < T_{op} < T_{max}$, $1.8 \leq V_{CC} \leq 5.5\text{V}$	$V_{DD} - 0.2$ to $V_{CC} + 0.2$ V_{DD} to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 125	$^{\circ}\text{C}$

3 Electrical characteristics

Table 3. Electrical characteristics measured at $V_{CC} = +1.8V$, $V_{dd} = 0V$, with C_L & R_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		$\mu V/^\circ C$
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2$ ⁽²⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2$ ⁽²⁾ $T_{min} \leq T_{amb} \leq T_{max}$		10	50 80	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	55 52	85		dB
A_{vd}	Large signal voltage gain	$V_{out} = 0.5V$ to $1.3V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	80 70	100 88		dB
V_{OH}	High level output voltage	$V_{id} = 100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 2k\Omega$	1.7 1.65 1.7 1.65	1.77 1.7		V
V_{OL}	Low level output voltage	$V_{id} = -100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 2k\Omega$		40 62	70 90 100 120	mV
I_o	Output source current	$V_{id} = 100mV$, $V_O = V_{DD}$	2	29		mA
	Output sink current	$V_{id} = -100mV$, $V_O = V_{CC}$	2	46		
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ $A_{VCL} = 1$, no load $T_{min} \leq T_{amb} \leq T_{max}$		120	170 200	μA
GBP	Gain bandwidth product	$R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$	300	480		kHz
SR	Slew rate	$R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$	0.1	0.18		V/ μs
ϕ_m	Phase margin	$C_L = 100pF$		60		Degrees
en	Input voltage noise	$f = 1kHz$		40		nV/ \sqrt{Hz}
THD	Total harmonic distortion			0.01		%

1. All parameter limits at temperatures other than $25^\circ C$ are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. Electrical characteristics measured at $V_{CC} = +3V$, $V_{dd} = 0V$, with C_L & R_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		$\mu V/^\circ C$
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2^{(2)}$ $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2^{(2)}$ $T_{min} \leq T_{amb} \leq T_{max}$		10	55 85	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	60 57	90		dB
A_{vd}	Large signal voltage gain	$V_{out} = 0.5V$ to $2.5V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	83 74	99 90		dB
V_{OH}	High level output voltage	$V_{id} = 100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 2k\Omega$	2.9 2.85 2.9 2.85	2.96 2.94		V
V_{OL}	Low level output voltage	$V_{id} = -100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$, $R_L = 2k\Omega$		10 46	90 100 120 130	mV
I_o	Output source current	$V_{id} = 100mV$, $V_O = V_{DD}$	2	47		mA
	Output sink current	$V_{id} = -100mV$, $V_O = V_{CC}$	2	47		
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ $A_{VCL} = 1$, no load $T_{min} \leq T_{amb} \leq T_{max}$		150	200 230	μA
GBP	Gain bandwidth product	$R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$	370	600		kHz
SR	Slew rate	$R_L = 10k\Omega$, $C_L = 100pF$, $A_V = 1$	0.12	0.2		V/ μs
ϕ_m	Phase margin	$C_L = 100pF$		60		Degrees
en	Input voltage noise	$f = 1kHz$		40		nV/ \sqrt{Hz}
THD	Total harmonic distortion	$V_{out} = 2V_{pk-pk}$, $A_V = -1$, $f = 1kHz$		0.005		%

1. All parameter limits at temperatures other than $25^\circ C$ are guaranteed by correlation.

2. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. Electrical characteristics measured at $V_{CC} = +5V$, $V_{dd} = 0V$, with C_L & R_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	$V_{icm} = V_{out} = V_{CC}/2$ TS1851/2/4 $T_{min} \leq T_{amb} \leq T_{max}$ TS1851A/2A/4A $T_{min} \leq T_{amb} \leq T_{max}$		0.1	3 6 1 1.5	mV
ΔV_{io}	Input offset voltage drift			2		$\mu V/^\circ C$
I_{io}	Input offset current	$V_{icm} = V_{out} = V_{CC}/2^{(2)}$ $T_{min} \leq T_{amb} \leq T_{max}$		1	9 25	nA
I_{ib}	Input bias current	$V_{icm} = V_{out} = V_{CC}/2^{(2)}$ $T_{min} \leq T_{amb} \leq T_{max}$		16	63 93	nA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0 \leq V_{icm} \leq V_{CC}$ $T_{min} \leq T_{amb} \leq T_{max}$	65 62	95		dB
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 1.8$ to $5V$	70	90		dB
A_{vd}	Large signal voltage gain	$V_{out} = 0.5V$ to $4V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	85 77	97 93		dB
V_{OH}	High level output voltage	$V_{id} = 100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}, R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}, R_L = 2k\Omega$	4.85 4.8 4.85 4.8	4.95 4.91		V
V_{OL}	Low level output voltage	$V_{id} = -100mV$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}, R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}, R_L = 2k\Omega$		40 80	180 200 180 200	mV
I_o	Output source current	$V_{id} = 100mV, V_O = V_{DD}$	2	48		mA
	Output sink current	$V_{id} = -100mV, V_O = V_{CC}$	2	48		
I_{CC}	Supply current (per amplifier)	$V_{out} = V_{CC}/2$ $A_{VCL} = 1$, no load $T_{min} \leq T_{amb} \leq T_{max}$		162	220 250	μA
GBP	Gain bandwidth product	$R_L = 10k\Omega, C_L = 100pF, f = 100kHz$	380	630		kHz
SR	Slew rate	$R_L = 10k\Omega, C_L = 100pF, A_V = 1$	0.13	0.25		$V/\mu s$
ϕ_m	Phase margin	$C_L = 100pF$		60		Degrees
en	Input voltage noise	$f = 1kHz$		40		nV/\sqrt{Hz}
THD	Total harmonic distortion	$V_{out}=2V_{pk-pk}, A_V=-1, f = 1kHz$		0.01		%

1. All parameter limits at temperatures other than $25^\circ C$ are guaranteed by correlation.
2. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 1. Input offset voltage distribution

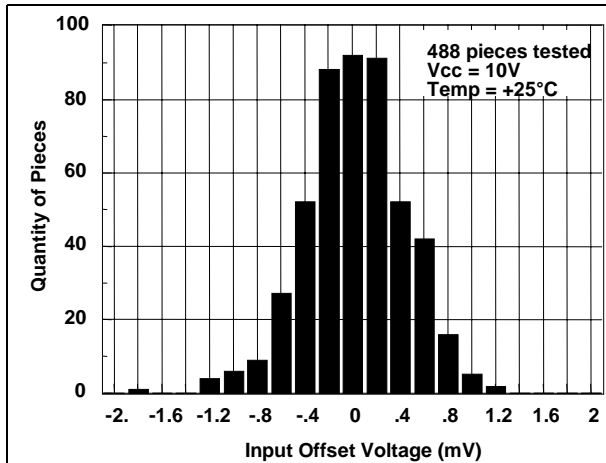


Figure 2. Input offset voltage vs. temperature

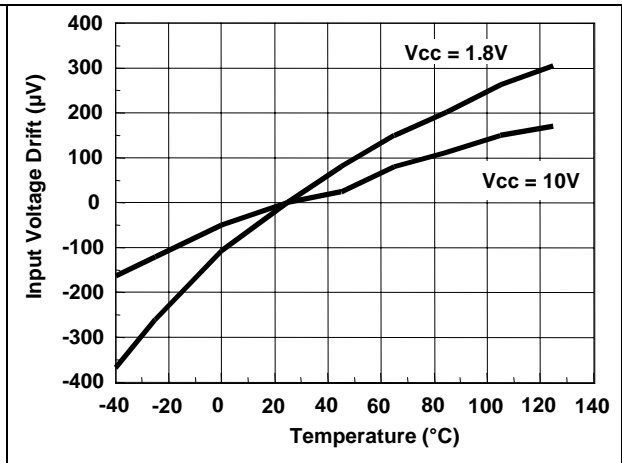


Figure 3. Input bias current vs. temperature

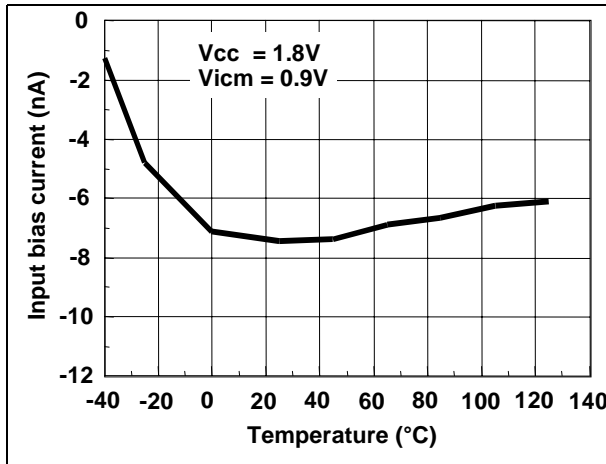


Figure 4. Input bias current vs. temperature

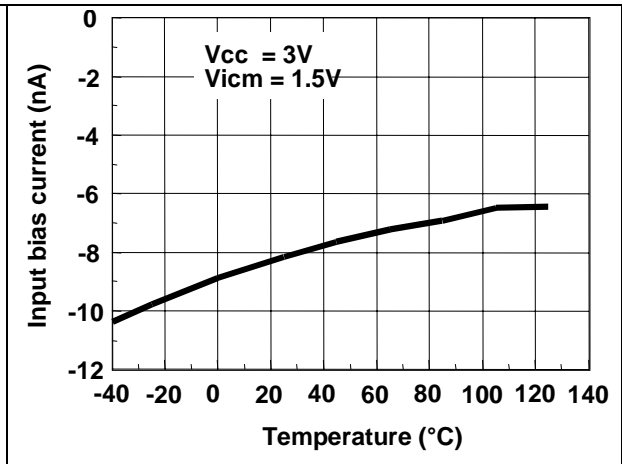


Figure 5. Input bias current vs. temperature

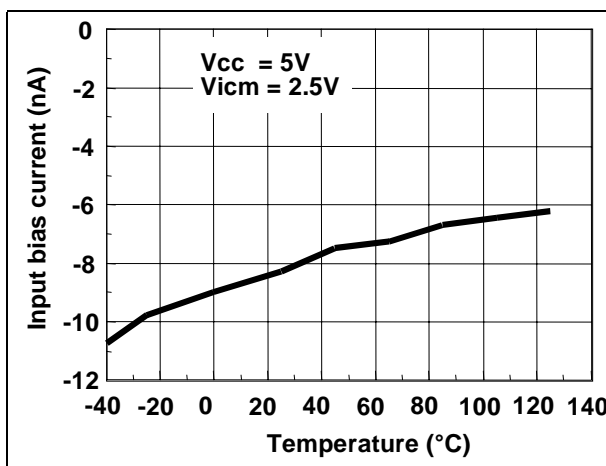


Figure 6. Supply current/amplifier vs. supply voltage

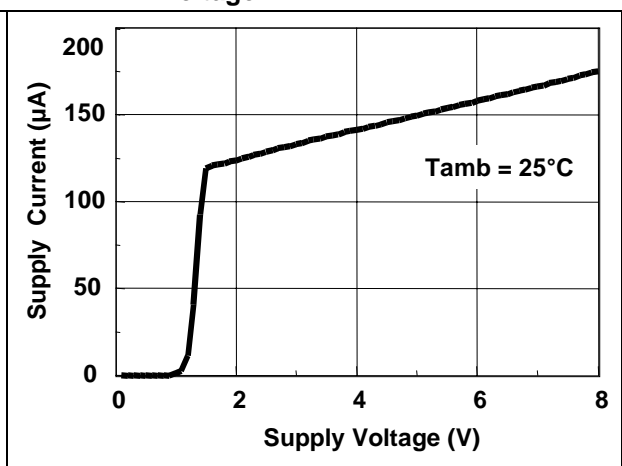


Figure 7. Supply current/amplifier vs. temperature

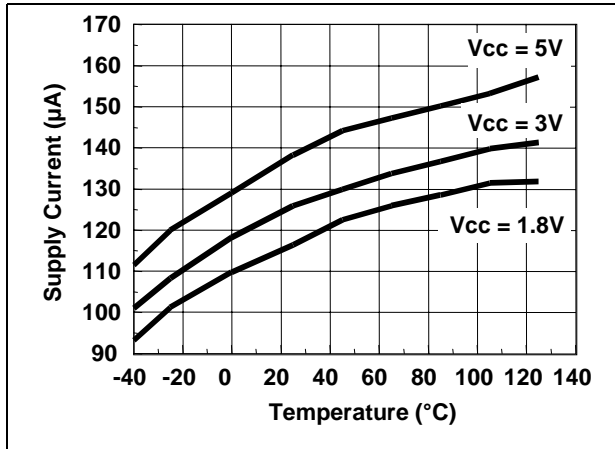


Figure 8. Common mode rejection vs. temperature

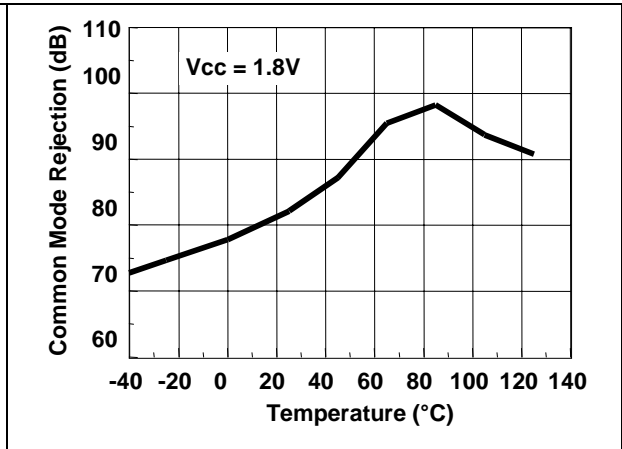


Figure 9. Common mode rejection vs. temperature

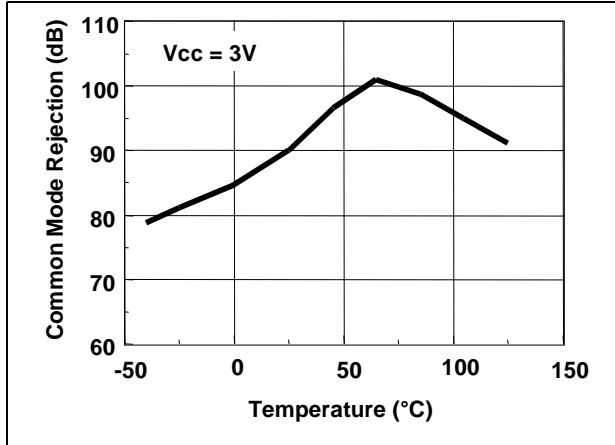


Figure 10. Gain and phasis vs. frequency

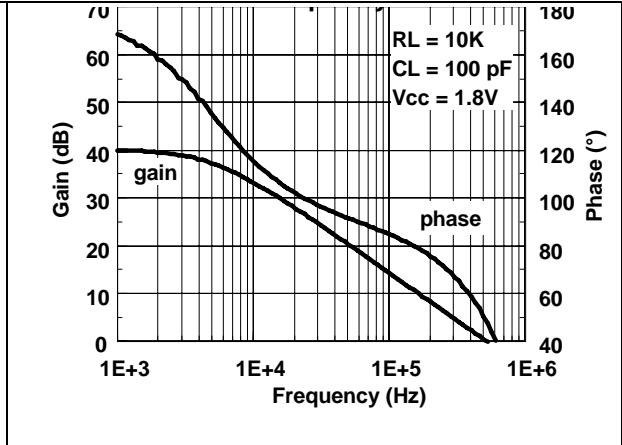


Figure 11. Supply voltage rejection vs. temperature

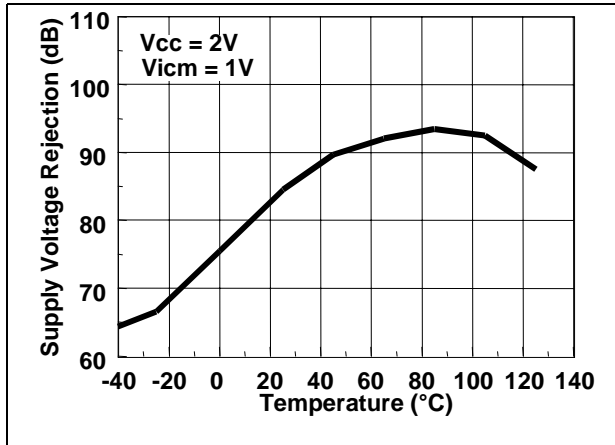


Figure 12. Gain and phasis vs. frequency

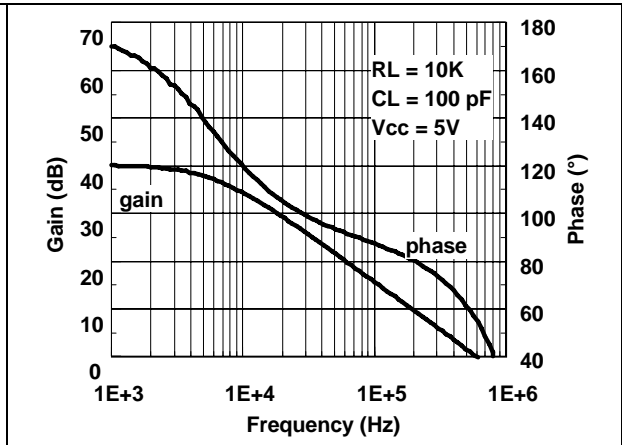


Figure 13. Common mode rejection vs. temperature

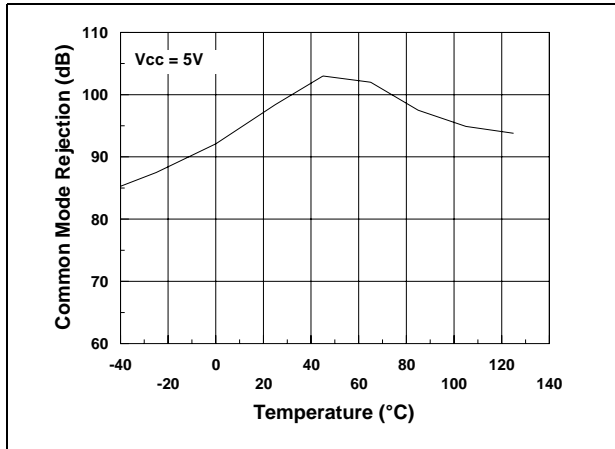


Figure 14. Supply voltage rejection vs. temperature

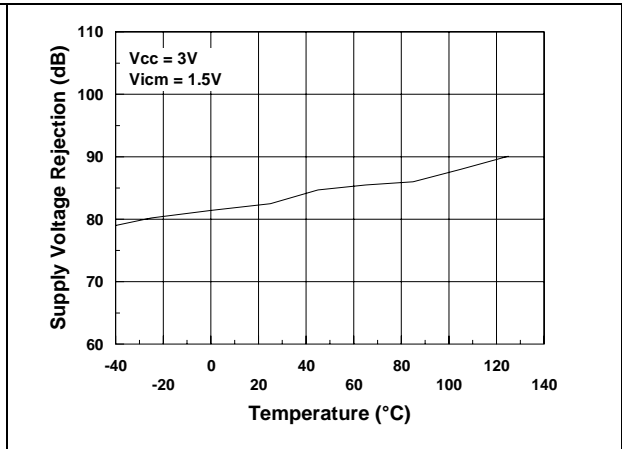


Figure 15. Supply voltage rejection vs. temperature

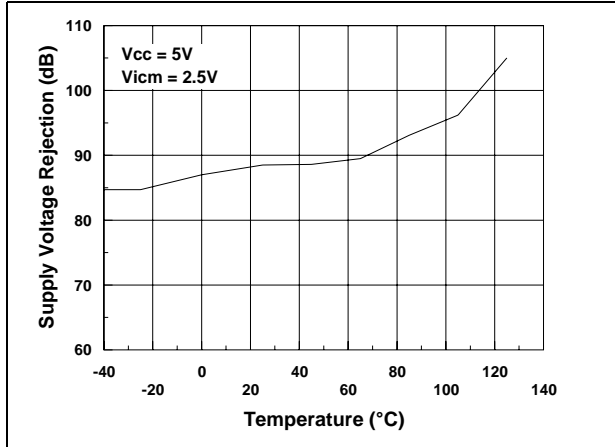


Figure 16. Open loop gain vs. temperature

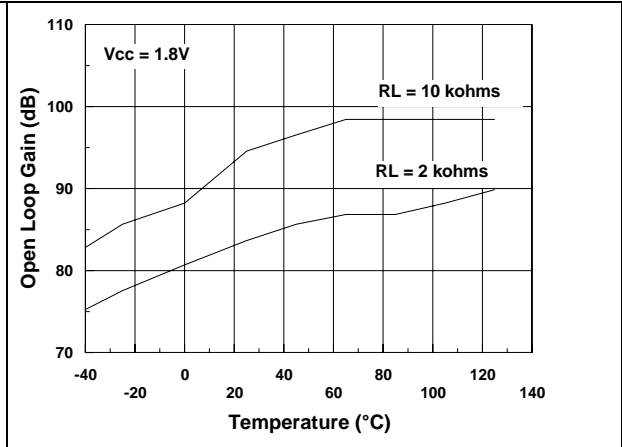


Figure 17. Open loop gain vs. temperature

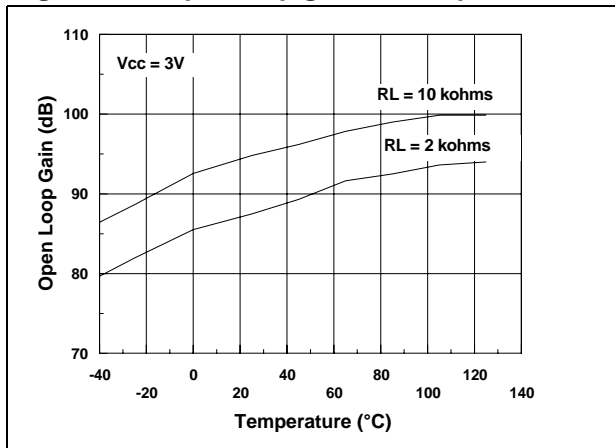


Figure 18. Open loop gain vs. temperature

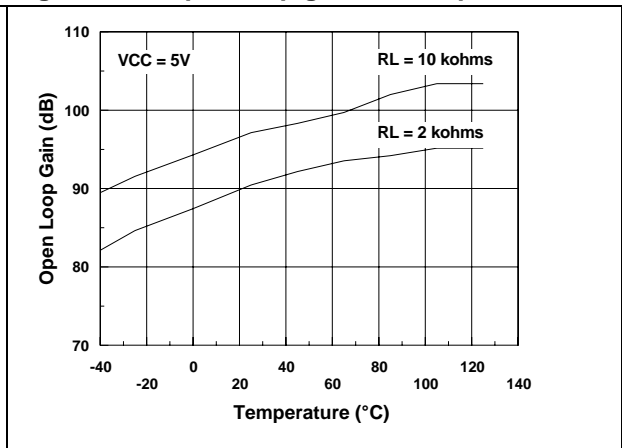


Figure 19. High level output voltage vs. temperature

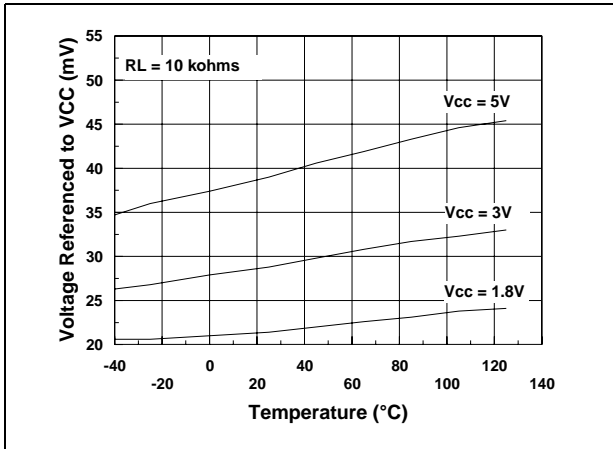


Figure 20. Low level output voltage vs. temperature

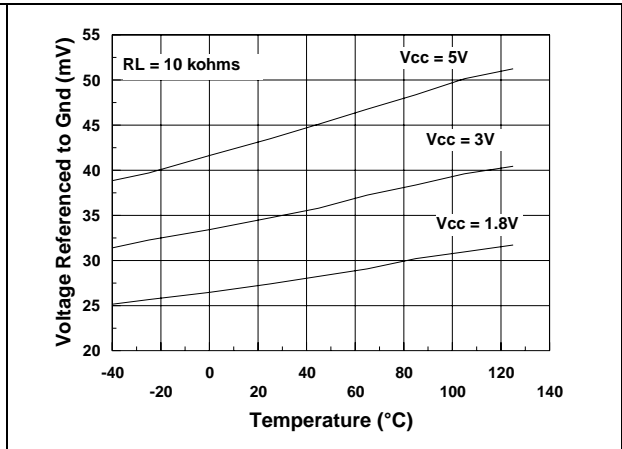


Figure 21. High level output voltage vs. temperature

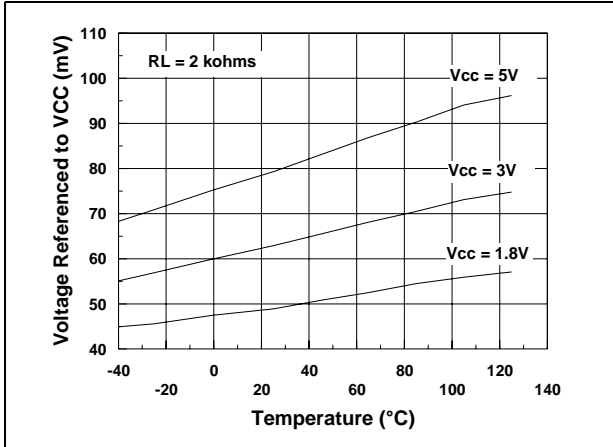


Figure 22. Low level output voltage vs. temperature

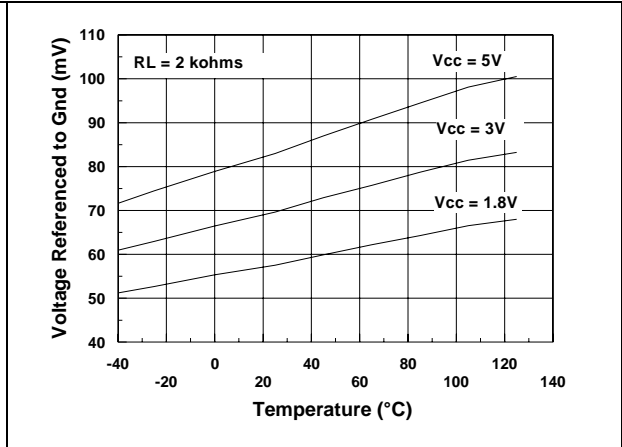


Figure 23. Output current vs. temperature

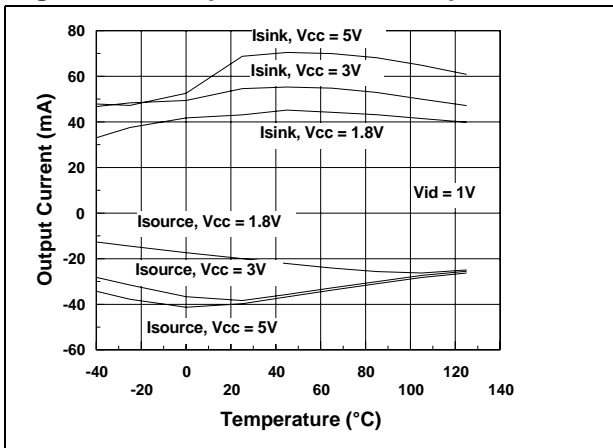


Figure 24. Output current vs. temperature

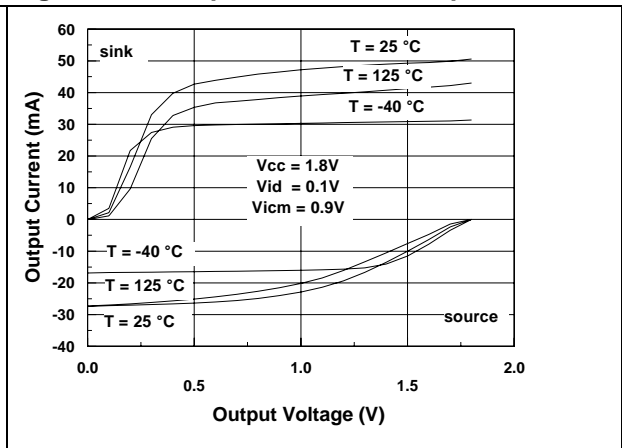


Figure 25. Output current vs. output voltage

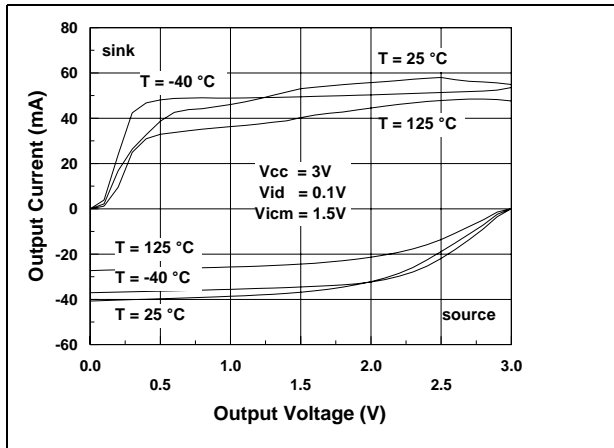


Figure 26. Output current vs. output voltage

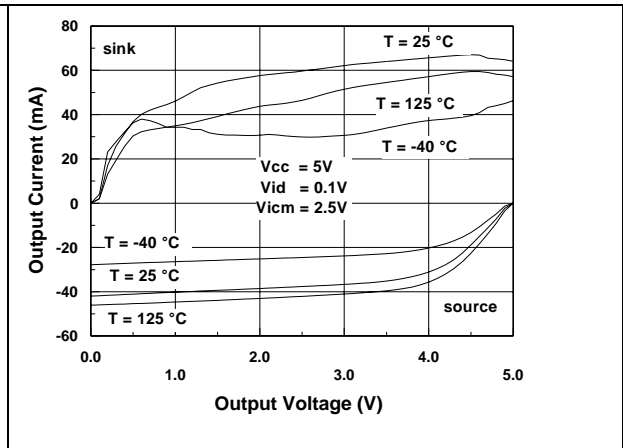


Figure 27. Gain and phasis vs. frequency

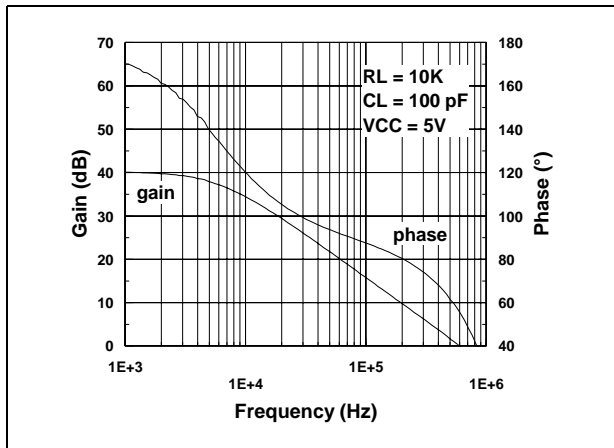


Figure 28. Gain bandwidth product vs. temperature

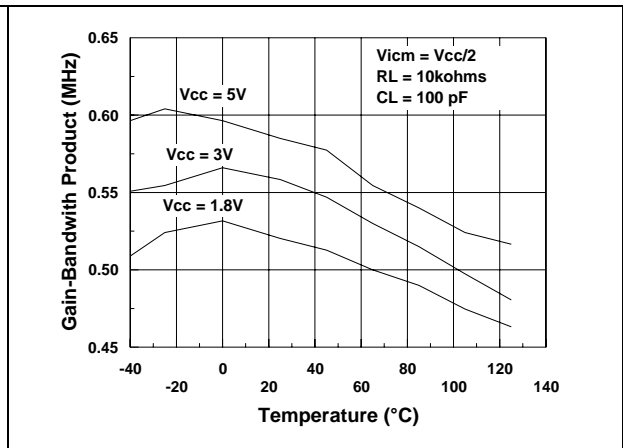


Figure 29. Gain bandwidth product vs. supply voltage

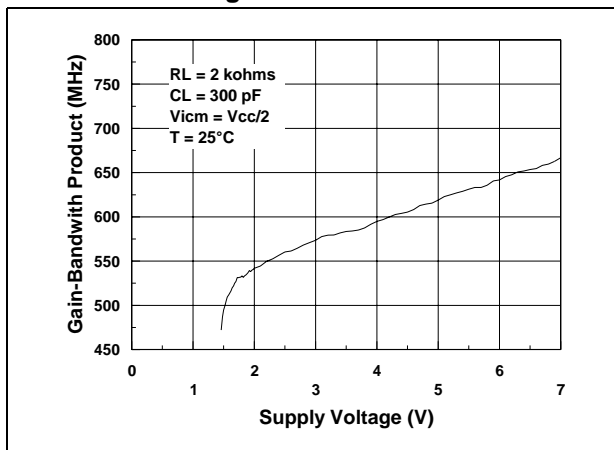


Figure 30. Slew rate vs. temperature

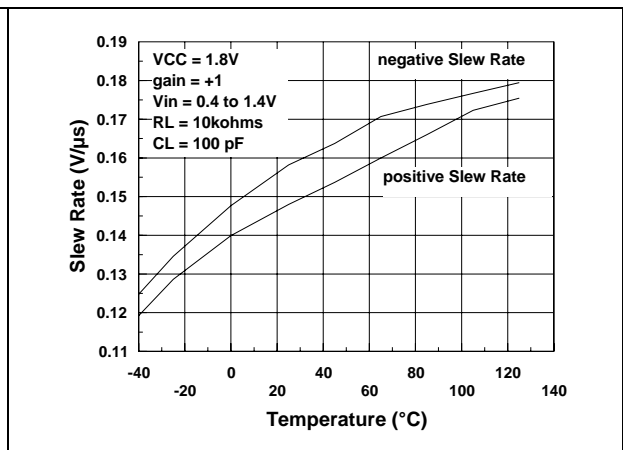


Figure 31. Slew rate vs. temperature

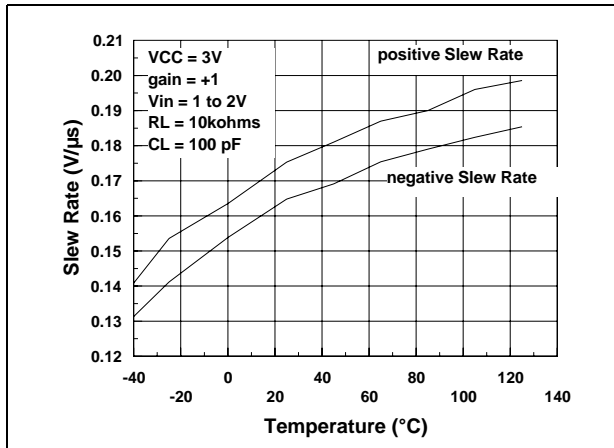


Figure 32. Slew rate vs. temperature

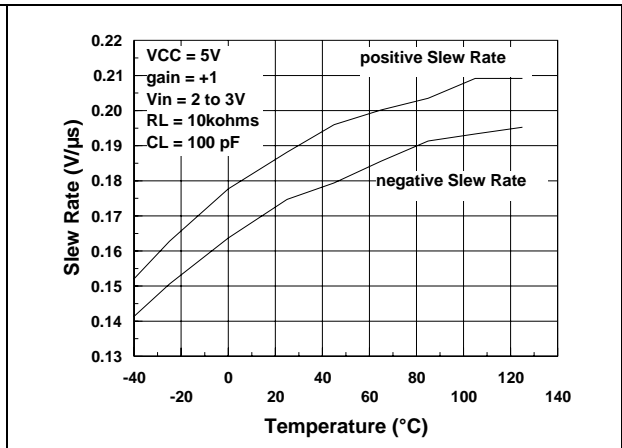


Figure 33. Phase margin vs. load capacitor

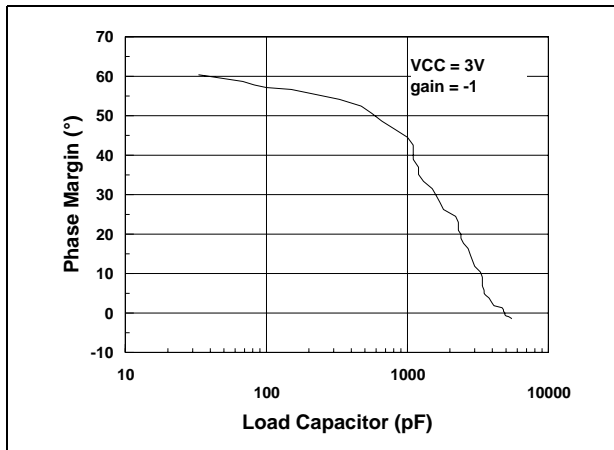


Figure 34. Phase margin vs. output current

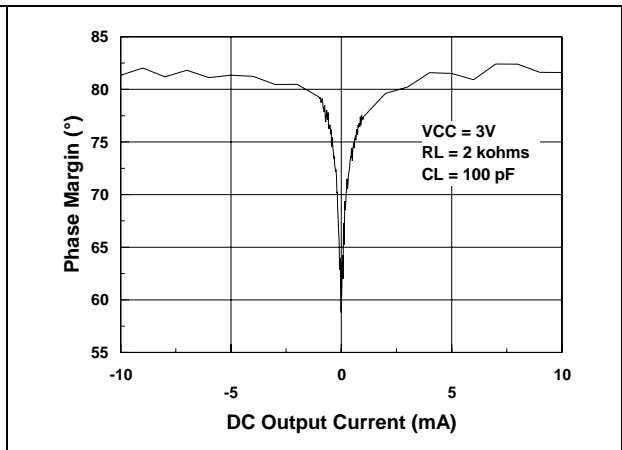


Figure 35. Equivalent input noise vs. frequency

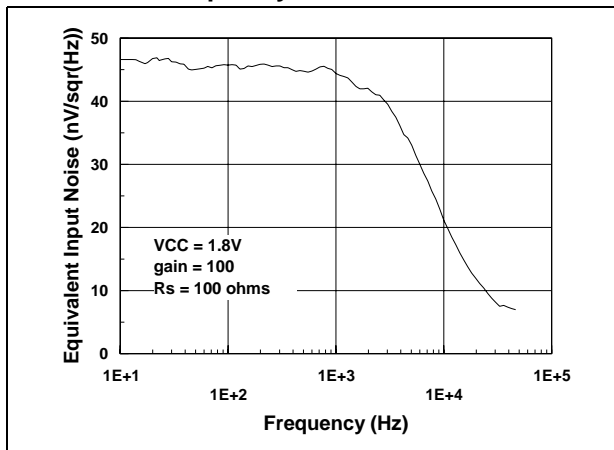


Figure 36. Distortion vs. output voltage

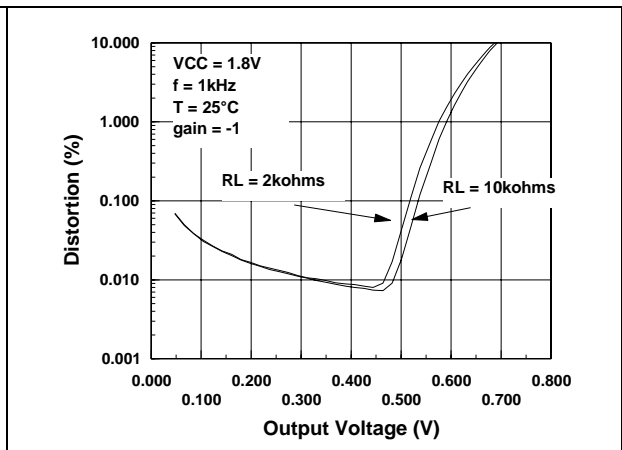


Figure 37. Distortion vs. output voltage

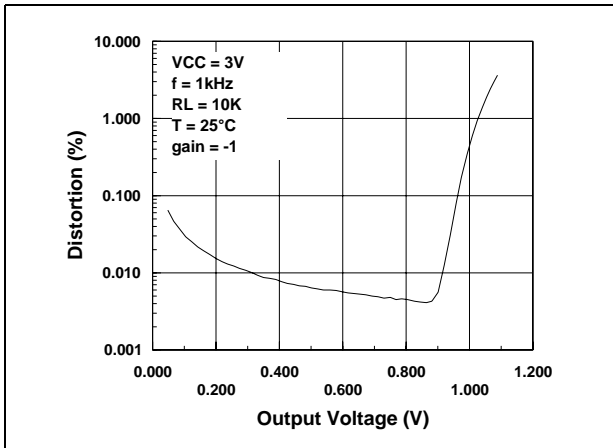


Figure 38. Distortion vs. output voltage

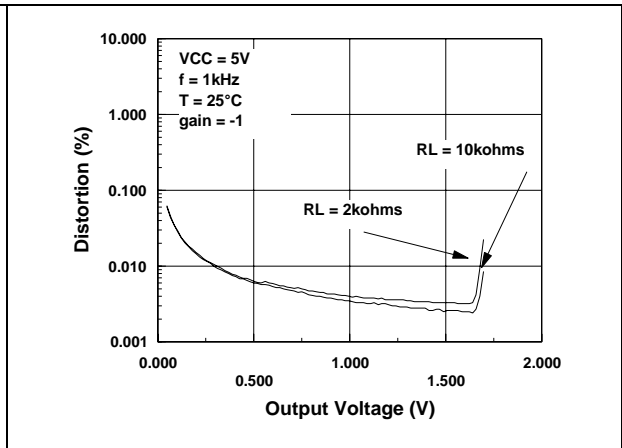
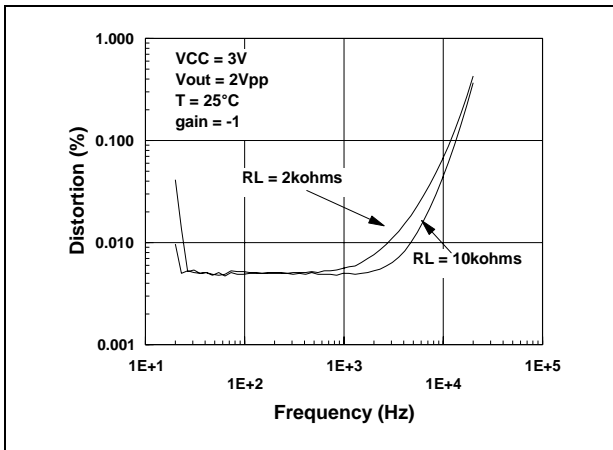


Figure 39. Distortion vs. frequency

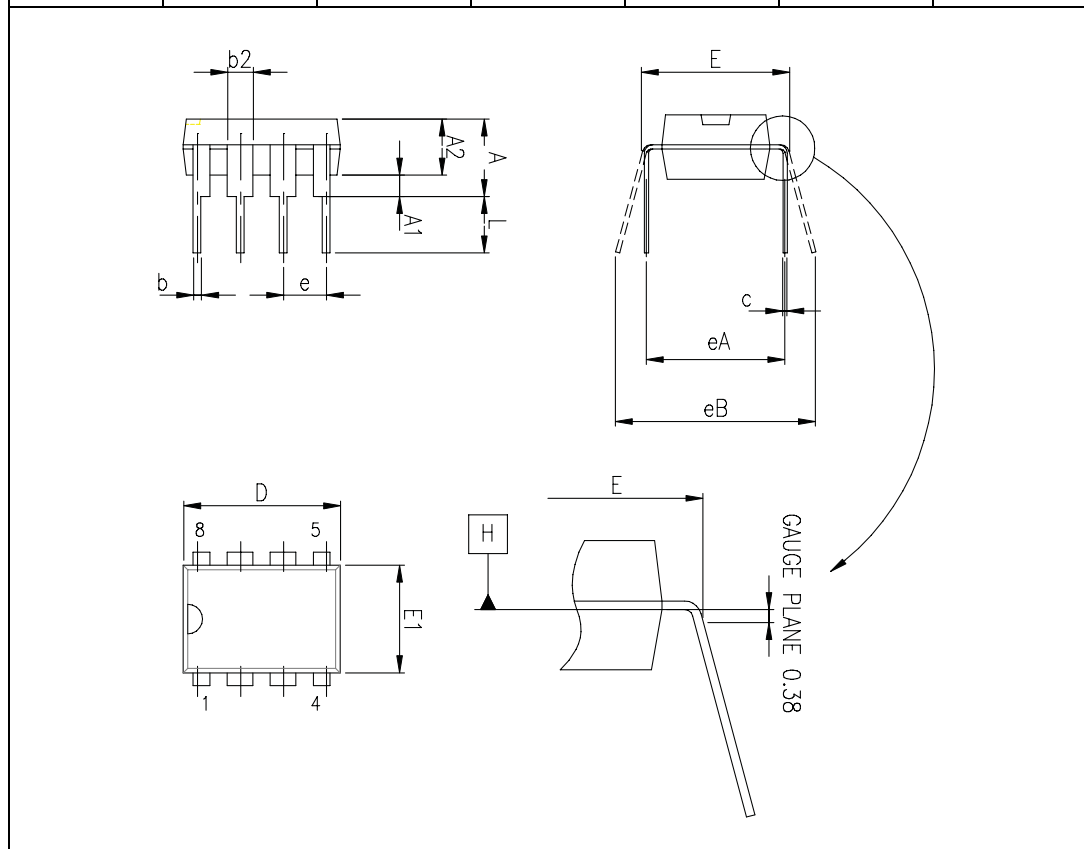


4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

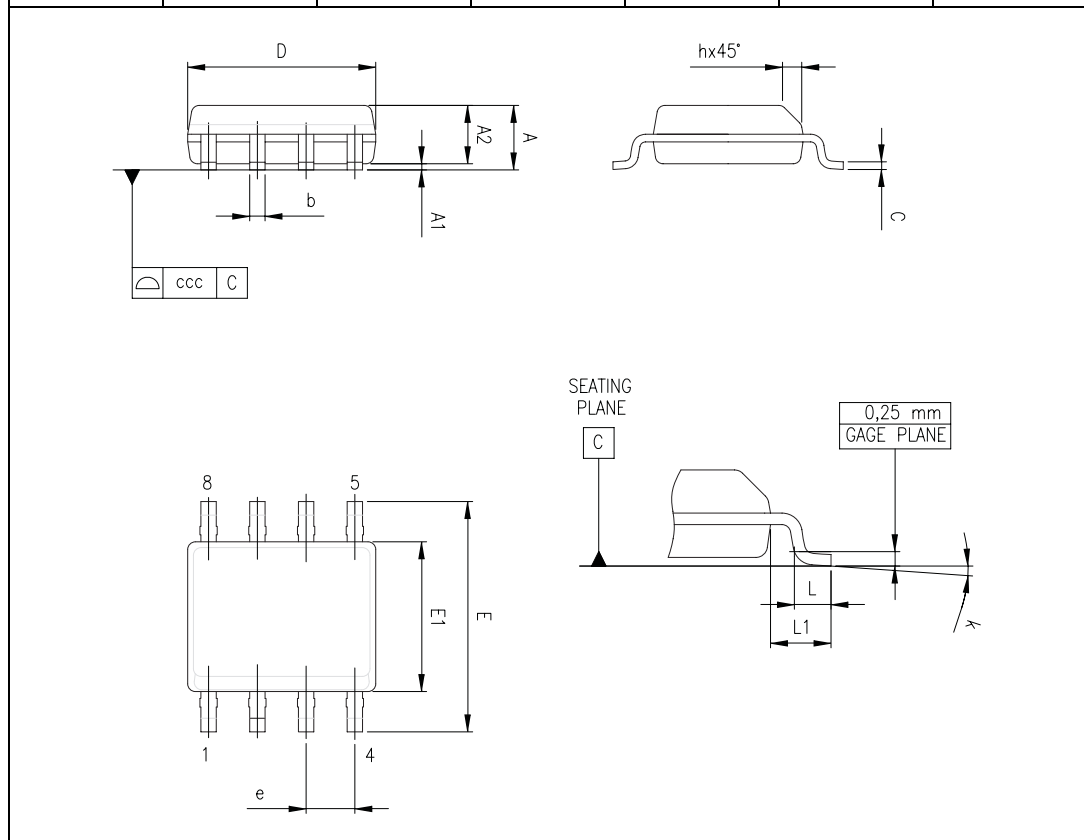
4.1 DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150



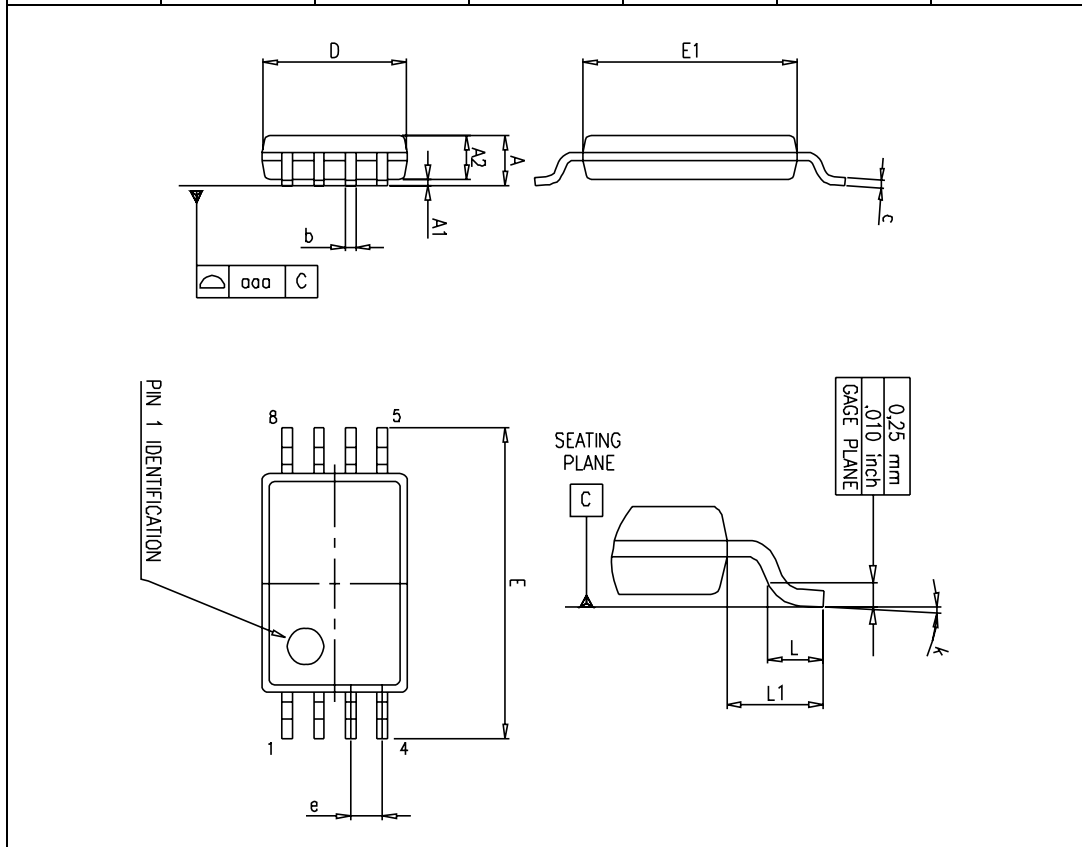
4.2 SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
H	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004



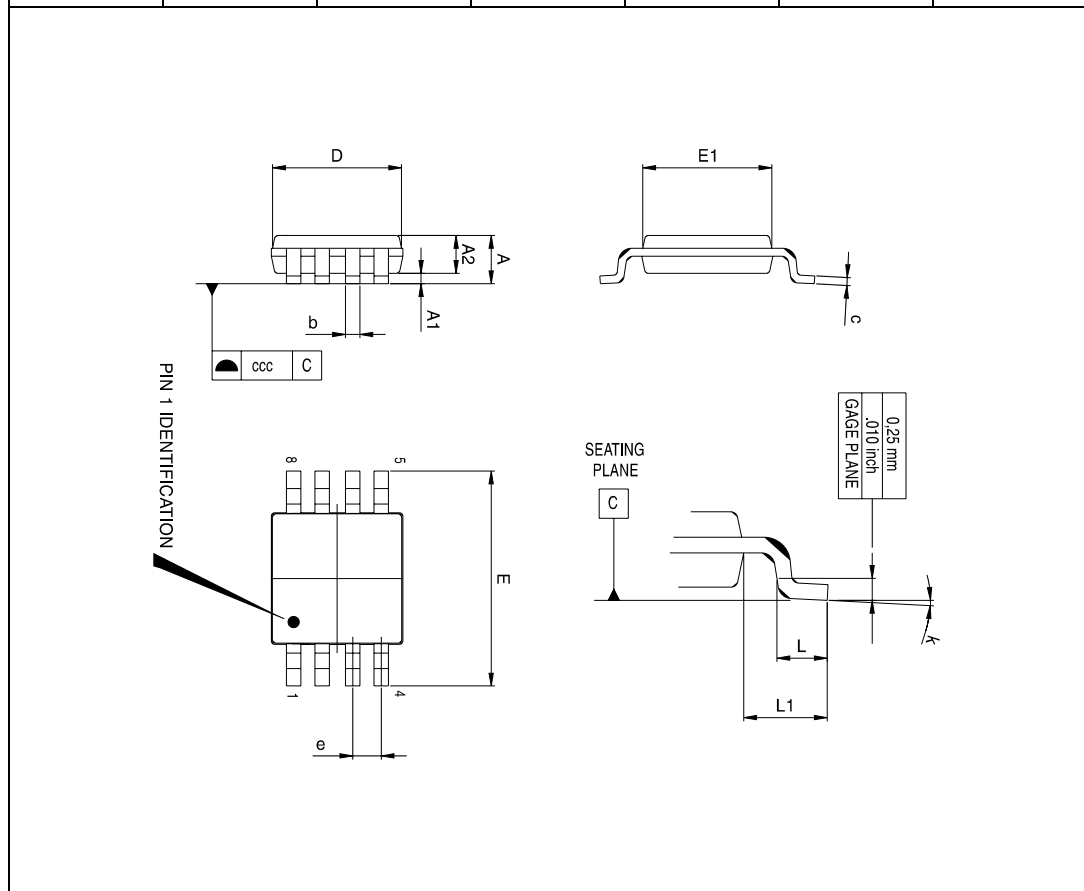
4.3 TSSOP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.1			0.004	



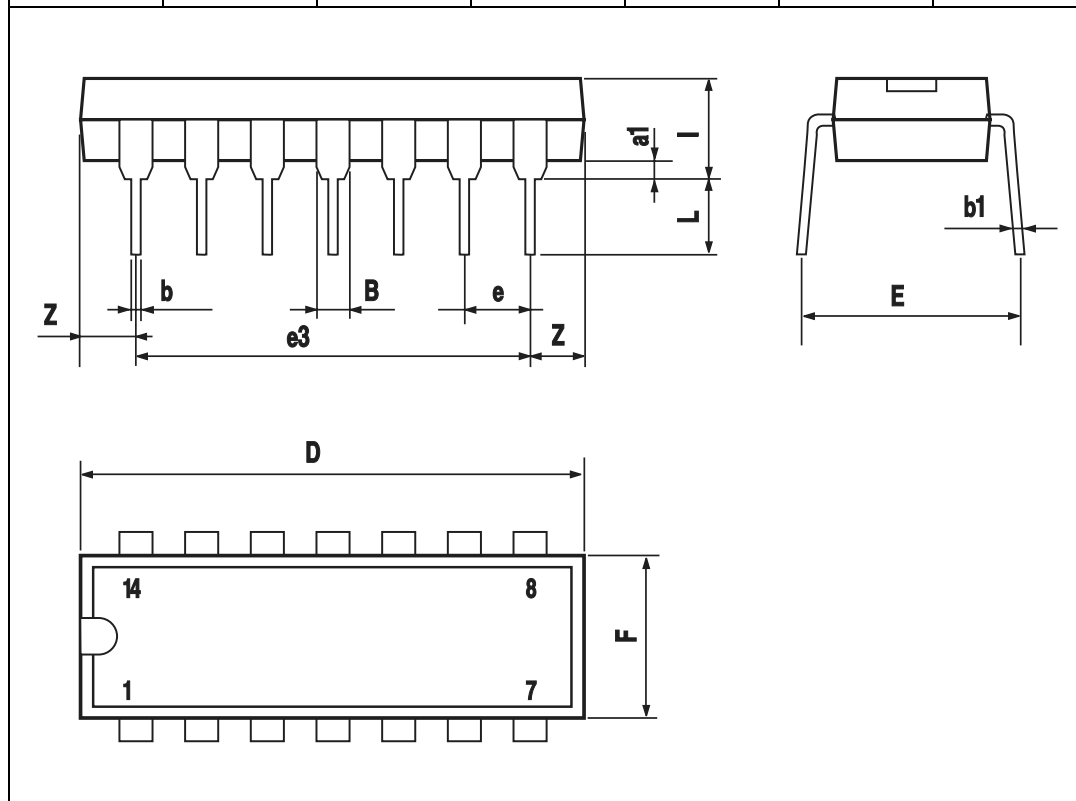
4.4 MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



4.5 DIP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



4.6 SO-14 package mechanical data

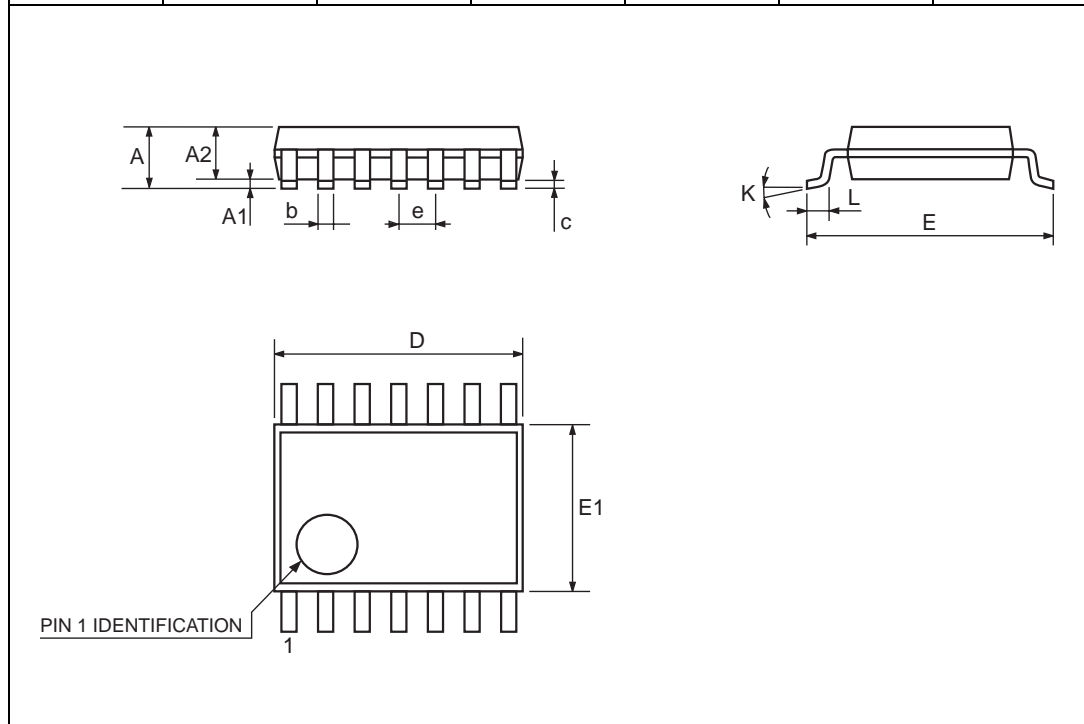
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

The image contains three mechanical drawings of the SO-14 package:

- Top View:** Shows the package footprint with dimensions D (total length), M (lead length), and F (width). Pin positions are labeled 1, 7, 8, and 14.
- Side View:** Shows the package height with dimensions A (total height), a2 (lead height), e (lead thickness), and b (lead width).
- Perspective View:** Shows the package with dimensions L (lead length), G (lead width), C (lead thickness), c1 (lead angle), a1 (lead thickness), b1 (lead width), and S (lead angle).

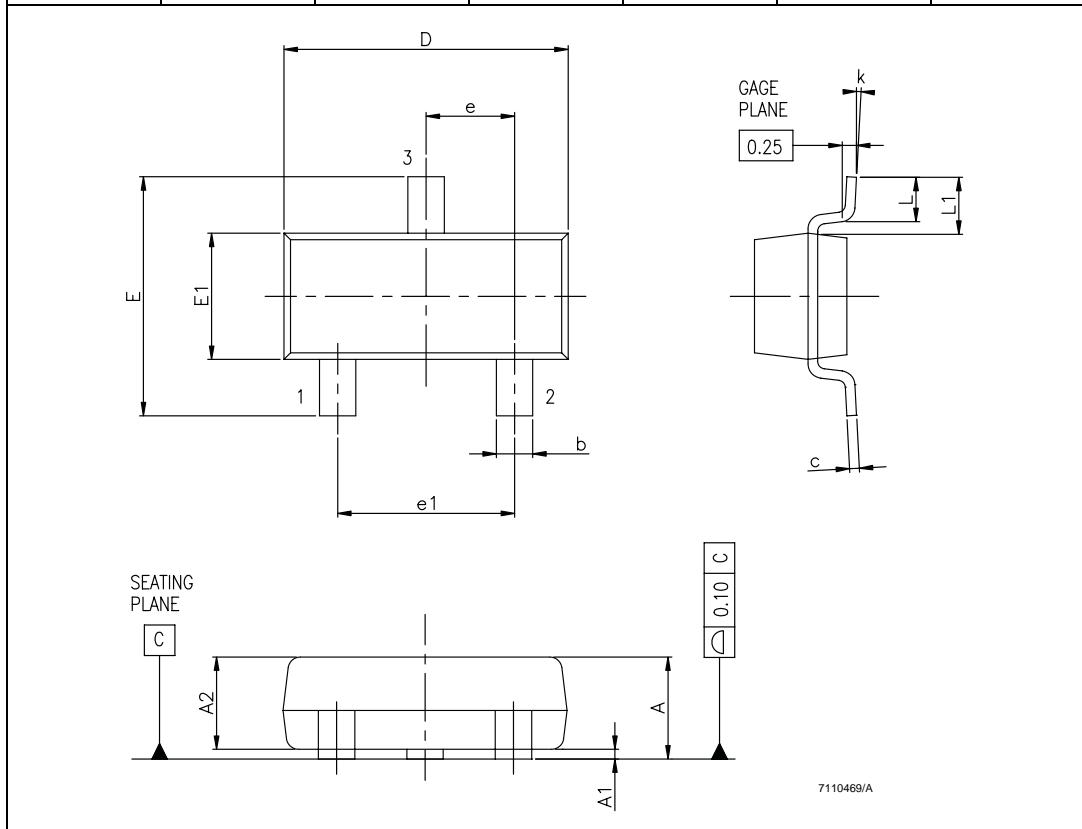
4.7 TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



4.8 SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.890		1.120	35.05		44.12
A1	0.010		0.100	0.39		3.94
A2	0.880	0.950	1.020	34.65	37.41	40.17
b	0.300		0.500	11.81		19.69
C	0.080		0.200	3.15		7.88
D	2.800	2.900	3.040	110.26	114.17	119.72
E	2.100		2.64	82.70		103.96
E1	1.200	1.300	1.400	47.26	51.19	55.13
e		0.950			37.41	
e1		1.900			74.82	
L	0.400		0.600	15.75		23.63
L1		0.540			21.27	
k	0°		8°	0°		8°



5 Ordering information

Table 6. Order codes

Part number	Temperature range	Package	Packing	Marking
TS1851ID/IDT	-40°C to +125°C	SO-8	Tube or Tape & reel	1851I
TS1851AID/AIDT				1851AI
TS1851ILT		SOT23-5L	Tape & reel	K161
TS1851AILT				K162
TS1852IN		DIP8	Tube	1852IN
TS1852AIN				1852AIN
TS1852ID/IDT		SO-8	Tube or Tape & reel	1852I
TS1852AID/AIDT				1852AI
TS1852IPT		TSSOP8 (Thin shrink outline package)	Tape & reel	1852I
TS1852AIPT				1852A
TS1852IST		MiniSO-8	Tape & reel	K161
TS1852AIST				K162
TS1854IN/AIN		DIP14	Tube	1854IN
TS1854ID/IDT		SO-14	Tube or Tape & reel	1854I
TS1854AID/AIDT				1854AI
TS1854IPT		TSSOP14 (Thin shrink outline package)	Tape & reel	1854I
TS1854AIPT				1854A

6 Revision history

Date	Revision	Changes
Feb-2002	1	First release.
May-2005	2	Modifications on AMR Table 1 on page 3 (explanation of V_{id} and V_i limits)
22-May-2007	3	Added limits in temperature in Table 3 , Table 4 , and Table 5 . Added SVR in Table 5 (SVR parameter removed from Table 3 and Table 4). Added equivalent input voltage noise in Table 3 , Table 4 , and Table 5 . Added R_{thjc} values in Table 1 on page 3 . Updated Table 6: Order codes .

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