# TPSM41625 4-V to 16-V Input, 25-A DC/DC Power Module with Current Sharing

## 1 Features

- Integrated inductor power solution
- 11-mm × 16-mm × 4.2-mm QFN package
  - All pins accessible from package perimeter
- Input voltage range: 4 V to 16 V
- Wide-output voltage range: 0.6 V to 7 V
- Selectable internal reference (±0.5% accuracy)
- Stackable up to two devices
  - Parallel outputs for higher current
  - Phase-interleaving for reduced ripple
- Efficiencies up to 97%
- Adjustable fixed switching frequency (300 kHz to 1 MHz)
- Allows synchronization to an external clock
- Advanced Current Mode provides ultra-fast load step response
- Power-good output
- Meets EN55011 radiated EMI limits
- Operating ambient range: –40°C to +105°C
- Operating IC junction range: –40°C to +125°C
- Create a custom design using the TPSM41625 With the WEBENCH® Power Designer

## 2 Applications

- Telecom and wireless infrastructure
- Industrial automated test equipment
- Enterprise switching and storage applications
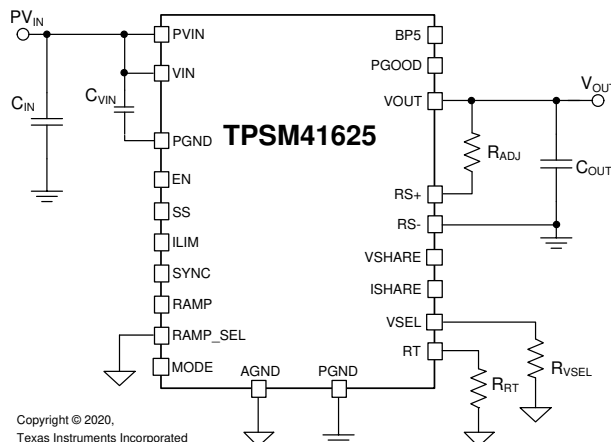- High-density distributed power systems

## 3 Description

The TPSM41625 power module is an easy-to-use integrated power supply that combines a DC/DC converter with power MOSFETs, a shielded inductor, and passives into a compact QFN package. This power solution requires few external components while maintaining the ability to adjust key parameters to meet specific design requirements. Applications requiring increased current can benefit from the ability to parallel two TPSM41625 devices.

The 11-mm × 16-mm × 4.2-mm, 69-pin QFN package with optimal package layout has excellent power dissipation capability which enhances thermal performance. The package footprint has all signal pins accessible from the perimeter and large thermal pads beneath the device. The TPSM41625 offers flexibilty with many features including power good signal, clock synchronization, programmable UVLO, soft-start timing selection, prebias start-up, as well as overcurrent and overtemperature protection making it a great product for powering a wide range of devices and systems.
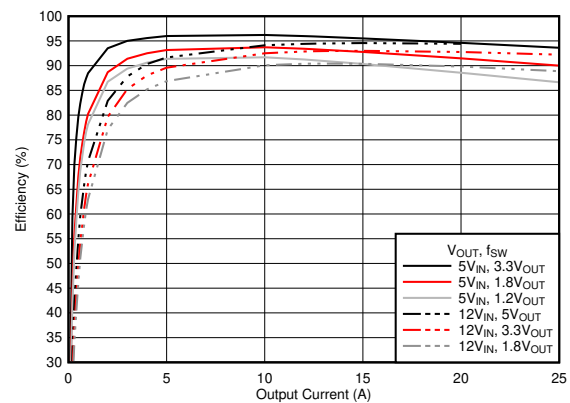
**Device Information**

| DEVICE NUMBER | PACKAGE [(1)](#) | BODY SIZE (NOM) |
|---|---|---|
| TPSM41625 | QFN (69) | 11 mm × 16 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**

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**Typical Efficiency**

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## Table of Contents

</div>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| September 2020 | * | Initial release |

<div style="writing-mode: vertical">ADVANCE INFORMATION</div>

Product Folder Links: *TPSM41625*

## 5 Pin Configuration and Functions
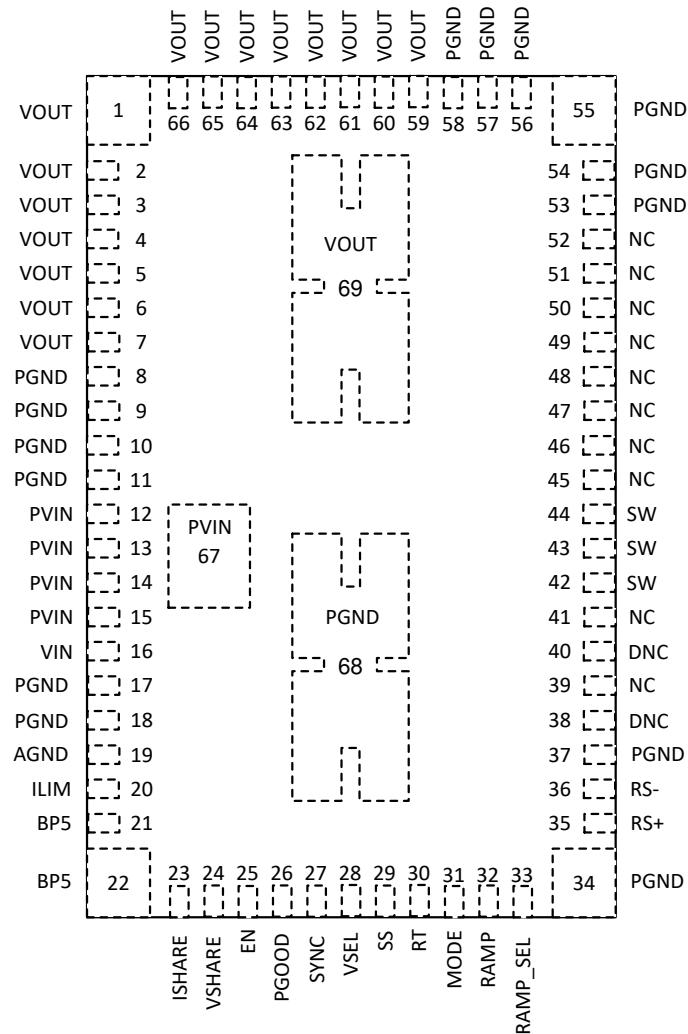


**Figure 5-1. 69-Pin QFN MOV Package (Top View)**

### Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | (1) | |
| AGND | 19 | G | Analog ground. Zero voltage reference for internal references and logic. Do not connect this pin to PGND; the connection is made internal to the device. |
| BP5 | 21, 22 | O | Output of an internal 5-V regulator used for the controller driver stage within the module. This output can be used to connect a pullup resistor to the PGOOD pin. Leave these pins open if not used as a pullup for PGOOD. |
| DNC | 38, 40 | – | Do Not Connect. Do not connect these pins to AGND, PGND, another DNC pin, or any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad. |
| EN | 25 | I | Enable pin. This pin turns the converter on when floated or opened. This pin is internally pulled up to the BP5 voltage when left open. The converter can be turned off by either driving it directly with a logic input or an open drain/collector device to connect this pin to AGND. An external voltage divider can be placed between this pin, AGND, and PVIN/VIN to create an external UVLO. |
| ILIM | 20 | I | Current limit setting pin. This pin sets the current limit threshold of the converter. Leave this pin open for the full current limit threshold. The current limit threshold can be lowered by connecting an appropriate resistor from this pin to AGND. |

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| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | (1) | |
| ISHARE | 23 | O | Current sharing pin. This pin is interconnected between modules for multi-phase configurations. Leave this pin open for single-phase configurations. |
| MODE | 31 | I | Mode select pin. This pin is used to configure the module for single-phase or multi-phase operation. For single-phase operation, this pin is used to select the API and Body Brake functions. For multi-phase operation, this pin selects the master/slave and SYNC configurations. |
| NC | 39, 41, 45-52 | – | Not connected. These pins are not connected to any circuitry within the module. It is recommended that these pins be connected to the PGND plane on the application board to enhance shielding and thermal performance. |
| PGND | 8-11, 17, 18, 34, 37, 53-58, 68 | G | This is the return path for the power stage of the device. Connect these pins to the input supply return, load return, and bypass capacitors associated with the PVIN and VOUT pins. |
| PGOOD | 26 | O | Power Good pin. Open-drain output that asserts low if the remote sense feedback voltage is not within the specified PGOOD thresholds. When using this signal as an output, a pullup resistor is required. If unused, leave this pin open. The BP5 output can be used as the pullup voltage source. |
| PVIN | 12-15, 67 | I | Input switching voltage. Supplies voltage to the power switches of the converter. Connect these pins to the input supply. Connect bypass capacitors between these pins and PGND, close to the module. |
| RAMP | 32 | I | Internal ramp selection. This pin is used to select an internal ramp amplitude. See Table 7-3 for recommended settings. An internal 78.7-kΩ resistor is connected between RAMP and RAMP_SEL within the module. To select the internal resistor, it is recommended to leave this pin open and to connect the RAMP_SEL pin to AGND. |
| RAMP_SEL | 33 | I | Internal default ramp selection. This pin is used to select the internal default ramp selection for the control loop. An internal 78.7-kΩ resistor is connected between RAMP and RAMP_SEL pins. Connect the RAMP_SEL pin to AGND and leave the RAMP pin open to select the internal resistor. |
| RS+ | 35 | I | Positive input to the internal differential remote sense amplifier. This pin is used for the feedback connection to VOUT. Connect this pin to the output voltage at the load. This connection can be made using a direct connection or an external upper feedback resistor, depending on the magnitude of VOUT and the VSEL selection. An internal 1-kΩ lower feedback resistor is connected across RS+ and RS– within the module. The RS+ connection is not needed for slave devices in multi-phase configurations, and should be left open. |
| RS– | 36 | I | Negative input to the internal differential remote sense amplifier. This pin is used for the feedback connection to VOUT return. Connect this pin to the output voltage return at the load. An internal 1-kΩ lower feedback resistor is connected across RS+ and RS– within the module. The RS- connection is not needed for slave devices in multi-phase configurations, and should be left open. |
| RT | 30 | I | Switching frequency setting pin. This analog pin is used to set the switching frequency of the converter by placing an external resistor from this pin to AGND. This pin also selects the phase interleaving of the module when used in multi-phase configurations. |
| SS | 29 | I | Soft-start selection pin. This pin is used to select the soft-start time. Ten possible selections are available by connecting an appropriate resistor from this pin to AGND. The selections range from 0.5 ms to 32 ms. |
| SW | 42-44 | O | Switch node. These pins are connected to the internal output inductor and switching MOSFETs. Connect these pins together using a small copper island beneath the device. Keep this copper island to a minimum to prevent issues with noise and EMI. |
| SYNC | 27 | I | Frequency synchronization pin. MODE can be used to configure this pin as a sync input or a sync output for external clock and multi-phase master/slave configurations. |
| VIN | 16 | I | Input bias voltage. Supplies the control circuitry of the power converter. Connect a 1-µF bypass capacitor from this pin to PGND (pins 17 and 18) in close proximity to the module. For split rail applications, connect this pin to an input bias supply. For strapped rail applications, connect this pin to PVIN through a 0 Ω to 10 Ω resistor. |
| VOUT | 1-7, 59-66, 69 | O | Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND in close proximity to the module. |
| VSEL | 28 | I | Internal reference voltage selection. This pin is used to select the desired internal reference voltage. Ten possible selections are available by connecting an appropriate resistor from this pin to AGND. The selections range from 0.6 V to 1.1 V. |
| VSHARE | 24 | O | Voltage sharing pin. This pin is interconnected between modules for multi-phase configurations. Leave this pin open for single-phase configurations. |

(1)    G = Ground, I = Input, O = Output, – = Not Connected

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | PVIN | | −0.3 | 17 | V |
| | PVIN to SW | DC | −0.3 | 25 | V |
| | | <10 ns | −5 | 25 | V |
| | VIN | | −0.3 | 18 | V |
| | VSEL, SS, MODE, RT, SYNC, EN, ISHARE, ILIM | | −0.3 | 7 | V |
| | RS+ | | −0.3 | 3.6 | V |
| | RS- | | −0.3 | 0.3 | V |
| | AGND, PGND | | −0.3 | 0.3 | V |
| | SW | DC | −0.3 | 20 | V |
| | | <10 ns | −5.0 | 20 | V |
| Output voltage | VOUT | | −0.3 | 7 | V |
| | BP5, RAMP | | −0.3 | 7 | V |
| | PGOOD | | −0.3 | 7 | V |
| | VSHARE | | −0.3 | 3.6 | V |
| Mechanical shock | Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted | | | tbd | G |
| Mechanical vibration | Mil-STD-883D, Method 2007.2, 20 to 2000 Hz | | | tbd | G |
| Operating IC junction temperature, $T_J$ [2] | | | −40 | 150 | °C |
| Operating ambient temperature, $T_A$ [2] | | | −40 | 105 | °C |
| Storage temperature, $T_{stg}$ | | | −40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | tbd | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | tbd | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | PV$_{IN}$, V$_{IN}$ | 4 | 16 | V |
|  | VSEL, SS, MODE, RT, SYNC, EN, ISHARE, ILIM | −0.1 | 5.5 | V |
|  | RS+ | −0.1 | 1.7 | V |
|  | RS- | −0.1 | 0.1 | V |
|  | AGND, PGND | −0.1 | 0.1 | V |
| Output voltage | V$_{OUT}$ | 0.6 | 7 | V |
|  | BP5, RAMP | −0.3 | 5.5 | V |
|  | PGOOD | -0.3 | 5.5 | V |
|  | VSHARE | −0.3 | 3.3 | V |
| Output current | I$_{OUT}$ | 0 | 25 | A |
| Operating IC junction temperature, T$_J$ |  | −40 | 125 | °C |
| Operating ambient temperature, T$_A$ |  | −40 | 105 | °C |

## 6.4 Thermal Information

| THERMAL METRIC [1] | | TPSM41625 | UNIT |
|---|---|---|---|
|  | | MOV (QFN) |  |
|  | | 69 PINS |  |
| R$_{\theta JA}$ | Junction-to-ambient thermal resistance [2] | 13.8 | °C/W |
| ψ$_{JT}$ | Junction-to-top characterization parameter [3] | 4.4 | °C/W |
| ψ$_{JB}$ | Junction-to-board characterization parameter [4] | 9.8 | °C/W |
| T$_{SHDN}$ | Thermal Shutdown Temperature | 165 | °C |
|  | Thermal Shutdown Hysteresis | 30 | °C |

(1)    For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2)    The junction-to-ambient thermal resistance, R$_{\theta JA}$, applies to devices soldered directly to a 90 mm × 90 mm, 6-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces R$_{\theta JA}$.

(3)    The junction-to-top characterization parameter, ψ$_{JT}$, estimates the junction temperature, T$_J$, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). T$_J$ = ψ$_{JT}$ × Pdis + T$_T$; where Pdis is the power dissipated in the device and T$_T$ is the temperature of the top of the device.

(4)    The junction-to-board characterization parameter, ψ$_{JB}$, estimates the junction temperature, T$_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). T$_J$ = ψ$_{JB}$ × Pdis + T$_B$; where Pdis is the power dissipated in the device and T$_B$ is the temperature of the board 1mm from the device.

## 6.5 Electrical Characteristics

Limits apply over $T_A$ = –40°C to +105°C, $PV_{IN}$= 12 V, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V, $V_{REF}$ = 1.0 V, $F_{SW}$ = 500 kHz, IOUT = 25 A, (unless otherwise noted); Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| $PV_{IN}$ | Input switching voltage | | 4 | | 16 | V |
| $V_{IN}$ | Input bias voltage | | 4 | | 16 | V |
| UVLO | $PV_{IN}$ undervoltage lockout | $PV_{IN}$ increasing, $I_{OUT}$ = 0 A | | 3.2 | | V |
| | | $PV_{IN}$ decreasing, $I_{OUT}$ = 2.5 A | | 3.0 | | V |
| | $V_{IN}$ undervoltage lockout | $V_{IN}$ increasing, $I_{OUT}$ = 0 A | | 3.8 | | V |
| | | $V_{IN}$ decreasing, $I_{OUT}$ = 2.5 A | | 3.6 | | V |
| $I_{VIN}$ | $V_{IN}$ bias current[1] | $V_{RS+}$ = 1.2 V, $I_{OUT}$ = 0 A, EN = OPEN, $T_A$ = 25°C | | 4.3 | | mA |
| $I_{VIN-STBY}$ | $V_{IN}$ standby current | $I_{OUT}$ = 0 A, EN = 0 V, $T_A$ = 25°C | | 4.3 | | mA |
| **OUTPUT VOLTAGE** | | | | | | |
| $V_{OUT}$ | Output voltage adjust | RS+ connected directly to $V_{OUT}$ | 0.6 | | 1.1 | V |
| | | RS+ connected to $V_{OUT}$ feedback divider | | | 7[1] [2] | V |
| | $V_{OUT}$ accuracy | 0.6V ≤ $V_{REF}$ ≤ 1.1V, $V_{RS+}$ = $V_{OUT}$, $I_{OUT}$ = 0A, -40°C ≤ $T_J$ = $T_A$ ≤ 125°C[1] | -0.5% | | 0.5% | |
| | Line regulation | Over $PV_{IN}$ range, $PV_{IN}$ = $V_{IN}$, $I_{OUT}$ = 0 A, $T_A$ = 25°C | | 0.01 | | % |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C | | 0.03 | | % |
| **OUTPUT CURRENT** | | | | | | |
| $I_{OUT}$ | Output current | Natural convection, $T_A$ = 25°C | 0 | | 25[2] | A |
| | Overcurrent threshold | | | 32 | | A |
| $I_{SHARE}$ | Current sharing for multi-phase operation[1] | $I_{OUT}$ ≤ 20 A/phase | | ±3 | | A |
| | | $I_{OUT}$ ≥ 20 A/phase | | ±15% | | |
| **BP5 REGULATOR** | | | | | | |
| $V_{BP5}$ | BP5 regulator output voltage | | 4.5 | 5 | 5.5 | V |
| $V_{BP5-DROPOUT}$ | BP5 regulator dropout voltage[1] | $V_{IN}$ = 4.5 V, $f_{SW}$ = 750 kHz, $T_A$ = 25°C | | | 365 | mV |
| **PERFORMANCE** | | | | | | |
| η | Efficiency | $I_{OUT}$ = 12.5 A | | 91 | | % |
| **RS+** | | | | | | |
| $R_{RS+-RS-}$ | Lower feedback resistor from RS+ to RS- | | 0.995 | 1 | 1.005 | kΩ |
| **ENABLE** | | | | | | |
| $V_{EN-H}$ | EN rising threshold | $I_{OUT}$ = 0 A | 1.45 | 1.6 | 1.75 | V |
| $V_{EN-L}$ | EN falling threshold | $I_{OUT}$ = 2.5 A | | 1.3 | | V |
| $I_{EN\_LKG}$ | EN input leakage current | $V_{IN}$ = 4.5 V, $I_{OUT}$ = 0 A | −1 | 0 | 1 | µA |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Soft-start time[1] | SS = OPEN | | | 4 | ms |
| $t_{SS-Range}$ | Soft-start range[1] | Programmable using SS pin | 0.5 | | 32 | ms |

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Limits apply over $T_A$ = –40°C to +105°C, $PV_{IN}$= 12 V, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V, $V_{REF}$ = 1.0 V, $F_{SW}$ = 500 kHz, IOUT = 25 A, (unless otherwise noted);  Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PGOOD** | | | | | | |
| $V_{PGOOD}$ | PGOOD thresholds[1] | $V_{RS+}$ rising (fault) | | 112% | | |
| | | $V_{RS+}$ falling (good) | | 105% | | |
| | | $V_{RS+}$ rising (good) | | 95% | | |
| | | $V_{RS+}$ falling (fault) | | 88% | | |
| $V_{PGOOD-LOW}$ | PGOOD low voltage with no supply voltage | $PV_{IN}$ = $V_{IN}$ = 0 V, $I_{PGOOD}$ = 80 µA | | | 0.8 | V |
| $I_{PGOOD-LKG}$ | PGOOD leakage current | $V_{IN}$ = 4.5 V, $V_{PGOOD}$ = 5 V, $I_{OUT}$ = 0 A | | | 15 | µA |
| **OVP / UVP** | | | | | | |
| $V_{OVP}$ | Overvoltage protection threshold[1] | $V_{RS+}$ rising | | 117% | | |
| $V_{UVP}$ | Under-voltage protection threshold[1] | $V_{RS+}$ falling | | 83% | | |
| **FREQUENCY and SYNC** | | | | | | |
| $f_{SW}$ | Switching frequency | VSEL = OPEN, RT = 44.2 kΩ, $I_{OUT}$ = 2.5 A | 450 | 500 | 550 | kHz |
| | Switching frequency range[1] | $I_{OUT}$ = 2.5 A | 300 | | 1000 | kHz |
| ton_min | Minimum on-time of SW[1] | | | 30 | | ns |
| toff_min | Minimum off-time of SW[1] | | | 250 | | ns |
| $V_{CLK-H}$ | Logic-high for SYNC[1] | | 2 | | | V |
| $V_{CLK-L}$ | Logic-low for SYNC[1] | | | | 0.8 | V |
| $T_{CLK-MIN}$ | Minimum pulse width for SYNC[1] | SYNC $F_{SW}$ = 500 kHz | 100 | | | ns |

(1)  Guaranteed by design, not production tested.

(2)  To determine IOUT range for a given set of conditions, see the Safe Operating Area graphs in "Typical Characteristics" section of the datasheet for more information.

**ADVANCE INFORMATION**

## 6.6 Typical Characteristics (PV$_{IN}$ = 12 V)

T$_A$ = 25°C, unless otherwise noted.
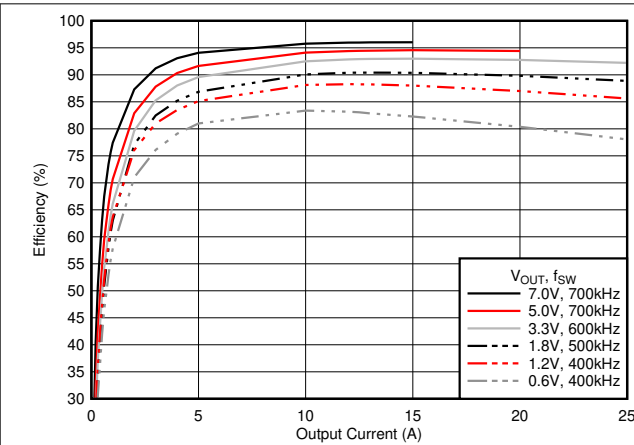


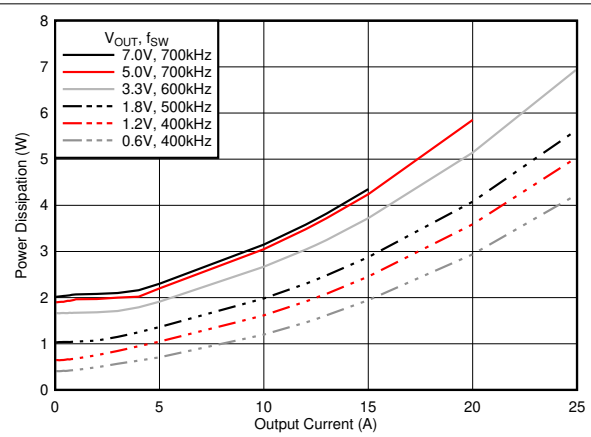**Figure 6-1. Efficiency vs Output Current**



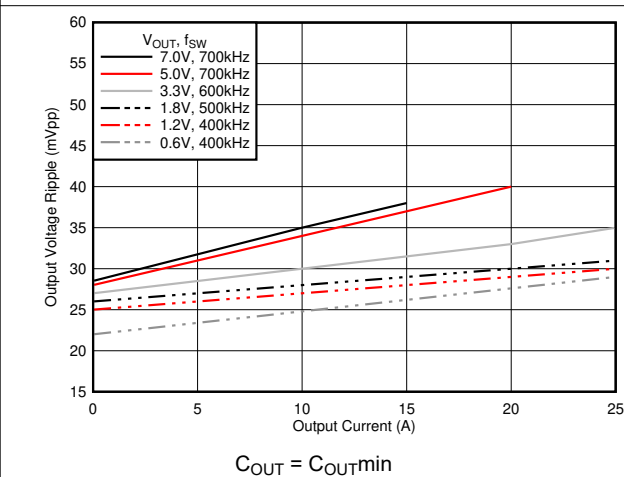**Figure 6-2. Power Dissipation vs Output Current**



C$_{OUT}$ = C$_{OUT}$min

**Figure 6-3. Output Voltage Ripple**



V$_{OUT}$ = 1.8 V          f$_{SW}$ = 500 kHz
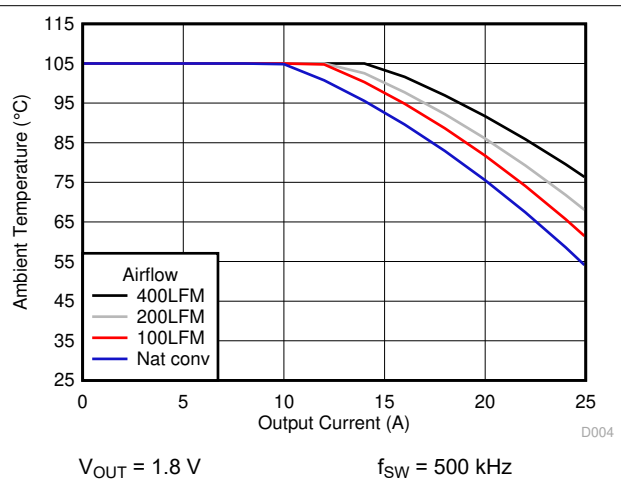
**Figure 6-4. Safe Operating Area**



V$_{OUT}$ = 3.3 V          f$_{SW}$ = 600 kHz
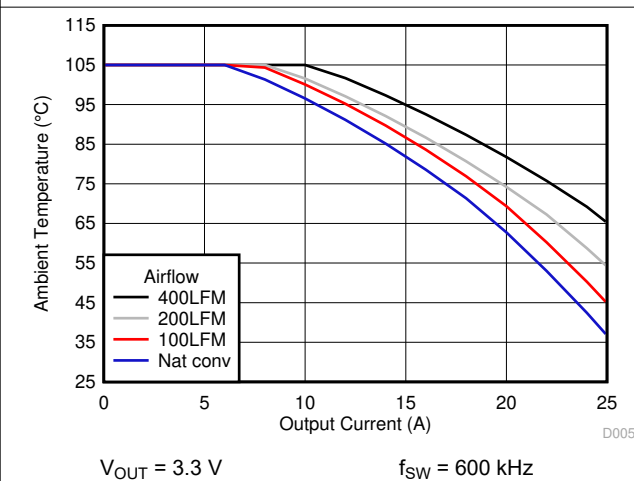
**Figure 6-5. Safe Operating Area**



V$_{OUT}$ = 5 V          f$_{SW}$ = 700 kHz
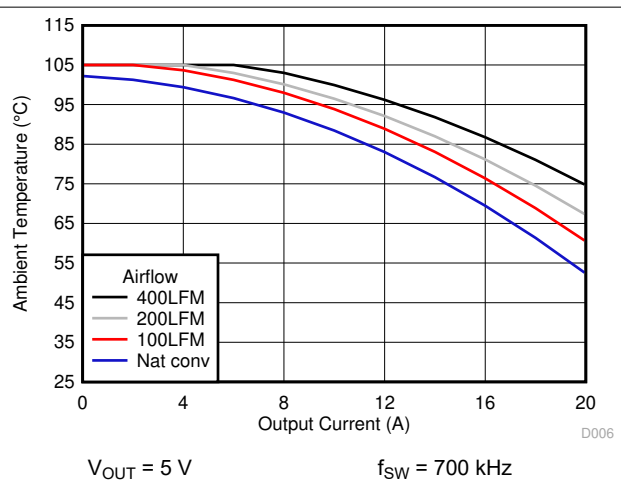
**Figure 6-6. Safe Operating Area**

**ADVANCE INFORMATION**

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Product Folder Links: *TPSM41625*

## 6.7 Typical Characteristics (PV$_{IN}$ = 5 V)

T$_A$ = 25°C, unless otherwise noted.

**ADVANCE INFORMATION**
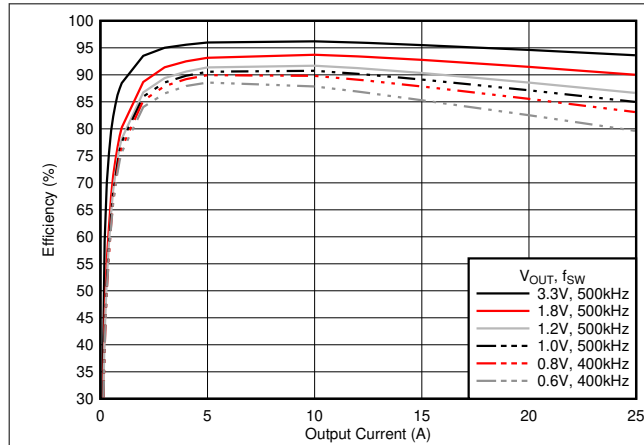


**Figure 6-7. Efficiency vs Output Current**
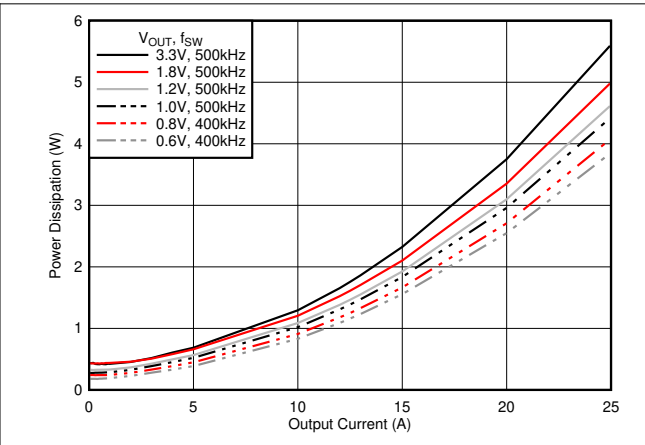


**Figure 6-8. Power Dissipation vs Output Current**



C$_{OUT}$ = C$_{OUT}$min
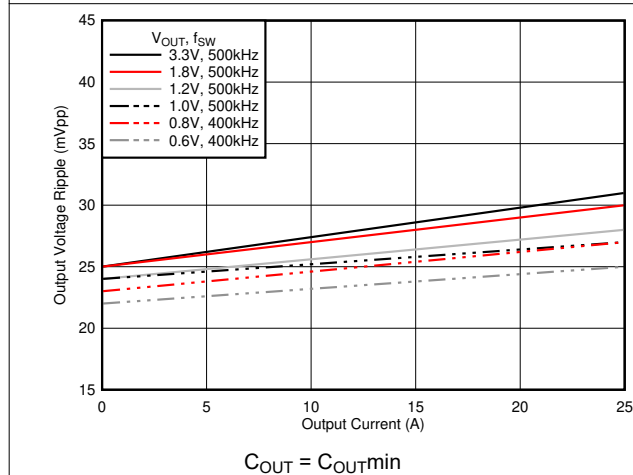
**Figure 6-9. Output Voltage Ripple**



V$_{OUT}$ = 1 V          f$_{SW}$ = 500 kHz
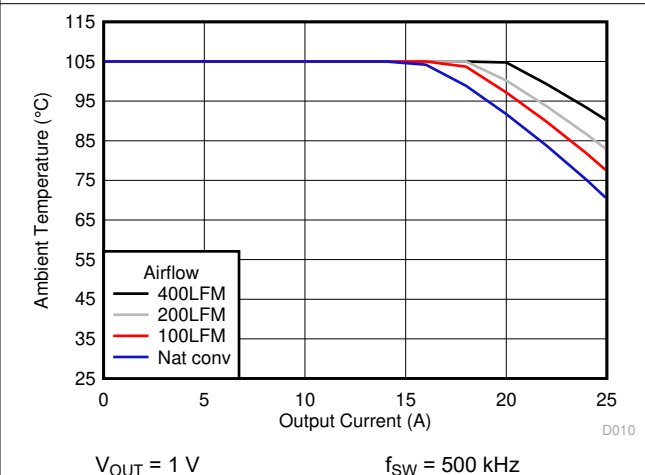
**Figure 6-10. Safe Operating Area**



V$_{OUT}$ = 1.8 V          f$_{SW}$ = 500 kHz
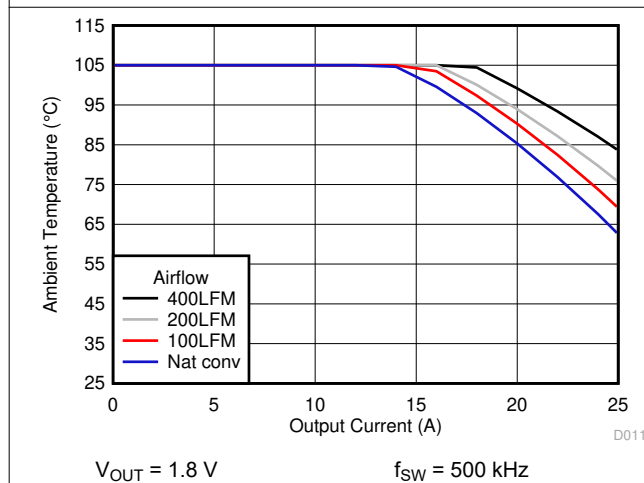
**Figure 6-11. Safe Operating Area**



V$_{OUT}$ = 2.5 V          f$_{SW}$ = 500 kHz

**Figure 6-12. Safe Operating Area**

Product Folder Links: *TPSM41625*

# 7 Detailed Description

## 7.1 Overview

The TPSM41625 is a full-featured, 4-V to 16-V input, 25-A, synchronous step-down converter with PWM, MOSFETs, inductor, and control circuitry integrated into a QFN package. The device integration enables small designs, while still leaving the ability to adjust key parameters to meet specific design requirements. The TPSM41625 provides an output voltage range of 0.6 V to 7 V, with a selectabl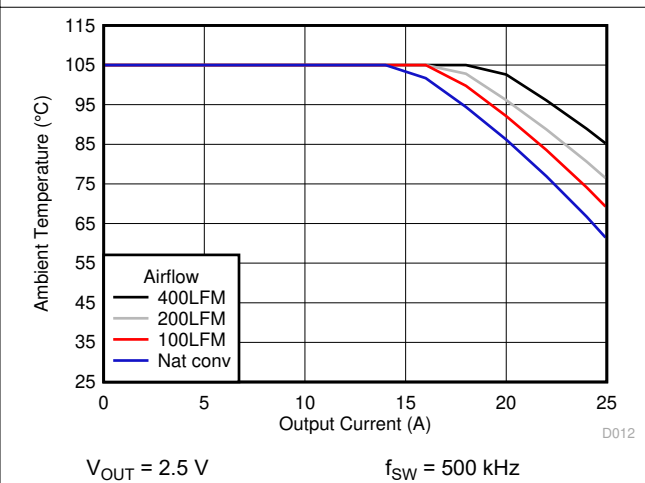e internal reference form 0.6 V to 1.1 V, for greater accuracy. An external resistor is used to adjust the output voltage to the desired output. The switching frequency is also adjustable by using an external resistor or a synchronization clock to accommodate various input and output voltage conditions and to optimize efficiency. Applications requiring increased current can benefit from the stackability (parallel outputs and phase-interleaving) of the TPSM41625 device.

The TPSM41625 has been designed for safe start-up into pre-biased loads. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the internal pullup current of the EN pin allows the device to operate with the EN pin floating. The EN pin can also be pulled low to put the device in standby mode to reduce input quiescent current. The device provides a power-good (PGOOD) signal to indicate when the output voltage is within regulation. Thermal shutdown and current limit features protect the device during an overload condition. A 69-pin QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

## 7.2 Functional Block Diagram



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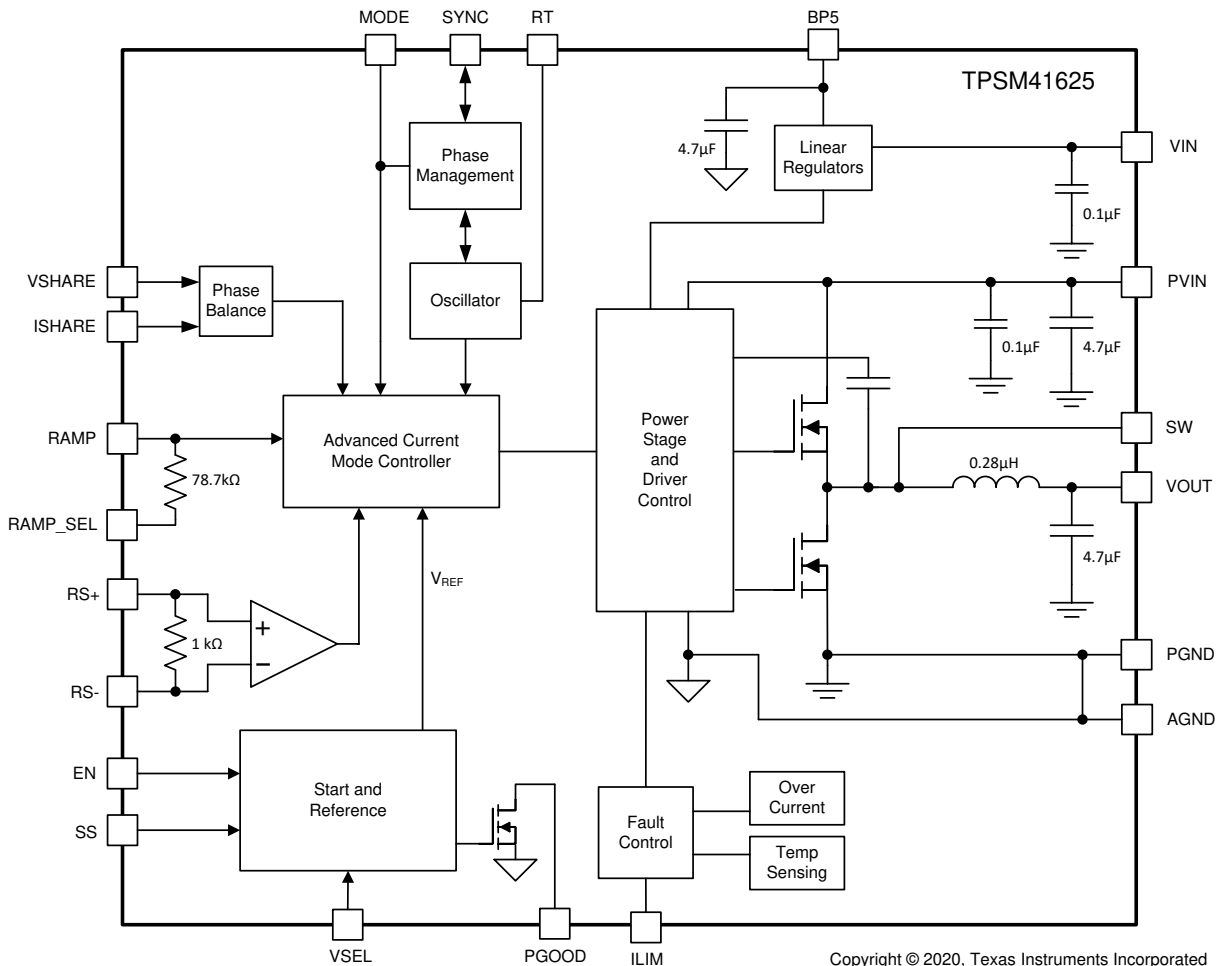
## 7.3 Feature Description

### 7.3.1 Setting the Output Voltage

The output voltage adjustment range of the TPSM41625 is 0.6 V to 7 V. Setting the output voltage requires first setting the internal reference voltage ($V_{REF}$). The internal reference voltage can be set from 0.6 V to 1.1 V using a resistor ($R_{VSEL}$) connected from VSEL (pin 28) to AGND (pin 19). Table 7-1 lists reference voltage selections and their corresponding setting resistors. If the required output voltage is the same as the reference voltage, connect the RS+ pin (pin 35) directly to VOUT to set the output voltage as shown in Figure 7-1. Output voltages greater than the reference voltage require an external voltage setting resistor ($R_{ADJ}$) between the RS+ pin and VOUT to set the output voltage as shown in Figure 7-2. The value for $R_{ADJ}$ can be calculated using Equation 1 or simply selected from the recommended values given in Table 7-2. Additionally, Table 7-3 includes the recommended switching frequency ($F_{SW}$), the recommended Ramp resistor ($R_{RAMP}$), and the minimum output capacitance for several output voltage ranges.

$$R_{ADJ} = \left( \frac{V_{OUT}}{V_{ref}} - 1 \right) \text{ (k}\Omega)$$

(1)

When setting the output voltage, selecting the highest reference voltage will result in the most accurate output voltage set point. The output voltage will be regulated at the connection point of RS+ or $R_{ADJ}$ to VOUT. Making the connection near the load improves regulation at the load.

**Table 7-1. Setting the Reference Voltage**

| $V_{REF}$ (V) | 0.6 | 0.7 | 0.75 | 0.8 | 0.85 | 0.9 | 0.95 | 1.0 | 1.05 | 1.1 |
|---|---|---|---|---|---|---|---|---|---|---|
| $R_{VSEL}$ Value (k$\Omega$)[1] | 0 | 8.66 | 15.4 | 23.7 | 34.8 | 51.1 | 78.7 | open | 121 | 187 |

(1) Resistors with ≤ 1% tolerance are recommended.

**Table 7-2. Setting the Output Voltage**

| $V_{OUT}$ (V) | 0.6 - 1.1 | 1.2 | 1.5 | 1.8 | 2.5 | 3.3 | 5.0 | 6.0 | 7.0 |
|---|---|---|---|---|---|---|---|---|---|
| $V_{REF}$ (V) [1] | 0.6 - 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 |
| $R_{ADJ}$ Value ($\Omega$)[1] | short | 90.9 | 365 | 634 | 1270 | 2000 | 3570 | 4420 | 5360 |

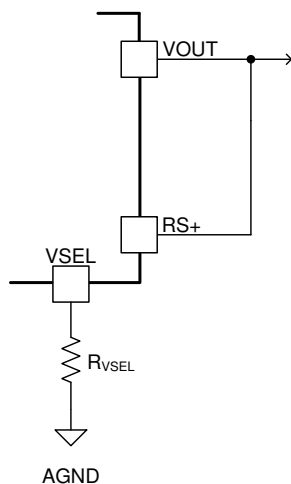(1) Selecting the highest reference voltage will result in the most accurate output voltage set point.



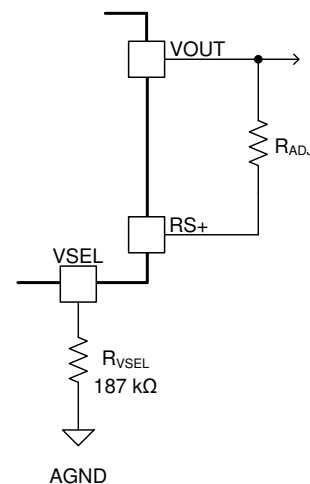**Figure 7-1. Setting the Output Voltage ($V_{OUT} = V_{REF}$)**

**Figure 7-2. Setting the Output Voltage ($V_{OUT} > V_{REF}$)**

Product Folder Links: *TPSM41625*

ADVANCE INFORMATION

**Table 7-3. Recommended F$_{SW}$, RAMP, and Required C$_{OUT}$**

| PV$_{IN}$ = 5 V | | | | | | |
|---|---|---|---|---|---|---|
| V$_{OUT}$ RANGE (V) | | RECOMMENDED F$_{SW}$ (kHz)[1] | ALLOWABLE F$_{SW}$ RANGE (KHZ) | R$_{RAMP}$ (kΩ) | MINIMUM REQUIRED C$_{OUT}$ (µF)[4] | |
| MIN | MAX | | | | MINIMUM CERAMIC[3] | ADDITIONAL REQUIRED CAPACITANCE[5] |
| 0.6 | < 0.8 | **400** | 300 - < 450 | 78.7 | 294[2] | 610 |
|  |  | 500 | 450 - < 550 | 187 |  | 490 |
|  |  | 600 | 550 - < 700 | 187 |  | 300 |
|  |  | 700 | 700 - 1000 | 78.7 |  | 280 |
| 0.8 | < 1.0 | **400** | 300 - < 450 | 78.7 | 289[2] | 600 |
|  |  | 500 | 450 - < 850 | 78.7 |  | 420 |
|  |  | 900 | 850 - 1000 | 78.7 |  | 240 |
| 1.0 | < 1.2 | **500** | 400 - 1000 | 187 | 284[2] | 190 |
| 1.2 | < 1.5 | **500** | 400 - 1000 | 187 | 277[2] | 100 |
| 1.5 | < 1.8 | **500** | 400 - 1000 | 187 | 266[2] | 90 |
| 1.8 | < 2.5 | **500** | 400 - 1000 | 187 | 254[2] | 85 |
| 2.5 | 3.3 | **500** | 400 - 1000 | 78.7 | 224[2] | 65 |
| PV$_{IN}$ = 12V | | | | | | |
| V$_{OUT}$ RANGE (V) | | RECOMMENDED F$_{SW}$ (kHz)[1] | ALLOWABLE F$_{SW}$ RANGE (kHz) | R$_{RAMP}$ (kΩ) | MINIMUM REQUIRED C$_{OUT}$ (µF)[4] | |
| MIN | MAX | | | | MINIMUM CERAMIC[3] | ADDITIONAL REQUIRED CAPACITANCE[5] |
| 0.6 | < 1.0 | **400** | 350 - < 450 | 78.7 | 294[2] | 760 |
|  |  | 500 | 450 - < 550 | 78.7 |  | 430 |
|  |  | 600 | 550 - 750 | 78.7 |  | 250 |
| 1.0 | < 1.2 | **400** | 350 - < 500 | 78.7 | 284[2] | 760 |
|  |  | 550 | 500 - < 600 | 78.7 |  | 430 |
|  |  | 600 | 600 - 1000 | 78.7 |  | 250 |
| 1.2 | < 1.8 | **400** | 350 - < 500 | 78.7 | 277[2] | 760 |
|  |  | 500 | 500 - < 600 | 121 |  | 185 |
|  |  | 600 | 600 - 1000 | 121 |  | 100 |
| 1.8 | < 2.5 | **400** | 350 - < 500 | 78.7 | 254[2] | 600 |
|  |  | 500 | 500 - < 600 | 187 |  | 430 |
|  |  | 600 | 600 - < 850 | 187 |  | 250 |
|  |  | 700 | 850 - 1000 | 78.7 |  | 90 |
| 2.5 | < 3.3 | **500** | 450 - < 650 | 78.7 | 224[2] | 450 |
|  |  | 700 | 650 - < 950 | 187 |  | 80 |
|  |  | 1000 | 950 - 1000 | 121 |  | 80 |
| 3.3 | < 5.0 | **600** | 550 - 1000 | 187 | 191[2] | 65 |
| 5.0 | 7.0 | **700** | 600 - 1000 | 187 | 134[2] | 0 |

(1)  The recommended F$_{SW}$ is shown in **bold** text. Increasing the frequency can reduce the required output capacitance as well as reduce ripple, however it may also reduce efficiency.

(2)  This value of minimum ceramic is the effective amount of 6x 47µF after taking into account DC bias and temperature derating.

(3)  The minimum required ceramic output capacitance must account for DC bias and temperature derating.

(4)  The Minimum Required output capacitance ensures start-up and stability. Additional output capacitance may be needed to meet transient response requirements.

(5)  The Additional Required Capacitance can be either ceramic or low-ESR polymer type. The total required output capacitance must include at least the amount of ceramic type listed in the Minimum Ceramic column.

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### 7.3.2 Output Voltage Current Rating

The rated output current of the TPSM41625 depends on the output voltage required for an application. The output current derates at output voltages above 3.3 V. The area under the curve in Figure 7-3 shows the operating range of the TPSM41625.



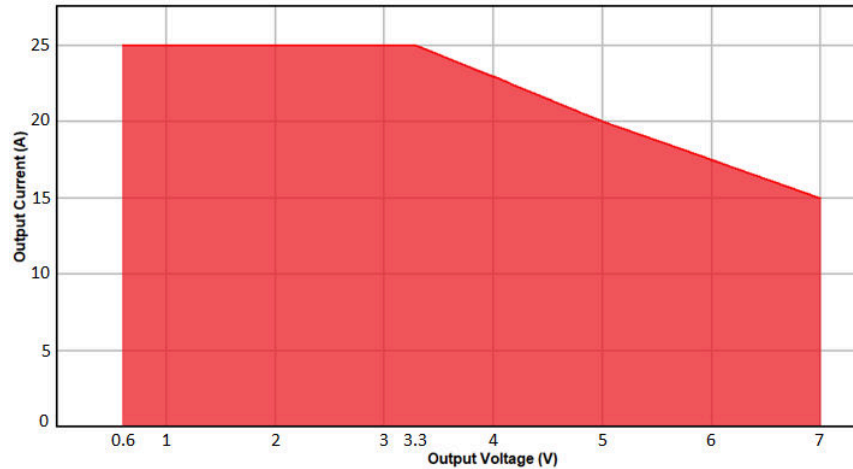**Figure 7-3. Output Voltage versus Output Current**

### 7.3.3 RS+/RS- Remote Sense Function

RS+ and RS- pins are the remote sensing inputs to the internal differential remote sense amplifier. An internal 1-kΩ lower feedback resistor is connected across RS+ and RS– within the module. The RS+ pin is used for the feedback connection to VOUT. Connect this pin to the output voltage at the load. This connection can be made using a direct connection or an external upper feedback resistor, depending on the magnitude of VOUT and the VSEL selection. The RS- pin is used for the feedback connection to VOUT return. Connect this pin to the output voltage return at the load. The RS- connection is not needed for slave devices in multi-phase configurations, and should be left open.

### 7.3.4 Ramp Select (RAMP and RAMP_SEL)

The RAMP and RAMP_SEL pins set the ramp amplitude for the internal control loop. Internal to the device, a 78.7-kΩ resistor is connected between RAMP and RAMP_SEL. Applications requiring 78.7-kΩ ramp setting should connect the RAMP_SEL pin to AGND and leave the RAMP pin open. Applications requiring a larger ramp setting resistor should connect it between the RAMP pin to AGND and leave the RAMP_SEL pin open. The recommended ramp setting resistor can be found in Table 7-3.

### 7.3.5 Switching Frequency (RT)

The switching frequency range of the TPSM41625 is 300 kHz to 1 MHz. The switching frequency can easily be set by connecting a resistor ($R_{RT}$) between the RT pin (pin 30) and AGND. Select $R_{RT}$ from Table 7-4 based on input voltage and desired switching frequency.

The switching frequency must be selected based on the input voltage and output voltage of the application. See Table 7-3 for the allowable switching frequency range for each output voltage.

**Table 7-4. $R_{RT}$ Frequency Setting Resistor (kΩ)**

| INPUT VOLTAGE | SWITCHING FREQUENCY | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 300 kHz | 350 kHz | 400 kHz | 450 kHz | 500 kHz | 550 kHz | 600 kHz | 650 kHz | 700 kHz | 750 kHz | 800 kHz | 850 kHz | 900 kHz | 950 kHz | 1 MHz |
| **5 V** | 69.8 | 59.0 | 52.3 | 45.3 | 40.2 | 36.5 | 33.2 | 30.1 | 28.0 | 26.1 | 23.7 | 22.1 | 21.0 | 19.6 | 18.2 |
| **8 V** | 73.2 | 61.9 | 53.6 | 47.5 | 42.2 | 38.3 | 34.8 | 32.4 | 29.4 | 27.4 | 25.5 | 23.7 | 22.1 | 21.0 | 19.6 |
| **10 V - 16 V** | 75.0 | 63.4 | 54.9 | 48.7 | 43.2 | 39.2 | 35.7 | 33.2 | 30.1 | 28.0 | 26.1 | 24.3 | 23.2 | 21.5 | 20.5 |

### 7.3.6 Synchronization (SYNC)

The TPSM41625 device can be synchronized to an external clock. When synchronizing, the external clock signal must be applied to the SYNC pin before the device reaches its VIN UVLO threshold. In a stand-alone configuration, the external clock frequency must be within ±20% of the frequency set by the $R_{RT}$ resistor.

In stackable configuration: (see *Section 7.3.7.1.1* for information on configuring the SYNC pins.)

1.  When there is no external system clock applied, the SYNC pin of the Master device should be configured as Sync-Out and the SYNC pin of the Slave device should be configured as Sync-In. Connecting the SYNC pins of the Master and any Slave devices will synchronize all devices to the frequency of the Master.
2.  When an external system clock is applied, the SYNC pin of the Master and Slave device should be configured as Sync-In and both devices will synchronize to the external system clock.

#### 7.3.6.1 Loss of Synchronization

This device does not support the dynamic application or removal of an external SYNC signal. If the external SYNC signal is removed, the device treats this as a clock fault and stops power conversion.

### 7.3.7 Stand-alone/Stackable Operation

The TPSM41625 can be operated as a single stand-alone device or two devices can be combined to operate together in a stackable configuration for increased current. These operation modes are selected using a resistor connected from MODE pin to AGND. In stand-alone mode, the resistor value connected to the MODE pin also selects whether the transient response feature is ON or OFF (see Table 7-8). In stackable mode, the transient response feature is not available. In stackable mode, the MODE resistor sets the device as master or slave, as well as SYNC pin function (sync in or sync out) of the master device (see Table 7-5).

**Table 7-5. MODE Pin Selections**

| OPERATION MODE | TRANSIENT FEATURE | SYNC MODE | MODE RESISTOR VALUE (kΩ) |
|---|---|---|---|
| Stand-alone | ON | Sync in | 78.7 |
| | | | 187 |
| | OFF | | open |
| Stackable | OFF | Master sync out | 23.7 |
| | | Master sync in | 34.8 |
| | | Slave sync in | 51.1 |

### 7.3.7.1 Stackable Synchronization

#### 7.3.7.1.1 Sync Configuration

In stackable mode, a resistor between the MODE pin and AGND sets the device as master or slave, as well as SYNC pin function (sync in or sync out) of the master device. See Table 7-6 for Mode resistor values.

**Table 7-6. MODE Setting for SYNC Function**

| SYNC FUNCTION | MODE RESISTOR VALUE (kΩ) | NOTE |
|---|---|---|
| Master sync out | 23.7 | • Sync pin to send out clock<br>• RT pin to set frequency |
| Master sync in | 34.8 | • Sync pin to receive clock<br>• RT pin to set sync point |
| Slave sync in | 51.1 | • Sync pin to receive clock<br>• RT pin to set sync point |

#### 7.3.7.1.2 Clock Sync Point Selection

The TPSM41625 device implements a unique clock synchronization scheme for phase interleaving between devices. This is only used when stacking multiple devices. The device will receive a clock signal through the SYNC pin and generate sync points to achieve phase interleaving. Sync point options can be selected with a resistor from the RT pin to AGND. Figure 7-4 shows the clock signals for a Master and a Slave device with a 180° phase shift. See Table 7-7 for clock sync options and the corresponding RT resistor value.
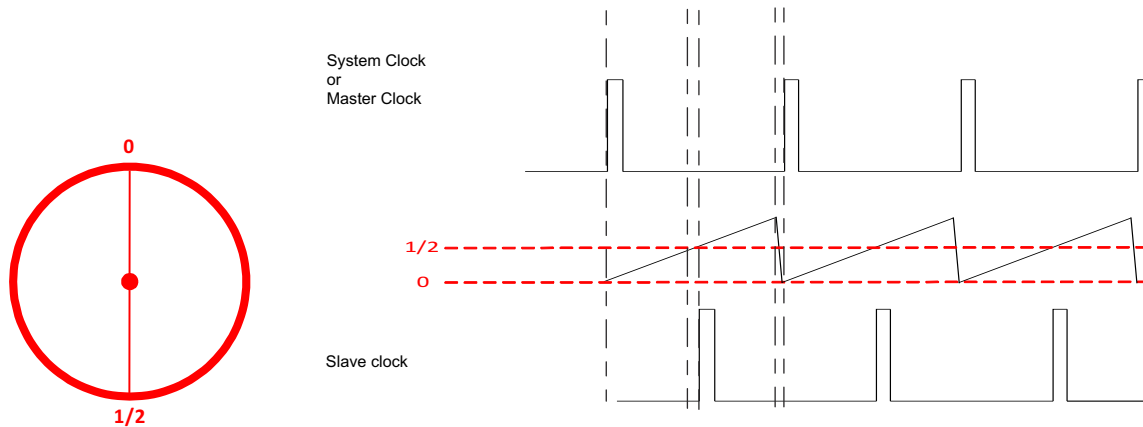


**Figure 7-4. 2-Phase Stackable with 180° Clock Phase Shift**

**Table 7-7. Sync Point Selection**

| CLOCK SYNC OPTIONS | RT RESISTOR VALUE (kΩ) |
|---|---|
| 0 (0° Interleaving) | SHORT |
| 1/2 (180° Interleaving) | OPEN |

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### 7.3.7.1.3 Configuration 1: Dual Phase Master Sync Out Clock-to-Slave

- Direct SYNC, VSHARE, and ISHARE connections between master and slave
- Switching frequency is set by RT pin of master, and pass to slave through SYNC pin. SYNC pin of master will be configured as sync out by its MODE pin.
- Slave receives clock from SYNC pin. Its RT pin determines the sync point for clock phase shift.
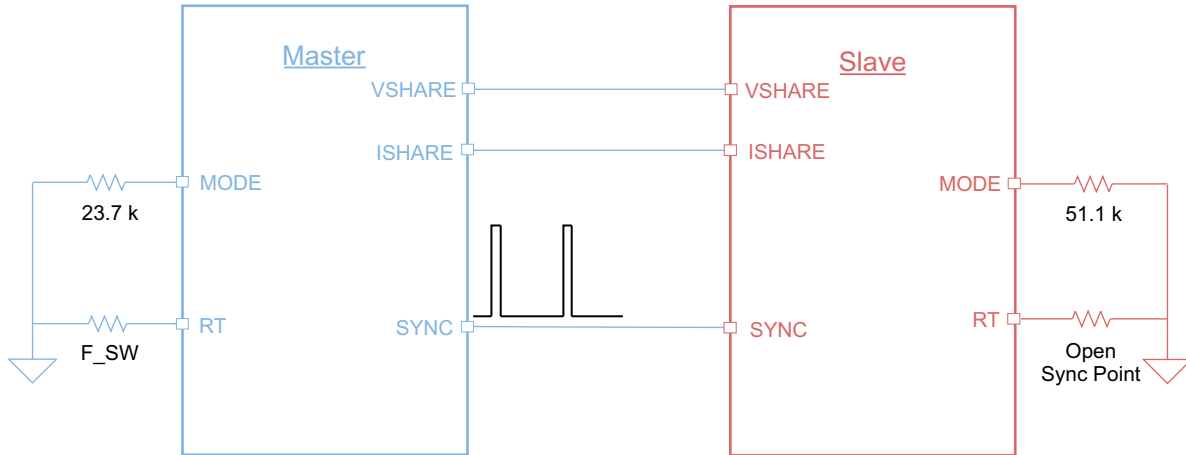


**Figure 7-5. 2-Phase Stackable with 180° Phase Shift: Master Sync Out Clock-to-Slave**

### 7.3.7.1.4 Configuration 2: Dual Phase Master and Slave Sync to External System Clock

- Direct connection between external clock and SYNC pin of master and slave
- Direct VSHARE and ISHARE connections between master and slave
- SYNC pin of master is configured as sync in by its MODE pin.
- Master and slave receive external system clock from SYNC pin. Their RT pin determine the sync point for clock phase shift.
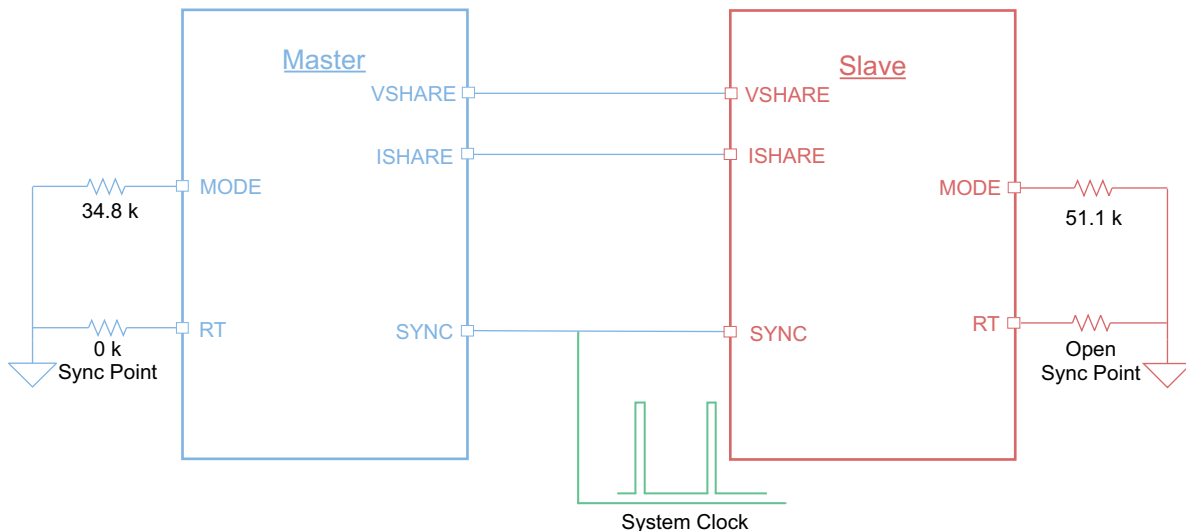


System Clock

**Figure 7-6. 2-Phase Stackable with 180° Phase Shift: Master and Slave Sync to External System Clock**

**ADVANCE INFORMATION**

Product Folder Links: *TPSM41625*

### 7.3.8 Improved Transient Performance versus Fixed Frequency (Stand-alone Operation Only)

The TPSM41625 is a fixed frequency converter. The major limitation for any fixed frequency converter is that during transient load step up, the output voltage drops until the next clock cycle of the converter before it can respond to the load change. The TPSM41625 implements a special circuitry to improve transient performance. During a load step up, the converter can issue an additional PWM pulse before the next available clock cycle to stop output voltage from further dropping, thus reducing the undershoot voltage. The additional pulse during a transient means that the device is not fixed frequency during the transient.

During load step-down, the TPSM41625 implements a body-brake function that turns off both high-side and low-side FET, and allows power to dissipate through the low-side body diode, reducing overshoot. This approach is very effective while having some impact on efficiency during transient.

In stand-alone mode, choose whether the transient response feature is enabled by placing either a 78.7-kΩ or 187-kΩ resistor between the MODE pin and AGND. A 78.7-kΩ MODE resistor is recommended when the output voltage is 0.6 V to 1.8 V or in applications that are more susceptible to noise. Leave the MODE pin open to operate in fixed frequency during a load step, (see Table 7-8).

**Table 7-8. Stand-Alone Operation Feature Selections**

| STAND-ALONE OPERATION | MODE RESISTOR VALUE (kΩ) |
|---|---|
| Transient Feature | 78.7 |
| | 187 |
| Fixed Frequency | open |

### 7.3.9 Output On/Off Enable (EN)

The EN pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low operating current state. The EN pin has an internal pullup to BP5, allowing the user to float the EN pin for enabling the device.

If an application requires controlling the EN pin, either drive it directly with a logic input or use an open drain/ collector device to interface with the pin. Applying a low voltage to the enable control (EN) pin disables the output of the supply. When the EN pin voltage exceeds the threshold voltage, the supply executes a soft-start power-up sequence.

### 7.3.10 Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the output voltage is between 92% and 108% of the set-point voltage, the PGOOD pin pulldown is released and the pin floats. A pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source of 5.5 V or less is recommended. The PGOOD pin is pulled low when the output voltage is lower than 88% or greater than 112% of the set-point voltage.

### 7.3.11 Soft-Start Operation

For the TPSM41625 device, the soft-start time controls the inrush current required to charge the output capacitors during start-up. When the device is enabled, the output voltage ramps from 0 V to the set-point voltage in the time selected by the SS pin. The device offers 10 selectable soft start options ranging from 0.5 ms to 32 ms. See Table 7-9 for details.

**Table 7-9. SS Pin Configuration**

| SS TIME | 0.5 ms | 1 ms | 2 ms | 4 ms | 5 ms | 8 ms | 12 ms | 16 ms | 24 ms | 32 ms |
|---|---|---|---|---|---|---|---|---|---|---|
| RESISTOR VALUE (kΩ) | 0 | 8.66 | 15.4 | OPEN | 23.7 | 34.8 | 51.1 | 78.7 | 121 | 187 |

### 7.3.12 Input Capacitor Selection

The TPSM41625 requires a minimum input capacitance of 88 µF of ceramic type. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. An additional 100 µF of non-ceramic, bulk capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. Table 7-10 includes a preferred list of capacitors by vendor.

**Table 7-10. Recommended Input Capacitors**

| VENDOR[1] | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
| --- | --- | --- | --- | --- | --- |
| | | | WORKING VOLTAGE (V) | CAPACITANCE (µF) [3] | ESR (mΩ) [2] |
| TDK | X7R | C3225X7R1E226M250AB | 25 | 22 | 2 |
| Murata | X7R | GRM32ER71E226KE15L | 25 | 22 | 2 |
| Panasonic | ZA | EEHZA1H101P | 50 | 100 | 28 |

(1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C
(3) Specified capacitance values

### 7.3.13 Output Capacitor Selection

The minimum required output capacitance of the TPSM41625 is a function of the output voltage and is shown in Table 7-3. The required capacitance can be comprised of all ceramic capacitors or a combination of ceramic and low-ESR polymer type capacitors. When adding additional capacitors, low-ESR capacitors like the ones recommended in Table 7-11 are required. The required capacitance above the minimum is determined by actual transient deviation requirements.

**Table 7-11. Recommended Output Capacitors**

| VENDOR[1] | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
| --- | --- | --- | --- | --- | --- |
| | | | WORKING VOLTAGE (V) | CAPACITANCE (µF) [3] | ESR (mΩ) [2] |
| Murata | X7R | GCM32ER70J476K | 6.3 | 47 | 2 |
| Taiyo Yuden | X7R | LMK325B7476MM-PR | 10 | 47 | 2 |
| Murata | X7R | GRM32ER71A476K | 10 | 47 | 2 |
| TDK | X5R | C3225X5R0J107M | 6.3 | 100 | 2 |
| Murata | X5R | GRM32ER60J107M | 6.3 | 100 | 2 |
| Murata | X5R | GRM32ER61A107M | 10 | 100 | 2 |
| Murata | X6S | GRM32EC80G227ME05L | 4.0 | 220 | 2 |
| Panasonic | POSCAP | 4TPE220MF | 4.0 | 220 | 15 |
| Kemet | T520 | T520D227M006ATE015 | 6.3 | 220 | 15 |
| Panasonic | POSCAP | 6TPE330MAA | 6.3 | 330 | 10 |
| Kemet | T520 | T520D337M006ATE010 | 6.3 | 330 | 10 |
| Kemet | T520 | T520X337M010ATE010 | 10 | 330 | 10 |

(1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C
(3) Specified capacitance values

### 7.3.14 Current Limit (ILIM)

The current limit of the TPSM41625 is internally set to 32 A (typ.) by leaving the ILIM pin open. Connecting a resistor between the ILIM pin and AGND adjusts the current limit threshold lower. Refer to Table 7-12 for current limit adjustment values.

**Table 7-12. Current Limit Adjust**

| CURRENT LIMIT REDUCTION | 10 % | 20 % | 30 % | 40 % | 50 % |
| --- | --- | --- | --- | --- | --- |
| $R_{ILIM}$ (kΩ) | 191 | 118 | 78.7 | 54.9 | 37.4 |

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### 7.3.15 Safe Start-up into Pre-Biased Outputs

The TPSM41625 device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch.

### 7.3.16 Overcurrent Protection

For protection against load faults, the TPSM41625 is protected from overcurrent conditions by cycle-by-cycle current limiting. In an extended overcurrent condition, the device enters hiccup mode to reduce power dissipation. In hiccup mode, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced, which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

### 7.3.17 Output Overvoltage and Undervoltage Protection

The device includes both output overvoltage protection and output undervoltage protection capability. The devices compare the RS+ pin voltage to internal selectable pre-set voltages. If the RS+ voltage with respect to RS- voltage rises above the output overvoltage protection threshold, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. Then, the device enters continuous restart hiccup.

If the RS+ pin voltage falls below the undervoltage protection level, after soft start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, then enters hiccup time-out delay prior to restart.

### 7.3.18 Overtemperature Protection

An internal temperature sensor protects the device from thermal runaway. The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 135°C typically.

## 7.4 Device Functional Modes

### 7.4.1 Active Mode

The TPSM41625 is in active mode when VIN is above the UVLO threshold and the EN pin voltage is above the EN high threshold. The EN pin has an internal current source to enable the output when the EN pin is left floating. If the EN pin is pulled low the device is put into a low quiescent current state.

### 7.4.2 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM41625. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode, the device is put into a low quiescent current state. The TPSM41625 also employs undervoltage lockout protection. If $V_{IN}$ is below the UVLO level, the output of the regulator turns off.

# 8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPSM41625 is a synchronous step-down DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 25 A. The following design procedure can be used to select components for the TPSM41625. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com/webench for more details.

## 8.2 Typical Application

The TPSM41625 requires only a few external components to convert from a wide input voltage supply range to a wide range of output voltages. Figure 8-1 shows a typical TPSM41625 schematic with only the minimum required components.
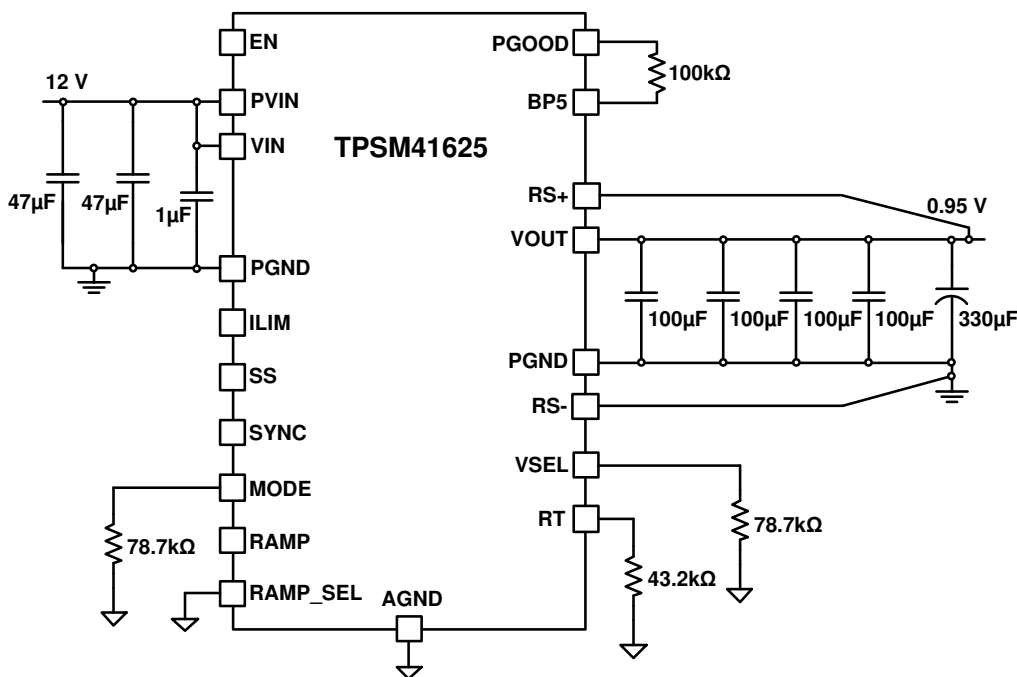


**Figure 8-1. TPSM41625 Typical Application**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1. Follow the design procedures in *Section 8.2.2*.

**Table 8-1. Design Example Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage $V_{IN}$ | 12 V typical |
| Output voltage $V_{OUT}$ | 0.95 V |
| Output current rating | 25 A |
| Key care-abouts | Small solution size |

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### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM41625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM41625 is externally adjustable by first setting the reference voltage, $V_{REF}$, using the VSEL pin and then, if needed, setting the output voltage adjust resistor $R_{ADJ}$. For this application, $V_{REF}$ is the same as the output voltage, so $R_{ADJ}$ is not needed and RS+ should be connected to the output rail, near the load.

To set the output voltage to 0.95 V, select $V_{REF}$ of 0.95 V by connecting a 78.7-kΩ resistor between VSEL pin and AGND and connect RS+ pin to the output voltage rail. VSEL resistor values for setting VREF can be found in Table 7-1.

#### 8.2.2.3 Setting the Switching Frequency

To set the switching frequency of the TPSM41625, a resistor ($R_{RT}$) between the RT pin and AGND is required. Select the value of $R_{RT}$ from Table 7-4. Before selecting the switching frequency, reference Table 7-3 for the allowable switching frequency range, required output capacitance, and RAMP setting for the desired output voltage.

For this application, after referencing Table 7-3, 500 kHz was selected and a 43.2-kΩ RT resistor is required for a 12-V input according to Table 7-4.

#### 8.2.2.4 RAMP Setting

The value of the RAMP resistor, $R_{RAMP}$, must be selected based on the switching frequency and output capacitance of the application, as shown in Table 7-3. For this application, the required $R_{RAMP}$ is 78.7 kΩ. There is a 78.7-kΩ resistor internal to the device connected between RAMP and RAMP_SEL. To select the internal 78.7-kΩ resistor, leave the RAMP pin open and connect RAMP_SEL to AGND.

#### 8.2.2.5 Input Capacitors

The TPSM41625 requires a minimum of 88 µF of ceramic input capacitance. Applications with load transient requirements can benefit from adding addition bulk input capacitance.

For this design, two 47-µF ceramic capacitors rated for 25 V are used for the input decoupling capacitors.

Additionally, a 1-µF bypass capacitor is required on the VIN pin, close to the device pins.

#### 8.2.2.6 Output Capacitors

The minimum required output capacitance for a 12-V input and 0.95-V output at 500 kHz switching frequency is 294 µF of ceramic capacitance, as well as an additional 430 µF of either ceramic or low-ESR polymer, as shown in Table 7-3.

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For this design, four 100-µF ceramic capacitors plus a 330-µF polymer capacitor where used to meet the requirements.
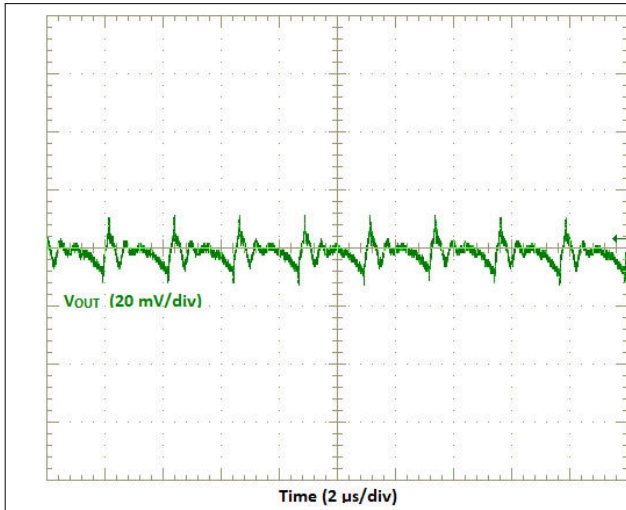
### 8.2.3 Application Waveforms



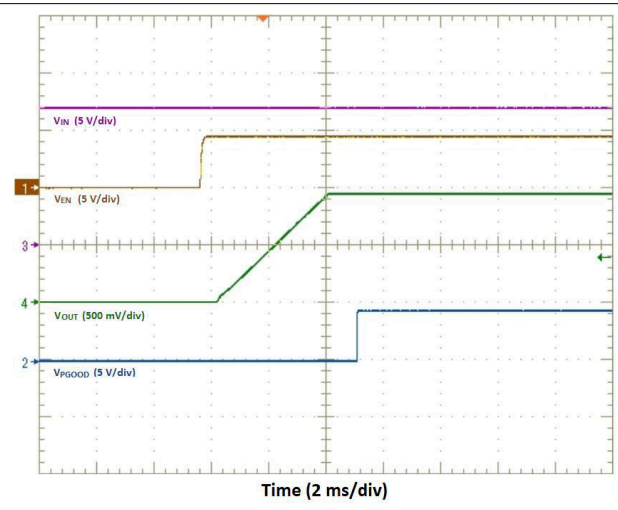**Figure 8-2. Output Ripple Waveform**



**Figure 8-3. Start-Up Waveforms**

## 9 Power Supply Recommendations

The TPSM41625 is designed to operate from an input voltage supply range between 4 V and 16 V. The input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM41625 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the TPSM41625 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. Typically, a 47-µF or 100-µF electrolytic capacitor will suffice.

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## 10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

### 10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 10-1 through Figure 10-4 shows a typical PCB layout. Some considerations for an optimized layout are:
- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place $R_{VSEL}$, $R_{ADJ}$, $R_{RT}$, $R_{MODE}$, and $C_{SS}$ as close as possible to their respective pins.
- Use multiple vias to connect the power planes (PVIN, VOUT, and PGND) to internal layers.
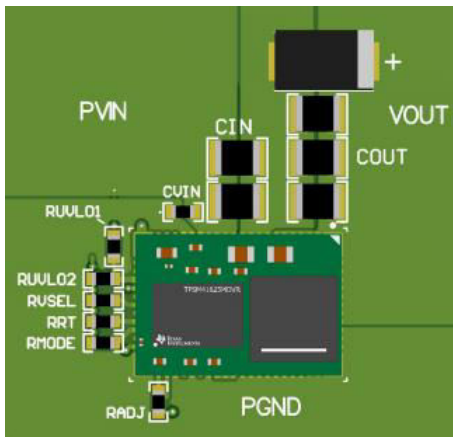
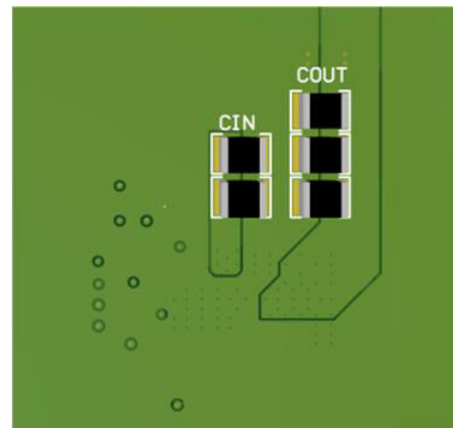### 10.2 Layout Examples



**Figure 10-1. Top-Layer Components (Top View)**
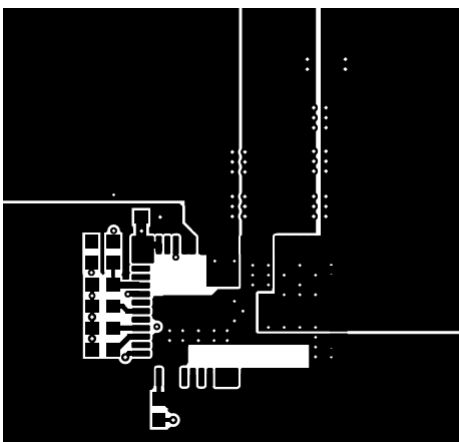


**Figure 10-2. Bottom-Layer Components (Top View)**
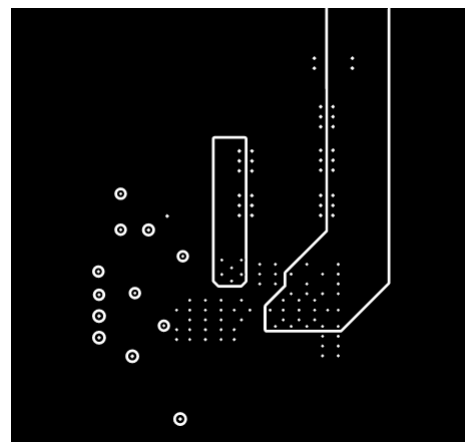


**Figure 10-3. Top-Layer Layout (Top View)**



**Figure 10-4. Bottom-Layer Layout (Top View)**

Product Folder Links: *TPSM41625*

## 10.3 Package Specifications

| TPSM41625 | | VALUE | UNIT |
|---|---|---|---|
| Weight | | 1.32 | grams |
| Flammability | Meets UL 94 V-O | | |
| MTBF Calculated Reliability | Per Bellcore TR-332, 50% stress, $T_A$ = 40°C, ground benign | | MHrs |

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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### 11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM41625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

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WEBENCH® are registered trademarks of Texas Instruments.
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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

**TI Glossary**          This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**ADVANCE INFORMATION**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTPSM41625MOVR | ACTIVE | QFM | MOS | 69 | 500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TPSM41625MOVR | PREVIEW | QFM | MOS | 69 | 500 | TBD | Call TI | Call TI | -40 to 125 | | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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