

# TPS7B63xx-Q1 300-mA 40-V High-Voltage, Ultralow-Quiescent-Current Watchdog LDO

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Maximum Output Current: 300 mA
- 4-V to 40-V Wide  $V_{IN}$  Input-Voltage Range With Up to 45-V Transients
- Fixed 3.3-V and 5-V Outputs
- Maximum Dropout Voltage: 400 mV at 300 mA
- Stable With Output Capacitor in Wide Range of Capacitance (4.7  $\mu$ F to 500  $\mu$ F) and ESR (0.001  $\Omega$  to 20  $\Omega$ )
- Low Quiescent Current ( $I_{(Q)}$ )
  - < 4  $\mu$ A When EN Is Low (Shutdown Mode)
  - 19  $\mu$ A Typical at Light Loads With  $\overline{WD\_EN}$  High (Watchdog Disabled)
- Configurable for Window Watchdog or Standard Watchdog
- Open-to-Closed Window Ratio Configurable as 1:1 or 8:1
- Fully Adjustable Watchdog Period (From 10 ms to 500 ms)
- 9% Accurate Watchdog Period
- Dedicated  $\overline{WD\_EN}$  Pin to Control Watchdog ON-OFF
- Fully Adjustable Power-Good Threshold and Power-Good Delay Period
- Low Input-Voltage Tracking to UVLO
- Integrated Fault Protection
  - Overload Current-Limit Protection
  - Thermal Shutdown
- 16-Pin HTSSOP Package

## 2 Applications

- Automotive MCU Power Supply
- Body Control Modules (BCM)
- Body Comfort Modules
- EV and HEV Battery Management Systems (BMS)
- Electronic Gear Shifter
- Transmission Control Unit (TCU)
- Electrical Power Steering (EPS)

## 3 Description

In automotive microcontroller or microprocessor power-supply applications, the watchdog is used to monitor the microcontroller working status to prevent software runaway. It is necessary for the watchdog to be independent of the microcontroller in a reliable system.

The TPS7B63xx-Q1 device is a family of 300-mA watchdog LDOs designed for an operating voltage up to 40 V, with typical quiescent current of only 19  $\mu$ A at light load. The devices integrate a programmable function for selecting a window watchdog or standard watchdog, with an external resistor to set the watchdog time within 9% accuracy.

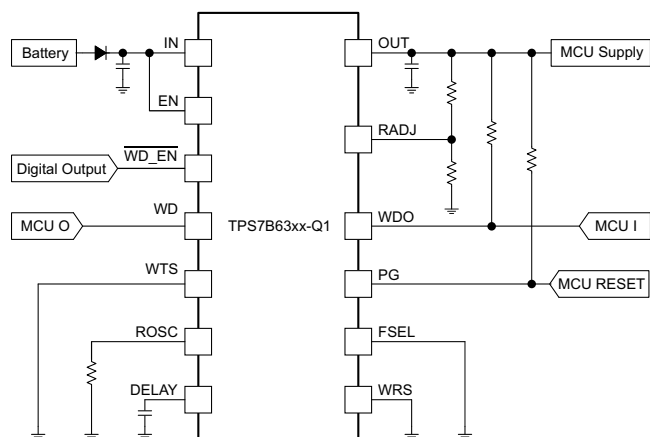
The PG pin on the TPS7B63xx-Q1 devices indicate when the output voltage is stable and in regulation. The power-good delay period and power-good threshold can be adjusted by selecting external components. The devices also feature integrated short-circuit and overcurrent protection. The combination of such features makes these devices particularly flexible and suitable to supply microcontroller in automotive applications.

### Device Information<sup>(1)</sup>

PART NUMBER	OUTPUT VOLTAGE	PACKAGE
TPS7B6333-Q1	Fixed 3.3 V	HTSSOP (16)
TPS7B6350-Q1	Fixed 5 V	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Schematic



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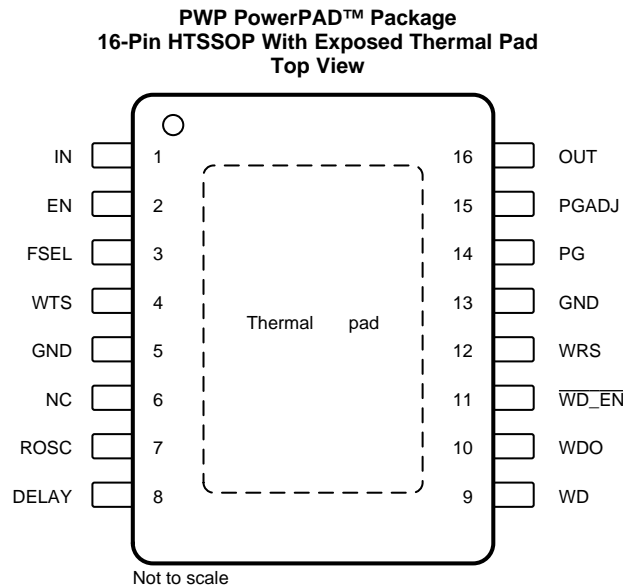
## 4 Revision History

### Changes from Original (February 2017) to Revision A

Page

• Changed <i>Typical Application Schematic</i> .....	<b>1</b>
• Changed <i>Dropout Voltage vs Output Current</i> graph .....	<b>8</b>
• Changed <i>Load Regulation</i> graph.....	<b>8</b>
• Changed <i>TPS7B63xx-Q1 Typical Application Schematic</i> .....	<b>20</b>

## 5 Pin Configuration and Functions



NC - No internal connection

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	8	O	Power-good delay-period adjustment pin. Connect this pin via a capacitor to ground to adjust the power-good delay time.
EN	2	I	Device enable pin. Pull this pin down to low-level voltage to disable the device. Pull this pin up to high-level voltage to enable the device.
FSEL	3	I	Internal oscillator-frequency selection pin. Pull this pin down to low-level voltage to select the high-frequency oscillator. Pull this pin up to high-level voltage to select the low-frequency oscillator.
GND	5, 13	—	Ground reference
IN	1	I	Device input power supply pin
NC	6	—	Not connected
OUT	16	O	Device 3.3-V or 5-V regulated output-voltage pin
PG	14	O	Power-good pin. Open-drain output pin. Pull this pin up to $V_{OUT}$ or to a reference through a resistor. When the output voltage is not ready, this pin is pulled down to ground.
PGADJ	15	O	Power-good threshold-adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to 91.6% of output voltage $V_{OUT}$ .
ROSC	7	O	Watchdog timer adjustment pin. Connect a resistor between the ROSC pin and the GND pin to set the duration of the watchdog monitor. Leaving this pin open or connecting this pin to ground results in the watchdog reporting a fault at the watchdog output (WDO).
WD	9	I	Watchdog service-signal input pin.
WDO	10	O	Watchdog status pin. Open-drain output pin. Pull this pin up to OUT or a reference voltage through a resistor. When watchdog fault occurs, this pin is pulled down to a low-level voltage.
$\overline{\text{WD\_EN}}$	11	I	Watchdog enable pin. Pull this pin down to a low level to enable the watchdog. Pull this pin up to a high level to disable the watchdog.
WRS	12	I	Window ratio-selection pin (only applicable for the window watchdog). Pull this pin down to a low level to set the open:closed window ratio to 1:1. Pull this pin up to high level to set the open:closed window ratio to 8:1.
WTS	4	O	Watchdog type-selection pin. To set the window watchdog, connect this pin to the GND pin. To set the standard watchdog, pull this pin high.
Thermal pad	—	—	Solder to board to improve the thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
Unregulated input	IN, EN	–0.3	45	V
Internal oscillator reference voltage	ROSC	–0.3	7	V
Power-good delay-timer output	DELAY	–0.3	7	V
Regulated output	OUT	–0.3	7	V
Power-good output voltage	PG	–0.3	7	V
Watchdog status output voltage	WDO	–0.3	7	V
Watchdog frequency selection, watchdog-type selection	FSEL, WTS	–0.3	45	V
Watchdog enable	$\overline{\text{WD\_EN}}$	–0.3	7	V
Watchdog service signal voltage	WD	–0.3	7	V
Window ratio selection	WRS	–0.3	7	V
Power-good threshold-adjustment voltage	PGADJ	–0.3	7	V
Operating junction temperature, $T_J$		–40	150	°C
Storage temperature, $T_{\text{stg}}$		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground.

## 6.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins (1, 14, 15, and 28)		±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input	IN	4	40	V
40-V pins	EN, FSEL, WTS	0	$V_{IN}$	V
Regulated output	OUT	0	5.5	V
Power good, watchdog status, reference oscillator	PG, WDO, ROSC	0	5.5	V
Low voltage pins	WD, $\overline{WD\_EN}$ , PGADJ, DELAY, WRS	0	5.5	V
Output current		0	300	mA
Ambient temperature, $T_A$		-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7B63xx-Q1	UNIT
		PWP (HTSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 6.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$ ,  $C_{OUT} \geq 4.7\ \mu\text{F}$ ,  $1\ \text{m}\Omega < \text{ESR} < 20\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE AND CURRENT (IN)</b>						
$V_{IN}$	Input voltage		4		40	V
$I_{(SLEEP)}$	Input sleep current	EN = OFF			4	$\mu\text{A}$
$I_{(Q)}$	Input quiescent current	$V_{IN} = 5.6\text{ V to }40\text{ V}$ for fixed 5-V $V_{OUT}$ ; $V_{IN} = 4\text{ V to }40\text{ V}$ for fixed 3.3-V $V_{OUT}$ ; EN = ON; watchdog disabled; $I_{OUT} < 1\ \text{mA}$ ; $T_J < 80^\circ\text{C}$		19	29.6	$\mu\text{A}$
		$V_{IN} = 5.6\text{ V to }40\text{ V}$ for fixed 5-V $V_{OUT}$ ; $V_{IN} = 4\text{ V to }40\text{ V}$ for fixed 3.3-V $V_{OUT}$ ; EN = ON; watchdog enabled; $I_{OUT} < 1\ \text{mA}$		28	42	
		$V_{IN} = 5.6\text{ V to }40\text{ V}$ for fixed 5-V $V_{OUT}$ ; $V_{IN} = 4\text{ V to }40\text{ V}$ for fixed 3.3-V $V_{OUT}$ ; EN = ON; watchdog enabled; $I_{OUT} < 100\ \text{mA}$		78	98	
$V_{(UVLO)}$	Undervoltage lockout, falling	Ramp $V_{IN}$ down until output is turned off			2.6	V
$V_{(UVLO\_HYST)}$	UVLO hysteresis			0.5		V
<b>ENABLE INPUT, WATCHDOG TYPE SELECTION AND FSEL (EN, WTS, AND FSEL)</b>						
$V_{IL}$	Low-level input voltage				0.7	V
$V_{IH}$	High-level input voltage		2			V
$V_{hys}$	Hysteresis			150		mV
<b>WATCHDOG ENABLE (<math>\overline{\text{WD\_EN}}</math> PIN)</b>						
$V_{IL}$	Low-level input threshold voltage for watchdog enable pin	Watchdog enabled			0.7	V
$V_{IH}$	High-level input threshold voltage for watchdog enable pin	Watchdog disabled	2			V
$I_{\text{WD\_EN}}$	Pulldown current for watchdog enable pin	$V_{\text{WD\_EN}} = 5\ \text{V}$			3	$\mu\text{A}$
<b>REGULATED OUTPUT (OUT)</b>						
$V_{OUT}$	Regulated output	$V_{IN} = 5.6\text{ V to }40\text{ V}$ for fixed 5-V $V_{OUT}$ ; $V_{IN} = 4\text{ V to }40\text{ V}$ for fixed 3.3-V $V_{OUT}$ ; $I_{OUT} = 0\text{ to }300\ \text{mA}$	-2%		2%	
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation	$V_{IN} = 5.6\text{ V to }40\text{ V}$			10	mV
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$I_{OUT} = 1\ \text{mA to }300\ \text{mA}$			20	mV
$V_{(dropout)}$	Dropout voltage ( $V_{IN} - V_{OUT}$ )	$I_{OUT} = 300\ \text{mA}^{(1)}$		300	400	mV
		$I_{OUT} = 200\ \text{mA}^{(1)}$		170	260	
$I_{OUT}$	Output current	$V_{OUT}$ in regulation	0		300	mA
$I_{(LIM)}$	Output current limit	$V_{OUT}$ shorted to ground, $V_{IN} = 5.6\text{ V to }40\text{ V}$	301	680	1000	mA
PSRR	Power supply ripple rejection <sup>(2)</sup>	$I_{OUT} = 100\ \text{mA}$ ; $C_{OUT} = 10\ \mu\text{F}$ ; frequency (f) = 100 Hz		60		dB
		$I_{OUT} = 100\ \text{mA}$ ; $C_{OUT} = 10\ \mu\text{F}$ ; frequency (f) = 100 kHz		40		
<b>POWER GOOD (PG, PGADJ)</b>						
$V_{OL(PG)}$	PG output, low voltage	$I_{OL} = 5\ \text{mA}$ , PG pulled low			0.4	V
$I_{(kg)(PG)}$	PG pin leakage current	PG pulled to $V_{OUT}$ through a 10-k $\Omega$ resistor			1	$\mu\text{A}$
$V_{(PG\_TH)}$	Default power-good threshold	$V_{OUT}$ powered above the internally set tolerance, PGADJ pin shorted to ground	89.6	91.6	93.6	% of $V_{OUT}$
$V_{(PG\_HYST)}$	Power-good hysteresis	$V_{OUT}$ falling below the internally set tolerance hysteresis		2		% of $V_{OUT}$

(1) This test is done with  $V_{OUT}$  in regulation, measuring the  $V_{IN} - V_{OUT}$  when  $V_{OUT}$  drops by 100 mV from the rated output voltage at the specified load.

(2) Design Information – Not tested, determined by characterization.

## Electrical Characteristics (continued)

 $V_{IN} = 14\text{ V}$ ,  $C_{OUT} \geq 4.7\ \mu\text{F}$ ,  $1\ \text{m}\Omega < \text{ESR} < 20\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>PGADJ</b>							
$V_{(\text{PGADJ\_TH})}$	Switching voltage for the power-good adjust pin	$V_{OUT}$ is falling		1.067	1.1	1.133	V
<b>POWER-GOOD DELAY</b>							
$I_{(\text{DLY\_CHG})}$	DELAY capacitor charging current			3	5	10	$\mu\text{A}$
$V_{(\text{DLY\_TH})}$	DELAY pin threshold to release PG high	Voltage at DELAY pin is ramped up		0.95	1	1.05	V
$I_{(\text{DLY\_DIS})}$	DELAY capacitor discharging current	$V_{\text{DELAY}} = 1\ \text{V}$		0.5			mA
<b>CURRENT VOLTAGE REFERENCE (ROSC)</b>							
$V_{\text{ROSC}}$	Voltage reference			0.95	1	1.05	V
<b>WATCHDOG (WD, WDO, WRS)</b>							
$V_{\text{IL}}$	Low-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins				30	% of $V_{OUT}$
$V_{\text{IH}}$	High-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins		70			% of $V_{OUT}$
$V_{(\text{HYST})}$	Hysteresis				10		% of $V_{OUT}$
$I_{\text{WD}}$	Pulldown current for the WD pin	$V_{\text{WDO}} = 5\ \text{V}$			2	4	$\mu\text{A}$
$V_{\text{OL}}$	Low-level watchdog output	$I_{\text{WDO}} = 5\ \text{mA}$				0.4	V
$I_{\text{Ikg}}$	WDO pin leakage current	WDO pin pulled to $V_{OUT}$ through 10-k $\Omega$ resistor				1	$\mu\text{A}$
<b>OPERATING TEMPERATURE RANGE</b>							
$T_J$	Junction temperature			-40		150	$^\circ\text{C}$
$T_{(\text{SD})}$	Junction shutdown temperature				175		$^\circ\text{C}$
$T_{(\text{HYST})}$	Hysteresis of thermal shutdown				25		$^\circ\text{C}$

## 6.6 Switching Characteristics

 $V_I = 14\ \text{V}$ ,  $C_O \geq 4.7\ \mu\text{F}$ ,  $1\ \text{m}\Omega < \text{ESR} < 20\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>POWER-GOOD DELAY (DELAY)</b>							
$t_{(\text{DEGLITCH})}$	Power-good deglitch time	100	180	250	$\mu\text{s}$		
$t_{(\text{DLY\_FIX})}$	Fixed power-good delay	No capacitor connect at DELAY pin		100	248	550	$\mu\text{s}$
$t_{(\text{DLY})}$	Power-on-reset delay	Delay capacitor value: $C_{(\text{DELAY})} = 100\ \text{nF}$			20		ms
<b>WATCHDOG (WD, WDO, WRS)</b>							
$t_{(\text{WD})}$	Watchdog window duration	$R_{(\text{ROSC})} = 20\ \text{k}\Omega \pm 1\%$ , FSEL = LOW		9	10	11	ms
		$R_{(\text{ROSC})} = 20\ \text{k}\Omega \pm 1\%$ , FSEL = HIGH		45	50	55	
$t_{(\text{WD\_TOL})}$	Tolerance of watchdog window duration using external resistor	Excludes tolerance of $R_{(\text{ROSC})} = 20\ \text{k}\Omega$ to 100 k $\Omega$		-10%		10%	
$t_{\text{p}(\text{WD})}$	Watchdog service-signal duration			100			$\mu\text{s}$
$t_{(\text{WD\_HOLD})}$	Watchdog output resetting time (percentage of settled watchdog window duration)				20		% of $t_{(\text{WD})}$
$t_{(\text{WD\_RESET})}$	Watchdog output resetting time	$R_{(\text{ROSC})} = 20\ \text{k}\Omega \pm 1\%$ , FSEL = LOW		1.8	2	2.2	ms
		$R_{(\text{ROSC})} = 20\ \text{k}\Omega \pm 1\%$ , FSEL = HIGH		9	10	11	

### 6.7 Typical Characteristics

$V_{IN} = 14\text{ V}$ ,  $V_{EN} \geq 2\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

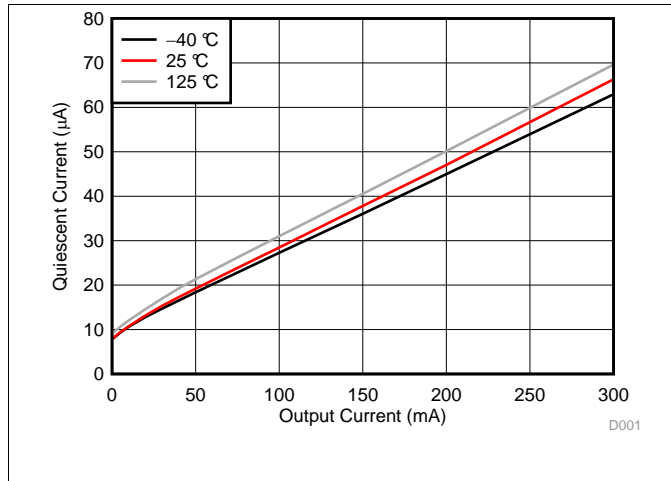


Figure 1. Quiescent Current vs Output Current

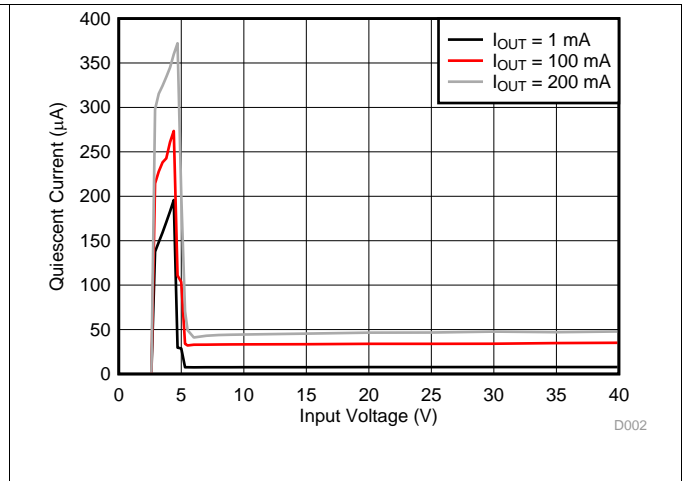


Figure 2. Quiescent Current vs Input Voltage

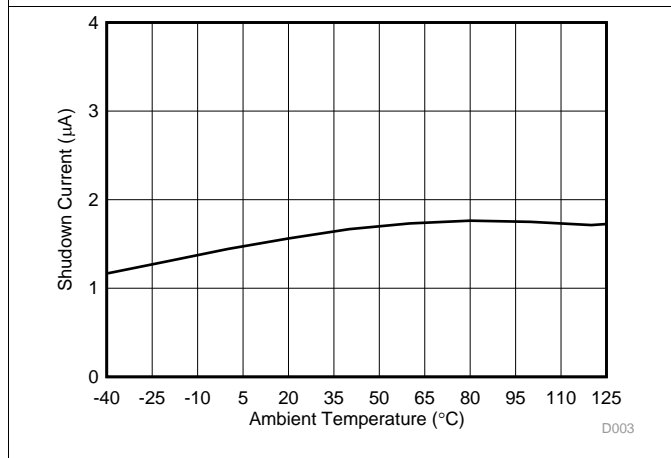


Figure 3. Shutdown Current vs Ambient Temperature

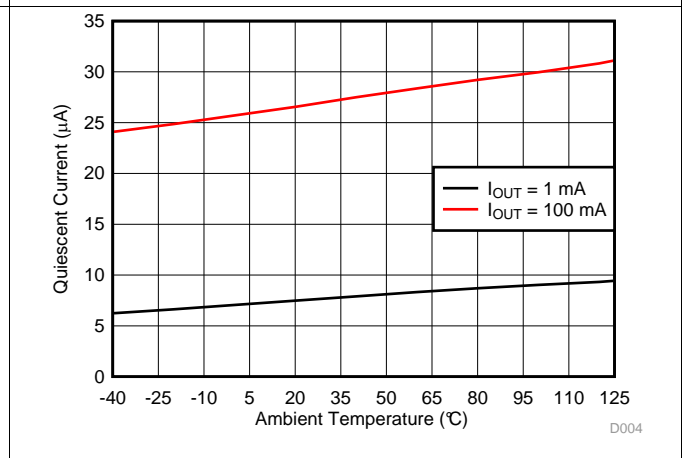


Figure 4. Quiescent Current vs Ambient Temperature

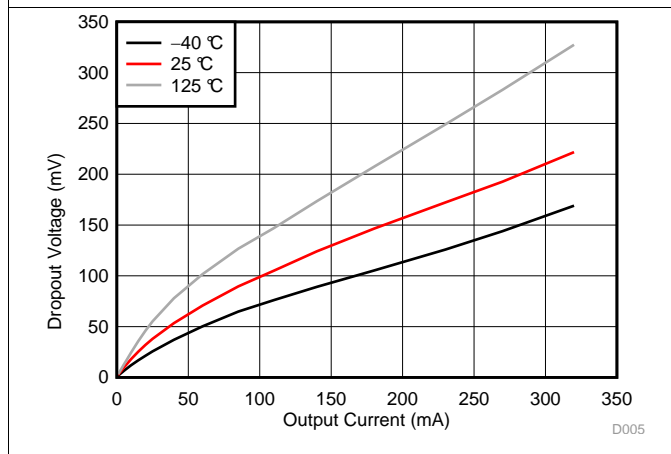


Figure 5. Dropout Voltage vs Output Current

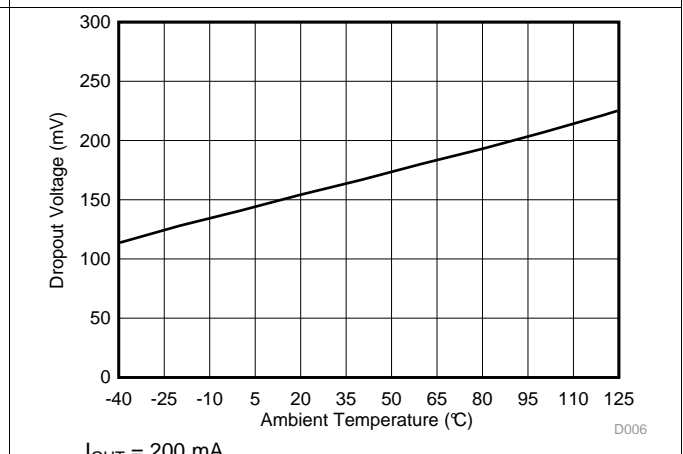


Figure 6. Dropout Voltage vs Ambient Temperature



Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$ ,  $V_{EN} \geq 2\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

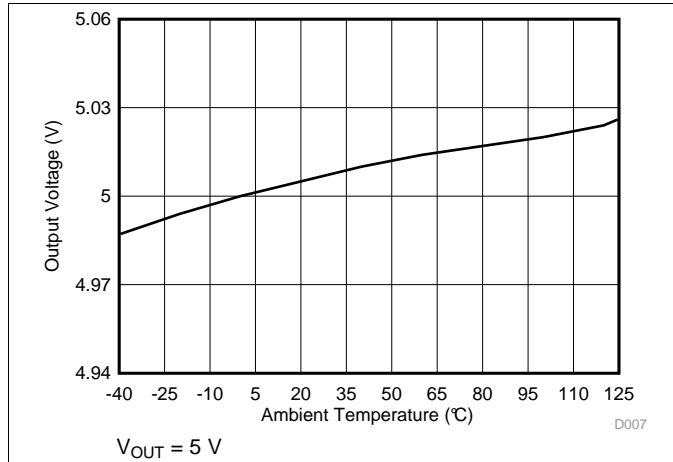


Figure 7. Output Voltage vs Ambient Temperature

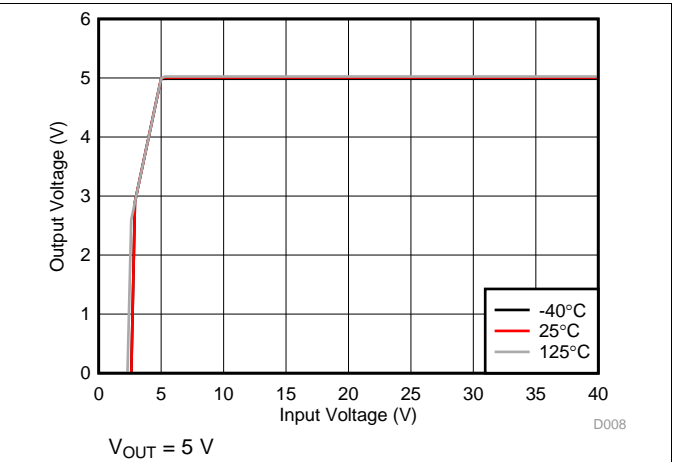


Figure 8. Output Voltage vs Input Voltage

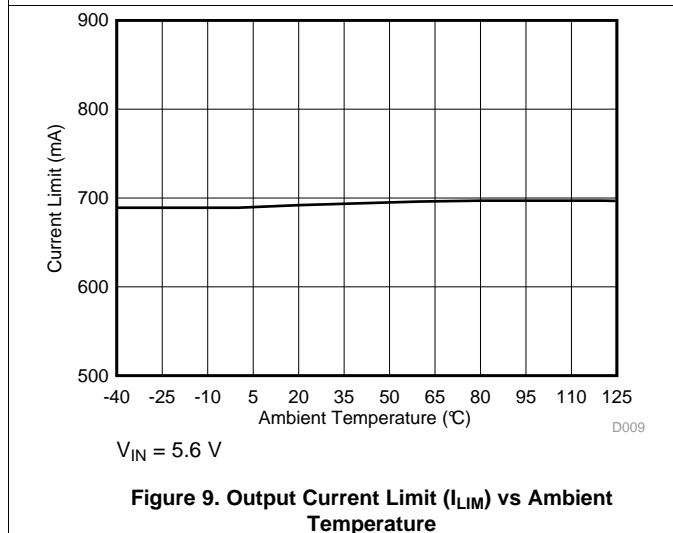


Figure 9. Output Current Limit ( $I_{LIM}$ ) vs Ambient Temperature

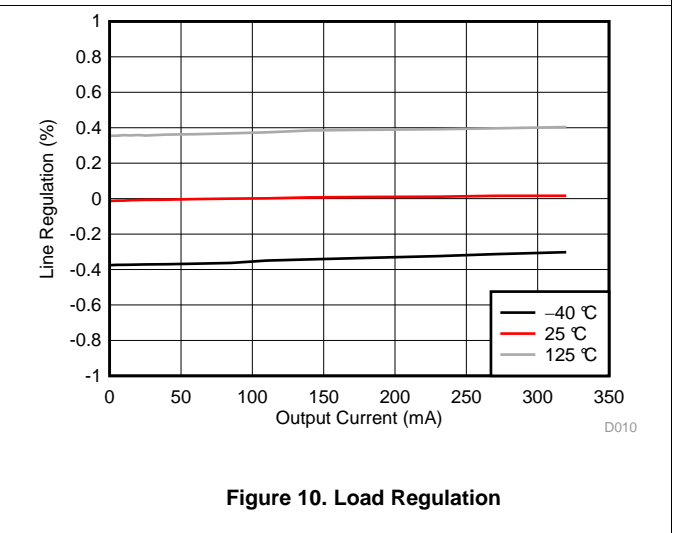


Figure 10. Load Regulation

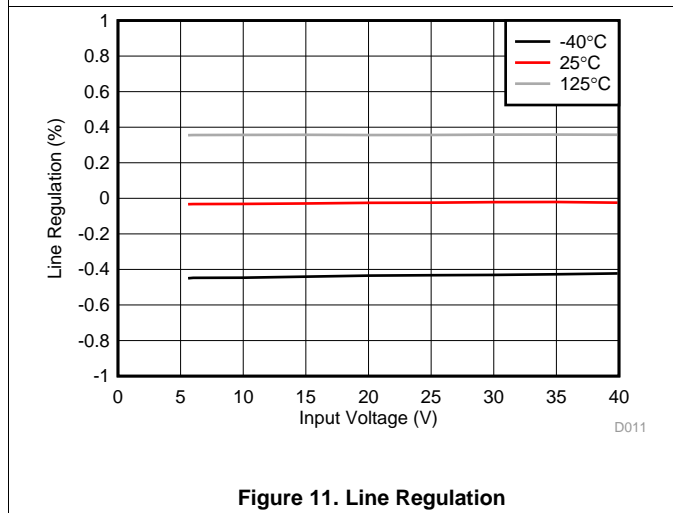


Figure 11. Line Regulation

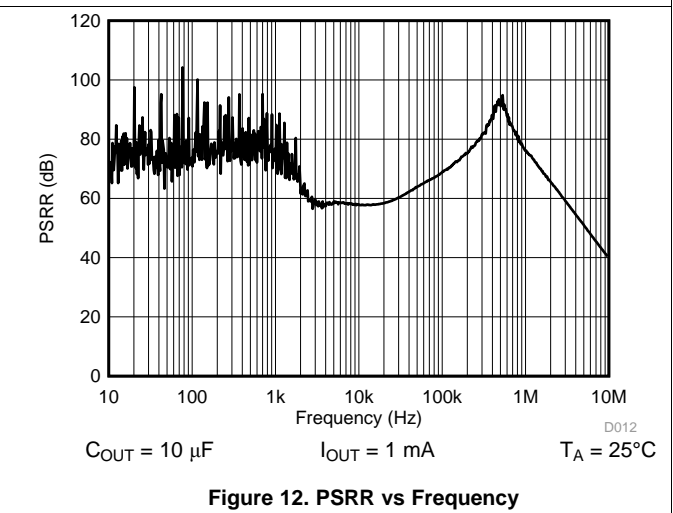


Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$ ,  $V_{EN} \geq 2\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

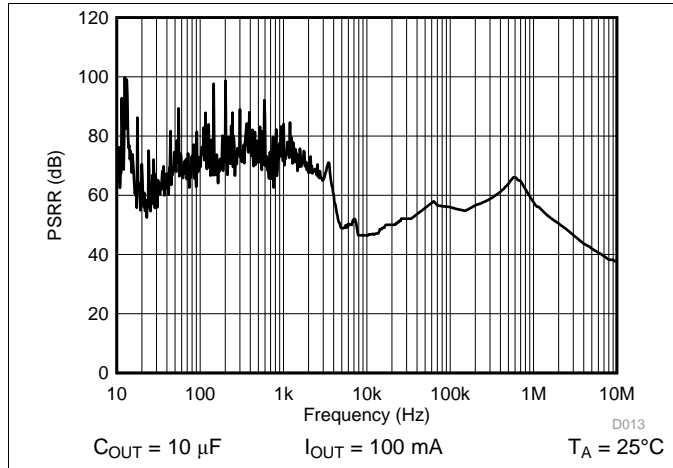


Figure 13. PSRR vs Frequency

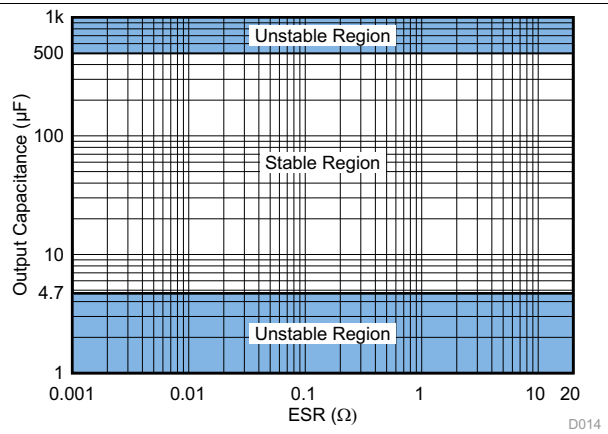


Figure 14. ESR Stability vs Output Capacitance

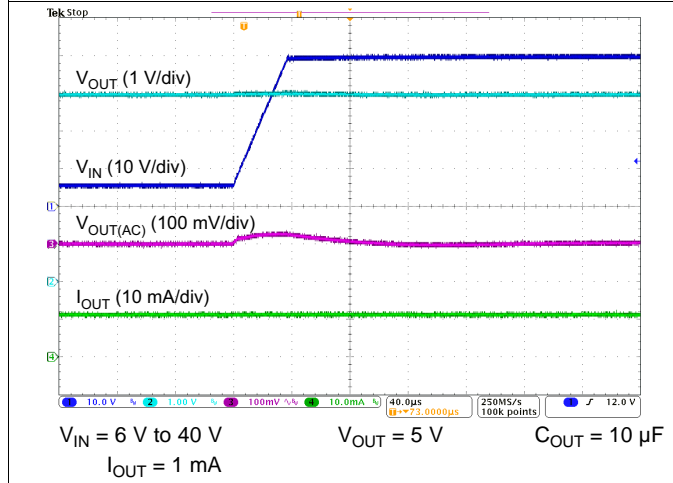


Figure 15. Line Transient

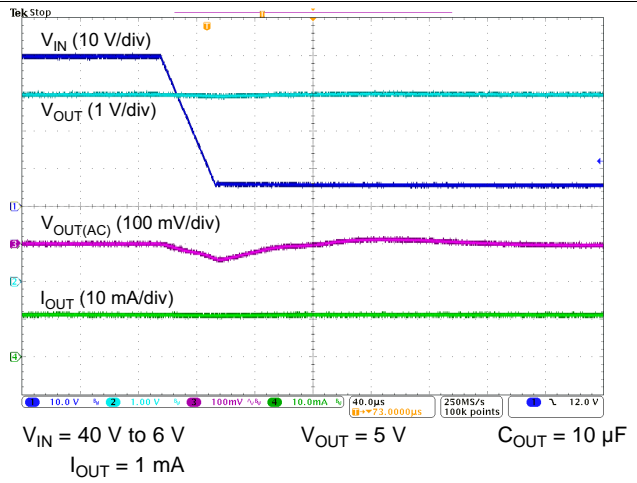


Figure 16. Line Transient

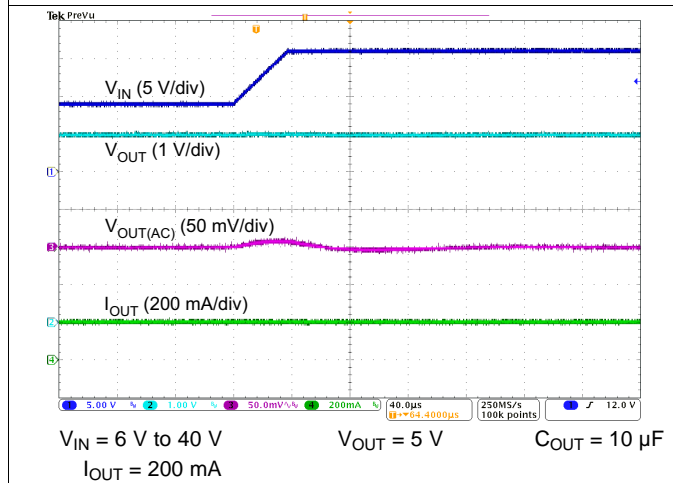


Figure 17. Line Transient

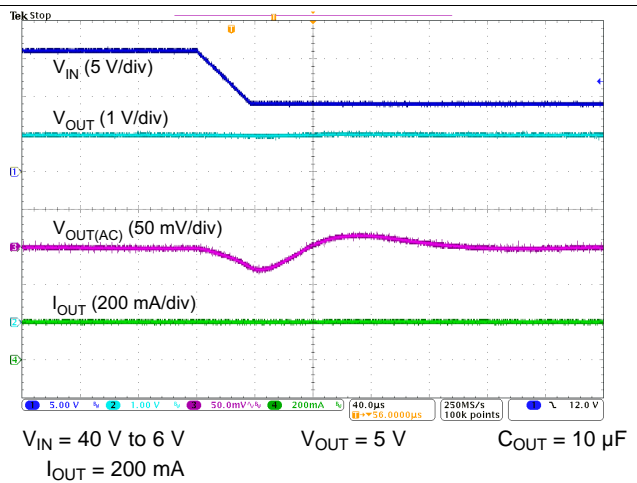
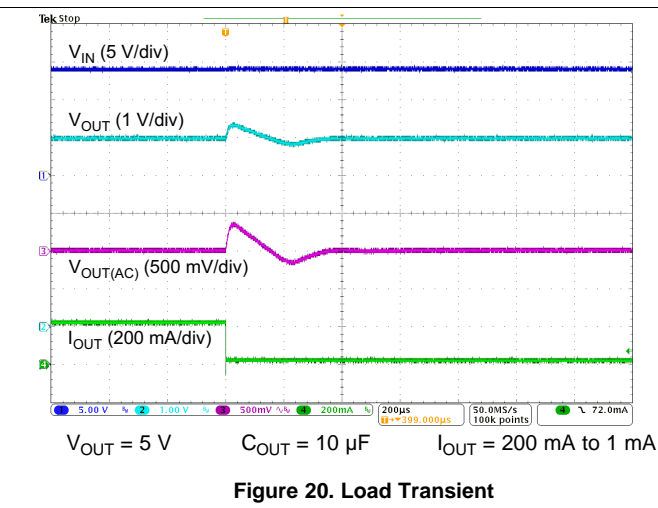
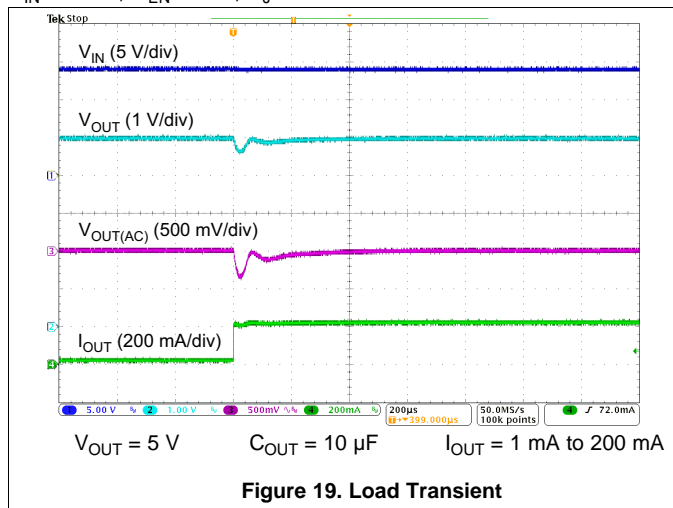


Figure 18. Line Transient

### Typical Characteristics (continued)

$V_{IN} = 14\text{ V}$ ,  $V_{EN} \geq 2\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise noted

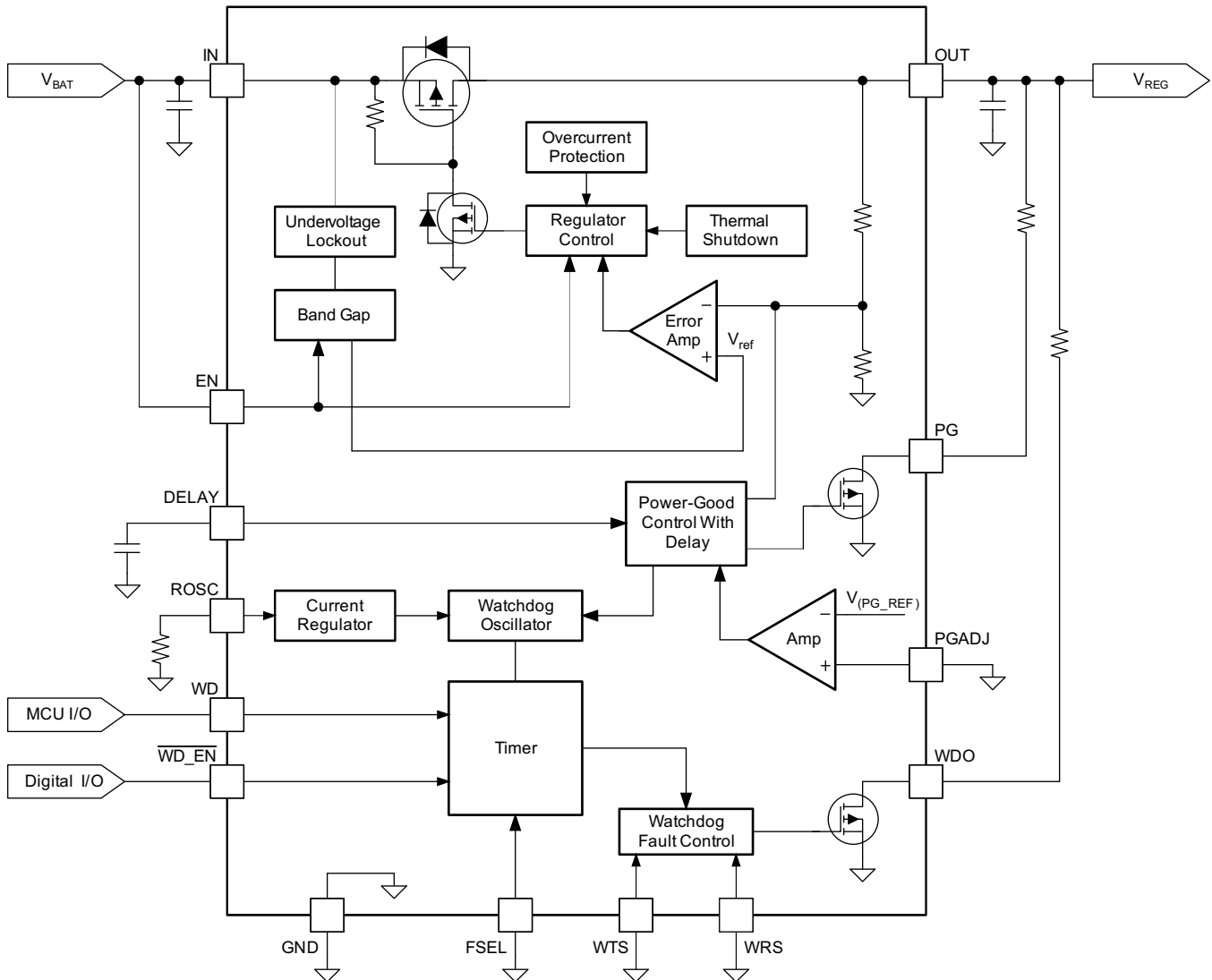


## 7 Detailed Description

### 7.1 Overview

The TPS7B63xx-Q1 device is a family of 300-mA, 40-V monolithic low-dropout linear voltage regulators with integrated watchdog and adjustable power-good threshold functionality. These voltage regulators consume only 19- $\mu$ A quiescent current in light-load applications. Because of the adjustable power-good delay (also called power-on-reset delay) and the adjustable power-good threshold, these devices are well-suited as power supplies for microprocessors and microcontrollers in automotive applications.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulator ON. Connect this input pin to an external microcontroller or a digital control circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

## Feature Description (continued)

### 7.3.2 Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pullup resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin. Connecting the PGADJ pin to GND sets the power-good threshold value to the default,  $V_{(PG\_TH)}$ . When  $V_{OUT}$  exceeds the default power-good threshold, the PG output turns high after the power-good delay period has expired. When  $V_{OUT}$  falls below  $V_{(PG\_TH)} - V_{(PG\_HYST)}$ , the PG output turns low after a short deglitch time.

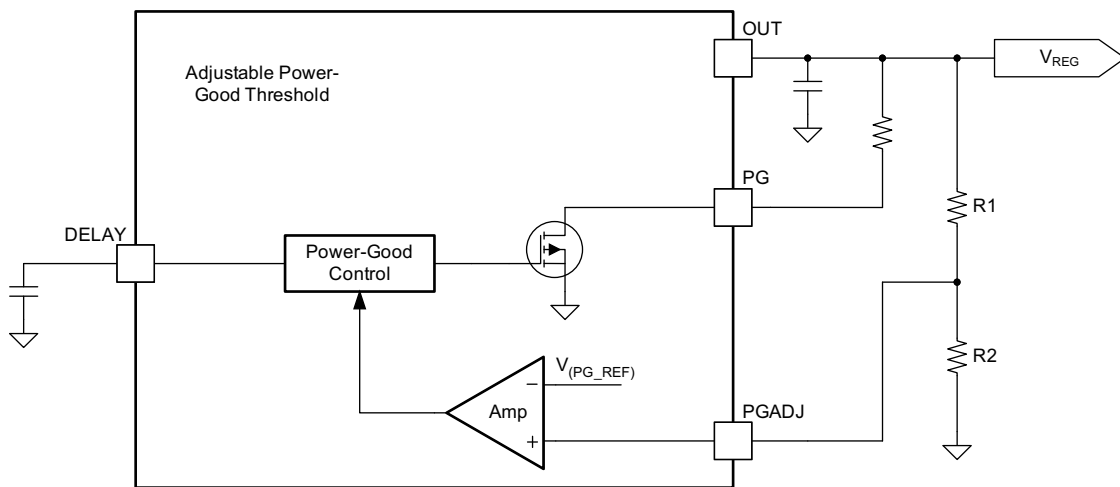
The power-good threshold is also adjustable from 1.1 V to 5 V by using an external resistor divider between PGADJ and OUT. The threshold can be calculated using Equation 1:

$$V_{(PG\_ADJ)} = V_{(PG\_REF)} \times \frac{R_1 + R_2}{R_2}$$

where

- $V_{(PG\_ADJ)}$  is the adjustable power-good threshold
- $V_{(PG\_REF)}$  is the internal comparator reference voltage of the PGADJ pin, 1.1 V typical, 2% accuracy specified under all conditions (1)

By setting the power-good threshold  $V_{(PG\_ADJ)}$ , when  $V_{OUT}$  exceeds this threshold, the PG output turns high after the power-good delay period has expired. When  $V_{OUT}$  falls below  $V_{(PG\_ADJ)} - V_{(PG\_HYST)}$ , the PG output turns low after a short deglitch time.



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Figure 21. Adjustable Power-Good Threshold

### 7.3.3 Adjustable Power-Good Delay Timer (DELAY)

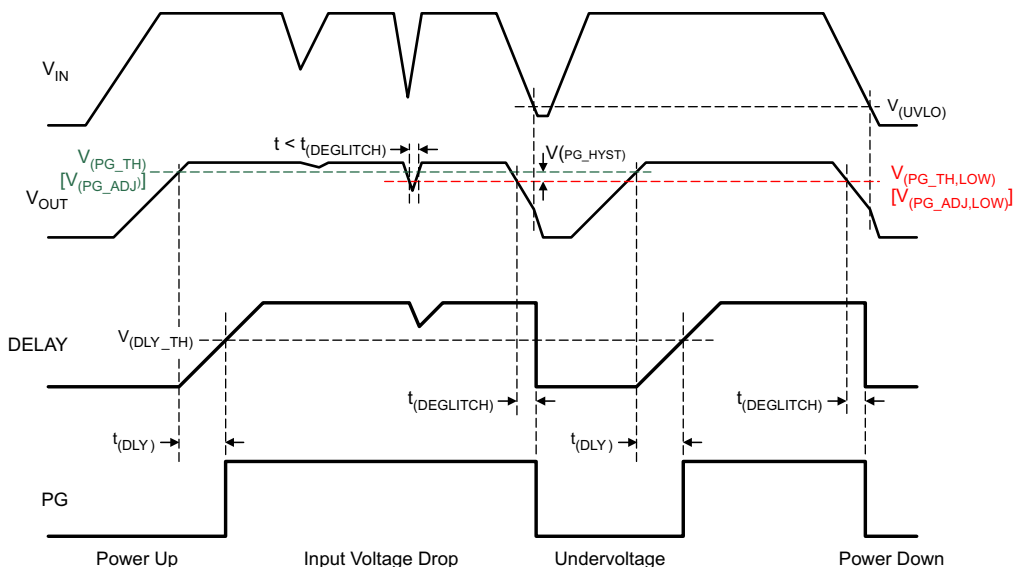
The power-good delay period is a function of the value set by an external capacitor on the DELAY pin before turning the PG pin high. Connecting an external capacitor from this pin to GND sets the power-good delay period. The constant current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator, and Equation 2 determines the power-good delay period:

$$t_{(DLY)} = \frac{C_{DELAY} \times 1V}{5 \mu A}$$

where

- $t_{(DLY)}$  is the adjustable power-good delay period
- $C_{DELAY}$  is the value of the power-good delay capacitor (2)

## Feature Description (continued)



**Figure 22. Power Up and Conditions for Activation of Power Good**

If the DELAY pin is open, the default delay time is  $t_{(DLY\_FIX)}$ .

### 7.3.4 Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage falls below an internal UVLO threshold,  $V_{(UVLO)}$ . This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required level.

### 7.3.5 Current Limit

These devices feature current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This protects devices from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to  $I_{(LIM)}$  to protect the device from excessive power dissipation.

### 7.3.6 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the  $T_{(SD)} - T_{(HYST)}$ , the output turns on again.

### 7.3.7 Integrated Watchdog

These devices have an integrated watchdog with fault (WDO) output option. Both window watchdog and standard watchdog are available in one device. The watchdog operation, service fault conditions, and differences between window watchdog and standard watchdog are described as follows.

## Feature Description (continued)

### 7.3.7.1 Window Watchdog (WTS, ROSC, FSEL and WRS)

These devices work in the window watchdog mode when the watchdog type selection (WTS) pin is connected to a low voltage level. The user can set the duration of the watchdog window by connecting an external resistor ( $R_{ROSC}$ ) to ground at the ROSC pin and setting the voltage level at the FSEL pin. The current through the  $R_{ROSC}$  resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

$$\text{FSEL low} \quad t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (3)$$

$$\text{FSEL high} \quad t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (4)$$

$$\text{Watchdog initialization} \quad t_{(WD\_INI)} = 8 \times t_{(WD)} \quad (5)$$

$$\text{Open and closed windows} \quad t_{(WD)} = t_{(OW)} + t_{(CW)} \quad (6)$$

$$\text{WRS low} \quad t_{(OW)} = t_{(CW)} = 50\% \times t_{(WD)} \quad (7)$$

$$\text{WRS high} \quad t_{(OW)} = 8 \times t_{(CW)} = (8 / 9) \times t_{(WD)} \quad (8)$$

where:

- $t_{(WD)}$  is the duration of the watchdog window
- $R_{ROSC}$  is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$  is the duration of the watchdog initialization
- $t_{(OW)}$  is the duration of the open watchdog window
- $t_{(CW)}$  is the duration of the closed watchdog window

For all the foregoing items, the unit of resistance is  $\Omega$  and the unit of time is s.

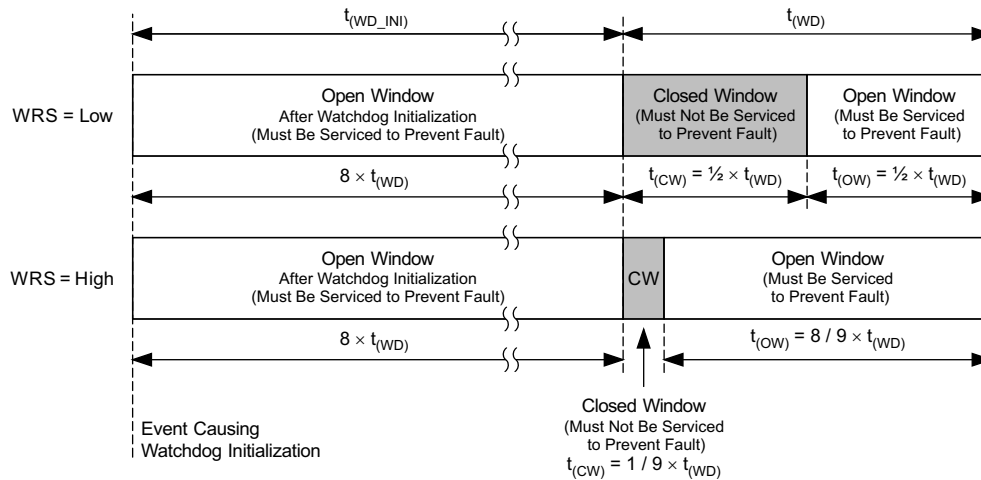
Table 1 illustrates several periods of watchdog window with typical conditions.

**Table 1. Several Typical Periods of Watchdog Window**

FSEL	$R_{(ROSC)}$ (k $\Omega$ )	$I_{(ROSC)}$ ( $\mu$ A)	$t_{(WD)}$ (ms)	WATCHDOG PERIOD TOLERANCE
High	200	5	500	15%
	100	10	250	
	50	20	125	10%
	40	25	100	
	25	40	62.5	
	20	50	50	
Low	100	10	50	10%
	50	20	25	
	40	25	20	
	25	40	12.5	
	20	50	10	

As shown in Figure 23, each watchdog window consists of an open window and a closed window. While the window ratio selection (WRS) pin is low, each open window ( $t_{(OW)}$ ) and closed window ( $t_{(CW)}$ ) has a width approximately 50% of the watchdog window ( $t_{(WD)}$ ). While the WRS pin is high, the ratio between open window and closed window is about 8:1. However, there is an exception to this; the first open window after watchdog initialization ( $t_{(WD\_INI)}$ ) is eight times the duration of the watchdog window. The watchdog must receive the service signal (by software, external microcontroller, and so forth) during this initialization open window.

A watchdog fault occurs when servicing the watchdog during a closed window, or not servicing during an open window.



**Figure 23. Watchdog Initialization, Open Window and Closed Window**

### 7.3.7.2 Standard Watchdog (WTS, ROSC and FSEL)

These devices work in the standard watchdog mode when the watchdog type selection (WTS) pin is connected to a high voltage level. The same as in window watchdog mode, the user can set the duration of the watchdog window by adjusting the external resistor ( $R_{ROSC}$ ) value at the ROSC pin and setting the voltage level at the FSEL pin. The current through the  $R_{ROSC}$  resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

$$\text{FSEL low} \quad t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (9)$$

$$\text{FSEL high} \quad t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (10)$$

$$\text{Watchdog initialization} \quad t_{(WD\_INI)} = 8 \times t_{(WD)} \quad (11)$$

where:

- $t_{(WD)}$  is the duration of the watchdog window
- $R_{ROSC}$  is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$  is the duration of the watchdog initialization

For all the foregoing items, the unit of resistance is  $\Omega$  and the unit of time is s

Compared with window watchdog, there is no closed window in standard watchdog mode. The standard watchdog receives a service signal at any time within the watchdog window. The watchdog fault occurs when not servicing watchdog during the watchdog window.

### 7.3.7.3 Watchdog Service Signal and Watchdog Fault Outputs (WD and WDO)

The watchdog service signal (WD) must stay high for at least 100  $\mu$ s. The WDO pin is the fault output terminal and is tied high through a pullup resistor to a regulated output supply. When a watchdog fault occurs, the devices momentarily pull WDO low for a duration of  $t_{(WD\_HOLD)}$ .

$$t_{(WD\_HOLD)} = 20\% \times t_{(WD)} \quad (12)$$



### 7.3.7.4 ROSC Status Detection (ROSC)

When a watchdog function is enabled, if the ROSC pin is shorted to GND or open, the watchdog output (WDO) pin remains low, indicating a fault status. If the watchdog function is disabled, ROSC pin status detection does not work.

### 7.3.7.5 Watchdog Enable (PG and $\overline{WD\_EN}$ )

When PG (power good) is high, an external microcontroller or a digital circuit can apply a high or low logic signal to the  $\overline{WD\_EN}$  pin to disable or enable the watchdog. A low input to this pin turns the watchdog on, and a high input turns the watchdog off. If PG is low, the watchdog is disabled and the watchdog-fault output (WDO) pin stays in the high-impedance state.

### 7.3.7.6 Watchdog Initialization

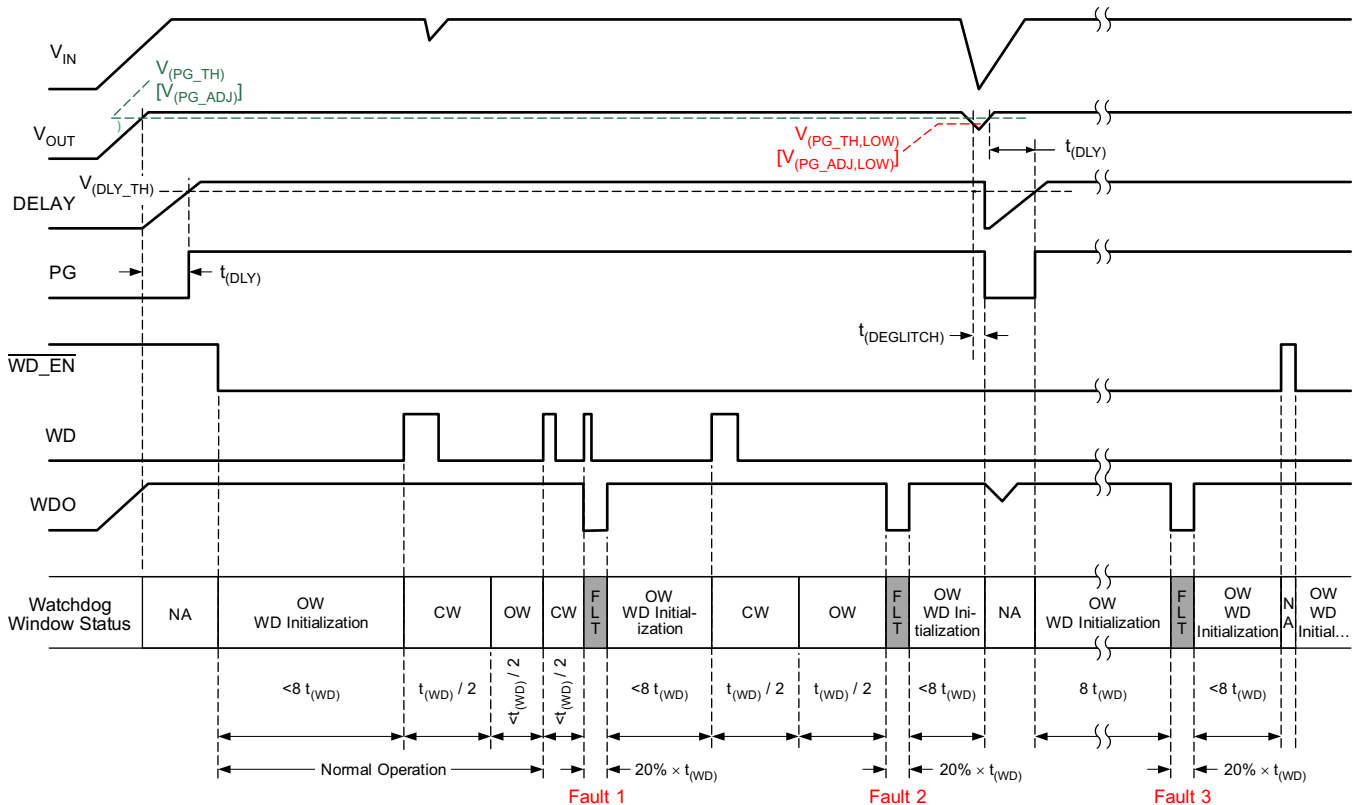
On power up and during normal operation, the watchdog initializes under the conditions shown in [Table 2](#).

**Table 2. Conditions for Watchdog Initialization**

EDGE	WHAT CAUSES THE WATCHDOG TO INITIALIZE
↑	Rising edge of PG (power good) while the watchdog is in the enabled state, for example, during soft power up
↓	Falling edge of $\overline{WD\_EN}$ while PG is already high, for example, when the microprocessor enables the watchdog after the device is powered up
↑	Rising edge of WDO while PG is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced

### 7.3.7.7 Window Watchdog Operation (WTS = Low)

The window watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is within certain ranges. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is out of the setting range. [Figure 24](#) shows the window watchdog initialization and operation for the TPS7B63xx-Q1 (WRS is low). After the output voltage is in regulation and PG is high, the window watchdog becomes enabled when an external signal pulls  $\overline{WD\_EN}$  (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of  $t_{(WD)}$ . A service signal applied to the WD pin during the initialization open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to  $V_{OUT}$  (typical), stays high as long as the watchdog receives a proper service signal and there is no other fault condition.


**Figure 24. Window Watchdog Operation**

Three different fault conditions occur in [Figure 24](#):

- Fault 1: The watchdog service signal is received during the closed window. The WDO is triggered once, receiving a WD rising edge during the closed window.
- Fault 2: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration  $t_{(WD)} / 2$ .
- Fault 3: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration  $8 \times t_{(WD)}$ .

### 7.3.7.8 Standard Watchdog Operation (WTS = High)

The standard watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is lower than a certain value. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is lower than the set value.

[Figure 25](#) shows the standard watchdog initialization and operation for the TPS7B63xx-Q1. Similar to the window watchdog, after output the voltage is in regulation and PG asserts high, the standard watchdog becomes enabled when an external signal pulls WD\_EN low. This causes the standard watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of  $t_{(WD)}$ . A service signal applied to the WD pin during the first open window resets the watchdog counter and another open window starts. To prevent a fault condition from occurring, watchdog service must occur during the every open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to  $V_{OUT}$  (typical), stays high as long as the watchdog receives proper service and there is not fault condition.

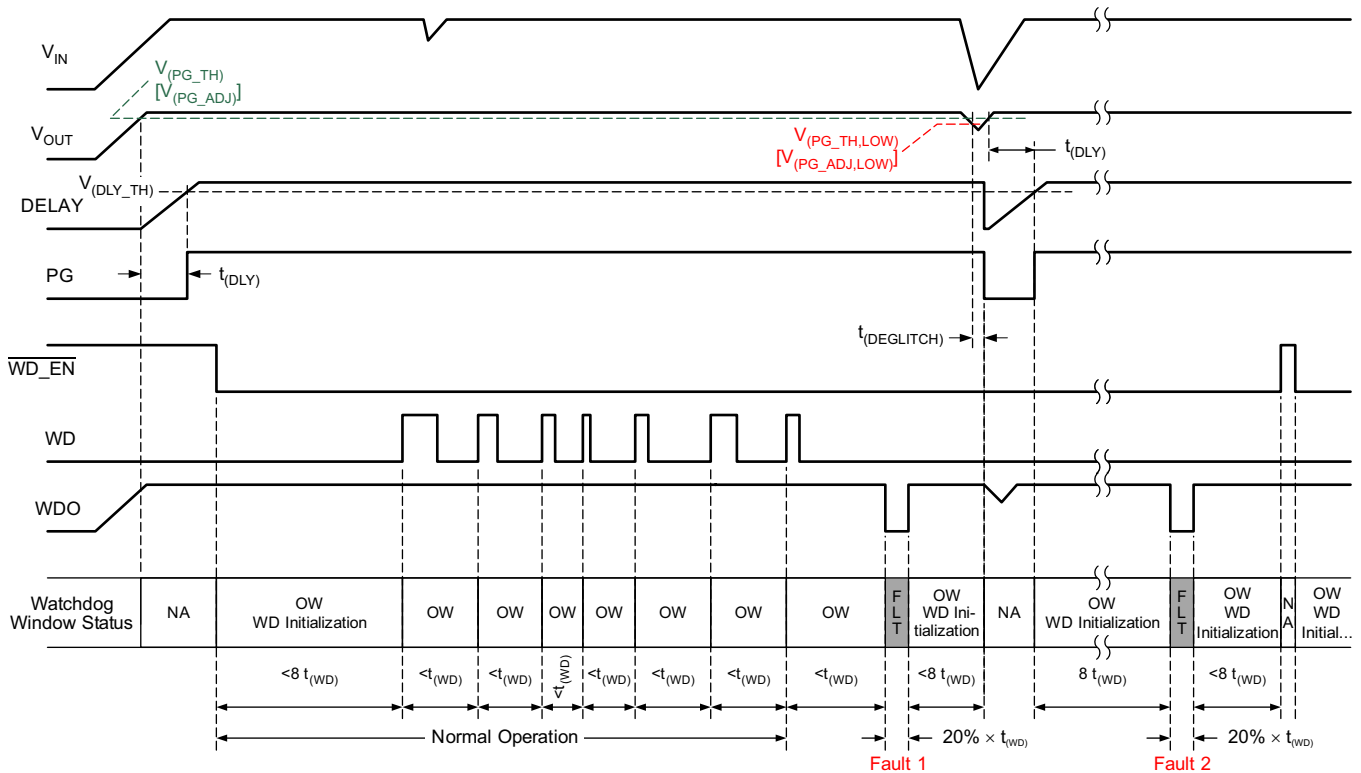


Figure 25. Standard Watchdog Operation

Two different fault conditions occur in Figure 25:

- Fault 1: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration  $t_{(WD)} / 2$ .
- Fault 2: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration  $8 \times t_{(WD)}$ .

## 7.4 Device Functional Modes

### 7.4.1 Operation With Input Voltage Lower Than 4 V

The devices normally operate with input voltages above 4 V. The devices can also operate at lower input voltages; the maximum UVLO voltage is 2.6 V. At input voltages below the actual UVLO voltage, the devices do not operate.

### 7.4.2 Operation With Input Voltage Higher Than 4 V

When the input voltage is greater than 4 V, if the input voltage is higher than the output set value plus the device dropout voltage, then the output voltage is equal to the set value. Otherwise, the output voltage is equal to the input voltage minus the dropout voltage.

## 8 Application and Implementation

### NOTE

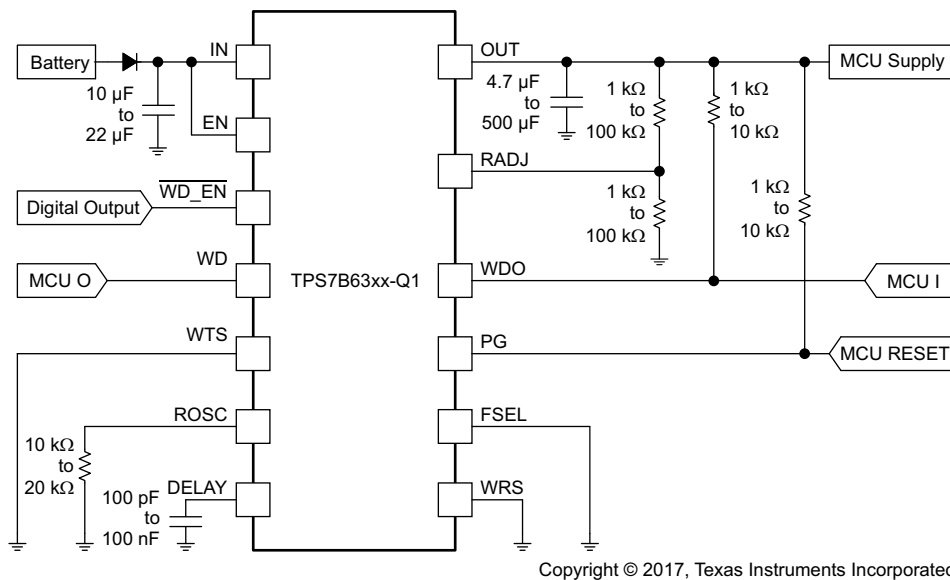
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7B63xx-Q1 device is a 300-mA low-dropout watchdog linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

### 8.2 Typical Application

Figure 26 shows a typical application circuit for the TPS7B63xx-Q1 device. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X7R.



**Figure 26. TPS7B63xx-Q1 Typical Application Schematic**

## Typical Application (continued)

### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#).

**Table 3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 V to 40 V for TPS7B6333-Q1 5.6 V to 40 V for TPS7B6350-Q1
Input capacitor range	10 $\mu$ F to 22 $\mu$ F
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	4.7 $\mu$ F to 500 $\mu$ F
Power-good threshold	Adjustable or fixed
Power-good delay capacitor	100 pF to 100 nF
Watchdog type	Standard watchdog or window watchdog
Watchdog window periods	10 ms to 500 ms

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current
- Power-good threshold
- Power-good delay capacitor
- Watchdog type
- Watchdog window period

#### 8.2.2.1 Input Capacitor

When using a TPS7B63xx-Q1 device, TI recommends adding a 10- $\mu$ F to 22- $\mu$ F capacitor with a 0.1  $\mu$ F ceramic bypass capacitor in parallel at the input to keep the input voltage stable. The voltage rating must be greater than the maximum input voltage.

#### 8.2.2.2 Output Capacitor

Ensuring the stability of the TPS7B63xx-Q1 device requires an output capacitor with a value in the range from 4.7  $\mu$ F to 500  $\mu$ F and with an ESR range from 0.001  $\Omega$  to 20  $\Omega$ . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

#### 8.2.2.3 Power-Good Threshold

The power-good threshold is set by connecting PGADJ to GND or to a resistor divider from OUT to GND. [Adjustable Power-Good Threshold \(PG, PGADJ\)](#) provides the method for setup of the power-good threshold.

#### 8.2.2.4 Power-Good Delay Period

The power-good delay period is set by an external capacitor ( $C_{\text{DELAY}}$ ) to ground, with a typical capacitor value from 100 pF to 100 nF. Calculate the correct capacitance for the application using [Equation 2](#).

#### 8.2.2.5 Watchdog Setup

The [Integrated Watchdog](#) section discusses the watchdog type selection and watchdog window-period setup method.

### 8.2.3 Application Curves

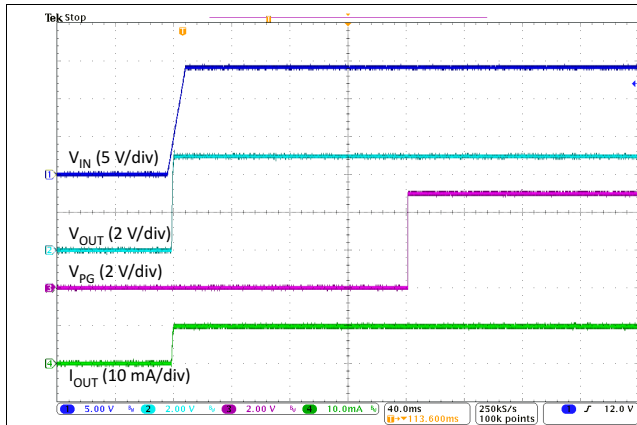


Figure 27. TPS7B6350-Q1 Power-Up Waveform

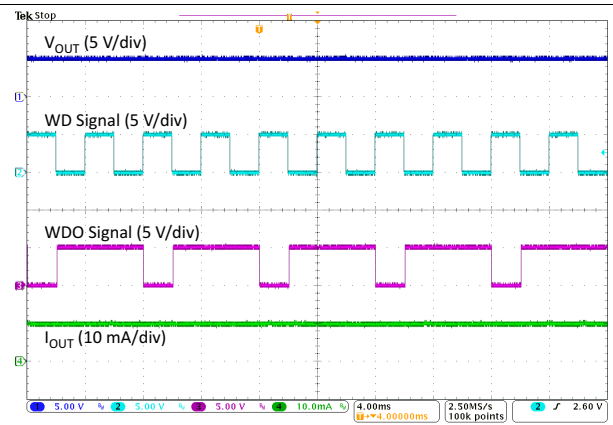


Figure 28. TPS7B6350-Q1 Watchdog Fault (High-Frequency Watchdog Service Signal)

## 9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B63xx-Q1 device, TI recommends adding a capacitor with a value of  $\geq 10 \mu\text{F}$  with a  $0.1 \mu\text{F}$  ceramic bypass capacitor in parallel at the input.

## 10 Layout

### 10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and high-current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of thermal limitation. To improve the thermal performance of the device and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as much as possible and putting enough thermal vias on the thermal pad. [Figure 29](#) shows an example layout.

### 10.2 Layout Example

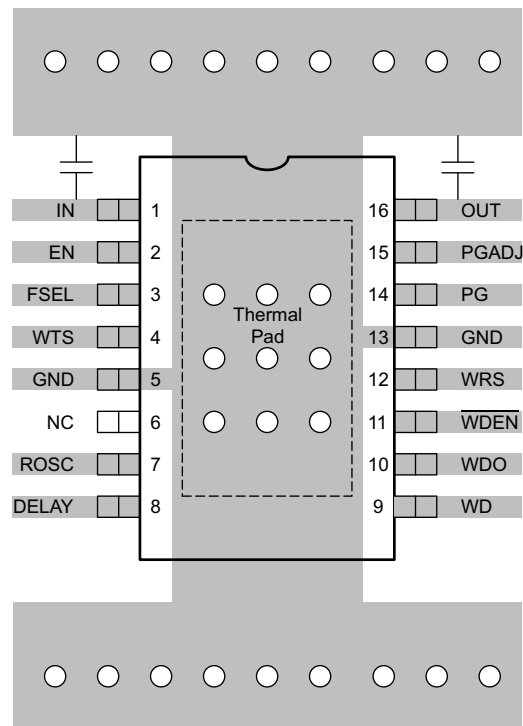


Figure 29. Layout Recommendation

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

[TPS7B63xx-Q1 Evaluation Module \(SLVUAZ6\)](#)

#### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7B6333-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS7B6350-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

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#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B6333QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6333Q	<a href="#">Samples</a>
TPS7B6350QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6350Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



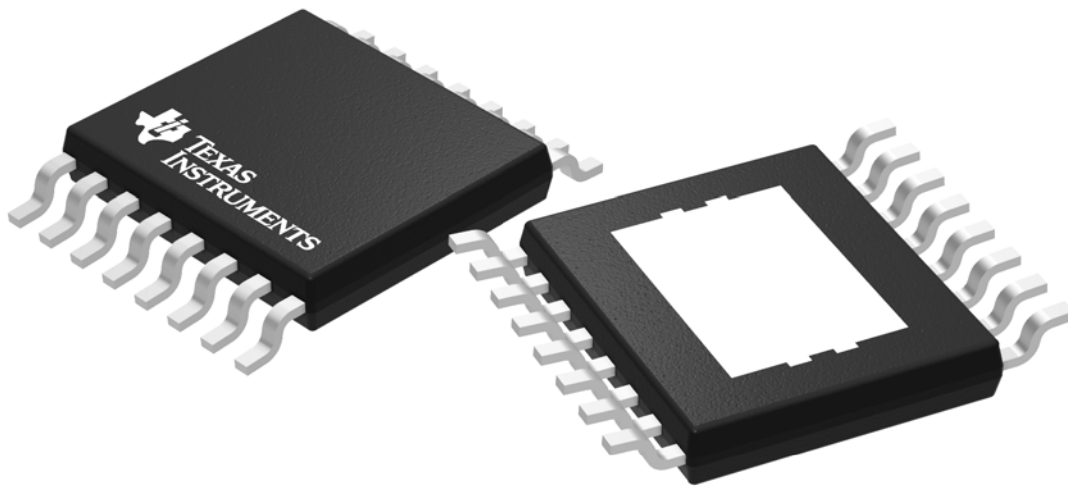
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6333QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B6350QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

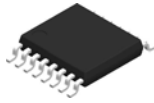

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6333QPWRQ1	HTSSOP	PWP	16	2000	367.0	367.0	38.0
TPS7B6350QPWRQ1	HTSSOP	PWP	16	2000	367.0	367.0	38.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

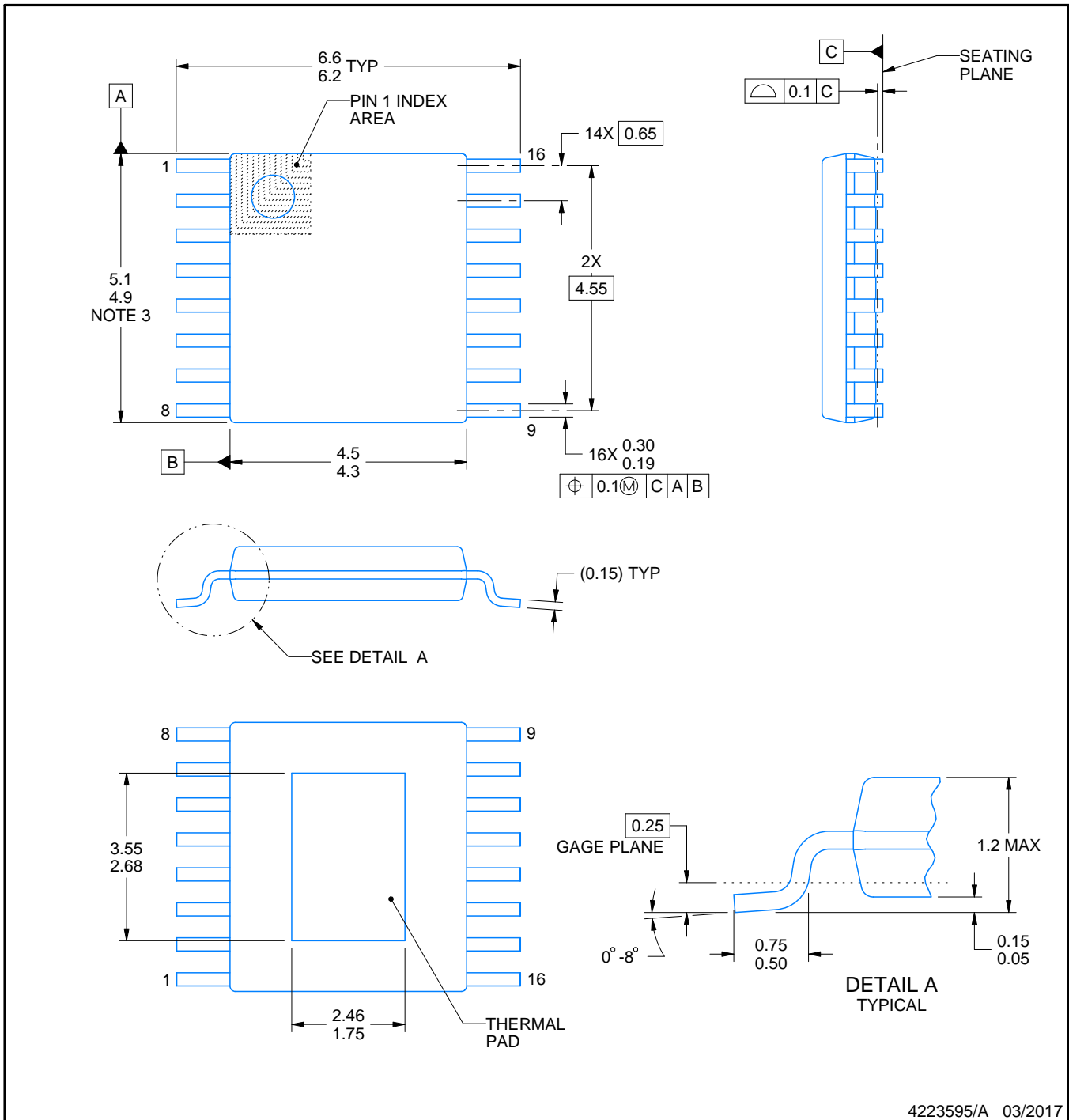
PWP0016J



# PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

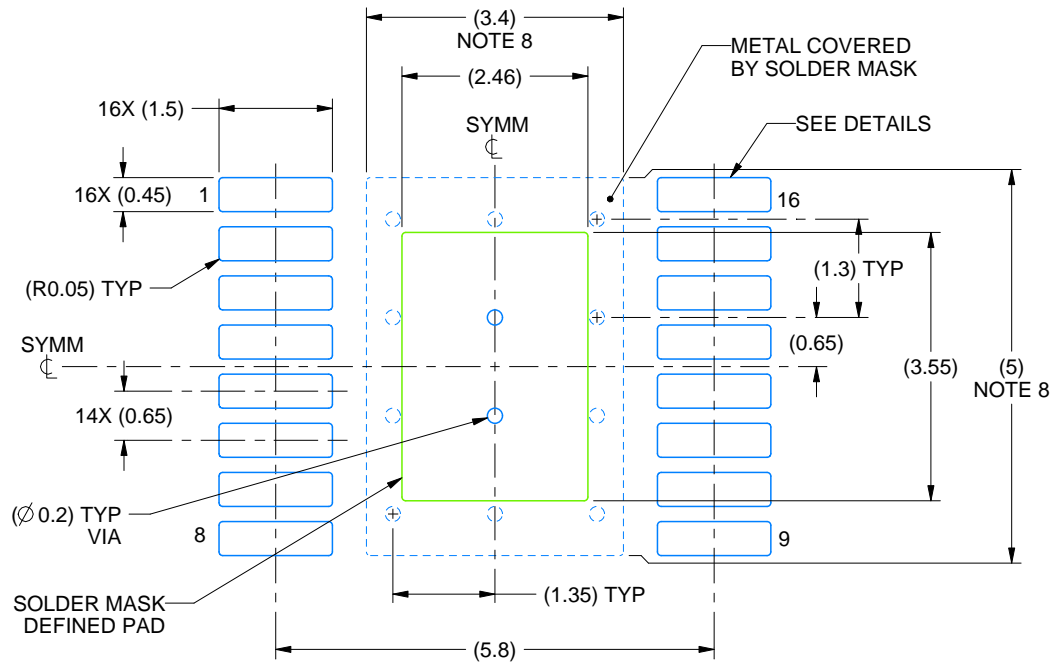
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

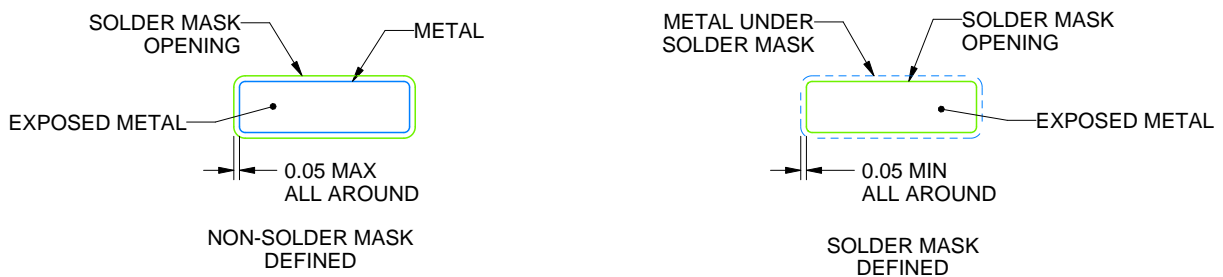
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

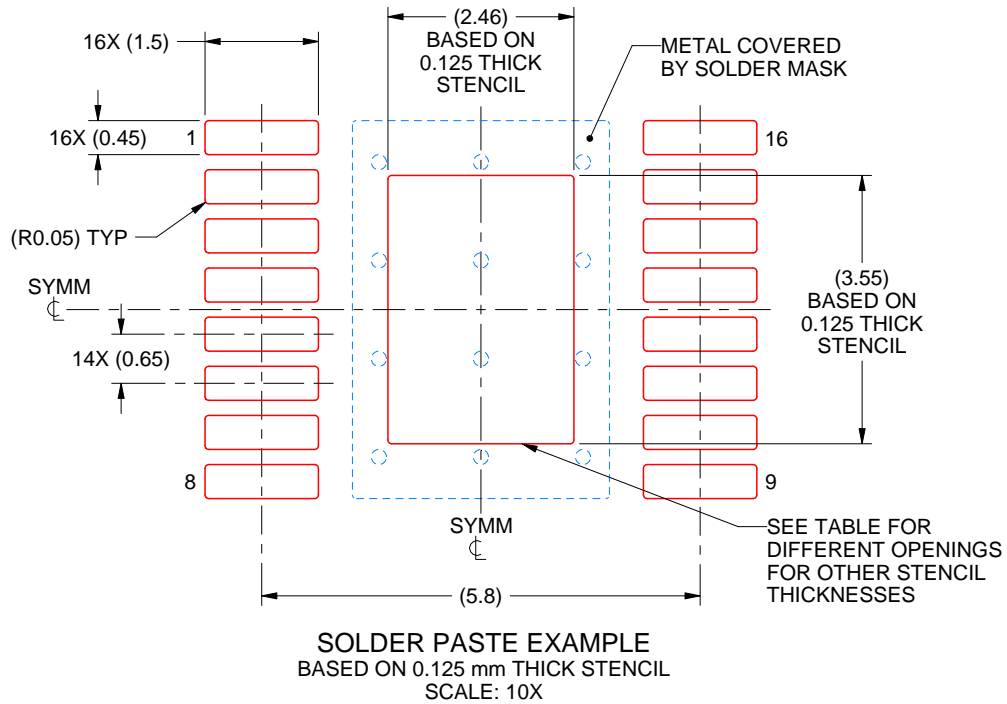
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



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