# ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 500-mA LOW-DROPOUT LINEAR REGULATORS

Check for Samples: TPS79501-Q1

## FEATURES

- **Qualified for Automotive Applications**
- **500-mA Low-Dropout Regulator With Enable**
- **High PSRR (50 dB at 10 kHz)**
- **Ultralow Noise (33 μ$V_{RMS}$, TPS79501-Q1)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 1-μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Low Dropout Voltage (110 mV at Full Load, TPS79501-Q1)**

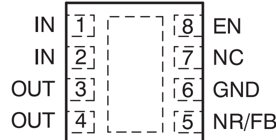
## APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Bluetooth®, Wireless LAN**

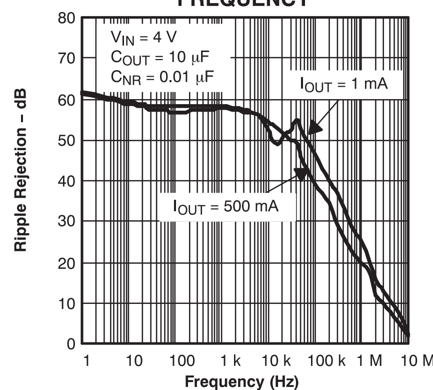
## DESCRIPTION

The TPS79501-Q1 low-dropout (LDO), low-power linear voltage regulator features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline SON package. The device is stable with a small 1-μF ceramic capacitor on the output. The TPS79501-Q1 uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 110 mV at 500 mA). The device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (265 μA, typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79501-Q1 exhibits approximately 33 μ$V_{RMS}$ of output voltage noise at 3-V output with a 0.1-μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.

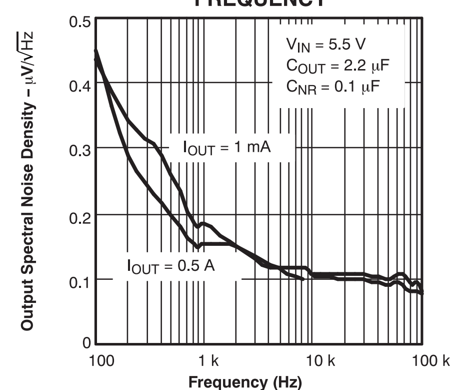
**DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)**




**RIPPLE REJECTION vs FREQUENCY**




**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION(1)

| $T_A$ | PACKAGE | | ORDERABLE | TOP-SIDE MARKING |
|---|---|---|---|---|
| -40°C to 125°C | SON – DRB | Tape and reel | TPS79501QDRBRQ1 | QVE |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating temperature (unless otherwise noted)(1)

| | VALUE |
|---|---|
| $V_{IN}$ range | –0.3 V to 6 V |
| $V_{EN}$ range | –0.3 V to $V_{IN}$ + 0.3 V |
| $V_{OUT}$ range | 6 V |
| Peak output current | Internally limited |
| Continuous total power dissipation | See the Thermal Information Table |
| Junction temperature range, $T_J$ | –40°C to 150°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## THERMAL INFORMATION

| THERMAL METRIC(1)(2) | | TPS795xx(3) DRB (8 PINS) | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(4) | 47.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(5) | 83 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(6) | n/a | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(7) | 2.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(8) | 17.8 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(9) | 12.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW and DRC packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
(b) DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections of this data sheet.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $\theta_{JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $\theta_{JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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## ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range ($T_J$ = –40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V[(1)], $I_{OUT}$ = 1 mA, $C_{OUT}$ = 10 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. Typical values are at +25°C.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| --- | --- | --- | --- | --- | --- |
| Input voltage, $V_{IN}$ [(1)] | | 2.7 | | 5.5 | V |
| Internal reference, $V_{FB}$ | | 1.200 | 1.225 | 1.250 | V |
| Continuous output current, $I_{OUT}$ | | 0 | | 500 | mA |
| Output voltage: Output voltage range | | 1.225 | | 5.5 – $V_{DO}$ | V |
| Output voltage: Accuracy, see Note [(2)] | 0 µA ≤ $I_{OUT}$ ≤ 500 mA, $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 5.5 V [(1)] | 0.98($V_{OUT}$) | $V_{OUT}$ | 1.02($V_{OUT}$) | V |
| Output voltage line regulation ($\Delta V_{OUT}\%/\Delta V_{IN}$) [(1)] | $V_{OUT}$ + 1 V ≤ $V_{IN}$ ≤ 5.5 V | | 0.05 | 0.12 | %/V |
| Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$) | 0 µA ≤ $I_{OUT}$ ≤ 500 mA, | | 3 | | mV |
| Dropout voltage [(3)] $V_{IN} = V_{OUT(nom)}$ - 0.1 V | $I_{OUT}$ = 500 mA | | 110 | 170 | mV |
| Output current limit | $V_{OUT}$ = 0 V | 2.4 | 2.8 | 4.2 | A |
| Ground pin current | 0 µA ≤ $I_{OUT}$ ≤ 500 mA | | 265 | 385 | µA |
| Shutdown current [(4)] | $V_{EN}$ = 0 V, 2.7 V ≤ $V_{IN}$ ≤ 5.5 V | | 0.07 | 1 | µA |
| FB pin current | $V_{FB}$ = 1.225 V | | | 1 | µA |
| Power-supply ripple rejection | f = 100 Hz, $I_{OUT}$ = 10 mA | | 59 | | dB |
| | f = 100 Hz, $I_{OUT}$ = 500 mA | | 58 | | |
| | f = 10 kHz, $I_{OUT}$ = 500 mA | | 50 | | |
| | f = 100 kHz, $I_{OUT}$ = 500 mA | | 39 | | |
| Output noise voltage | BW = 100 Hz to 100 kHz, $I_{OUT}$ = 500 mA, $C_{NR}$ = 0.001 µF | | 46 | | $\mu V_{RMS}$ |
| | BW = 100 Hz to 100 kHz, $I_{OUT}$ = 500 mA, $C_{NR}$ = 0.0047 µF | | 41 | | |
| | BW = 100 Hz to 100 kHz, $I_{OUT}$ = 500 mA, $C_{NR}$ = 0.01 µF | | 35 | | |
| | BW = 100 Hz to 100 kHz, $I_{OUT}$ = 500 mA, $C_{NR}$ = 0.1 µF | | 33 | | |
| Time, start-up | $R_L$ = 6 Ω, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.001 µF | | 50 | | µs |
| | $R_L$ = 6 Ω, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.0047 µF | | 75 | | |
| | $R_L$ = 6 Ω, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF | | 110 | | |
| High-level enable input voltage | 2.7 V ≤ $V_{IN}$ ≤ 5.5 V | 1.7 | | $V_{IN}$ | V |
| Low-level enable input voltage | 2.7 V ≤ $V_{IN}$ ≤ 5.5 V | | | 0.7 | V |
| EN pin current | $V_{EN}$ = 0 V | 1 | | 1 | µA |
| UVLO threshold | $V_{CC}$ rising | 2.25 | | 2.65 | V |
| UVLO hysteresis | | | 100 | | mV |

(1) Minimum $V_{IN}$ is 2.7 V or $V_{OUT}$ + $V_{DO}$, whichever is greater.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured since minimum $V_{IN}$ = 2.7 V.
(4) For adjustable version, this applies only after $V_{IN}$ is applied; then $V_{EN}$ transitions high to low.

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## FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION

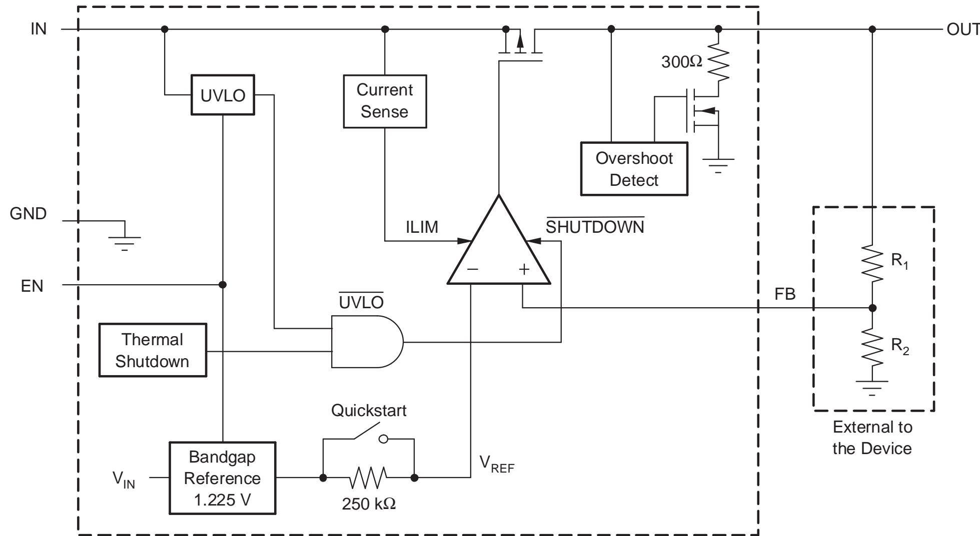


**Table 1. Terminal Functions**

| NAME | 3x3 SON (DRB) PIN NO. | DESCRIPTION |
|---|---|---|
| IN | 1, 2 | Unregulated input to the device |
| GND | 6 | Regulator ground |
| EN | 8 | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used. |
| NR | 5 | Noise-reduction pin for fixed versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise. |
| FB | 5 | Feedback input voltage for the adjustable device. |
| OUT | 3, 4 | Regulator output. |
| NC | 7 | Not connected |

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

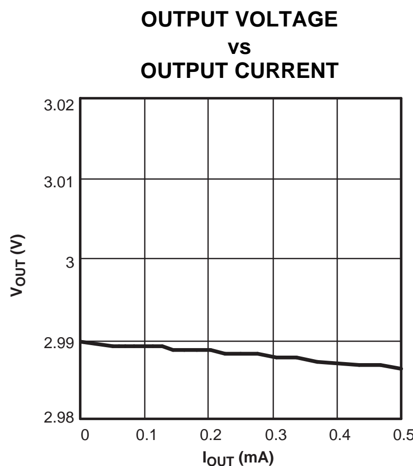


Figure 1.

**OUTPUT VOLTAGE vs JUNCTION TEMPERATURE**

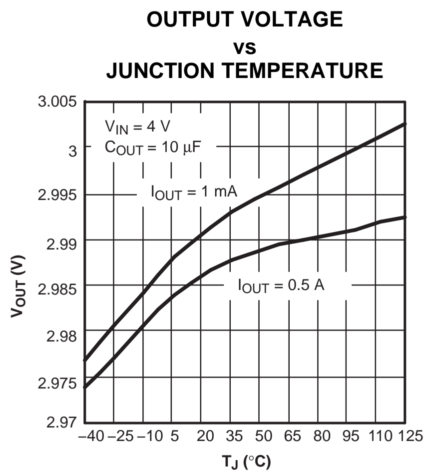


Figure 2.

**GROUND CURRENT vs JUNCTION TEMPERATURE**

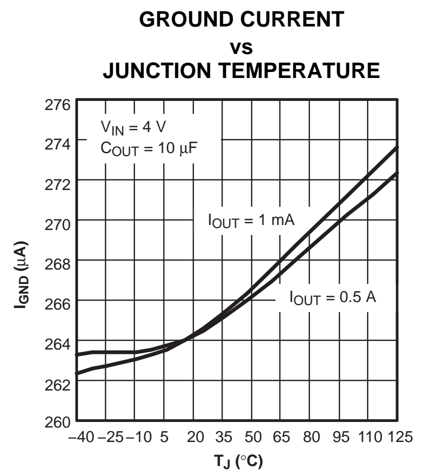


Figure 3.


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## TYPICAL CHARACTERISTICS (continued)

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

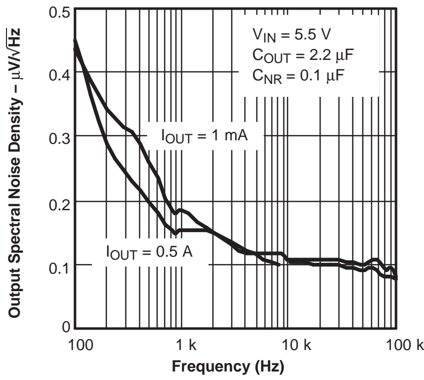


Figure 4.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

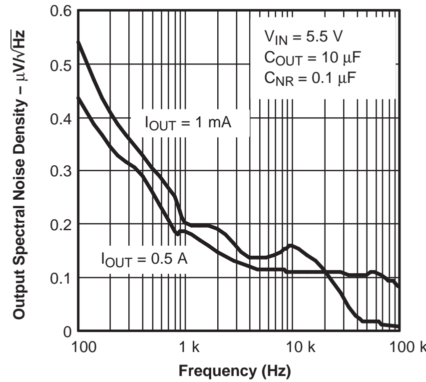


Figure 5.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

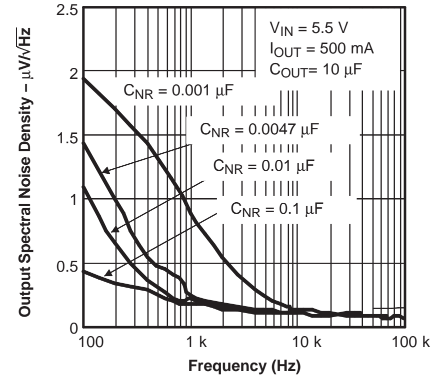


Figure 6.

ROOT MEAN SQUARED OUTPUT NOISE vs $C_{NR}$

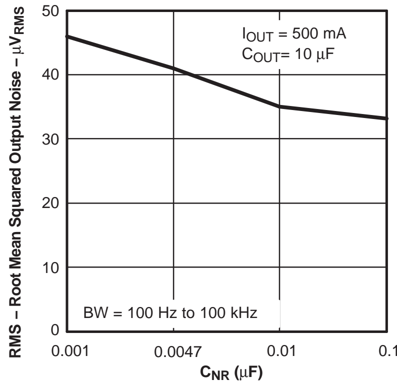


Figure 7.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

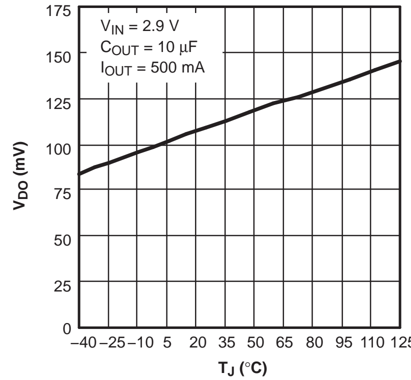


Figure 8.

RIPPLE REJECTION vs FREQUENCY

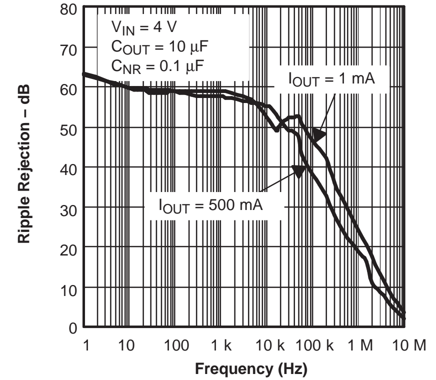


Figure 9.

RIPPLE REJECTION vs FREQUENCY

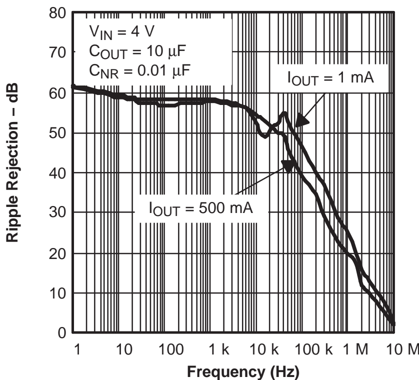


Figure 10.

RIPPLE REJECTION vs FREQUENCY

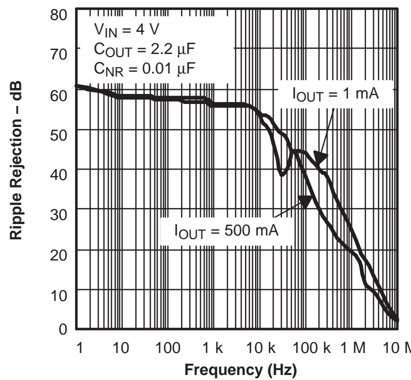


Figure 11.

RIPPLE REJECTION vs FREQUENCY

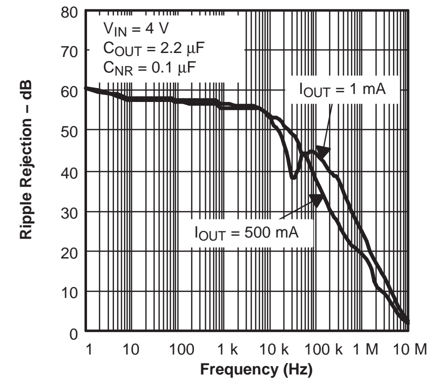


Figure 12.

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## TYPICAL CHARACTERISTICS (continued)

START-UP TIME

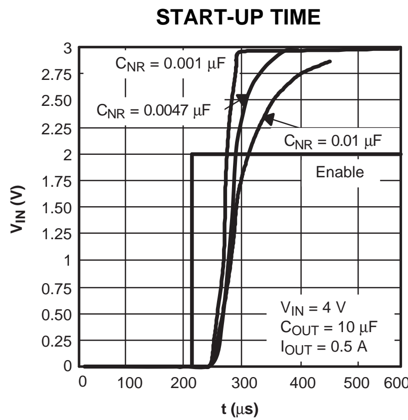


Figure 13.

LINE TRANSIENT RESPONSE

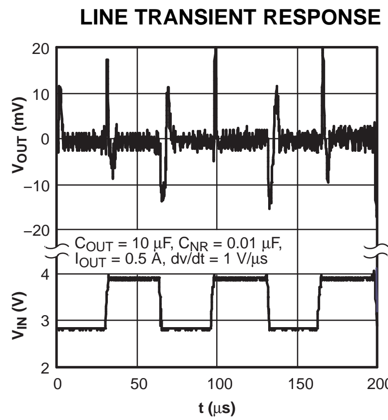


Figure 14.

LINE TRANSIENT RESPONSE

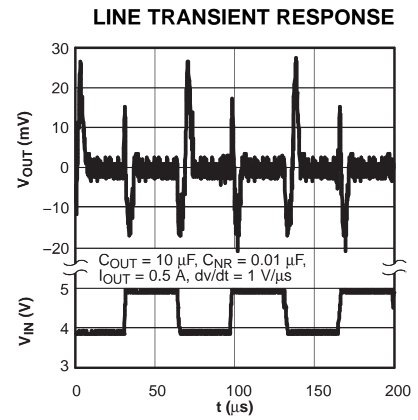


Figure 15.

LOAD TRANSIENT RESPONSE

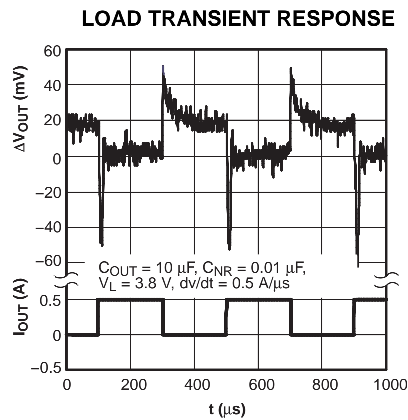


Figure 16.

POWER UP/POWER DOWN

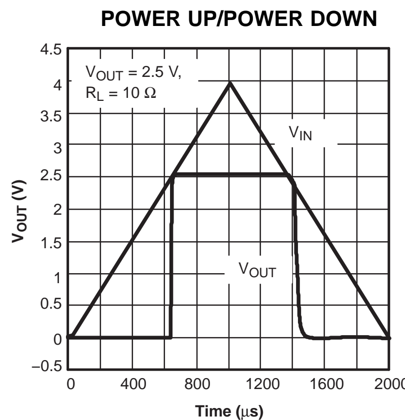


Figure 17.

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

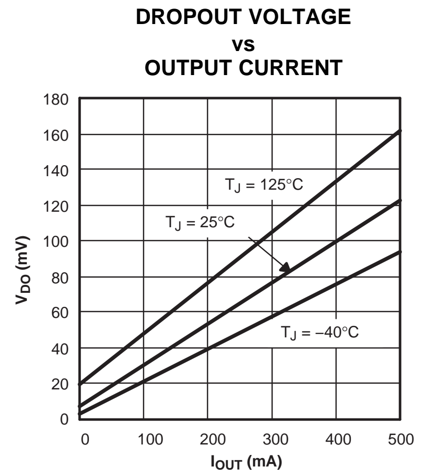


Figure 18.

DROPOUT VOLTAGE
vs
INPUT VOLTAGE

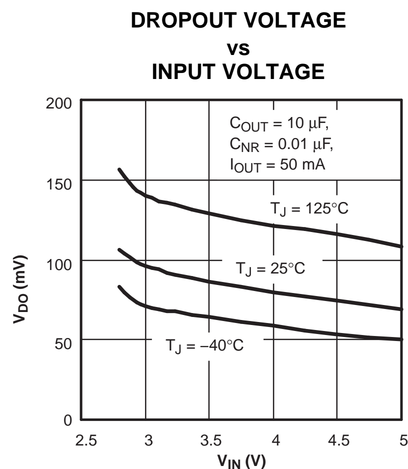


Figure 19.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE
(ESR)
vs
OUTPUT CURRENT

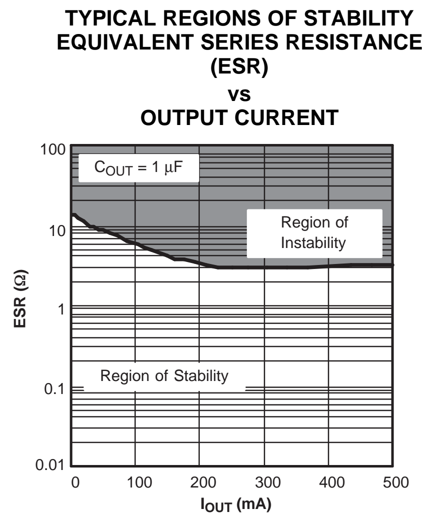


Figure 20.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE
(ESR)
vs
OUTPUT CURRENT

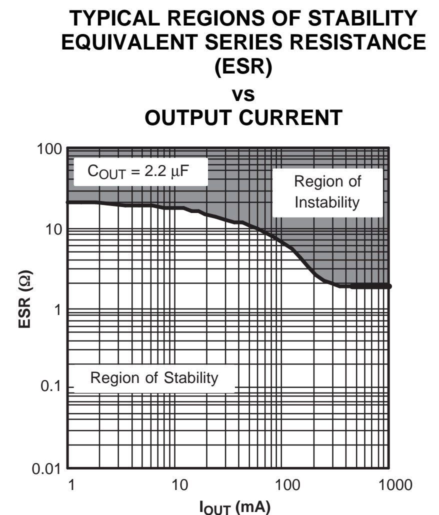


Figure 21.


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## TYPICAL CHARACTERISTICS (continued)

**TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR)**
**vs**
**OUTPUT CURRENT**

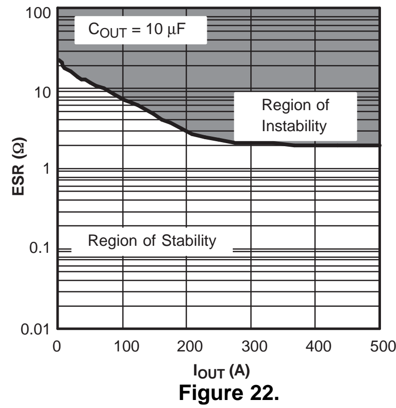


**Figure 22.**

## APPLICATION INFORMATION

The TPS79501-Q1 low-dropout (LDO) regulator has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA typical), and an enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 23.

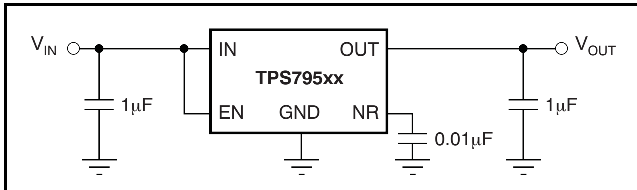


**Figure 23. Typical Application Circuit**

## EXTERNAL CAPACITOR REQUIREMENTS

Although not required, it is good analog design practice to place a 0.1μF to 2.2μF capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS79501-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 μF. Any 1 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS79501-Q1 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-μF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the Functional Block Diagram.

For example, the TPS79501-Q1 exhibits only 33 $\mu V_{RMS}$ of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

## BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

## REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in application report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site (www.ti.com).


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## PROGRAMMING THE TPS79501-Q1 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79501-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

- $V_{REF}$ = 1.2246 V typ (the internal reference voltage)

Resistors $R_1$ and $R_2$ should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose $R_2$ = 30.1 kΩ to set the divider current at 40 μA, $C_1$ = 15 pF for stability, and then calculate $R_1$ using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated as Equation 3:

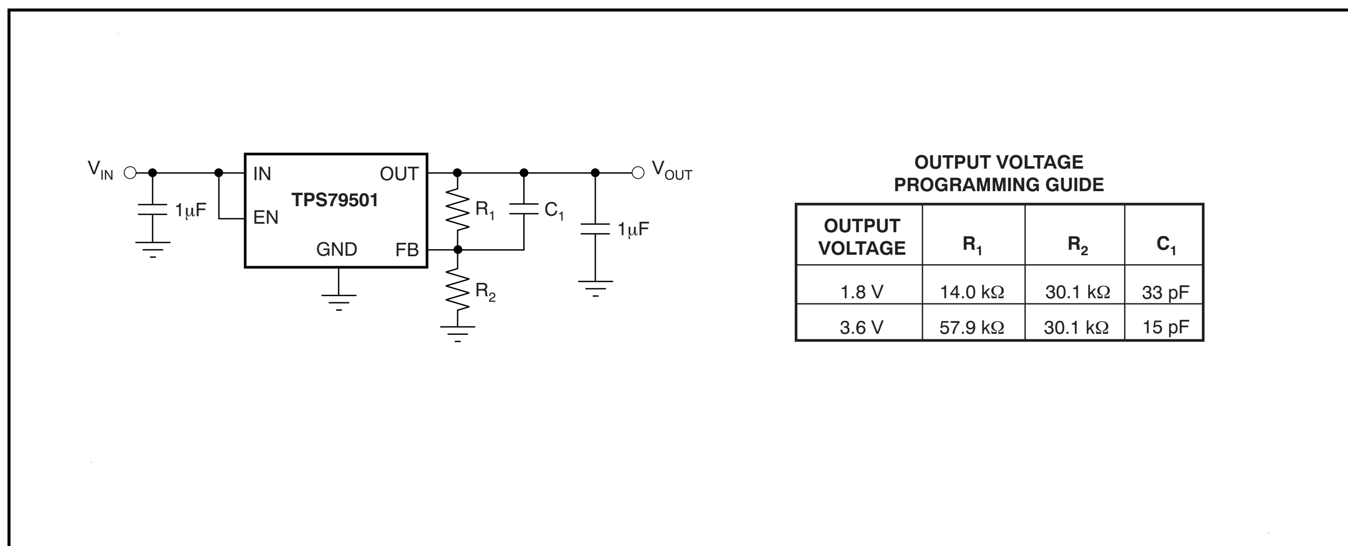
$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within Figure 24. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μF instead of 1 μF.

## REGULATOR PROTECTION

The TPS79501-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS79501-Q1 features internal current limiting and thermal protection. During normal operation, the TPS79501-Q1 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.




OUTPUT VOLTAGE PROGRAMMING GUIDE

| OUTPUT VOLTAGE | $R_1$ | $R_2$ | $C_1$ |
|---|---|---|---|
| 1.8 V | 14.0 kΩ | 30.1 kΩ | 33 pF |
| 3.6 V | 57.9 kΩ | 30.1 kΩ | 15 pF |

**Figure 24. TPS79501-Q1 Adjustable LDO Regulator Programming**

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## THERMAL INFORMATION

### Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

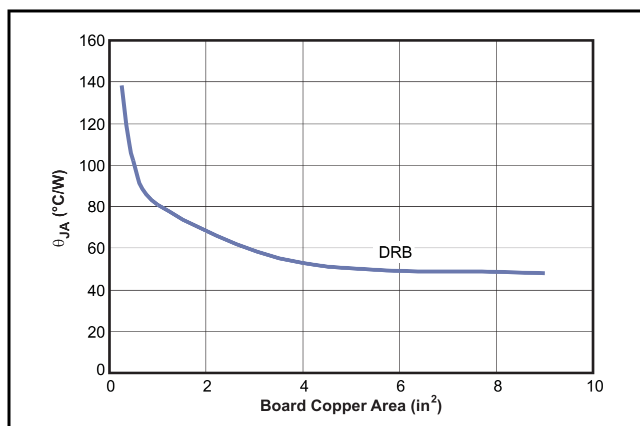
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125^oC - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 25.




Note: $\theta_{JA}$ value at board size of 9 in$^2$ (that is, 3 in × 3 in) is a JEDEC standard.

**Figure 25. $\theta_{JA}$ vs Board Size**

Figure 25 shows the variation of $\theta_{JA}$ as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effect of heat spreading in the ground plane and should not be used to estimate the thermal performance in real application environments.

**NOTE:** When the device is mounted on an application PCB, it is strongly recommended to use $\Psi_{JT}$ and $\Psi_{JB}$, as explained in the *Estimating Junction Temperature* section.

## ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, as shown in the Thermal Information table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC}$,*Top* parameter is also listed.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \quad (6)$$

Where $P_D$ is the power dissipation shown by Equation 5, $T_T$ is the temperature at the center-top of the IC package, and $T_B$ is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (as Figure 27 shows).

**NOTE:** Both $T_T$ and $T_B$ can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring $T_T$ and $T_B$, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 26, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have little dependency on board size. That is, using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 6 is a good way to estimate $T_J$ by simply measuring $T_T$ or $T_B$, regardless of the application board size.

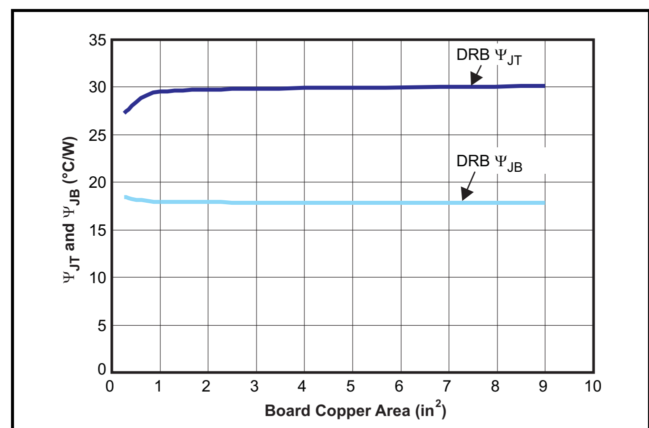



**Figure 26. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size**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For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

For further information, see the application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.

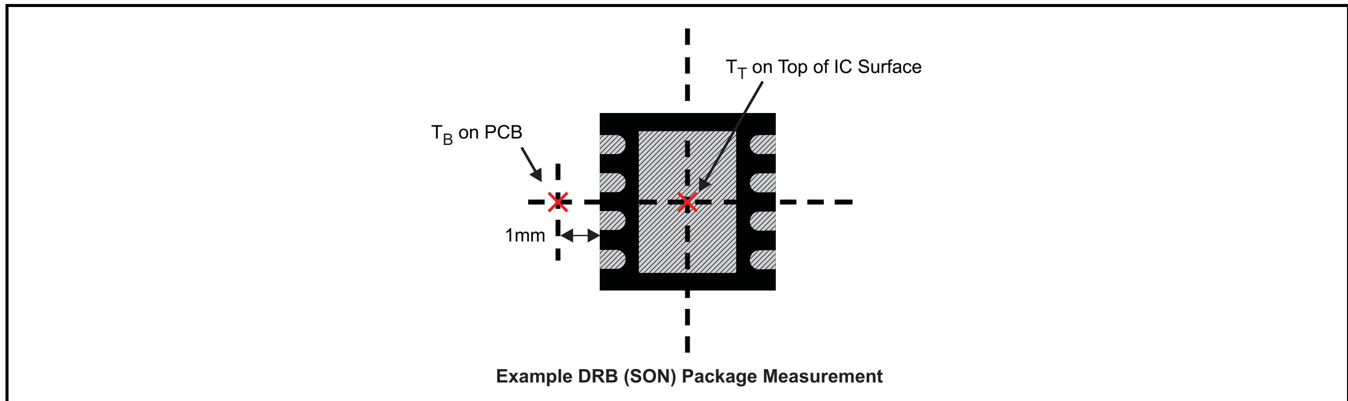


Figure 27. Measuring Point for $T_T$ and $T_B$

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS79501QDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | Request Free Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TPS79501-Q1 :**

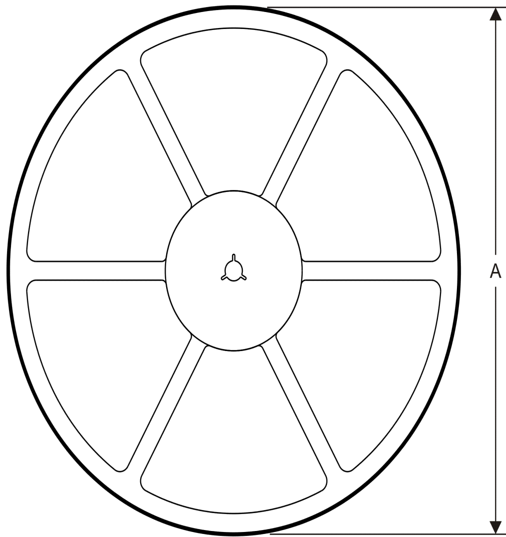
- Catalog: TPS79501

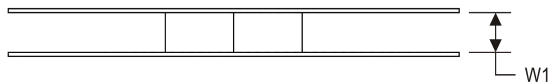
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

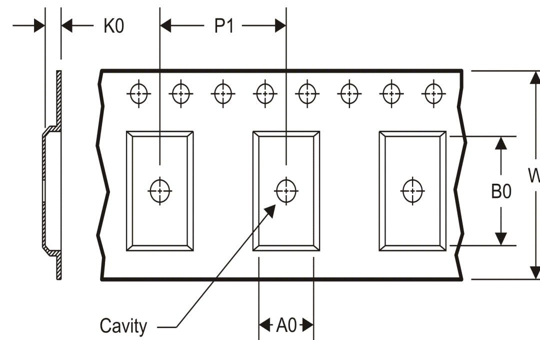
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



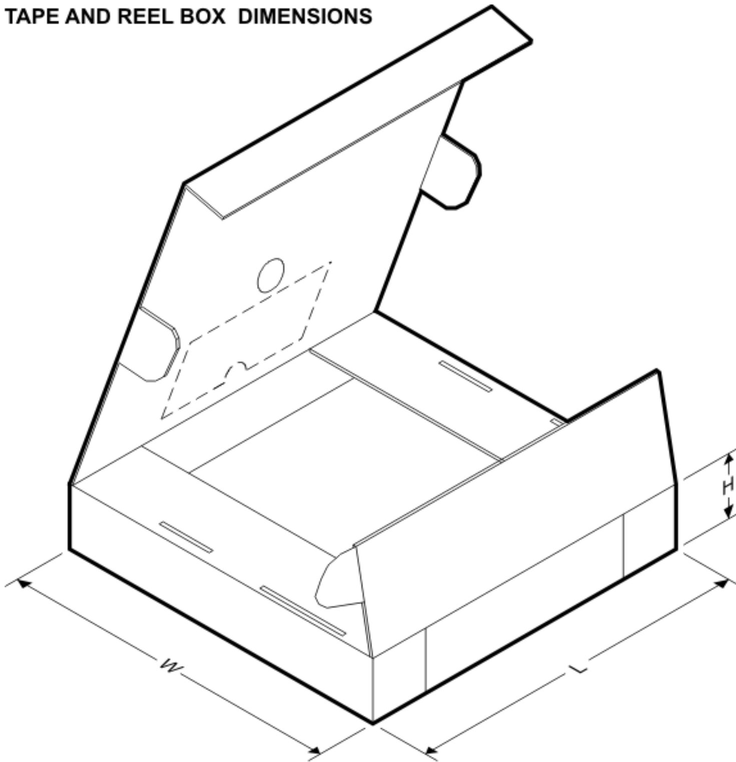

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79501QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

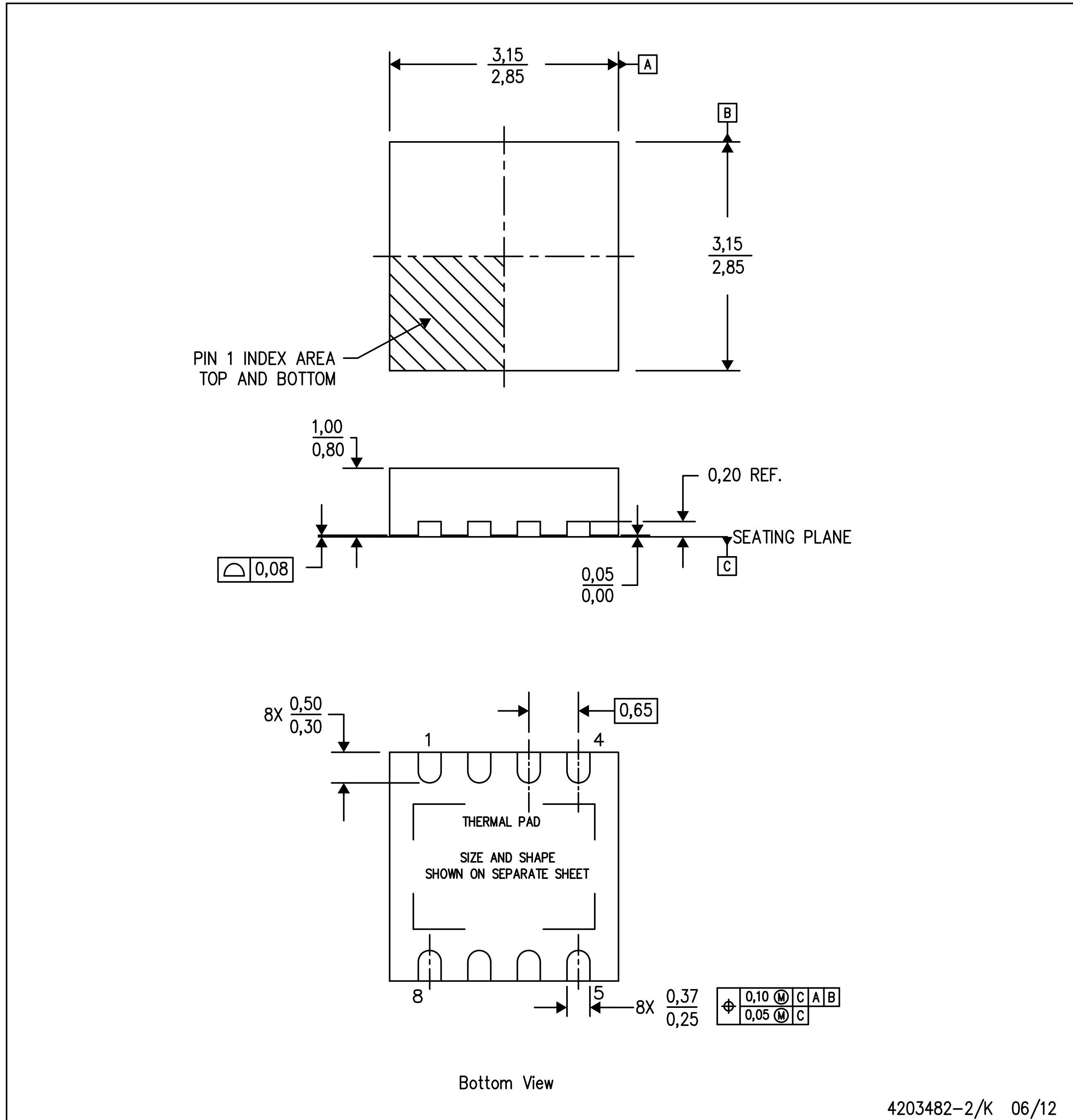
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS79501QDRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

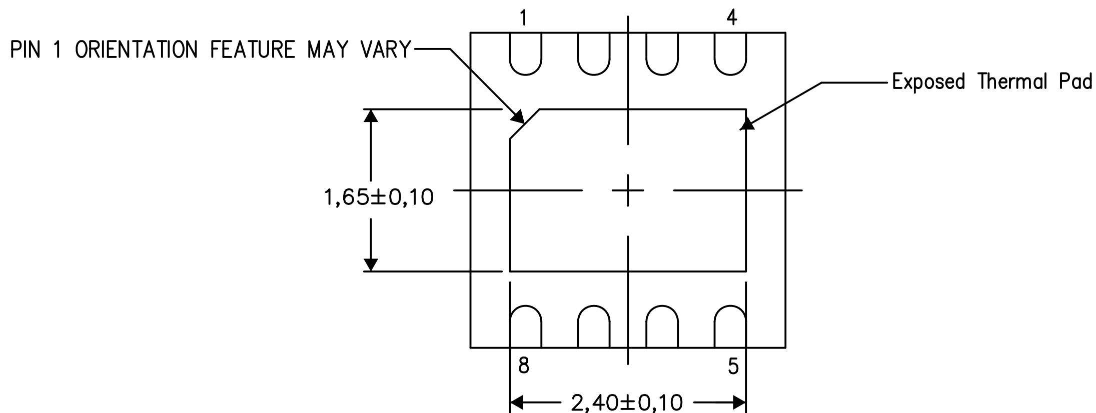
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



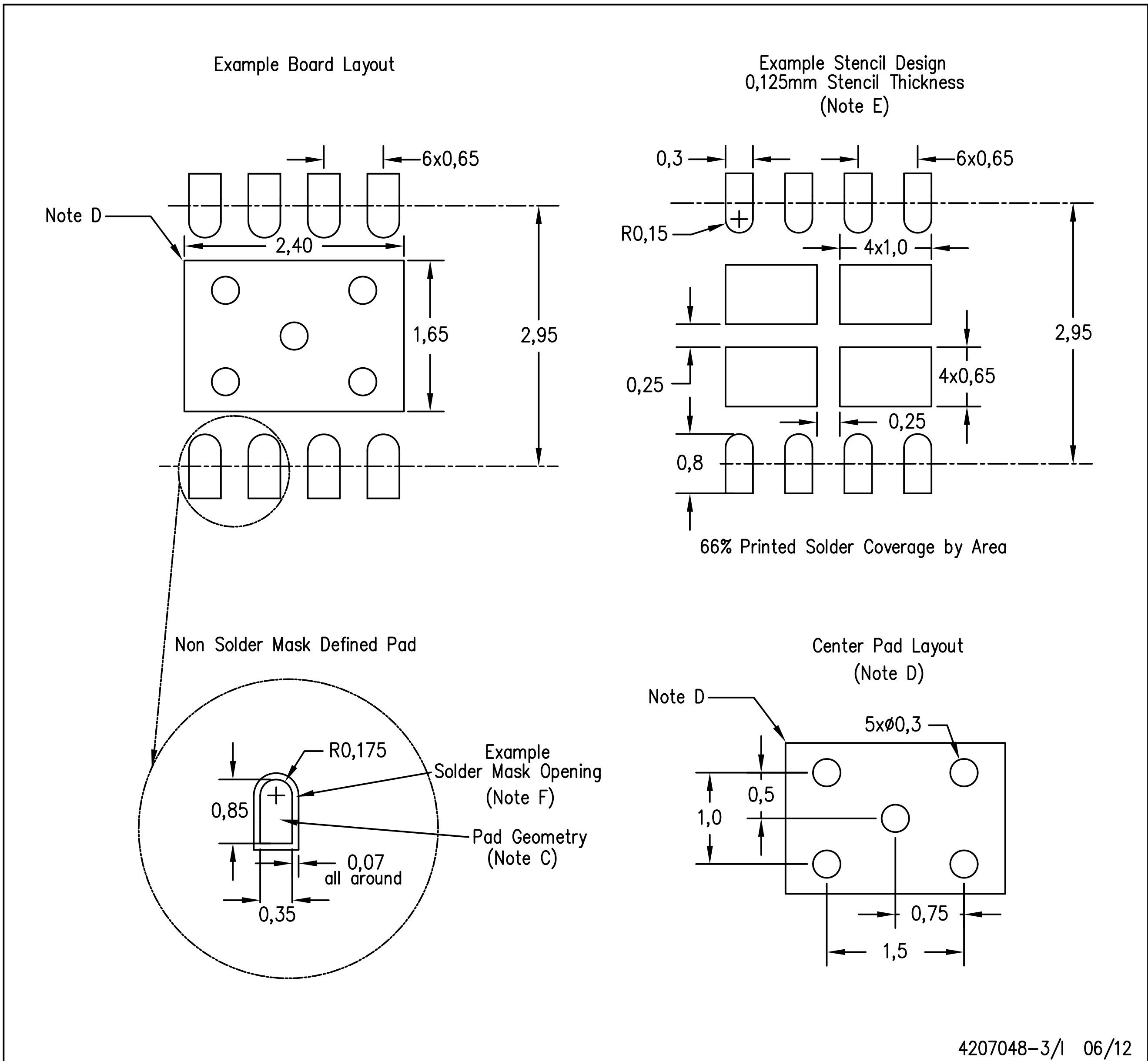

Bottom View

Exposed Thermal Pad Dimensions

4206340-3/M 06/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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