

# TPS720-Q1

## 350-mA, Ultra-Low $V_{IN}$ , RF Low-Dropout Linear Regulator With BIAS Pin

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C6
- Input Voltage Range: 1.1 V to 4.5 V
- Output Voltage Range: 0.9 V to 3.0 V
- High-Performance LDO: 350 mA
- Low Quiescent Current: 38  $\mu\text{A}$
- Excellent Load Transient Response:  $\pm 15$  mV for  $I_{LOAD} = 0$  mA to 350 mA in 1  $\mu\text{s}$
- Low Noise: 48  $\mu\text{V}_{RMS}$  (10 Hz to 100 kHz)
- 80-dB  $V_{IN}$  PSRR (10 Hz to 10 kHz)
- 70-dB  $V_{BIAS}$  PSRR (10 Hz to 10 kHz)
- Fast Start-Up Time: 140  $\mu\text{s}$
- Built-In Soft-Start With Monotonic  $V_{OUT}$  Rise and Start-Up Current Limited to 100 mA +  $I_{LOAD}$
- Overcurrent and Thermal Protection
- Low Dropout: 110 mV at  $I_{LOAD} = 350$  mA
- Stable with a 2.2- $\mu\text{F}$  Output Capacitor
- Package: 2-mm x 2-mm, 6-Pin WSON

### 2 Applications

- Camera Modules
- FPD Link Power
- Automotive Infotainment
- USB HUB Power

### 3 Description

The TPS720-Q1 family of dual-rail, low-dropout linear regulators (LDOs) offers outstanding ac performance (PSRR, load and line transient response) and consume a very low quiescent current of 38  $\mu\text{A}$ .

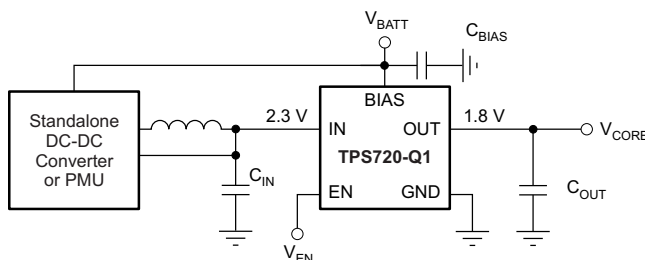
The  $V_{BIAS}$  rail that powers the control circuit of the LDO draws very low current (on the order of the LDO quiescent current) and can be connected to any power supply that is equal to or greater than 1.4 V above the output voltage. The main power path is through  $V_{IN}$  and can be a lower voltage than  $V_{BIAS}$ ; this path can be as low as  $V_{OUT} + V_{DO}$ , increasing the efficiency of the solution in many power-sensitive applications. For example,  $V_{IN}$  can be an output of a high-efficiency, dc-dc, step-down regulator.

The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads when the IN pin is left floating. The light-load drive current is sourced from  $V_{BIAS}$  under this condition. This feature is particularly useful in power-saving applications where the dc-dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load.

The TPS720-Q1 is stable with ceramic capacitors and uses an advanced BICMOS fabrication process that yields a dropout of 110 mV at a 350-mA output load. The TPS720-Q1 has the unique feature of providing a monotonic  $V_{OUT}$  rise (overshoot limited to 3%) with  $V_{IN}$  inrush current limited to 100 mA +  $I_{LOAD}$  with an output capacitor of 2.2  $\mu\text{F}$ .

The TPS720-Q1 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over load, line, process, and temperature extremes. The TPS720-Q1 is available in a 6-pin WSON package. This family of devices is fully specified over the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Simplified Schematic



#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS720-Q1	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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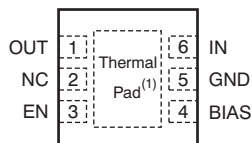
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## 4 Revision History

DATE	REVISION	NOTES
February 2016	*	Initial release.

## 5 Pin Configuration and Functions

**DRV Package**  
**6-Pin WSON With Exposed Thermal Pad**  
**Top View**



(1) Connecting the WSON (DRV) package thermal pad to ground is recommended.

### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT	O	Output pin. A 2.2- $\mu$ F ceramic capacitor is connected from this pin to ground for stability and to provide load transients; see the <a href="#">Input and Output Capacitor Requirements</a> section.
2	NC	—	No connection
3	EN	I	Enable pin. A logic high signal on this pin turns the device on and regulates the voltage from IN to OUT. A logic low on this pin turns the device off.
4	BIAS	I	Bias supply pin. Bypassing this input with a ceramic capacitor to ground is recommended for better transient performance; see the <a href="#">Input and Output Capacitor Requirements</a> section.
5	GND	—	Ground pin
6	IN	I	Input pin. This pin can be a maximum of 4.5 V; $V_{IN}$ must not exceed $V_{BIAS}$ . Bypass this input with a ceramic capacitor to ground; see the <a href="#">Input and Output Capacitor Requirements</a> section.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

at  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted); all voltages are with respect to GND<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN}^{(2)}$	Input voltage (steady-state)	-0.3	$V_{BIAS}$ or 5 <sup>(3)</sup>	V
$V_{IN\_PEAK}^{(4)}$	Peak transient input		5.5	V
$V_{BIAS}$	Bias voltage	-0.3	6	V
$V_{EN}$	Enable voltage	-0.3	6	V
$V_{OUT}$	Output voltage	-0.3	5	V
$I_{OUT}$	Peak output current	Internally limited		
	Output short-circuit duration	Indefinite		
$P_{DISS}$	Total continuous power dissipation	See <a href="#">Thermal Information</a>		
$T_J$	Operating junction temperature	-55	125	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) To ensure proper device operation,  $V_{IN}$  must be less than or equal to  $V_{BIAS}$  under all conditions.
- (3) Whichever is less.
- (4) For durations no longer than 1 ms each, for a total of no more than 1000 occurrences over the lifetime of the device.

## 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500
		Machine model (MM)	±100

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage (steady-state)	1.1		$V_{BIAS}$ or 4.5 <sup>(1)</sup>	V
$V_{BIAS}$	Bias voltage	2.6 or $V_{OUT} + 1.4$ <sup>(2)</sup>		5.5	V
$V_{OUT}$	Output voltage	0.9		3.0	V
$I_{OUT}$	Peak output current	0		350	mA
$V_{EN}$	Enable voltage	0		5.5	V
$C_{IN}$	Input capacitance		1		μF
$C_{BIAS}$	Bias capacitance		0.1		μF
$C_{OUT}$ <sup>(3)</sup>	Output capacitance	2.2			μF

(1) Whichever is less.

(2) Whichever is greater.

(3) Maximum ESR must be less than 250 mΩ.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS720-Q1	UNIT
		DRV (WSON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.6\text{ V}$  (whichever is greater),  $V_{IN} \geq V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage		1.1 <sup>(1)</sup>	$V_{BIAS}$ or 4.5 <sup>(2)</sup>		V
$V_{BIAS}$	Bias voltage		2.6		5.5	V
$V_{OUT}$ <sup>(3)</sup>	Output voltage <sup>(4)</sup>		0.9		3	V
	Output accuracy	Over $V_{BIAS}$ , $V_{IN}$ , $I_{OUT}$ , $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{OUT} + 1.4\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 4.5\text{ V}$ , $0\text{ mA} \leq I_{OUT} \leq 350\text{ mA}$	-2%		2%	
		Over $V_{BIAS}$ , $V_{IN}$ , $I_{OUT}$ , $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{OUT} + 1.4\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 4.5\text{ V}$ , $0\text{ mA} \leq I_{OUT} \leq 350\text{ mA}$ , $V_{OUT} < 1.2\text{ V}$	-25		25	mV
$V_{IN}$ floating	$V_{OUT} + 1.4\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ }\mu\text{A}$		$\pm 1\%$			
$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN}$ line regulation	$V_{IN} = (V_{OUT} + 0.5\text{ V})$ to $4.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$		16		$\mu\text{V}/\text{V}$
$\Delta V_{OUT}/\Delta V_{BIAS}$	$V_{BIAS}$ line regulation	$V_{BIAS} = (V_{OUT} + 1.4\text{ V})$ or $2.6\text{ V}$ (whichever is greater) to $5.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$		16		$\mu\text{V}/\text{V}$
	$V_{IN}$ line transient	$\Delta V_{IN} = 400\text{ mV}$ , $t_{RISE} = t_{FALL} = 1\text{ }\mu\text{s}$		$\pm 200$		$\mu\text{V}$
	$V_{BIAS}$ line transient	$\Delta V_{BIAS} = 600\text{ mV}$ , $t_{RISE} = t_{FALL} = 1\text{ }\mu\text{s}$		$\pm 0.8$		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 350\text{ mA}$ (no load to full load)		-15		$\mu\text{V}/\text{mA}$
	Load transient	$0\text{ mA} \leq I_{OUT} \leq 350\text{ mA}$ , $t_{RISE} = t_{FALL} = 1\text{ }\mu\text{s}$		$\pm 15$		mV
$V_{DO\_IN}$	$V_{IN}$ dropout voltage <sup>(5)</sup>	$V_{IN} = V_{OUT(NOM)} - 0.1\text{ V}$ , $(V_{BIAS} - V_{OUT(NOM)}) = 1.4\text{ V}$ , $I_{OUT} = 350\text{ mA}$		110	200	mV
$V_{DO\_BIAS}$	$V_{BIAS}$ dropout voltage <sup>(6)</sup>	$V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ , $I_{OUT} = 350\text{ mA}$		1.09	1.4	V
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	420	600	800	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 100\text{ }\mu\text{A}$		38		$\mu\text{A}$
		$I_{OUT} = 0\text{ mA}$ to $350\text{ mA}$		54	80	
$I_{SHDN}$	Shutdown current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{ V}$		0.5	2.5	$\mu\text{A}$
PSRR	$V_{IN}$ power-supply rejection ratio	$V_{IN} - V_{OUT} \geq 0.5\text{ V}$ , $V_{BIAS} = V_{OUT} + 1.4\text{ V}$ , $I_{OUT} = 350\text{ mA}$	$f = 10\text{ Hz}$	85	dB	
			$f = 100\text{ Hz}$	85		
			$f = 1\text{ kHz}$	85		
			$f = 10\text{ kHz}$	80		
			$f = 100\text{ kHz}$	70		
			$f = 1\text{ MHz}$	50		
PSRR	$V_{BIAS}$ power-supply rejection ratio	$V_{IN} - V_{OUT} \geq 0.5\text{ V}$ , $V_{BIAS} = V_{OUT} + 1.4\text{ V}$ , $I_{OUT} = 350\text{ mA}$	$f = 10\text{ Hz}$	80	dB	
			$f = 100\text{ Hz}$	80		
			$f = 1\text{ kHz}$	75		
			$f = 10\text{ kHz}$	65		
			$f = 100\text{ kHz}$	55		
			$f = 1\text{ MHz}$	35		
$V_N$	Output noise voltage	$\text{BW} = 10\text{ Hz}$ to $100\text{ kHz}$ , $V_{BIAS} \geq 2.6\text{ V}$ , $V_{IN} = V_{OUT} + 0.5\text{ V}$		48		$\mu\text{V}_{\text{RMS}}$
$I_{VIN\_INRUSH}$	Inrush current on $V_{IN}$	$V_{BIAS} = (V_{OUT} + 1.4\text{ V})$ or $2.6\text{ V}$ (whichever is greater), $V_{IN} = V_{OUT} + 0.5\text{ V}$		$100 + I_{LOAD}$		mA
$V_{EN(HI)}$	Enable pin high (enabled)		1.1			V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V

(1) Performance specifications are ensured to a minimum  $V_{IN} = V_{OUT} + 0.5\text{ V}$ .

(2) Whichever is less.

(3) Minimum  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.6\text{ V}$  (whichever is greater) and  $V_{IN} = V_{OUT} + 0.5\text{ V}$ .

(4)  $V_O$  nominal value is factory programmable through the onchip EEPROM.

(5) Measured for devices with  $V_{OUT(NOM)} \geq 1.2\text{ V}$ .

(6)  $V_{BIAS} - V_{OUT}$  with  $V_{OUT} = V_{OUT(NOM)} - 0.1\text{ V}$ . Measured for devices with  $V_{OUT(NOM)} \geq 1.8\text{ V}$ .

## Electrical Characteristics (continued)

over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.6\text{ V}$  (whichever is greater),  $V_{IN} \geq V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{EN}$	Enable pin current	$V_{EN} = 5.5\text{ V}$ , $V_{IN} = 4.5\text{ V}$ , $V_{BIAS} = 5.5\text{ V}$			1	$\mu\text{A}$
UVLO	Undervoltage lockout	$V_{BIAS}$ rising	2.35	2.45	2.59	V
	UVLO hysteresis	$V_{BIAS}$ falling		150		mV
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		160		$^{\circ}\text{C}$
		Reset, temperature decreasing		140		
$T_J$	Operating junction temperature		-40		125	$^{\circ}\text{C}$

## 6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{STR}$	Start-up time	$V_{OUT} = 95\% V_{OUT(NOM)}$ , $I_{OUT} = 350\text{ mA}$ , $C_{OUT} = 2.2\text{ }\mu\text{F}$		140		$\mu\text{s}$

### 6.7 Typical Characteristics

over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.6\text{ V}$  (whichever is greater),  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

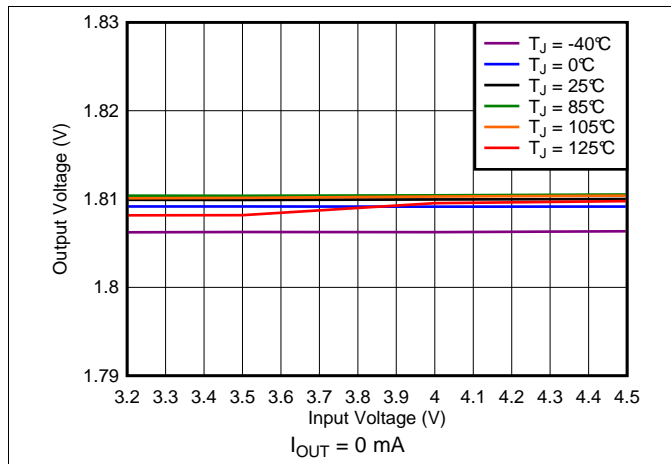


Figure 1.  $V_{IN}$  Line Regulation (No Load)

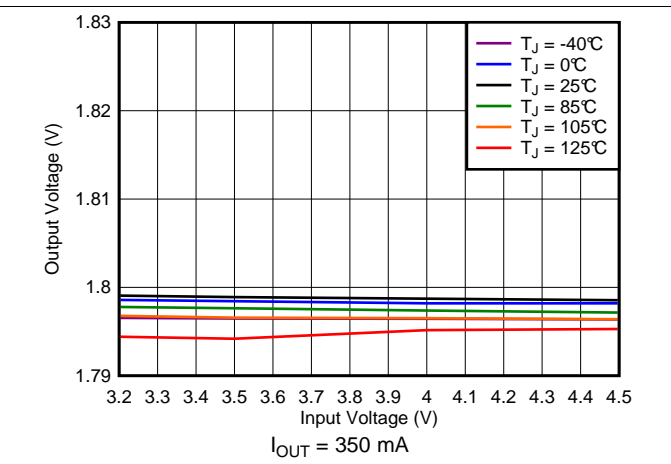


Figure 2.  $V_{IN}$  Line Regulation (350 mA)

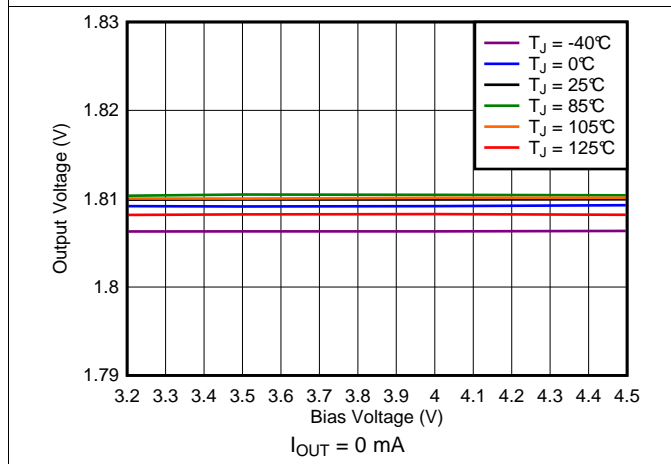


Figure 3.  $V_{BIAS}$  Line Regulation (No Load)

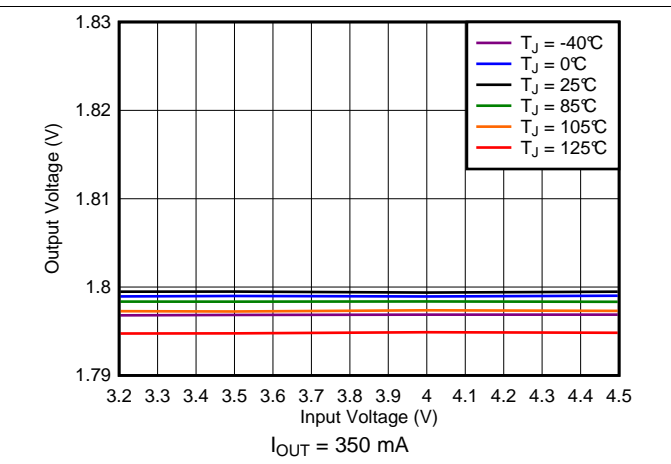


Figure 4.  $V_{BIAS}$  Line Regulation (350 mA)

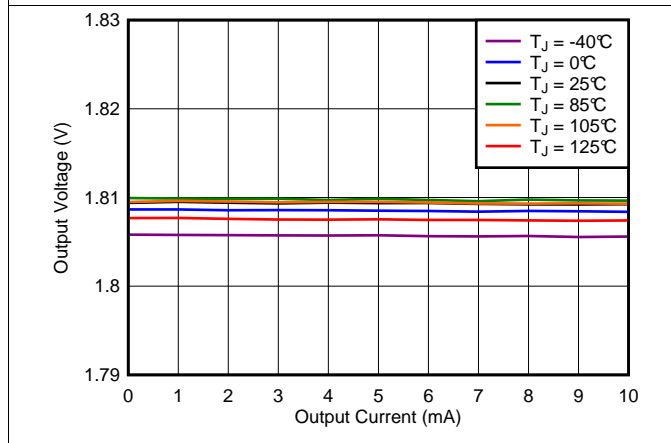


Figure 5. Load Regulation Under Light Loads

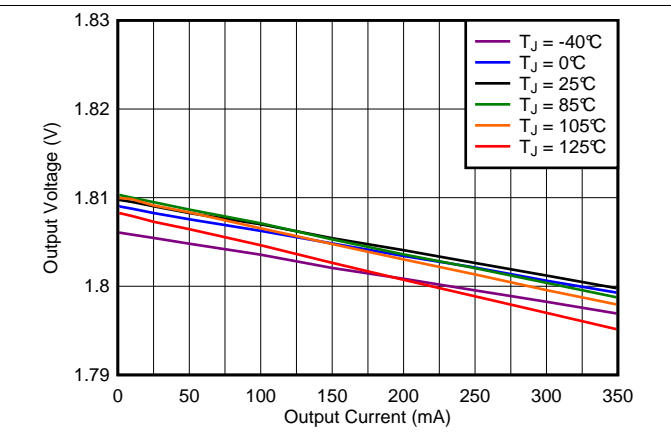


Figure 6. Load Regulation

Typical Characteristics (continued)

over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4\text{ V})$  or  $2.6\text{ V}$  (whichever is greater),  $V_{IN} = V_{OUT} + 0.5\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 1.1\text{ V}$ , and  $C_{OUT} = 2.2\text{ }\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^{\circ}\text{C}$

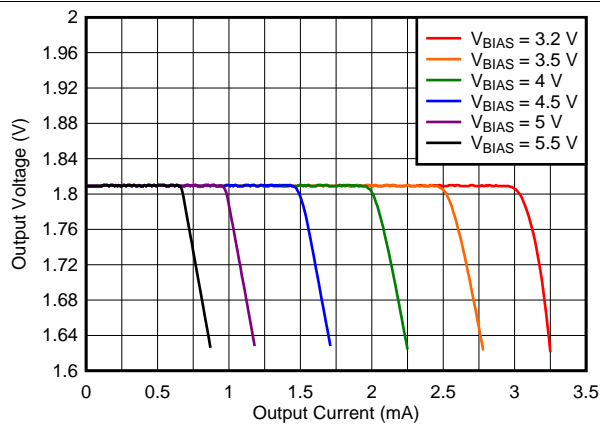


Figure 7. Load Regulation With  $V_{IN}$  Floating

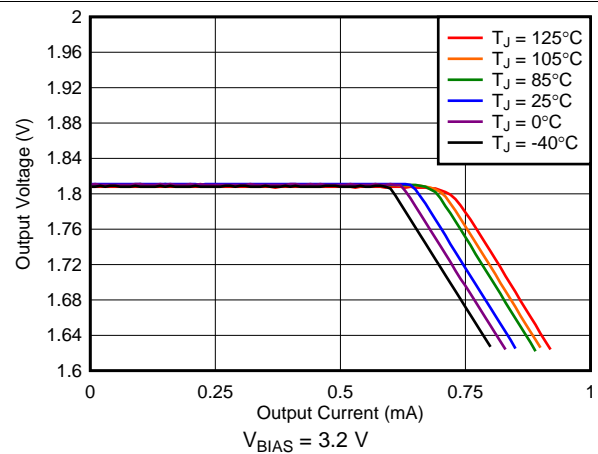


Figure 8. Load Regulation With  $V_{IN}$  Floating

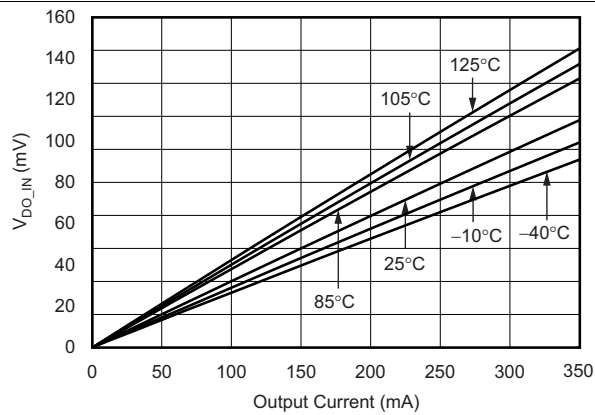


Figure 9.  $V_{IN}$  Dropout Voltage vs Output Current

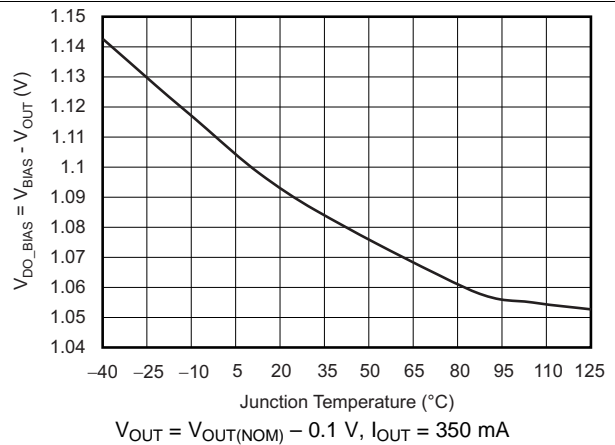


Figure 10.  $V_{BIAS}$  Dropout Voltage vs Junction Temperature

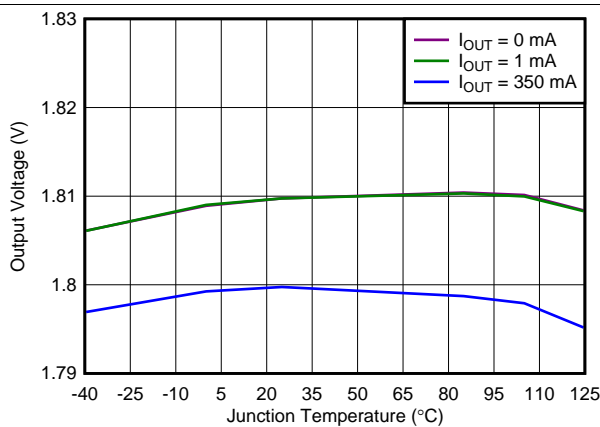


Figure 11. Output Voltage vs Junction Temperature

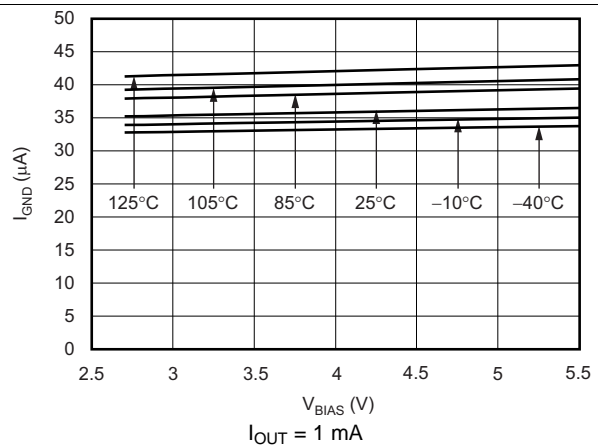


Figure 12. Ground Pin Current vs  $V_{BIAS}$  Voltage



Typical Characteristics (continued)

over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4 \text{ V})$  or  $2.6 \text{ V}$  (whichever is greater),  $V_{IN} = V_{OUT} + 0.5 \text{ V}$ ,  $I_{OUT} = 1 \text{ mA}$ ,  $V_{EN} = 1.1 \text{ V}$ , and  $C_{OUT} = 2.2 \mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

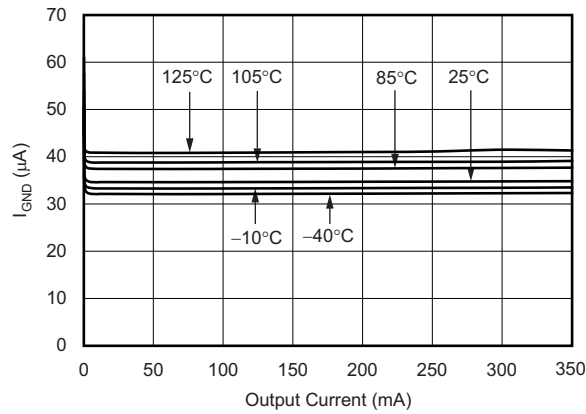


Figure 13. Ground Pin Current vs Output Current

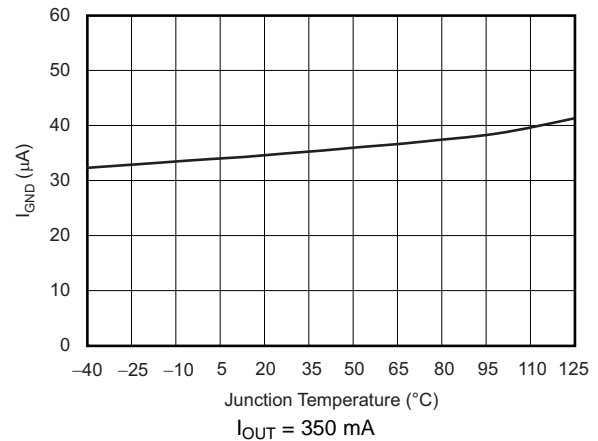


Figure 14. Ground Pin Current vs Junction Temperature

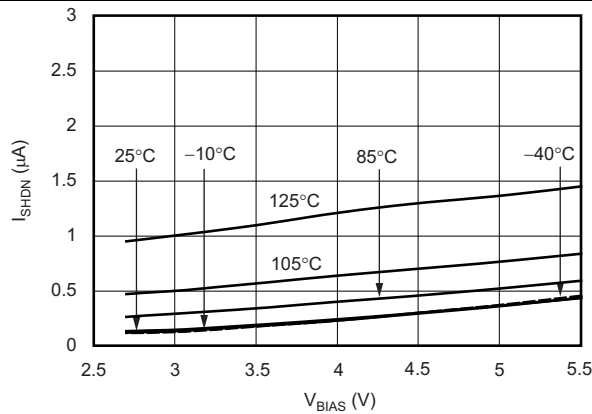


Figure 15. Shutdown Current vs  $V_{BIAS}$  Voltage

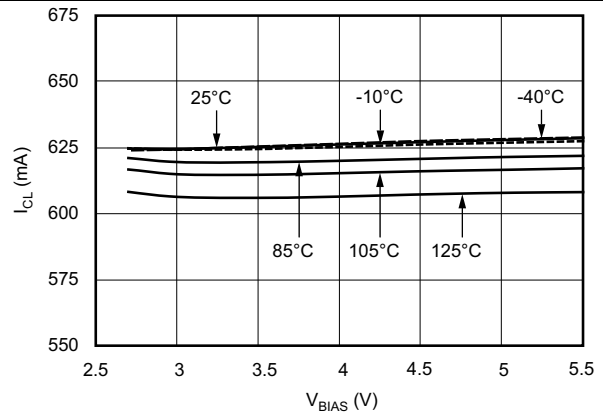


Figure 16. Current Limit vs  $V_{BIAS}$  Voltage

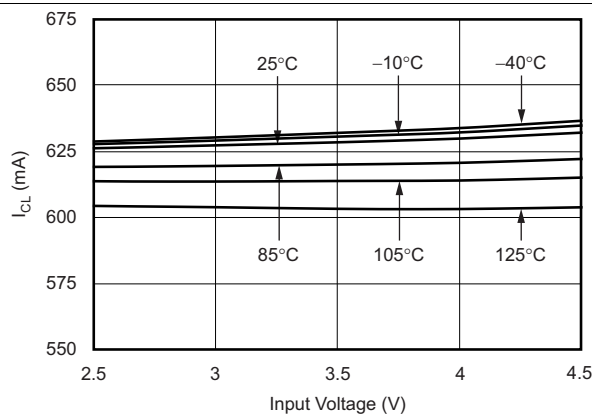


Figure 17. Current Limit vs Input Voltage

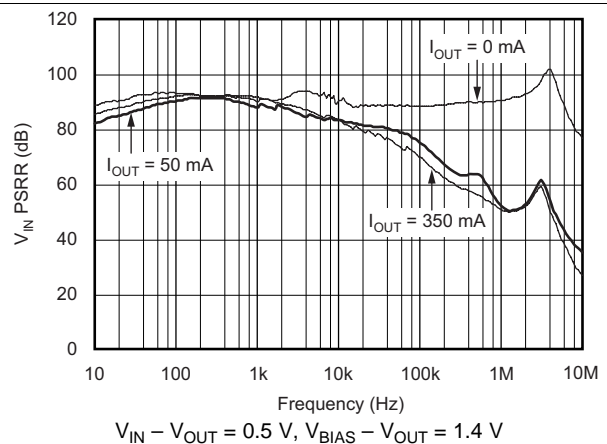


Figure 18.  $V_{IN}$  Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{BIAS} = (V_{OUT} + 1.4 \text{ V})$  or  $2.6 \text{ V}$  (whichever is greater),  $V_{IN} = V_{OUT} + 0.5 \text{ V}$ ,  $I_{OUT} = 1 \text{ mA}$ ,  $V_{EN} = 1.1 \text{ V}$ , and  $C_{OUT} = 2.2 \mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^{\circ}\text{C}$

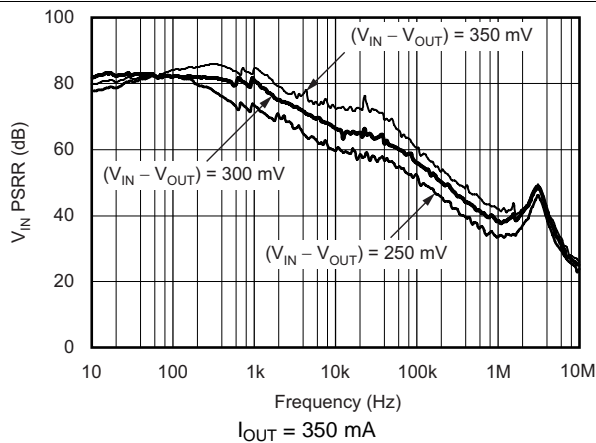


Figure 19.  $V_{IN}$  Power-Supply Rejection Ratio vs Frequency

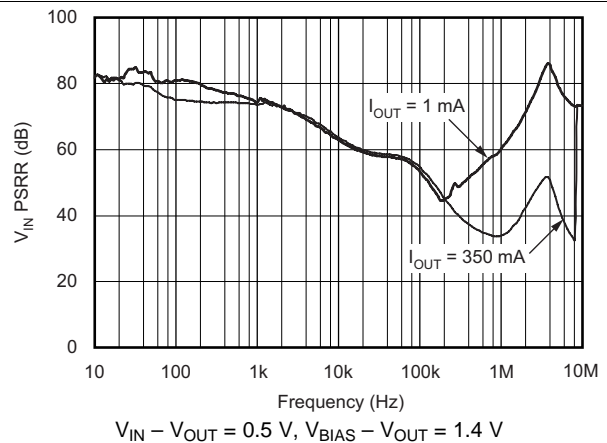


Figure 20.  $V_{BIAS}$  Power-Supply Rejection Ratio vs Frequency

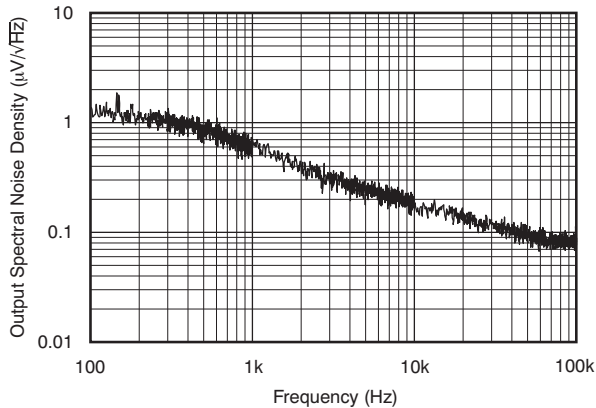
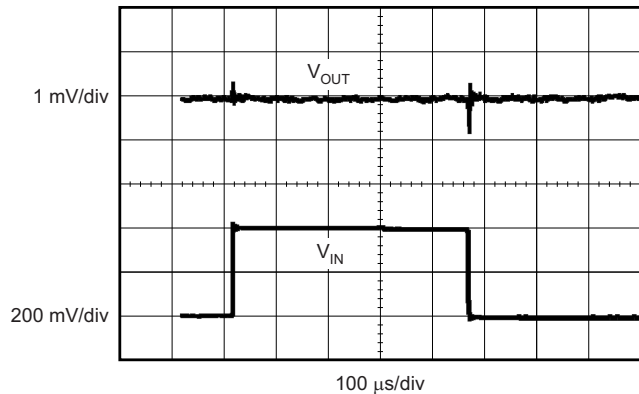
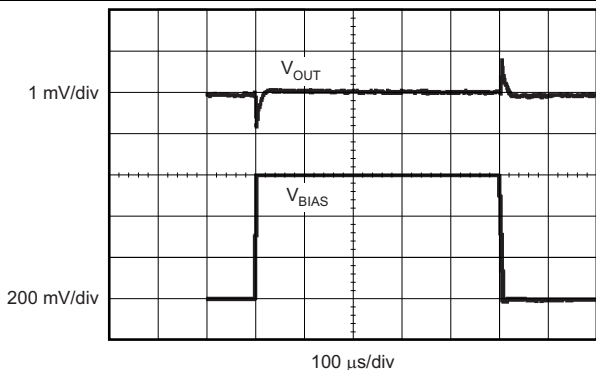


Figure 21. Output Spectral Noise Density vs Frequency



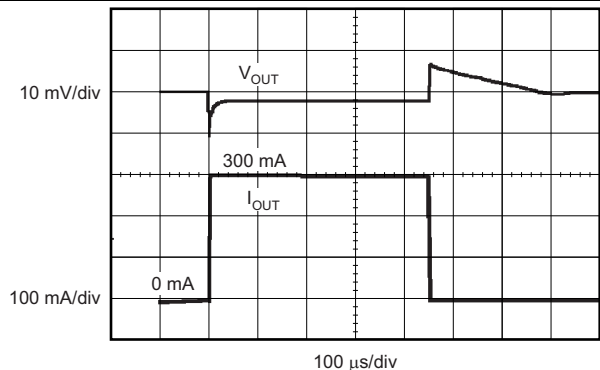
$V_{IN} = 2.1$  to  $2.5 \text{ V}$ ,  $V_{OUT} = 1.8 \text{ V}$ ,  $V_{BIAS} = 3.2 \text{ V}$ ,  $V_{IN}$  slew rate =  $1 \text{ V}/\mu\text{s}$ ,  $I_{OUT} = 350 \text{ mA}$

Figure 22.  $V_{IN}$  Line Transient Response



$V_{IN} = 2.3 \text{ V}$ ,  $V_{OUT} = 1.8 \text{ V}$ ,  $V_{BIAS} = 3.2 \text{ V}$  to  $3.8 \text{ V}$ ,  $V_{BIAS}$  slew rate =  $600 \text{ mV}/\mu\text{s}$ ,  $I_{OUT} = 350 \text{ mA}$

Figure 23.  $V_{BIAS}$  Line Transient Response



$V_{IN} = 2.3 \text{ V}$ ,  $V_{OUT} = 1.8 \text{ V}$ ,  $V_{BIAS} = 3.2 \text{ V}$ ,  $t_{RISE} = 1 \mu\text{s}$

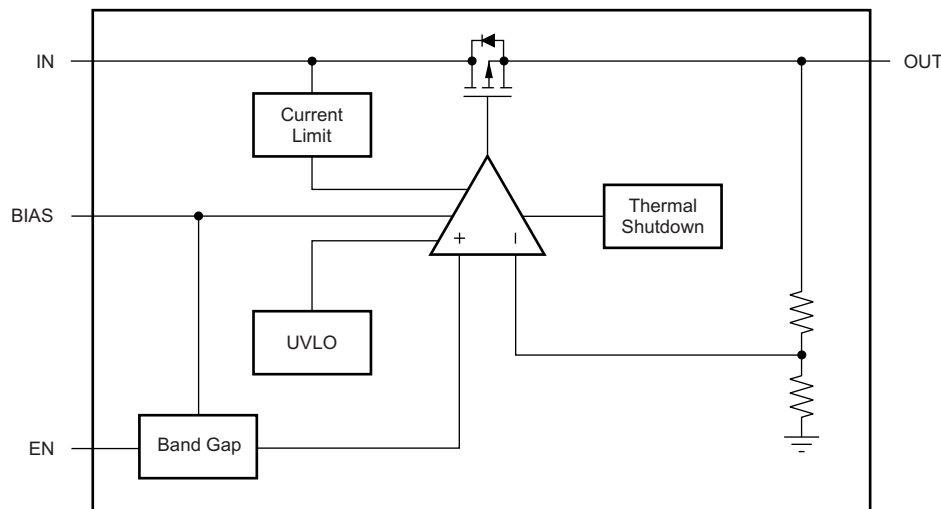
Figure 24. Load Transient Response

## 7 Detailed Description

### 7.1 Overview

The TPS720-Q1 family of LDO regulators uses innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1 MHz) at very low headroom ( $V_{IN} - V_{OUT}$ ). The implementation of the BIAS pin on the TPS720-Q1 vastly improves efficiency of low  $V_{OUT}$  applications by allowing the use of a pre-regulated, low-voltage input supply. The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads ( $< 500 \mu\text{A}$ ) when the IN pin is left floating. The light-load drive current is sourced from  $V_{BIAS}$  under this condition. This feature is particularly useful in power-saving applications where the dc-dc converter connected to the IN pin is disabled but the LDO is still required to regulate the voltage to a light load. These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Internal Current Limit

The TPS720-Q1 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is  $V_{OUT} = I_{LIMIT} \times R_{LOAD}$ . The NMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{OUT}$  until thermal shut down is triggered and the device is turned off. When the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Considerations](#) section for more details.

The NMOS pass element in the TPS720-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

#### 7.3.2 Inrush Current Limit

The TPS720-Q1 family of LDO regulators implements a novel inrush current limit circuit architecture: the current drawn through the IN pin is limited to a finite value. This  $I_{INRUSHLIMIT}$  charges the output to its final voltage. All current drawn through  $V_{IN}$  charges the output capacitance when the load is disconnected. [Equation 1](#) shows the inrush current limit performed by the circuit.

$$I_{INRUSHLIMIT}(A) = C_{OUT}(\mu F) \times 0.0454545 (V/\mu s) + I_{LOAD}(A) \quad (1)$$

## Feature Description (continued)

Assuming a  $C_{OUT}$  of 2.2  $\mu\text{F}$  with the load disconnected (that is,  $I_{LOAD} = 0$ ), the  $I_{INRUSHLIMIT}$  is calculated to be 100 mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3 V, then the LDO charges the output capacitor to the final output value in approximately 28.6  $\mu\text{s}$ .

Another consideration is when a load is connected to the output of an LDO. The TPS720-Q1 inrush current limit circuit employs a technique that supplies not only the  $I_{INRUSHLIMIT}$ , but also the additional current required by the load. If  $I_{LOAD} = 350$  mA, then  $I_{INRUSHLIMIT}$  calculates to be approximately 450 mA (from [Equation 1](#)).

### 7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

### 7.3.4 Undervoltage Lockout (UVLO)

The TPS720-Q1 uses an undervoltage lockout circuit on the BIAS pin to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature that typically ignores undershoot transients on the input if these transients are less than 50  $\mu\text{s}$  in duration.

## 7.4 Device Functional Modes

Driving the EN pin over 1.1 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 500 nA, typically.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Input and Output Capacitor Requirements

Although a capacitor is not required for stability on the IN pin, good analog design practice is to connect a 0.1- $\mu\text{F}$  to 1- $\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located far from the power source. If source impedance is not sufficiently low, a 0.1- $\mu\text{F}$  input capacitor may be necessary to ensure stability.

The BIAS pin does not require an input capacitor because BIAS does not source high currents. However, if source impedance is not sufficiently low, then a small 0.1- $\mu\text{F}$  bypass capacitor is recommended.

The TPS720-Q1 is designed to be stable with standard ceramic capacitors with values of 2.2  $\mu\text{F}$  or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 250 m $\Omega$ .

#### 8.1.2 Output Regulation With the IN Pin Floating

The TPS720-Q1 supports a novel feature where the output of the LDO regulates under light loads when the IN pin is left floating. Under normal conditions when the IN pin is connected to a power source, the BIAS pin draws only tens of milliamperes. However, when the IN pin is floating, an innovative circuit is used that allows a maximum current of 500  $\mu\text{A}$  to be drawn by the load through the BIAS pin and maintains the output in regulation. This feature is particularly useful in power-saving applications where a dc-dc converter connected to the IN pin is disabled, but the LDO is required to regulate the output voltage to a light load.

Figure 25 shows an application example where a microcontroller is not turned off (to maintain the state of the internal memory), but where the regulated supply (shown as the TPS62xxx) is turned off to reduce power. In this case, the TPS720-Q1 BIAS pin provides sufficient load current to maintain a regulated voltage to the microcontroller.

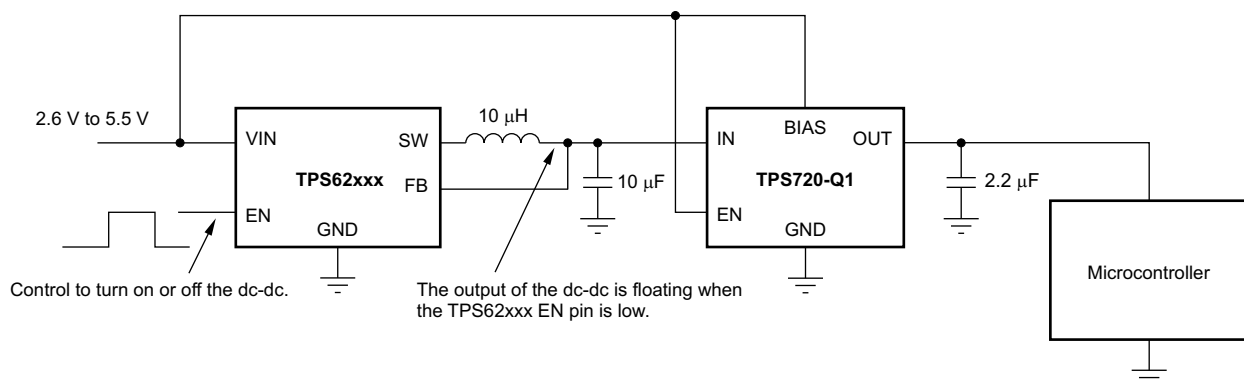


Figure 25. Floating IN Pin Regulation Example

## Application Information (continued)

### 8.1.3 Dropout Voltage

The TPS720-Q1 uses a NMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the NMOS pass element.  $V_{DO}$  approximately scales with output current because the NMOS device behaves as a resistor in dropout.

PSRR and transient response are degraded when  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in [Figure 19](#).

### 8.1.4 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

### 8.1.5 Minimum Load

The TPS720-Q1 is stable with no output load. Although some LDOs suffer from low loop gain at very light output loads, the TPS720-Q1 employs an innovative, low-current mode circuit under very light or no-load conditions thereby improving output voltage regulation performance.

## 8.2 Typical Application

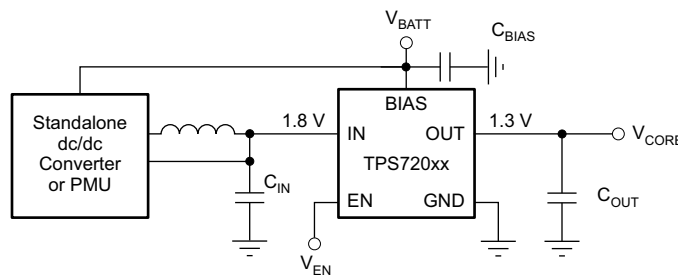


Figure 26. Typical Application Schematic (TDB update)

### 8.2.1 Design Requirements

[Table 1](#) shows the parameters for this design example.

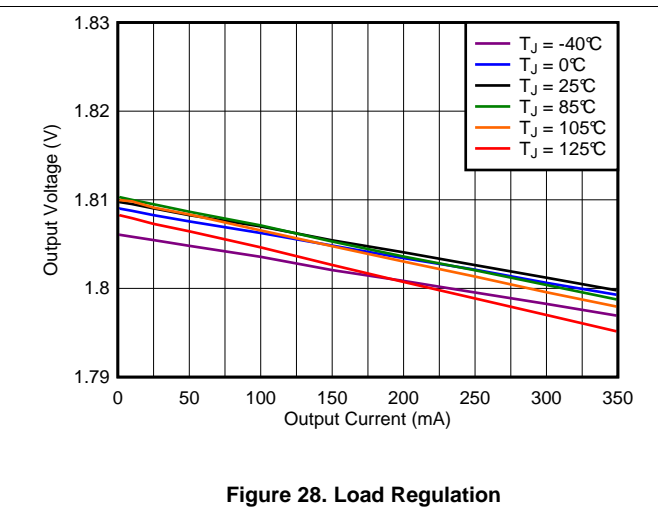
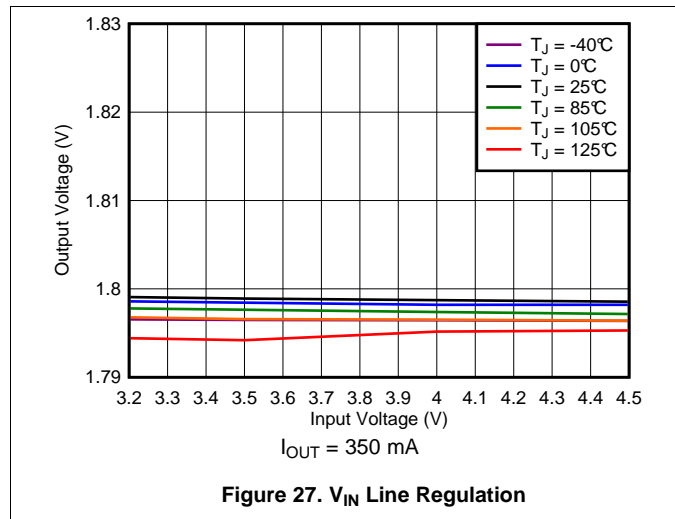
Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{IN}$	2.3 V
$V_{BIAS}$	3.2 V
$V_{OUT}$	1.8 V
$I_{OUT}$	10-mA typical, 350-mA peak

### 8.2.2 Detailed Design Procedures

Select the minimum recommended component size because a small-size solution is desired in this design example. Set  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 100 \text{ nF}$ , and  $C_{OUT} = 2.2 \mu\text{F}$ .

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

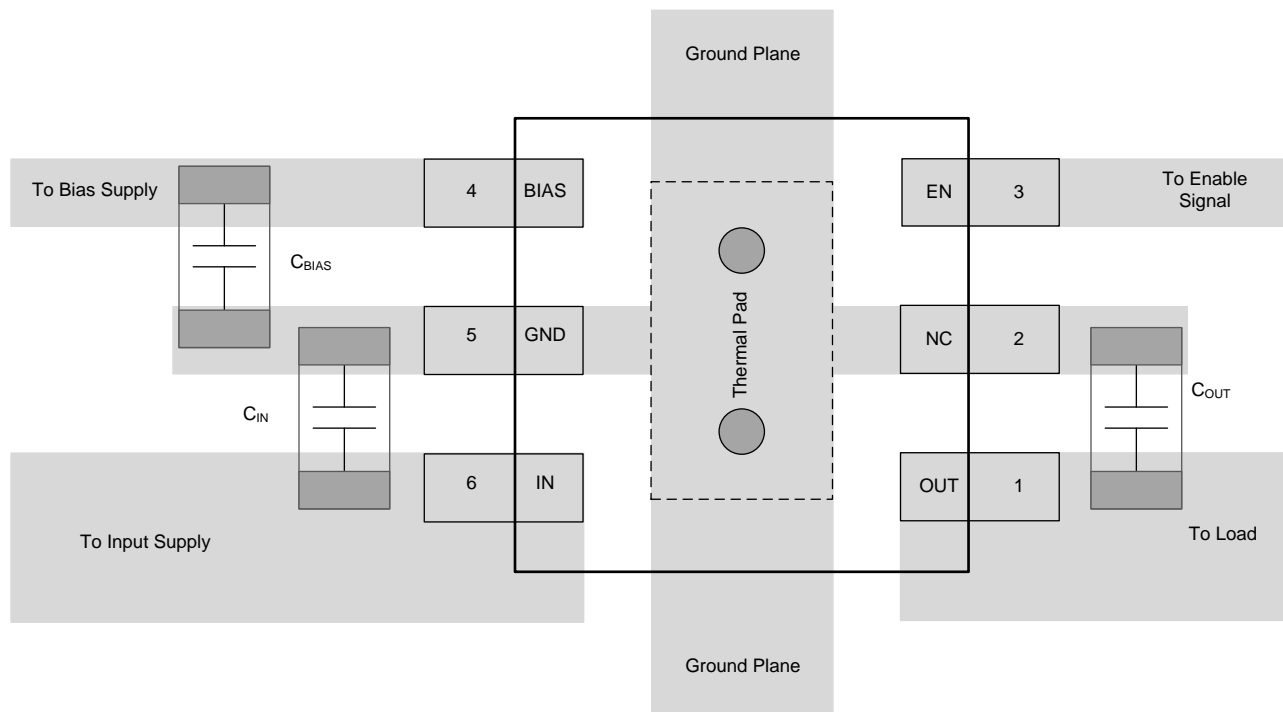
The input supply and bias supply for the LDO must be within its recommended operating conditions and must provide adequate headroom for the device to have a regulated output. The minimum capacitor requirements must be met, and if the input supply is noisy, then additional input capacitors with low ESR can help improve transient performance.

## 10 Layout

### 10.1 Layout Guidelines

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for  $V_{IN}$  and  $V_{OUT}$  is recommended with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. High equivalent series resistance (ESR) capacitors can degrade PSRR. The BIAS pin draws very little current and can be routed as a signal (make sure to shield the BIAS pin from high-frequency coupling).

### 10.2 Layout Example



**Figure 29. Recommended Layout**



### 10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS720-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS720-Q1 into thermal shutdown degrades device reliability.

### 10.4 Power Dissipation

The printed-circuit-board (PCB) area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ), as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS720-Q1. The [TPS720xxDRVEVM evaluation module](#) (and [related user guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

#### 11.1.2 Device Nomenclature

**Table 2. Device Nomenclature<sup>(1)(2)</sup>**

PRODUCT	V <sub>OUT</sub>
TPS720xx(x)QyyyzQ1	<p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V).</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for 3000 pieces, T is for 250 pieces.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.9 V to 3.0 V in 50-mV increments are available. Contact the factory for details and availability.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- TPS6200x-Q1 Data Sheet, [SGLS243](#)
- *TPS720xxDRVEVM Evaluation Module*, [SBVU024](#)
- *Using New Thermal Metrics*, [SBVA025](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72009QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11P	<a href="#">Samples</a>
TPS72010QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11Q	<a href="#">Samples</a>
TPS72011QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11I	<a href="#">Samples</a>
TPS72012QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11R	<a href="#">Samples</a>
TPS72015QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11J	<a href="#">Samples</a>
TPS72018QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11K	<a href="#">Samples</a>
TPS72025QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11W	<a href="#">Samples</a>
TPS720285QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11M	<a href="#">Samples</a>
TPS72028QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11L	<a href="#">Samples</a>
TPS72029QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11N	<a href="#">Samples</a>
TPS72030QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	11O	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

---

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS720-Q1 :**

- Catalog: [TPS720](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
- (D) The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

## THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

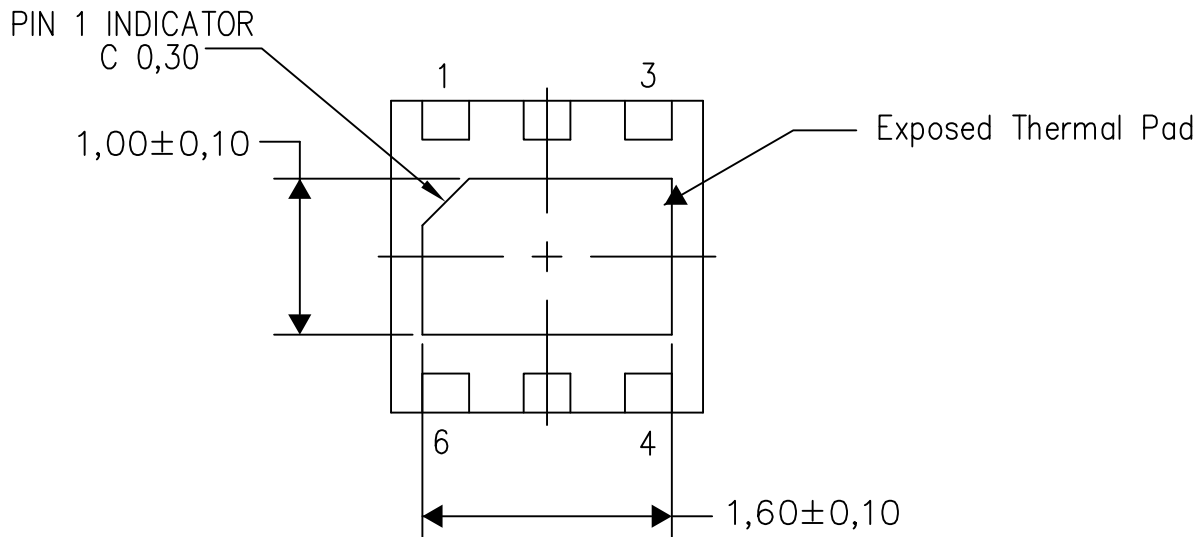
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

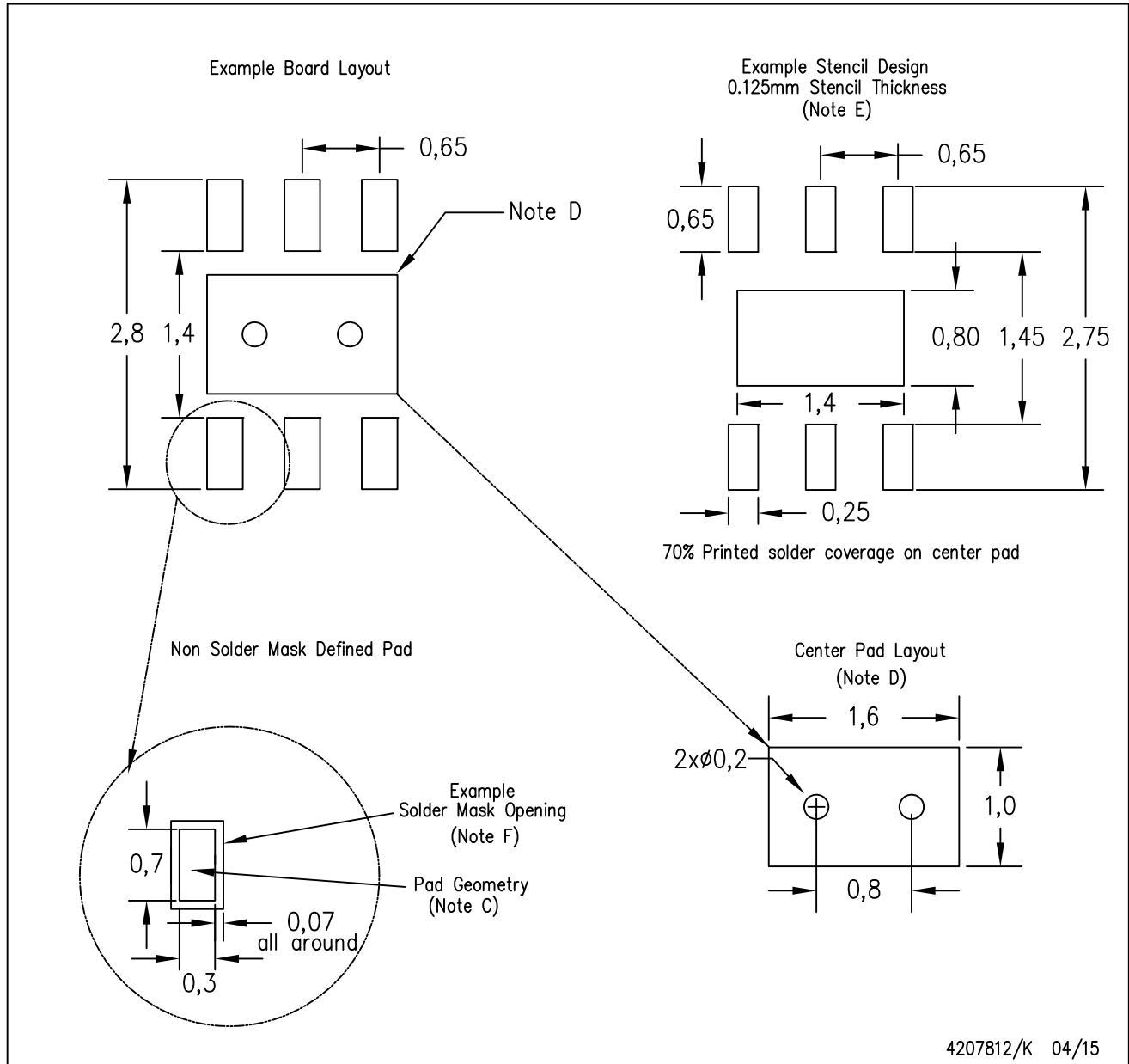
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.



## IMPORTANT NOTICE

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