TPS65321-Q1 36-V Step-Down Converter With Eco-mode™ and LDO Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- One High-VIN Step-Down DC-DC Converter
  - Input Range of 3.6-V to 36-V
  - 250-mΩ High-Side MOSFET
  - Maximum Load Current 3.2-A, Output Adjustable 1.1-V to 20-V
  - Adjustable Switch-Mode Frequency 100-kHz to 2.5-MHz
  - Synchronizes to External Clock
  - Maximum 140-µA Operating Quiescent Current
    - High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme
  - Reset Output-Pin (Active Low, Open-Drain)
- One High-VIN Low-Dropout (LDO) Voltage Regulator
  - Input Range of 3-V to 36-V
  - 280-mA Current Capability With Typical 35-µA Operating Quiescent Current in No-Load Condition
  - Low-Dropout Voltage of 300-mV at I_O = 200-mA (Typical)
- Overcurrent Protection for Both Regulators
- Overtemperature Protection
- 14-Pin HTSSOP Package With PowerPAD™ Integrated Circuit Package

2 Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Telematics, eCall
- 12-V and 24-V Industrial and Commercial Low Power System

3 Description

The TPS65321-Q1 device is a combination of a high-VIN DC-DC step-down converter, referred to as the buck regulator, with an adjustable switch-mode frequency from 100-kHz to 2.5-MHz, and a high-VIN 280-mA low-dropout (LDO) regulator. The input range is 3.6-V to 36-V for the buck regulator, and 3-V to 36-V for the LDO regulator. The buck regulator has an integrated high-side MOSFET and an active-low, open-drain power-good output-pin (nRST). The LDO regulator also has an integrated MOSFET and features a low-input supply current of 35-µA typical in no-load condition. The low-voltage tracking feature enables the TPS65321-Q1 device to track the input supply during cold-crank conditions.

The buck regulator provides a flexible design to fit system needs. The external loop compensation circuit allows for optimization of the converter response for the appropriate operating conditions. A low-ripple pulse-skip mode reduces the no-load input-supply current to maximum 140-µA.

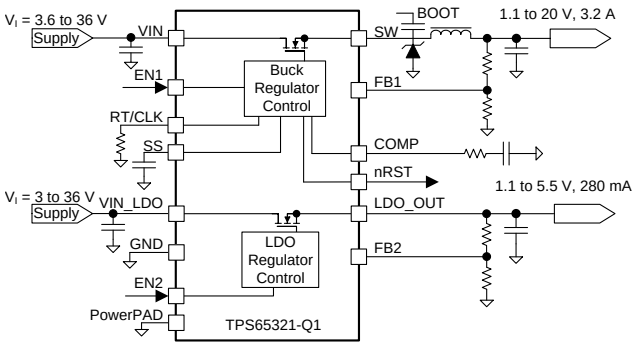
The device has built-in protection features such as soft start, current-limit, thermal sensing, and shutdown because of excessive power dissipation. Furthermore, the device has an internal undervoltage-lockout (UVLO) function that turns off the device when the supply voltage is too low.

Device Information(1)

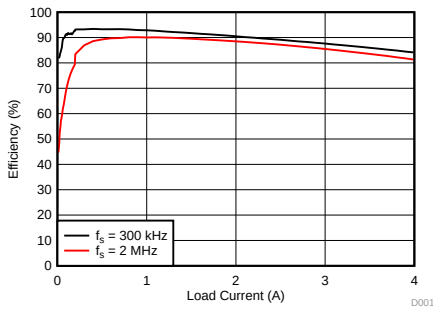
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65321-Q1	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Buck Efficiency Versus Output Current



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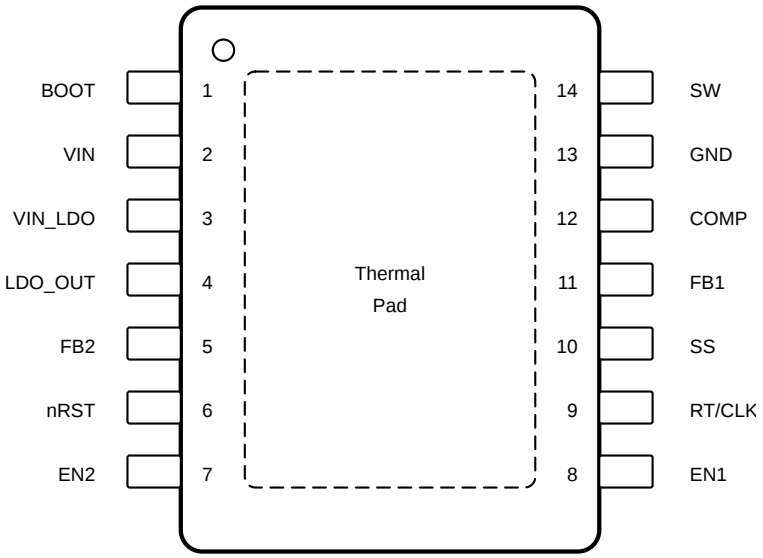
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2015) to Revision A	Page
• Changed the device status from *Product Preview* to *Production Data*	1

5 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between the BOOT and SW pins to supply the bias voltage for the integrated high-side MOSFET.
COMP	12	O	The COMP pin is the error-amplifier output of the buck regulator, and the input to the output switch-current comparator of the buck regulator. Connect frequency-compensation components to the COMP pin.
EN1	8	I	The EN1 pin is the enable and disable input for the buck regulator (high-voltage tolerant) and is internally pulled to ground. Pull this pin up externally to enable the buck regulator.
EN2	7	I	The EN2 pin is the enable and disable input for the LDO regulator (high-voltage tolerant) and is internally pulled to ground. Pull this pin up externally to enable the LDO regulator.
FB1	11	I	The FB1 pin is the feedback pin of the buck regulator. Connect an external resistive divider between the buck regulator output, the FB2 pin, and the GND pin to set the desired output voltage of the buck regulator.
FB2	5	I	The FB2 pin is the feedback pin of the LDO regulator. Connect an external resistive divider between the LDO_OUT pin, the FB2 pin, and the GND pin to set the desired output voltage of the LDO regulator.
GND	13	—	This pin is the ground pin.
LDO_OUT	4	O	This pin is the LDO regulator output.
nRST	6	O	The nRST pin is the active low, open drain reset output of the buck regulator. Connect this pin with an external bias voltage through an external resistor. This pin is asserted high after the buck regulator begins regulating.
RT/CLK	9	I	Connect this pin to an external resistor to ground to program the switching frequency of the buck regulator. An alternative option is to feed an external clock to provide a reference for the switching frequency of the buck regulator.
SS	10	I	Connect this pin to an external capacitor to ground which sets the soft-start time of the buck regulator.
SW	14	I	The SW pin is the source node of the internal high-side MOSFET of the buck regulator.
VIN	2	—	The VIN pin is the input supply pin for the internal biasing and high-side MOSFET of the buck regulator.
VIN_LDO	3	—	The VIN_LDO pin is the input supply pin for the LDO regulator.
Exposed PowerPAD		—	Electrically connect the PowerPAD to ground and solder to the ground plane of the PCB for thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply inputs	VIN	–0.3	40	V
	VIN_LDO	–0.3	40	
Control	EN1, EN2	–0.3	40	V
	EN1-VIN, EN2-VIN		1	
Buck converter	FB1	–0.3	3.6	V
	SW	–0.3 –2 V for 30 ns	40	
	BOOT	–0.3	46	
	BOOT-SW		8	
	COMP	–0.3	3.6	
	SS	–0.3	3.6	
	RT/CLK, SS	–0.3	3.6	
	nRST	–0.3	7	
LDO regulator	LDO_OUT	–0.3	7	V
	FB2	–0.3	7	
Operating ambient temperature, T_A			125	°C
Operating junction temperature range, T_J		–40	150	
Storage temperature, T_{stg}		–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 — All pins	±500	
		Charged-device model (CDM), per AEC Q100-011 — Corner pins (1, 7, 8, and 14)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply inputs	VIN	3.6	36	V
	VIN_LDO	3	36	
Buck regulator	BOOT1	3.6	42	V
	SW1	–1	36	
	VFB1	0	0.8	
	SS	0	3	
	COMP	0	3	
	RT/CLK	0	3	
	nRST	0	5.25	
LDO regulator	LDO_OUT	1.1	5.5	V
	VFB2	0	0.8	
Control	EN1	0	36	V
	EN2	0	36	
Temperature	Operating junction temperature range, T_J	–40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS65321-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_I = 6 V to 27 V, EN1 = EN2 = V_I, over-operating free-air temperature range T_A = –40°C to 125°C and maximum operating junction temperature T_J = –150°C, unless otherwise noted. V_I is the voltage on the battery-supply terminals, VIN and VIN_LDO.

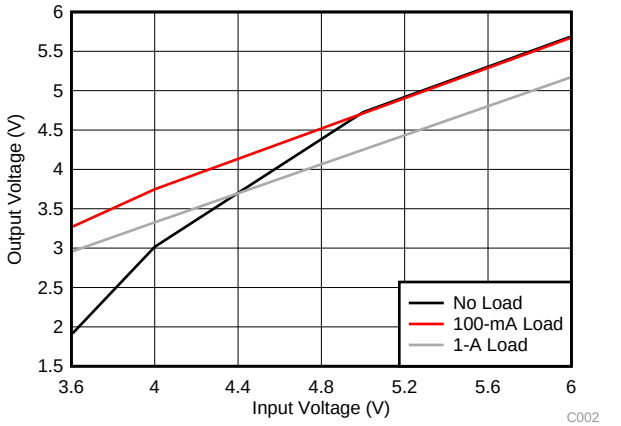
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN (INPUT POWER SUPPLY)						
	Operating input voltage	Normal mode, after initial start-up	3.6	12	36	V
	Shutdown supply current	$V_{(EN1)}$ = $V_{(EN2)}$ = 0 V, 25°C		2	7	µA
	Initial start-up voltage		6		36	V
ENABLE AND UVLO (EN1 AND EN2 TERMINALS)						
	Enable low level				0.7	V
	Enable high level		2.5			V
$V_{(VIN)(f)}$	Internal UVLO falling threshold	Ramp $V_{(VIN)}$ down until output turns OFF	1.8	2.6	3	V
$V_{(VIN)(r)}$	Internal UVLO rising threshold	Ramp $V_{(VIN)}$ up until output turns ON	2.2	2.8	3.2	V
BUCK REGULATOR						
$I_{(Qon)}$	Operating: non-switching supply	Measured at the VIN terminal $V_{(FB1)}$ = 0.83 V, $V_{(VIN)}$ = 12 V, 25°C		110	140	µA
	Output capacitance	ESR = 0.001 Ω to 0.1 Ω, large output capacitance may be required for load transient	10			µF
$V_{(ref1)}$	Voltage reference for FB1 terminal	Buck regulator output: 1.1 V to 20 V. Buck regulator in Continuous Conducting Mode without Pulse-Skipping	0.788	0.8	0.812	V
	DC output voltage accuracy	Includes voltage references, DC load and line regulation, process and temperature	–2%		2%	
$DC_{(LDR)}$	DC Load regulation, ΔV_{OUT} / V_{OUT}	I_{OUT} = 0 to I_{OUTmax}		0.5%		
$T_{(LDSR)}$	Transient load step response	$V_{(VIN)}$ = 12V, I_{OUT} = 200 mA to 3A, T_R = T_F = 1 µs, Buck Output Voltage = 5V, f_S = 2 MHz		5%		
BUCK REGULATOR: HIGH-SIDE MOSFET						
$r_{(DS(on)\ HS\ FET)}$	On-resistance	$V_{(VIN)}$ = 12 V, $V_{(SW)}$ = 6 V		127	250	mΩ
t_{on}min	Minimum on-time	f_S = 2.5 MHz		115		ns
BUCK REGULATOR: CURRENT-LIMIT						
	Current-limit threshold	$V_{(VIN)}$ = 12 V, T_J = 25°C	4	6		A
BUCK REGULATOR: TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK TERMINAL)						
f_S	Switching-frequency range using RT mode		100		2500	kHz
	Switching frequency	Under fixed-frequency PWM mode, with 200 kΩ connected between terminal RT/CLK and GND	523	585	640	kHz
	Switching-frequency range using CLK mode		300		2200	kHz
	Minimum CLK input pulse width	Measures at CLK input = 2.2 MHz		30		ns
RT/CLK	High threshold			1.9	2.2	V
RT/CLK	Low threshold		0.5	0.7		V
RT/CLK	Falling edge to SW rising edge delay	Measured at 500 kHz with external clock connected to RT/CLK terminal		60		ns
PLL	Lock-in time	Measured at 500 kHz		100		µs
LDO REGULATOR						
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{(VIN\_LDO)}$ = 6 V to 30 V, $I_{(LDO\_OUT)}$ = 10 mA, $V_{(LDO\_OUT)}$ = 3.3 V			20	mV
$\Delta V_{O(\Delta IL)}$	Load regulation	$I_{(LDO\_OUT)}$ = 10 mA to 200 mA, $V_{(VIN\_LDO)}$ = 12 V, $V_{(LDO\_OUT)}$ = 3.3 V			35	mV
$V_{DROPOUT}$	Dropout voltage ($V_{(VIN\_LDO)}$ – $V_{(LDO\_OUT)}$)	$I_{(LDO\_OUT)}$ = 200 mA		300	450	mV
$I_{(LDO\_OUT)}$	Output current	$V_{(LDO\_OUT)}$ in regulation, $V_{(VIN)}$ ≥ 4V			280	mA
$V_{I(VIN\_LDO)}$	Operating input voltage on VIN_LDO terminal	$V_{(LDO\_OUT)}$ in regulation	3		36	V
$V_{(ref2)}$	Voltage reference FB2 terminal	$V_{(LDO\_OUT)}$ = 1.1 V to 5.5 V	0.788	0.8	0.812	V
$I_{CL(LDO\_OUT)}$	Output current-limit	$V_{(LDO\_OUT)}$ = 0 V (the LDO_OUT terminal is shorted to ground)	280		1000	mA

Electrical Characteristics (continued)

V_I = 6 V to 27 V, EN1 = EN2 = V_I, over-operating free-air temperature range T_A = –40°C to 125°C and maximum operating junction temperature T_J = –150°C, unless otherwise noted. V_I is the voltage on the battery-supply terminals, VIN and VIN_LDO.

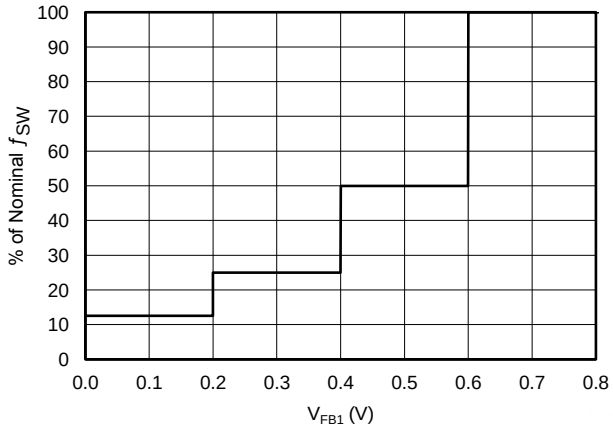
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(LDO)}$	Quiescent current	$V_{(VIN)}$ = 12 V; Measured at VIN pin $V_{(EN1)}$ = 0 V, $V_{(EN2)}$ = 5 V, $I_{(LDO\_OUT)}$ = 0.01 mA to 0.75 mA		35	50	µA
PSRR	Power supply ripple rejection	$V_{(VIN\_LDO)(rip)}$ = 0.5 V_{PP}, $I_{(LDO\_OUT)}$ = 200 mA, frequency (f) = 100 Hz, $V_{(LDO\_OUT)}$ = 5 V and $V_{(LDO\_OUT)}$ = 3.3 V		60		dB
		$V_{(VIN\_LDO)(rip)}$ = 0.5 V_{PP}, $I_{(LDO\_OUT)}$ = 200 mA, f = 150 kHz, $V_{(LDO\_OUT)}$ = 5 V and $V_{(LDO\_OUT)}$ = 3.3 V		30		dB
$C_{(LDO\_OUT)}$	Output capacitor	ESR = 0.001 Ω to 100 mΩ, large output capacitance may be required for load transient $V_{(LDO\_OUT)}$ ≥ 3.3 V	1		40	µF
$C_{(LDO\_OUT)}$	Output capacitor	ESR = 0.001 Ω to 100 mΩ, large output capacitance may be required for load transient 1.2 V ≤ $V_{(LDO\_OUT)}$ < 3.3 V	20		40	µF
BUCK REGULATOR: RESET (nRST TERMINAL)						
	RESET threshold	$V_{(FB1)}$ decreasing	85%	90%	95%	
V_{OL}	Output low	nRST terminal asserted low due to falling $V_{(FB1)}$, < 1-mA sinking current into nRST terminal	0	0.045	0.4	V
	Filter time	Delay before asserting nRST low	7	14	21	µs
OVER TEMPERATURE PROTECTION						
T_{SD}	Thermal-shutdown trip point			175		ºC
T_{hys}	Hysteresis			10		ºC

6.6 Typical Characteristics



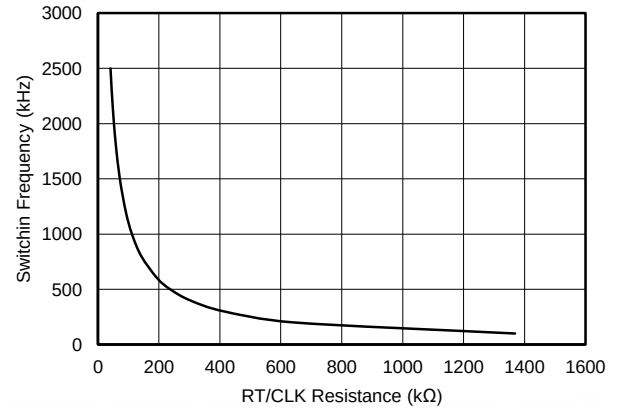
f_S = 2 MHz 3.6 V ≤ $V_{(VIN)}$ ≤ 6 V

Figure 1. Maximum-Possible Buck-Regulator Output Voltage



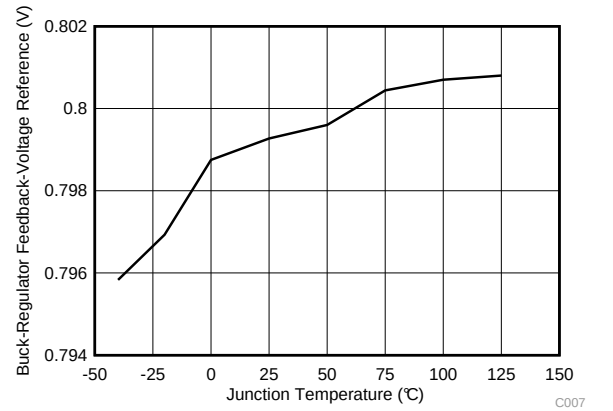
$V_{(VIN)}$ = 12 V

Figure 2. Buck-Regulator Switching Frequency vs $V_{(FB1)}$ Feedback Voltage



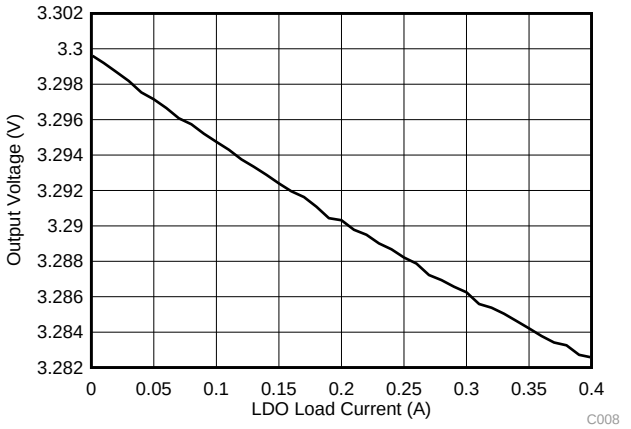
$V_{(VIN)}$ = 12 V T_J = 25°C

Figure 3. Buck-Regulator Switching Frequency vs RT_CLK Resistance



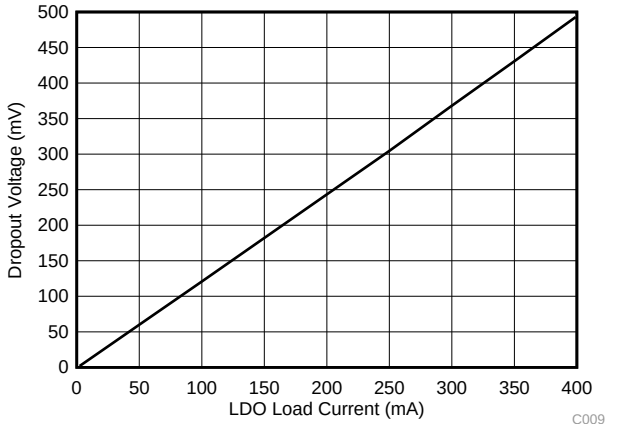
No Load $V_{(VIN)}$ = 12 V

Figure 4. Buck-Regulator Feedback-Voltage Reference ($V_{(FB1)}$) vs Junction Temperature



$V_{(VIN\_LDO)}$ = 5 V $V_{(LDO\_OUT)}$ = 3.3 V

Figure 5. LDO-Regulator Load Regulation



$V_{(LDO\_OUT)}$ = 5 V

Figure 6. LDO-Regulator Dropout Voltage vs Load Current

Typical Characteristics (continued)

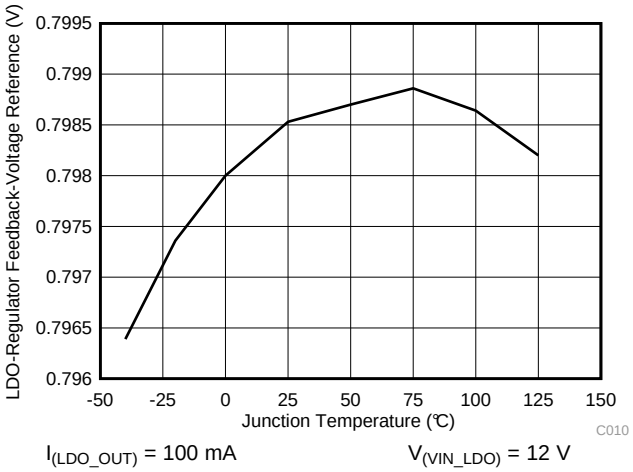


Figure 7. LDO-Regulator Feedback-Voltage Reference ($V_{(FB2)}$) vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS65321-Q1 device is a 36-V, 3.2-A, DC-DC step-down converter (also referred to as a buck regulator) with a 280-mA low-dropout (LDO) linear regulator. Both of these regulators have low quiescent consumption during a light load to prolong battery life.

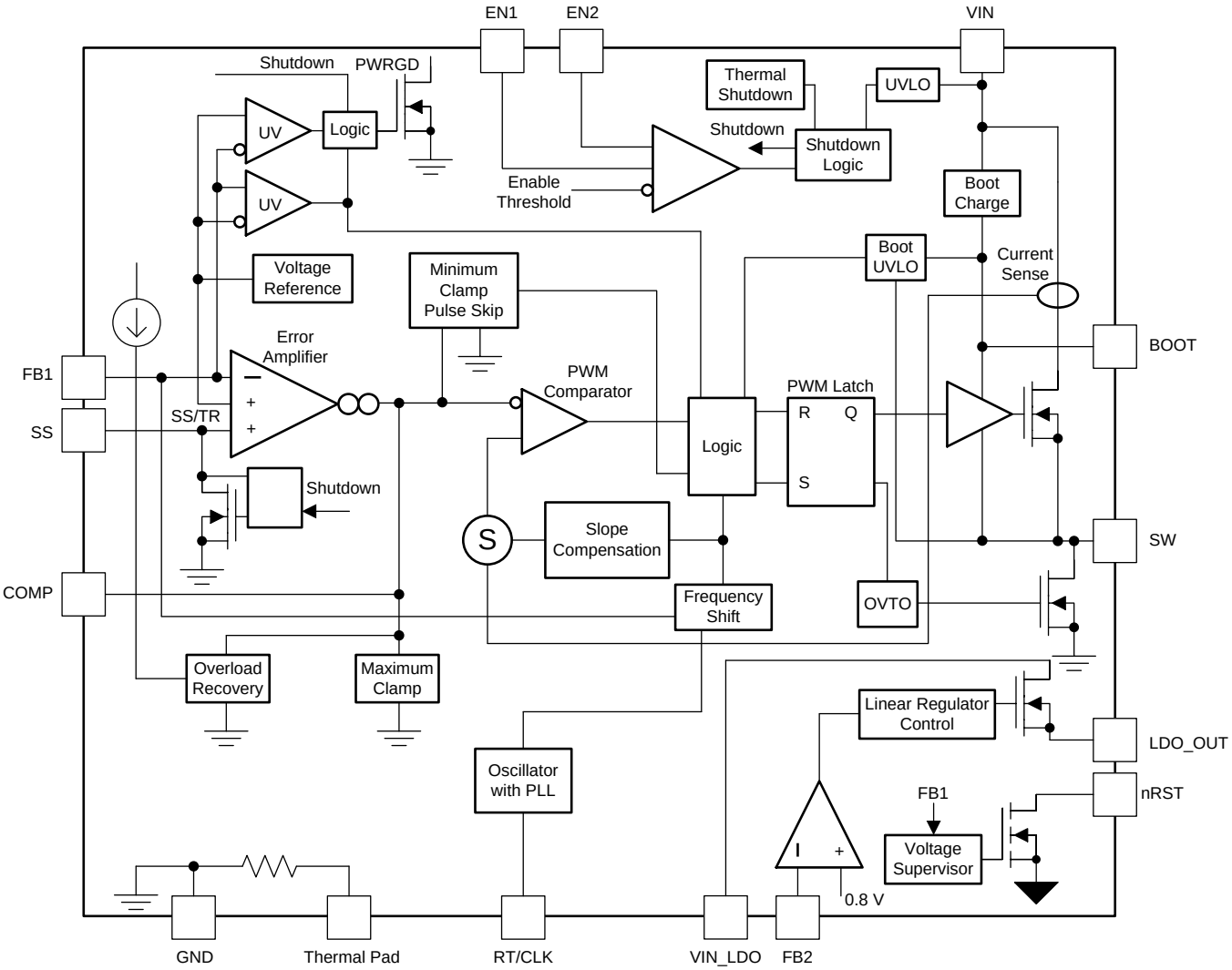
The buck regulator improves performance during line and load transients by implementing a constant-frequency and current-mode control (CCM) that reduces output capacitance which simplifies external frequency-compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output-filter components. The switching frequency is adjusted by using a resistor to ground on the RT/CLK pin. The buck regulator has an internal phase-locked loop (PLL) on the RT/CLK pin that synchronizes the power-switch turnon to the falling edge of an external system clock.

The TPS65321-Q1 device reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT pin and the SW pin supplies the bias voltage for the integrated high-side MOSFET. The TPS65321-Q1 device can operate at high duty cycles under the dropout mode operation. The output voltage can step-down to as low as the 0.8-V reference. The soft start minimizes inrush currents and provides power-supply sequencing during power up. Connect a small-value capacitor to the pin to adjust the soft-start time. For critical power-supply sequencing requirements couple a resistor divider to the pin.

The LDO regulator consumes only about a 35-µA current in light load. The LDO regulator also tracks the battery when the battery voltage is low (in a cold-crank condition).

The buck regulator of the TPS65321-Q1 device has a power-good open-drain output (nRST) that asserts low when the regulated output voltage is less than 90% (typical) of the nominal output voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Buck Regulator

7.3.1.1 Fixed-Frequency PWM Control

The TPS65321-Q1 buck regulator uses an adjustable, fixed-frequency peak current-mode control. An internal voltage reference compares the output voltage through external resistors on the FB1 pin to an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The device compares the error amplifier output to the high-side power-switch current. When the power-switch current reaches the level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the COMP pin voltage to a maximum level.

7.3.1.2 Slope Compensation Output

The TPS65321-Q1 buck regulator adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations. The available peak-inductor current remains constant over the full duty-cycle range.

7.3.1.3 Pulse-Skip Eco-mode™ Control Scheme

The TPS65321-Q1 buck regulator operates in a pulse-skip mode at light load currents to improve efficiency by reducing switching and gate-drive losses. The design of the TPS65321-Q1 buck regulator is such that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping-current threshold, the buck regulator enters pulse-skip mode. This current threshold is the current level corresponding to a nominal COMP voltage, or 720 mV. The current at which entry to the pulse-skip mode occurs depends on switching frequency, inductor selection, output-capacitor selection, and compensation network.

In pulse-skip mode, the buck regulator clamps the COMP pin voltage at 720 mV, inhibiting the high-side MOSFET. Further decreases in load current or in output voltage cannot drive the COMP pin below this clamp-voltage level. Because the buck regulator is not switching, the output voltage begins to decay. As the voltage-control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high-side MOSFET turns on and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP pin voltage. The output current recharges the output capacitor to the nominal voltage, then the peak switch current begins to decrease, and eventually falls below the pulse-skip-mode threshold, at which time the buck regulator enters Eco-mode again.

For pulse-skip-mode operation, the TPS65321-Q1 buck regulator senses the peak current, not the average or load current. Therefore, the load current where the buck regulator enters pulse-skip mode is dependent on the output inductor value. When the load current is low and the output voltage is within regulation, the buck regulator enters a sleep mode and draws only 140-µA input quiescent current. The internal PLL remains operating when the buck regulator is in sleep mode.

7.3.1.4 Dropout Mode Operation and Bootstrap Voltage (BOOT)

The TPS65321-Q1 buck regulator has an integrated boot regulator and requires a small ceramic capacitor between the BOOT pin and the SW pin to provide the gate-drive voltage for the high-side MOSFET. The BOOT capacitor recharges when the high-side MOSFET is off and the low-side diode conducts. The value of this ceramic capacitor must be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and over voltage.

To improve drop out, the high-side MOSFET of the TPS65321-Q1 buck regulator remains on for 7 consecutive switching cycles, and is forced off during the 8th switching cycle to allow the low-side diode to conduct and refresh the charge on the BOOT capacitor. Because the current supplied by the BOOT capacitor is low, the high-side MOSFET can remain on before it is required to refresh the BOOT capacitor. The effective duty cycle of the switching regulator under this operation can be higher than the fixed-frequency PWM operation through skipping switching cycles.

Feature Description (continued)

7.3.1.5 Error Amplifier

The buck converter of the TPS65321-Q1 buck regulator has a transconductance amplifier acting as the error amplifier. The error amplifier compares the FB1 voltage to the lower of the internal soft-start (SS) voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 310 µS during normal operation. During the soft-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the voltage on the FB1 pin is below 0.8 V and the buck regulator is regulating using an internal SS voltage, the gm is 70 µS. For frequency compensation, external compensation components (capacitor with series resistor and an optional parallel capacitor) must be connected between the COMP pin and the GND pin.

7.3.1.6 Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable band-gap circuit.

7.3.1.7 Adjusting the Output Voltage

A resistor divider from the output node to the FB1 pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. Start with 10 kΩ for the R2 resistor and use Equation 1 to calculate R1. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the FB1 input current are noticeable.

$$R1 = R2 \times \frac{V_O - 0.8\ (V)}{0.8\ (V)} \quad (1)$$

where

- V_O = buck regulator output voltage

7.3.1.8 Soft-Start and Tracking Pin (SS/TR)

The TPS65321-Q1 buck regulator effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft-start time. The TPS65321-Q1 buck regulator has an internal pullup current source of 2 µA that charges the external soft-start capacitor. Equation 2 shows the calculations for the soft-start time (10% to 90%). The voltage reference (V_{ref}) is 0.8 V and the soft-start current (I_{ss}) is 2 µA. The soft-start capacitor must remain lower than 0.47 µF and greater than 1 nF.

$$C_{ss}\ (nF) = \frac{t_{ss}\ (ms) \times I_{ss}\ (\mu A)}{V_{ref}\ (V) \times 0.8} \quad (2)$$

where

- The voltage reference (V_{ref}) is 0.8 V.
- The soft-start current (I_{SS}) is 2 µA.

At power up with the EN1 pin or after recovering from a UVLO event or from a thermal shutdown event, the TPS65321-Q1 buck regulator does not begin switching until the soft-start pin, SS/TR, discharges to less than 40 mV to ensure a proper power up.

7.3.1.9 Reset Output, nRST

The nRST pin pf the TPS65321-Q1 is a open-drain output between the nRST pin and the GND pin. The power-on-reset output asserts low until the output voltage on the FB1 pin exceeds the setting thresholds (91%) and the deglitch timer has expired. Additionally, whenever the EN1 pin is low or open, nRST immediately asserts low regardless of the output voltage. If a thermal shutdown occurs because of excessive thermal conditions, this pin also asserts low. When the nRST is released (not asserted low) an external resistor connected to any external bias voltage pulls up this nRST pin.

Feature Description (continued)

7.3.1.10 Overload-Recovery Circuit

The TPS65321-Q1 buck regulator has an overload recovery (OLR) circuit. The OLR circuit soft-starts the output from the overload voltage to the nominal regulation voltage on removal of the fault condition. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the FB1 pin voltage using an internal pulldown of 382 µA when the error amplifier changes to a high voltage from a fault condition. On removal of the fault condition, the output soft starts from the fault voltage to nominal output voltage.

7.3.1.11 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS65321-Q1 buck regulator is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is 0.5 V (typical) and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 3 or the curves in Figure 2.To reduce the solution size, the user typically sets the switching frequency as high as possible. However, consider tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time. The minimum controllable on-time is 100 ns (typical) and limits the maximum operating input voltage. The frequency-shift circuit also limits the maximum switching frequency. The following sections discuss more details of the maximum switching frequency.

$$R_T\ (k\Omega) = \frac{206033}{f_S^{1.0888}\ (kHz)} \tag{3}$$

7.3.1.12 Overcurrent Protection and Frequency Shift

The TPS65321-Q1 buck regulator implements current-mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and COMP pin voltage are compared. When the peak-switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. Internal clamping of the error-amplifier output functions as a switch current-limit.

The TPS65321-Q1 buck regulator also implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 V on the FB1 pin. During short-circuit events (particularly with high-input-voltage applications), the control loop has a finite minimum controllable on-time, and the output has a low voltage. During the switch on-time, the inductor current ramps to the peak current-limit because of the high input voltage and minimum on-time. During the switch off-time, the inductor typically does not have enough off-time and output voltage for the inductor to ramp down by the ramp-up amount. The frequency shift effectively increases the off-time which allows the current to ramp down.

7.3.1.13 Selecting the Switching Frequency

The switching frequency that is selected must be the lower value of the two equations, Equation 4 and Equation 5. Equation 4 is the maximum switching-frequency limitation set by the minimum controllable on-time. Setting the switching frequency above this value causes the regulator to skip switching pulses. The device maintains regulation, but pulse-skipping leads to high inductor current and a significant increase in output ripple voltage.

Use Equation 5 to calculate the maximum switching frequency limit set by the frequency-shift protection. For adequate output short-circuit protection at high input voltages, set the switching frequency to a value less than the f_S(maxshift) frequency. In Equation 5, to calculate the maximum switching frequency one must take into account that the output voltage decreases from the nominal voltage to 0 volts, and the f_{div} integer increases from 1 to 8 corresponding to the frequency shift.

$$f_S(\text{max skip}) = \left(\frac{1}{t_{on}}\right) \times \left(\frac{(I_L \times R_{dc} + V_O + V_d)}{(V_I - I_L \times R_{hs} + V_d)}\right)$$

where

- I_L = inductor current
- R_{dc} = inductor resistance
- V_I = maximum input voltage
- V_O = buck regulator output voltage

Feature Description (continued)

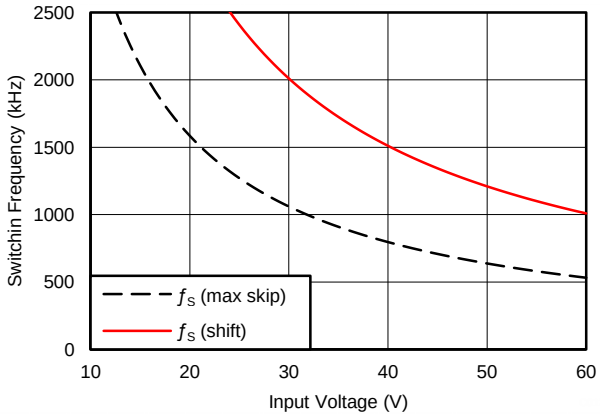
- V_d = diode voltage drop
- R_{hs} = FET on resistance (127 mΩ, trypical)
- t_{on} = controllable on-time (100 ns, typical) (4)

$$f_S(\text{shift}) = \left(\frac{f_{div}}{t_{on}}\right) \times \left(\frac{(I_L \times R_{dc} + V_{O(SC)} + V_d)}{(V_I - I_L \times R_{hs} + V_d)}\right)$$

where

- $V_{O(SC)}$ = buck regulator output voltage during short-circuit condition
- f_{div} = frequency divide factor (equals 1, 2, 4 or 8) (5)

In Figure 8 the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is 0 V, the resistance of the inductor is 0.13 Ω, the FET on-resistance is 0.127 Ω, and the diode voltage drop is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping.



V_O = 3.3 V I_L = 1 A

Figure 8. Maximum Switching Frequency Versus Input Voltage

7.3.1.14 How to Interface to RT/CLK Pin

The RT/CLK pin synchronizes the buck regulator to an external system clock. To implement the synchronization feature, connect a square wave to the RT/CLK pin through the circuit network shown in Figure 9. The square-wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and must have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the SW pin synchronizes with the falling edge of the RT/CLK pin signal. Design the external synchronization circuit in such a way that the device has the default frequency-set resistor connected from the RT/CLK pin to ground if the synchronization signal turns off. TI recommends using a frequency-set resistor connected as shown in Figure 9 through a 50-Ω resistor to ground. The resistor must set the switching frequency close to the external CLK frequency. TI also recommends AC-coupling the synchronization signal through a 10-pF ceramic capacitor to the RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces SW jitter in heavy-load applications when synchronizing to an external clock, and in applications that transition from synchronizing to RT mode. The first time CLK is pulled above the CLK threshold, the device switches from the RT resistor frequency to PLL mode. Along with the resulting removal of the internal 0.5-V voltage source, the CLK pin becomes high-impedance as the PLL starts to lock onto the external signal. Because there is a PLL on the buck regulator, the switching frequency can be higher or lower than the frequency set with the external resistor. The buck regulator transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 ms.

Feature Description (continued)

When the buck regulator transitions from the PLL mode to the resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz, then reapplies the 0.5-V voltage. The resistor then sets the switching frequency. The switching-frequency divisor changes to 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 V on the FB1 pin. The buck regulator implements a digital frequency shift to enable synchronizing to an external clock during standard start-up and fault conditions.

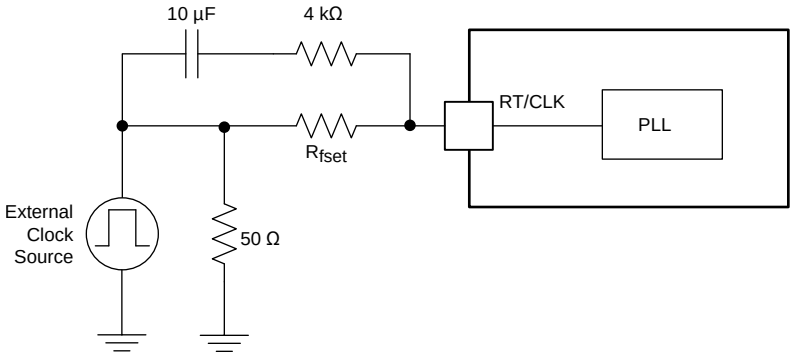


Figure 9. Synchronizing to a System Clock

7.3.1.15 Overvoltage Transient Protection

The TPS65321-Q1 buck regulator incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, with the buck regulator output overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB1 pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage, thus requesting the maximum output current. On removal of the condition, the buck regulator output rises and the error-amplifier output transitions to the steady-state duty cycle. In some applications, the buck regulator output voltage can respond faster than the error-amplifier output can respond which leads to possible output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the FB1-pin voltage to the OVTP threshold (which is 109% of the internal voltage reference). The FB1 pin voltage exceeding the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The FB1 voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on at the next clock cycle.

7.3.1.16 Small-Signal Model for Loop Response

Figure 10 shows an equivalent model for the buck-regulator control loop which can be modeled in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{ea} of 310 µS. Model the error amplifier using an ideal voltage-controlled current source. Resistor, R_O, and capacitor, C_O, model the open-loop gain and frequency response of the amplifier. The 1-mV AC-voltage source between nodes *a* and *b* effectively breaks the control loop for the frequency-response measurements. Plotting *c* versus *a* shows the small-signal response of the frequency compensation. Plotting *a* versus *b* shows the small-signal response of the overall loop. Check the dynamic loop response by replacing R_L with a current source that has the appropriate load-step amplitude and step rate in a time-domain analysis. This equivalent model is only valid for continuous-conduction-mode designs.

Feature Description (continued)

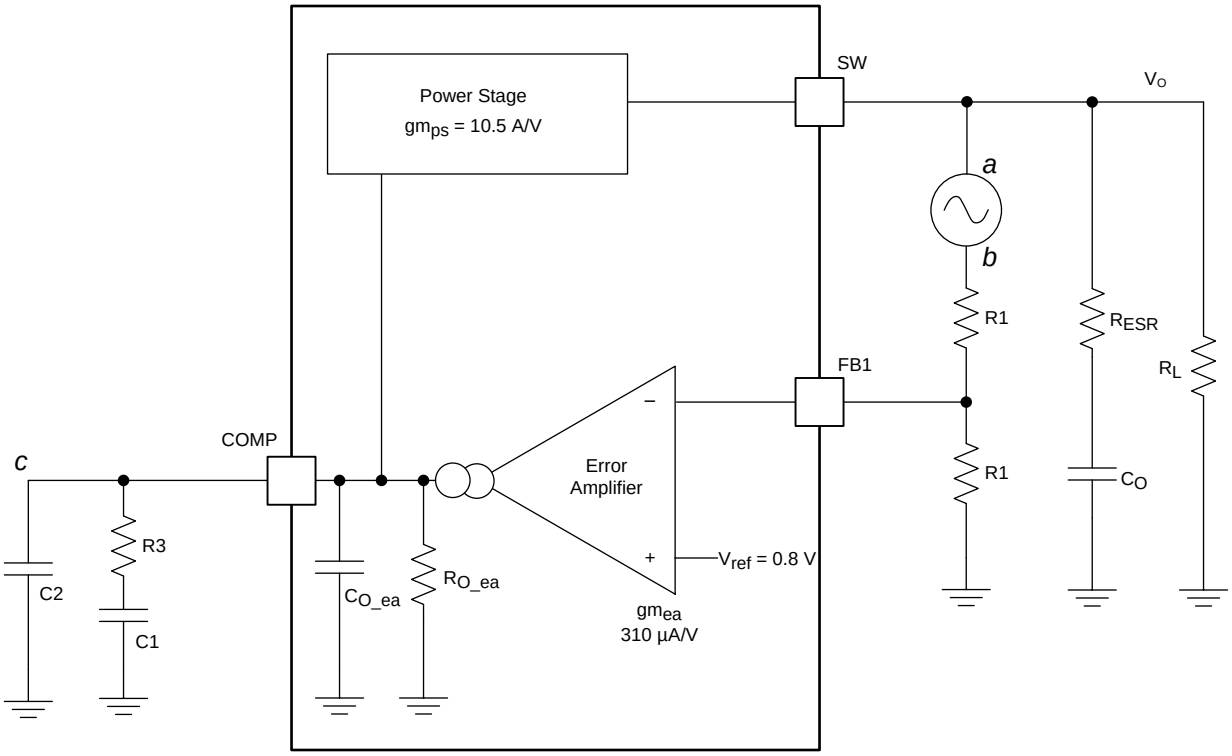


Figure 10. Small-Signal Model for Loop Response

7.3.1.17 Simple Small-Signal Model for Peak-Current Mode Control

Figure 11 shows a simple small-signal model that can be used to understand how to design the frequency compensation. A voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor can approximate the TPS65321-Q1 buck regulator power stage. Equation 6 shows the control-to-output transfer function, which consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current divided by the change in COMP pin voltage (node *c* in Figure 10) is the power-stage transconductance. The gm_{ps} for the TPS65321 buck regulator power-stage is 10.5 A/V. Use Equation 7 to calculate the low-frequency gain of the power stage which is the product of the transconductance and the load resistance.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load seems problematic at first, but the dominant pole moves with the load current (see Equation 8). The dashed line in the right half of Figure 11 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes designing the frequency compensation easier. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high-ESR aluminum-electrolytic capacitors can reduce the number of frequency-compensation components required to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 9).

Feature Description (continued)

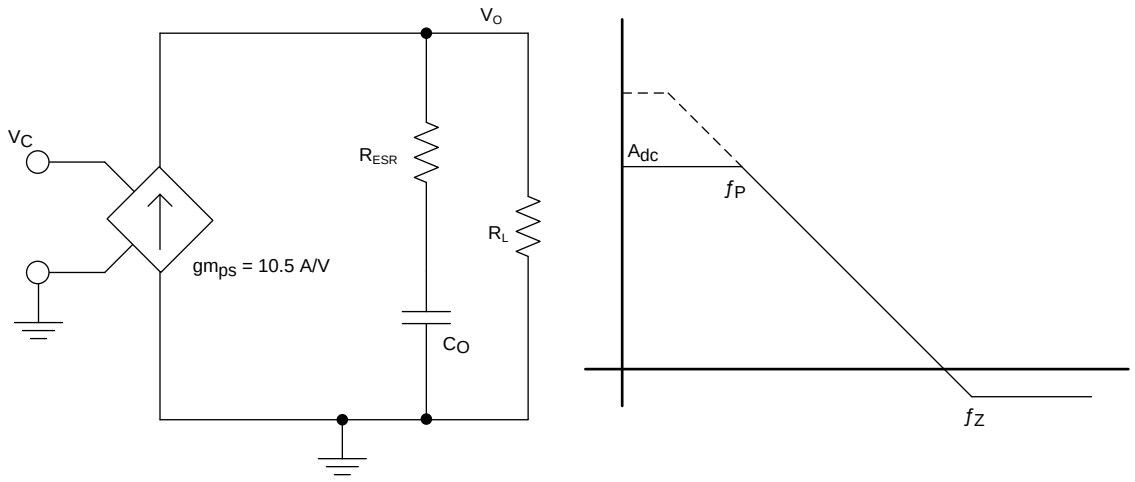


Figure 11. Simple Small-Signal Model and Frequency Response for Peak-Current Mode

$$\frac{V_O}{V_C} = A_{dc} \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (6)$$

$$A_{dc} = gm_{ps} \times R_L \quad (7)$$

$$f_{P\_mod} = \frac{1}{2\pi \times R_L \times C_O} \quad (8)$$

$$f_{Z\_mod} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (9)$$

7.3.1.18 Small-Signal Model for Frequency Compensation

The buck regulator of the TPS65321-Q1 device uses a transconductance amplifier as the error amplifier. Figure 12 shows compensation circuits. Implementation of Type 2 circuits is most likely in high-bandwidth power-supply designs. The purpose of loop compensation is to ensure stable operation while maximizing dynamic performance. Use of the Type 1 circuit is with power-supply designs that have high-ESR aluminum electrolytic or tantalum capacitors. Equation 10 and Equation 11 show how to relate the frequency response of the amplifier to the small-signal model in Figure 12. Modeling of the open-loop gain and bandwidth uses R_O and C_O shown in Figure 12. See the *Typical Applications* section for a design example with a Type 2A network that has a low-ESR output capacitor. For stability purposes, the target must have a loop-gain slope that is –20 dB/decade at the crossover frequency. Also, the crossover frequency must not exceed one-fifth of the switching frequency (120 kHz in the case of a 600-kHz switching frequency).

For dynamic purposes, the higher the bandwidth, the faster the load-transient response. A large DC gain means high DC-regulation accuracy (DC voltage changes little with load or line variations). To achieve this loop gain, set the compensation components according to the shape of the control-output bode plot.

Equation 10 through Equation 20 serve as a reference to calculate the compensation components. R_O and C1 form the dominant pole (P1). A resistor (R3) and a capacitor (C1) in series to ground work as zero (Z1). In addition, add a lower-value capacitor (C2) in parallel with R3 to work as an optional pole. This capacitor can filter noise at switching frequency, and is also required if the output capacitor has high ESR.

Feature Description (continued)

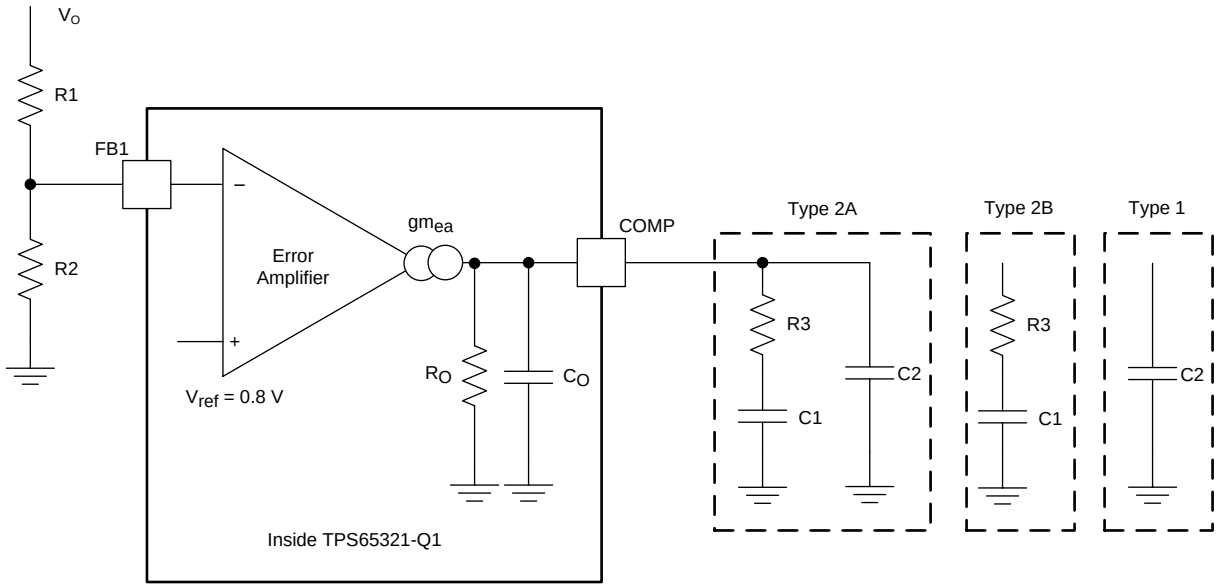


Figure 12. Types of Frequency Compensation

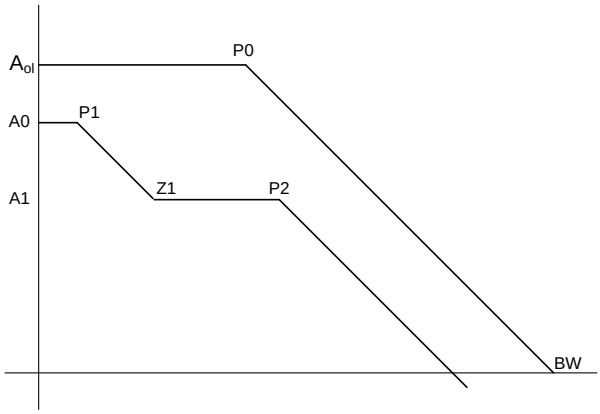


Figure 13. Frequency Response of the Type 2 Frequency Compensation

$$R_{O\_ea} = \frac{A_{ol}\ (V/V)}{gm_{ea}} \tag{10}$$

$$C_{O\_ea} = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \tag{11}$$

$$P0 = \frac{1}{2\pi \times R_{O\_ea} \times C_{O\_ea}} \tag{12}$$

$$EA = A0 \times \frac{\left(1 + \frac{2}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{2}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{2}{2\pi \times f_{P2}}\right)} \tag{13}$$

$$A0 = gm_{ea} \times R_{O\_ea} \times \frac{R2}{R1 + R2} \tag{14}$$

Feature Description (continued)

$$A1 = gm_{ea} \times R_{O\_ea} \,||\, R3 \times \frac{R2}{R1 + R2} \quad (15)$$

$$P1 = \frac{1}{2\pi \times R_{O\_ea} \times C1} \quad (16)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (17)$$

$$P2 = \frac{1}{2\pi \times R3 \times C2} \quad \text{Type 2A} \quad (18)$$

$$P2 = \frac{1}{2\pi \times R3 \times C_{O\_ea}} \quad \text{Type 2B} \quad (19)$$

$$P2 = \frac{1}{2\pi \times R_{O\_ea} \times C2} \quad \text{Type 1} \quad (20)$$

7.3.2 LDO Regulator

The LDO regulator on the TPS65321-Q1 device can be used to supply low power consumption rails. The quiescent current in standby mode is about 35 µA under typical operating condition. The LDO regulator require both supplies from VIN and VIN_LDO to function. The current capability of the LDO regulator is 280 mA under the full VIN_LDO input range, while $V_{(VIN)}$ ≥ 4 V. When VIN becomes less than 4 V, the current capability of the LDO regulator decreases.

7.3.2.1 Charge-Pump Operation

The LDO regulator has an internal charge-pump that turns on or off depending on the input voltage. The charge-pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. The charge-pump switching thresholds are hysteretic. Figure 14 shows the typical switching thresholds for the charge pump.

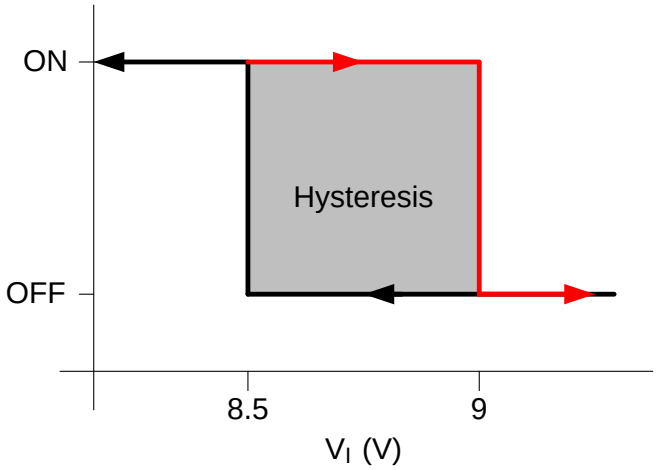


Figure 14. Charge-Pump Switching Thresholds

Table 1. Typical Quiescent Current Consumption

	CHARGE PUMP ON	CHARGE PUMP OFF
LDO I_Q	300 µA	35 µA

7.3.2.2 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a drop out voltage ($V_{DROPOUT}$). This feature allows for a smaller input capacitor and can possibly eliminate the need to use a boost convertor during cold-crank conditions.

7.3.2.3 Adjusting the Output Voltage

A resistor divider from the output node to the FB2 pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. Referring to the schematics in Figure 15, begin with 10 kΩ as the selected value for the R6 resistor and use Equation 21 to calculate the value of the R5 resistor.

$$R5 = R6 \times \frac{V_{(LDO\_OUT)} - 0.8\ (V)}{0.8\ (V)} \tag{21}$$

To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the FB2 input current are noticeable.

7.3.3 Thermal Shutdown

The device implements an internal thermal shutdown as protection if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the buck regulator to stop switching and disables the LDO regulator when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device re-initiates the power-up sequence.

7.3.4 Enable and Undervoltage Lockout

The TPS65321-Q1 device enable pins (EN1 and EN2) are high-voltage-tolerant input pins with an internal pulldown circuit. A high input activates the device and turns on the regulators.

The TPS65321-Q1 device has an internal UVLO circuit to shut down the output if the input voltage falls below an internally-fixed UVLO-falling threshold level. This UVLO circuit ensures that both regulators are not latched into an unknown state during low-input-voltage conditions. The regulators power up when the input voltage exceeds the UVLO-rising threshold level.

7.4 Device Functional Modes

The device has two hardware-enable pins as listed in Table 2. The EN1 pin enables and disables the buck regulator, and the EN2 pin enables and disables the LDO regulator.

Table 2. Device Operation Modes

BUCK REGULATOR	LDO REGULATOR	DESCRIPTION
EN1	EN2	
0	0	Both the buck regulator and the LDO regulator are disabled.
0	1	The buck regulator is disabled. The LDO regulator is enabled.
1	0	The buck regulator is enabled and the LDO regulator is disabled.
1	1	Both the buck regulator and the LDO regulator are enabled.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65321-Q1 buck regulator operates with a supply voltage of 3.6 V to 36 V. The TPS65321-Q1 LDO regulator operates with a supply voltage of 3 V to 36 V. To reduce power dissipation, TI recommends to use the output voltage of the buck regulator as the input supply for the LDO regulator. To use the output voltage of the buck regulator in this way, the selected buck-regulator output voltage must be higher than the selected LDO-regulator output voltage.

To optimize the switching performance (such as low jitter) in automotive applications with input voltages that have wide ranges, TI recommends to operate the device at higher frequencies, such as 2 MHz, which also helps achieve AM-band compliance requirements (that extends until 1.7 MHz).

8.2 Typical Applications

8.2.1 2.2-MHz Switching Frequency, 9-V to 16-V Input, 3.3-V Output Buck Regulator, 5-V Output LDO Regulator

This example details the design of a high-frequency switching regulator and linear regulator using ceramic output capacitors.

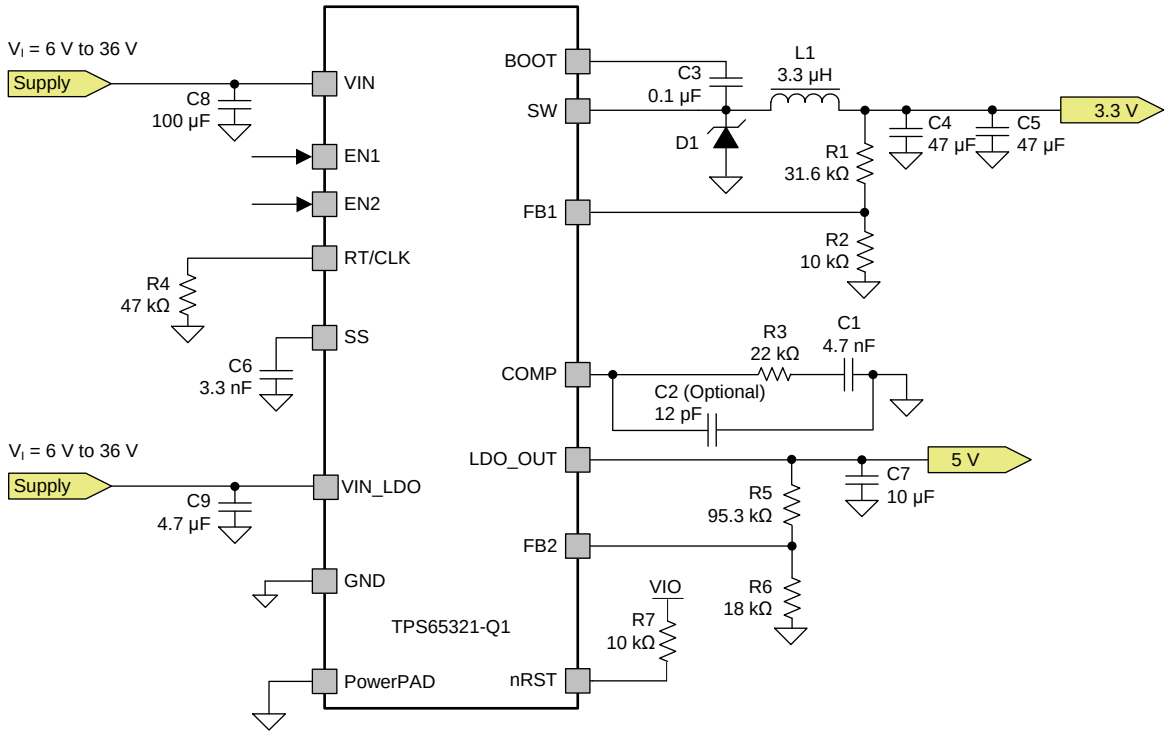


Figure 15. TPS65321-Q1 Design Example With 2.2-MHz Switching Frequency

Typical Applications (continued)

8.2.1.1 Design Requirements

A few parameters must be known to begin the design process. The determination of these parameters is typically at the system level. This example begins with the parameters listed in Table 3.

Table 3. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, VIN1	6 V to 36 V, nominal 12 V
Output voltage, VREG1 (buck regulator)	3.3 V ± 2%
Maximum output current, I_{O_max1}	3 A
Minimum output current, I_{O_min1}	0.01 A
Transient response, 0.01 A to 0.8 A	3%
Output ripple voltage	1%
Switching frequency, f_{SW}	2.2 MHz
Input voltage, VIN_LDO	6 V to 36 V, nominal 12 V
Output voltage, VREG2 (LDO regulator)	5 V ± 2%

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switching Frequency Selection for the Buck Regulator

The first step is to decide on a switching frequency for the regulator. Typically, the user selects the highest switching frequency possible because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The selectable switching frequency is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency-shift limitation.

Consider minimum on-time and frequency-shift protection as calculated with Equation 4 and Equation 5. To find the maximum switching frequency for the regulator, select the lower value of the two results. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit. The typical minimum on-time, $t_{ON\text{-}min}$, is 100 ns for the TPS65321-Q1 device. For this example, where the output voltage is 3.3 V and the maximum input voltage is 36 V, use a switching frequency of 2200 kHz. Use Equation 3 to calculate the timing resistance for a given switching frequency. The R4 resistor sets the switching frequency. A 2.2-MHz switching frequency requires a 47-kΩ resistor (see R4 in Figure 15).

8.2.1.2.2 Output Inductor Selection for the Buck Regulator

Use Equation 22 to calculate the minimum value of the output inductor. The output capacitor filters the inductor ripple current. Therefore, selecting high inductor-ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines can be used to select this value. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

$$L_O\,\text{min} = \frac{V_I\,\text{max} - V_O}{I_O \times K_{IND}} \times \frac{V_O}{V_I\,\text{max} \times f_S} \tag{22}$$

For designs using low-ESR output capacitors such as ceramics, use a value as high as K_{IND} = 0.3. When using higher-ESR output capacitors, K_{IND} = 0.2 yields better results. In a wide-input voltage regulator, selecting an inductor ripple current on the larger side is best because it allows the inductor to still have a measurable ripple current with the input voltage at a minimum.

For this design example, use K_{IND} = 0.2 and the minimum inductor value which is calculated as 2.27 µH. For this design, select standard value which is 3.3 µH (see L1 in Figure 15). Use Equation 23 to calculate the inductor ripple current (I_{ripple}). For the output filter inductor, do not to exceed the RMS-current and saturation-current ratings. Use Equation 24 and Equation 25 to calculate the RMS current (I_{L-RMS}) and the peak inductor (I_{L-peak}).

$$I_{ripple} = \frac{V_O \times (V_I max - V_O)}{V_I max \times L_o \times f_S} \quad (23)$$

$$I_{L-RMS} = \sqrt{I_O^2 + \frac{1}{12} I_{ripple}^2} \quad (24)$$

$$I_{L-peak} = I_O + \frac{I_{ripple}}{2} \quad (25)$$

For this design, the RMS inductor current is 3.0 A, the peak inductor current is 3.21 A, and the inductor ripple current is 0.41 A. The selected inductor is a Coilcraft XAL4030-332ME and has a saturation-current rating of 5.5 A and an RMS-current rating of 5 A. As the equation set demonstrates, lower ripple current reduces the output ripple voltage of the buck regulator but requires a larger value of inductance. Selecting higher ripple currents increases the output ripple voltage of the buck regulator but allows for a lower inductance value.

8.2.1.2.3 Output Capacitor Selection for the Buck Regulator

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output ripple voltage, and how the buck regulator responds to a large change in load current. Select the output capacitance based on the most stringent of these three criteria. The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the buck regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The buck regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage, and to adjust the duty cycle to react to the change. Size the output capacitor to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Use Equation 26 to calculate the minimum output capacitance required to supply the difference in current.

$$C_O > \frac{2 \times \Delta I_O}{f_S \times \Delta V_O} \quad (26)$$

where

- ΔI_O is the change in the buck-regulator output current
- f_S is the switching frequency of the buck regulator
- ΔV_O is the allowable change in the buck-regulator output voltage

For this example, the specified transient load response is a 3% change in V_O for a load step from 0.01 A to 0.8 A. For this example, ΔI_O = 0.8 – 0.01 = 0.79 A and ΔV_O = 0.03 × 3.3 = 0.1 V. Using these numbers results in a minimum capacitance of 7.2 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that must be take into consideration.

The catch diode of the regulator cannot sink current. Therefore any stored energy in the inductor produces an output-voltage overshoot when the load current rapidly decreases. Also, size the output capacitor to absorb the energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. Size the capacitor to maintain the desired output voltage during these transient periods.

Use Equation 27 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value.

$$C_O > L_O \times \frac{(I_{OH}^2 - I_{OL}^2)}{(V_f^2 - V_i^2)}$$

where

- L_O is the output inductance of the buck regulator
- I_{OH} is the output current of the buck regulator under heavy load
- I_{OL} is the output current of the buck regulator under light load
- V_f is the final peak output voltage of the buck regulator
- V_i is the initial capacitor voltage of the buck regulator (27)

For this example, the worst-case load step is from 3 A to 0.01 A. The output voltage increases during this load transition, and the stated maximum in the specification is 3% of the output voltage (see the *Electrical Characteristics* table). This makes V_f = 1.03 × 3.3 = 3.4 V_i is the initial capacitor voltage, which is the nominal output voltage of 3.3 V. Using these numbers in Equation 27 yields a minimum capacitance of 30 µF.

Equation 28 calculates the minimum output capacitance needed to meet the output ripple-voltage specification. Equation 28 yields 0.8 µF.

$$C_O > \frac{1}{8 \times f_S} \times \frac{1}{\frac{V_{O-ripple}}{I_{L-ripple}}}$$

where

- $V_{O\text{-}ripple}$ is the maximum allowable output ripple voltage of the buck regulator
- $I_{L\text{-}ripple}$ is the inductor ripple current of the buck regulator (28)

Use Equation 29 to calculate the maximum ESR required for the output capacitor to meet the output voltage ripple specification. As a result of Equation 29, the ESR should be less than 80 mΩ.

$$R_{ESR} < \frac{V_{O-ripple}}{I_{L-ripple}} \quad (29)$$

The most stringent criterion for the output capacitor is 30 µF of capacitance to keep the output voltage in regulation during a load transient.

Factor in additional capacitance deratings for aging, temperature, and DC bias which increase this minimum value. For this example, two 47-µF, 25-V ceramic capacitors with 3 mΩ of ESR are used (see C4 and C5 in Figure 15). Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (RMS) value of the maximum ripple current.

Use Equation 30 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 30 yields 119 mA.

$$I_{CO(RMS)} < \frac{V_O \times (V_I max - V_O)}{\sqrt{12} \times V_I max \times L_O \times f_S} \quad (30)$$

8.2.1.2.4 Catch Diode Selection for the Buck Regulator

The TPS65321-Q1 device requires an external catch diode between the SW pin and GND (see D1 in Figure 15). The selected diode must have a reverse voltage rating equal to or greater than $V_I$max. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode because of low forward voltage of these diodes. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage is. Although the design example has an input voltage up to 36 V, select a diode with a minimum of 40-V reverse voltage to allow input voltage transients up to the rated voltage of the TPS65321-Q1 device.

For the example design, the selection of a Schottky diode is SL44-E3/57 based on the low forward voltage of this diode. This diode is also available in a larger package size, which has better thermal characteristics. The typical forward voltage of the SL44-E3/57 is 0.44 V.

Also, select a diode with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time, multiplied by the forward voltage of the diode, equals the conduction losses of the diode. At higher switching frequencies, consider the AC losses of the diode. The AC losses of the diode are because the charging and discharging of the junction capacitance and reverse recovery.

8.2.1.2.5 Input Capacitor Selection for the Buck Regulator

The TPS65321-Q1 device requires a high-quality ceramic input decoupling capacitor (type X5R or X7R) of at least 3 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS65321-Q1 device. Use Equation 31 to calculate the input ripple current ($I_{CI(RMS)}$).

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. Minimize the capacitance variations because of temperature by selecting a dielectric material that is stable over temperature. Designers usually select X5R and X7R ceramic dielectrics for power regulator capacitors because these capacitors have a high capacitance-to-volume ratio and are fairly stable over temperature. Also, select the output capacitor with the DC bias taken into consideration. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

This design requires a ceramic capacitor with at least a 40-V voltage rating to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, or 100 V. For this design example. The selection for this example is a 100-µF, 50-V capacitor (see C8 in Figure 15).

$$I_{CI(RMS)} = I_O\,max \times \sqrt{\frac{V_O}{V_I\,min} \times \frac{(V_I\,min - V_O)}{V_I\,min}} \tag{31}$$

The input-capacitance value determines the input ripple voltage of the regulator. Use Equation 32 to calculate the input ripple voltage (ΔV_I).

$$\Delta V_I = \frac{I_O\,max \times 0.25}{C_I \times f_S} \tag{32}$$

Using the design example values, I_{Omax} = 3 A, C_I = 100 µF, f_S = 2200 kHz, yields an input ripple voltage of 3.4 mV and an RMS input ripple current of 1.49 A.

8.2.1.2.6 Soft-Start Capacitor Selection for the Buck Regulator

The soft-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power up which is useful if a load requires a controlled-voltage slew rate. This feature is also useful if the output capacitance is large and requires large amounts of current to charge the capacitor quickly to the output voltage level. The large currents required to charge the capacitor may make the TPS65321-Q1 device reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage-slew rate solves both of these problems.

The soft-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Use Equation 33 to calculate the minimum soft-start time, t_{ss}, required to charge the output capacitor, C_O, from 10% to 90% of the output voltage, V_O, with an average soft-start current of $I_{ss(avg)}$.

$$t_{ss} > \frac{C_O \times V_O \times 0.8}{I_{ss(avg)}} \tag{33}$$

In the example, to charge the effective output capacitance of 94 µF up to 3.3 V while only allowing the average output current to be 3 A requires a 0.083-ms soft-start time.

When the soft-start time is known, use Equation 2 to calculate the soft-start capacitor. For the example circuit, the soft-start time is not too critical because the output-capacitor value is 2 × 47 µF, which does not require much current to charge to 3.3 V. The example circuit has the soft-start time set to an arbitrary value of 1 ms, which requires a 3.125-nF soft-start capacitor. This design uses the next-larger standard value of 3.3 nF.

8.2.1.2.7 Bootstrap Capacitor Selection for the Buck Regulator

Connect a 0.1-µF ceramic capacitor between the BOOT and SW pins for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

8.2.1.2.8 Output Voltage and Feedback Resistor Selection for the Buck Regulator

The voltage divider of R1 and R2 sets the output voltage. For the design example, the selected value of R2 is 10 kΩ, and the calculated value of R1 is 32.1 kΩ. Because of current leakage of the FB1 pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output-voltage accuracy. Selecting higher resistor values decreases the quiescent current and improves efficiency at low output currents, but can introduce noise immunity problems.

8.2.1.2.9 Frequency Compensation Selection for the Buck Regulator

Several possible methods exist to design closed loop compensation for DC-DC converters. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the buck regulator. Ignoring the slope compensation usually causes the actual crossover frequency to be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero, and that the ESR zero is at least 10 times greater than the modulator pole.

To begin, use Equation 34 to calculate the modulator pole, f_{P_mod}, and Equation 35 to calculate the ESR zero, f_{z_mod}.

$$f_{P\_mod} = \frac{1}{2\pi \times R_L \times C_O} = \frac{I_{max}}{2\pi \times V_O \times C_O} \tag{34}$$

$$f_{Z\_mod} = \frac{1}{2\pi \times R_{ESR} \times C_O} \tag{35}$$

Use Equation 36 and Equation 37 to calculate an estimate starting point for the crossover frequency, f_{CO}, to design the compensation.

$$f_{CO} = \sqrt{f_{P\_mod} \times f_{Z\_mod}} \tag{36}$$

$$f_{CO} = \sqrt{f_{P\_mod} \times \frac{f_S}{2}} \tag{37}$$

For the example design, f_{P_mod} is 1.54 kHz and f_{Z_mod} is 564 kHz. Equation 36 is the geometric mean of the modulator pole and the ESR zero and Equation 37 is the mean of the modulator pole and the switching frequency. Equation 36 yields 29.5 kHz and Equation 37 results 41.1 kHz. Use the lower value of Equation 36 or Equation 37 for an initial crossover frequency.

For this example, the target f_{CO} value is 29.5 kHz. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

The total loop gain, which consists of the product of the modulator gain, the feedback voltage-divider gain, and the error amplifier gain at f_{CO} equal to 1. Use Equation 38 to calculate the compensation resistor, R3 (see the schematic in Figure 15).

$$R3 = \left(\frac{2\pi \times f_{CO} \times C_O}{gm_{ps}}\right) \times \left(\frac{V_O}{V_{ref} \times gm_{ea}}\right) \tag{38}$$

Assume the power-stage transconductance, gm_{ps}, is 10.5 S. The output voltage (V_O), reference voltage (V_{ref}), and amplifier transconductance, (gm_{ea}) are 3.3 V, 0.8 V, and 310 µS, respectively. The calculated value for R3 is 22.1 kΩ. For this design, use a value of 22 kΩ for R3. Use Equation 39 to set the compensation zero to the modulator pole frequency.

$$C1 = \frac{1}{2\pi \times R3 \times f_{P\_mod}} \quad (39)$$

Equation 37 yields 4.69 nF for compensating capacitor C1 (see the schematic in Figure 15). For this design, select a value of 4.7 nF for C1.

To implement a compensation pole as needed, use an additional capacitor, C2, in parallel with the series combination of R3 and C1. Use Equation 40 and Equation 41 to calculate the value of C2 and select the larger resulting value to set the compensation pole. Type 2B compensation does not use C2 because it would demand a low ESR of the output capacitor.

$$C2 = \frac{C_O \times R_{ESR}}{R3} \quad (40)$$

$$C2 = \frac{1}{\pi \times R3 \times f_S} \quad (41)$$

8.2.1.2.10 LDO Regulator

Depending on the end application, use different values of external components can be used. To program the output voltage, carefully select the feedback resistors, R5 and R6 (see the schematic in Figure 15). Using smaller resistors results in higher current consumption, whereas using very large resistors impacts the sensitivity of the regulator. Therefore selecting feedback resistors such that the sum of R5 and R6 is between 20 kΩ and 200 kΩ is recommended.

If the desired regulated output voltage is 5 V on selecting R6, the value of R5 can be calculated. With V_{ref} = 0.8 V (typical), V_O = 5 V, and selecting R6 = 18 kΩ, the calculated value of R5 is 95.3 kΩ.

Depending on application requirements, a larger output capacitor for the LDO regulator may be required (see C10 in Figure 15) to prevent the output from temporarily dropping down during fast load steps. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. Additionally, a bypass capacitor can be connected at the output to decouple high-frequency noise based on the requirements of the end application.

8.2.1.2.11 Power Dissipation

8.2.1.2.11.1 Power Dissipation Losses of the Buck Regulator

Use the following equations to calculate the power dissipation losses for the buck regulator. These losses are applicable for continuous-conduction-mode (CCM) operation.

1. Conduction loss:

   $P_{CON} = I_O^2 \times r_{DS(on)} \times (V_O / V_I)$

   where

   - I_O is the buck regulator output current
   - V_O is the buck regulator output voltage
   - V_I is the input voltage

   (42)

2. Switching loss:

   $P_{SW} = ½ \times V_I \times I_O \times (t_r + t_f) \times f_S$

   where

   - t_r is the FET switching rise time (t_r maximum = 20 ns)
   - t_f is the FET switching fall time (t_f maximum = 20 ns)
   - f_S is the switching frequency of the buck regulator

   (43)

3. Gate drive loss:

   $P_{Gate} = V_{drive} \times Q_g \times f_{sw}$

   where

   - V_{drive} is the FET gate-drive voltage (typically V_{drive} = 6 V)
   - $Q_g = 1 \times 10^{-9}$ (nC, typical)

   (44)

8.2.1.2.12 Power Dissipation Losses of the LDO Regulator

$$P_{LDO} = (V_{VIN\_LDO} - V_{(LDO\_OUT)}) \times I_{(LDO\_OUT)} \quad (45)$$

8.2.1.2.13 Total Device Power Dissipation Losses and Junction Temperature

1. Supply loss:

$$P_{IC} = V_I \times I_{Q\text{-}normal} \quad (46)$$

2. Total power loss:

$$P_{Total} = P_{CON} + P_{SW} + P_{Gate} + P_{LDO} + P_{IC} \quad (47)$$

For a given operating ambient temperature T_A:

$$T_J = T_A + R_{th} \times P_{Total}$$

where

- T_J is the junction temperature in °C
- T_A is the ambient temperature in °C
- R_{th} is the thermal resistance of package in (°C/W)
- P_{Total} is the total power dissipation (W) (48)

For a given maximum junction temperature $T_{J\text{-}max}$ = 150°C, the allowed Total power dissipation is given as:

$$T_{A\text{-}max} = T_{J\text{-}max} - R_{th} \times P_{Total} \quad (49)$$

where

- $T_{A\text{-}max}$ is the maximum ambient temperature in °C
- $T_{J\text{-}max}$ is the maximum junction temperature in °C (50)

Additional power losses occur in the regulator circuit because of the inductor AC and DC losses, the Schottky diode, and trace resistance that impact the overall efficiency of the regulator.

Figure 16 shows the thermal derating profile of the 14-pin HTSSOP Package With PowerPAD™ . It is important to consider additional cooling strategies if necessary to maintain the junction temperature of the device below the maximum junction temperature of 150 °C.

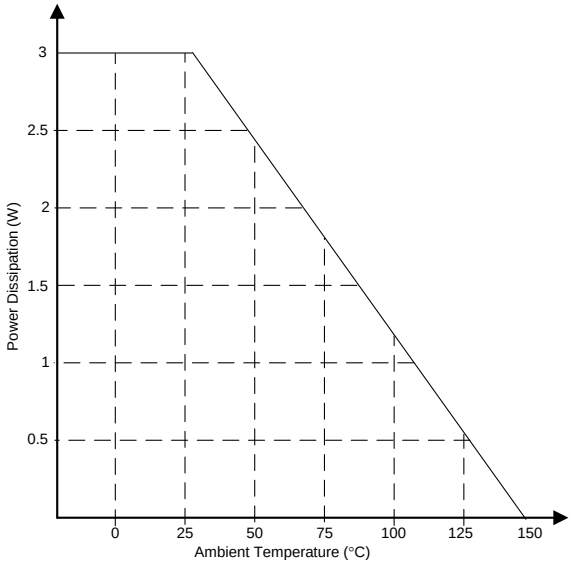


Figure 16. Thermal Derating Profile of TPS65321-Q1 in 14-pin HTSSOP Package With PowerPAD

8.2.1.3 Application Curves

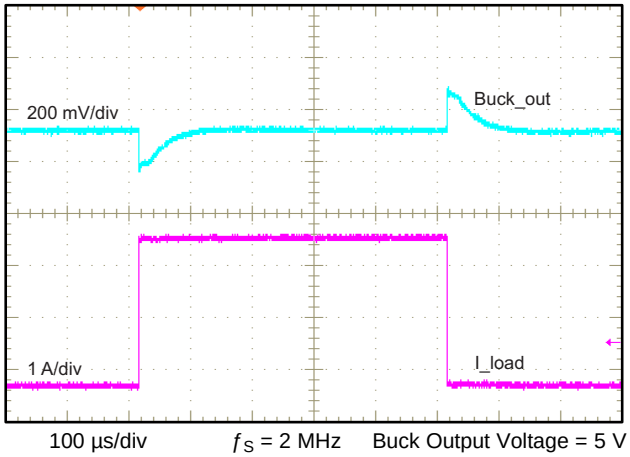


Figure 17. Buck Regulator Output at Load Transient (200 mA to 3 A)

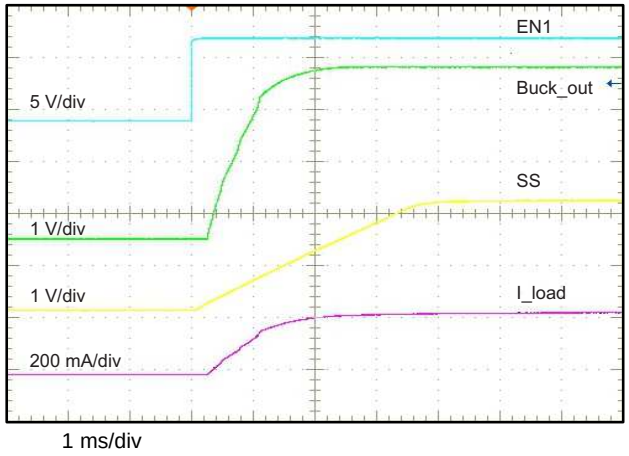


Figure 18. Buck-Regulator Startup Operation

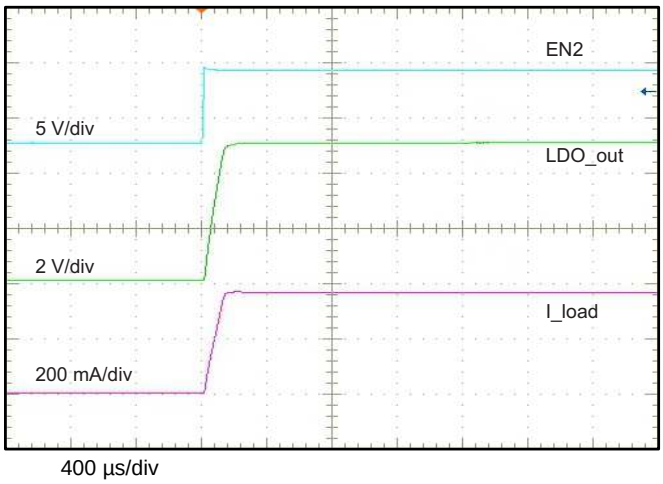


Figure 19. LDO Regulator Startup Operation

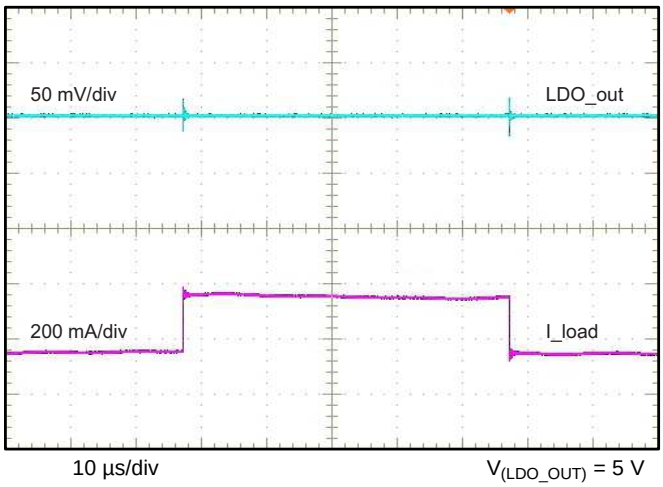


Figure 20. LDO-Regulator Output at Load Transient (50 mA to 300 mA)

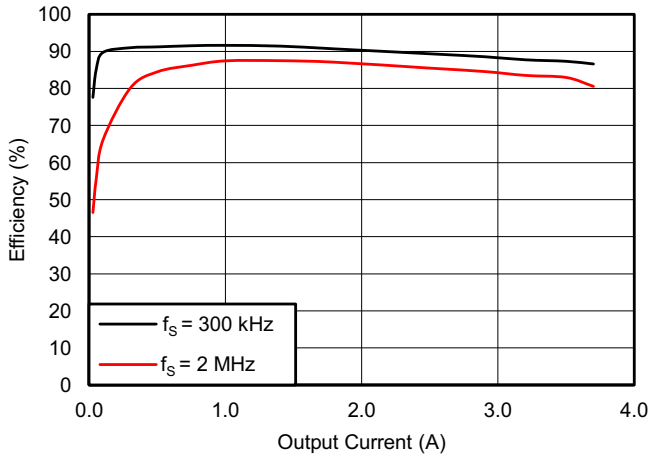
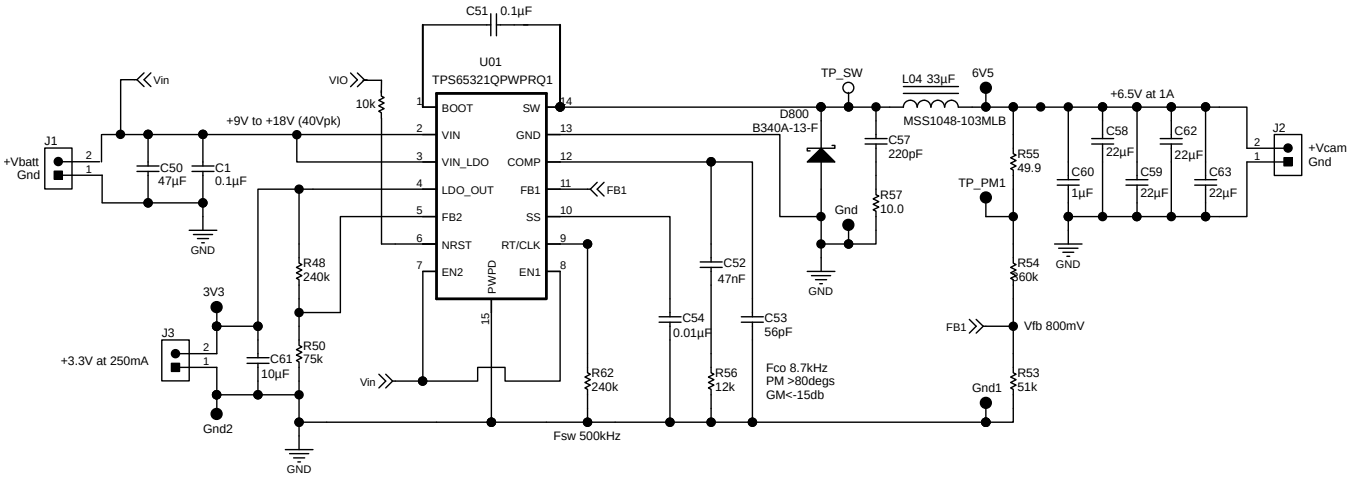


Figure 21. Buck Efficiency Versus Output Current

8.2.2 Design Example With 500-kHz Switching Frequency



R55 is for test purposes only.

Figure 22. TPS65321-Q1 Design Example With 500-kHz Switching Frequency

8.2.2.1 Design Requirements

This example begins with the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, VIN1	9 V to 18 V, typical 12 V
Output voltage, VREG1 (buck regulator)	6.5 V ± 2%
Maximum output current I_{O_max1}	1 A
Minimum output current I_{O_min1}	0.01 A
Transient response 0.01 A to 1 A	3%
Output ripple voltage	1%
Switching frequency f_{SW}	500 kHz
Output voltage, VREG2 (LDO regulator)	3.3 V ± 2%
Overvoltage threshold	106% of output voltage
Undervoltage threshold	91% of output voltage

8.2.2.2 Detailed Design Procedure

For the 500-kHz switching-frequency design, make the adjustments as outlined in the following sections. For sections such as LDO-component calculations, bootstrap-capacitor selection, and others that are not listed in this section, see the *2.2-MHz Switching Frequency, 9-V to 16-V Input, 3.3-V Output Buck Regulator, 5-V Output LDO Regulator* section.

8.2.2.2.1 Selecting the Switching Frequency

For 500-kHz operation, use a 240-kΩ resistor which is calculated using Equation 3. The R62 resistor sets this switching frequency.

8.2.2.2.2 Output Inductor Selection

Using Equation 22, the inductor value is calculated as 27.7 µH with K_{IND} = 0.3. This design example can allow for a higher ripple current, therefore, select the nearest standard value of 33 µH. The RMS and peak inductor-current ratings are calculated using Equation 24 and Equation 25 which result in 1.00 A and 1.13 A, respectively. The value of the output-filter inductor must not exceed the RMS-current and saturation-current ratings.

8.2.2.2.3 Output Capacitor

For this example, the specified transient load response is a 3% change in V_O for a load step from 0.01 A to 1 A (full load). For this example, $\Delta I_O = 1 - 0.01 = 0.99$ A and $\Delta V_O = 0.03 \times 6.5 = 0.195$ V. Using these numbers results in a minimum capacitance of 20.31 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Aluminum electrolytic and tantalum capacitors have higher ESR that should be considered. The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output-voltage overshoot when the load current rapidly decreases. Also, size the output capacitor to absorb the energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. Size the capacitor to maintain the desired output voltage during these transient periods. Use Equation 27 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value.

For this example, the worst-case load step is from 1 A to 0.01 A. The output voltage increases during this load transition, and the stated maximum in our specification is 3% of the output voltage resulting in $V_f = 1.03 \times 6.5 = 6.7$. The initial capacitor voltage, V_i, is the nominal output voltage of 5 V. Using these values, Equation 27 yields a minimum capacitance of 3.88 µF. Equation 28 calculates the minimum output capacitance required to meet the output ripple-voltage specification. Equation 28 yields 10.6 µF. Equation 29 calculates the maximum ESR an output capacitor can have to meet the output ripple-voltage specification. Equation 29 indicates the ESR should be less than 60.2 mΩ.

The most stringent criterion for the output capacitor is 20.31 µF of capacitance to keep the output voltage in regulation during a load transient.

Factor in additional capacitance deratings for aging, temperature, and DC bias which increase this minimum value. For this example, four 22-µF, 25-V and one 1-µF, 25-V ceramic capacitors with 10 mΩ of ESR are used. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 30 to calculate the RMS ripple current that the output capacitor must support. For this design example, Equation 30 yields 240 mA.

8.2.2.2.4 Compensation

This design example use a different approach for calculating compensation values, beginning with the desired crossover frequency. Ensure that the crossover frequency is maintained at 10 kHz to provide reasonable phase margin (PM). To achieve circuit stability, a phase margin greater than 60 degrees and a gain margin less than 15 dB is required. Next, place the zero close to the load pole. The zero is determined using C52 and R56. For this example, select a value of 10 kΩ for R56 which results in a value of approximately 4.7 nF for C52. The pole, resulting from C53 and R56, can be placed between 10 times the crossover frequency and 1/3 of the switching frequency. The gain is adjusted to be maintained over 60 degrees of phase margin and –15 dB of gain margin. The resulting value of C53 is approximately 100 pF for a pole frequency of 159 kHz.

Use the following component values:

R56 = 12 kΩ
C53 = 56 pF
C52 = 47 nF

8.2.2.3 Application Curve

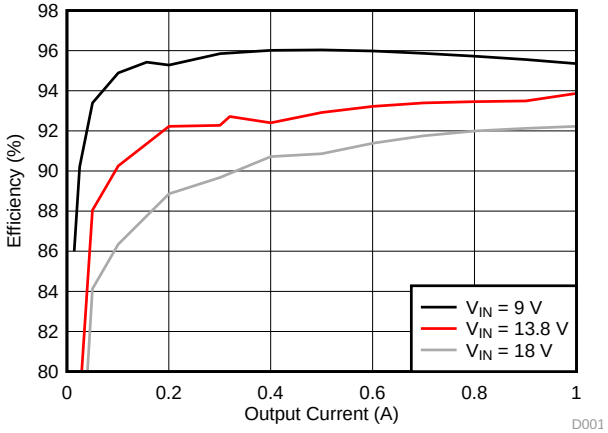


Figure 23. Efficiency vs Output Current

9 Power Supply Recommendations

The buck regulator is designed to operate from an input voltage supply range between 3.6 V and 36 V. The linear regulator is designed to operate from an input supply voltage up to 36 V. Both input supplies must be well regulated. If the input supply connected to the VIN pin is located more than a few inches from the TPS65321-Q1 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

TI recommends the guidelines that follow for PCB layout of the TPS65321-Q1 device.

- **Inductor**
  Use a low-EMI inductor with a ferrite-type shielded core. Other types of inductors can also be used, however, these inductors must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.
- **Input Filter Capacitors**
  Locate input ceramic filter capacitors close to the VIN pin. TI recommends surface-mount capacitors to minimize lead length and reduce noise coupling.
- **Feedback**
  Route the feedback trace for minimum interaction with any noise sources associated with the switching components. TI recommends to place the inductor away from the feedback trace to prevent creating an EMI noise source.
- **Traces and Ground Plane**
  All power (high-current) traces must be as thick and short as possible. The inductor and output capacitors must be as close to each other as possible to reduce EMI radiated by the power traces because of high switching currents. In a two-sided PCB, TI recommends using ground planes on both sides of the PCB to help reduce noise and ground loop errors. The ground connection for the input capacitors, output capacitors, and device ground should connect to this ground plane, where the connection between input capacitors and the catch-diode is the most critical. In a multi-layer PCB, the ground plane separates the power plane (where high switching currents and components are) from the signal plane (where the feedback trace and components are) for improved performance. Also, arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. This placement prevents magnetic field reversal caused by the traces between the two half-cycles, and helps reduce radiated EMI.

10.2 Layout Example

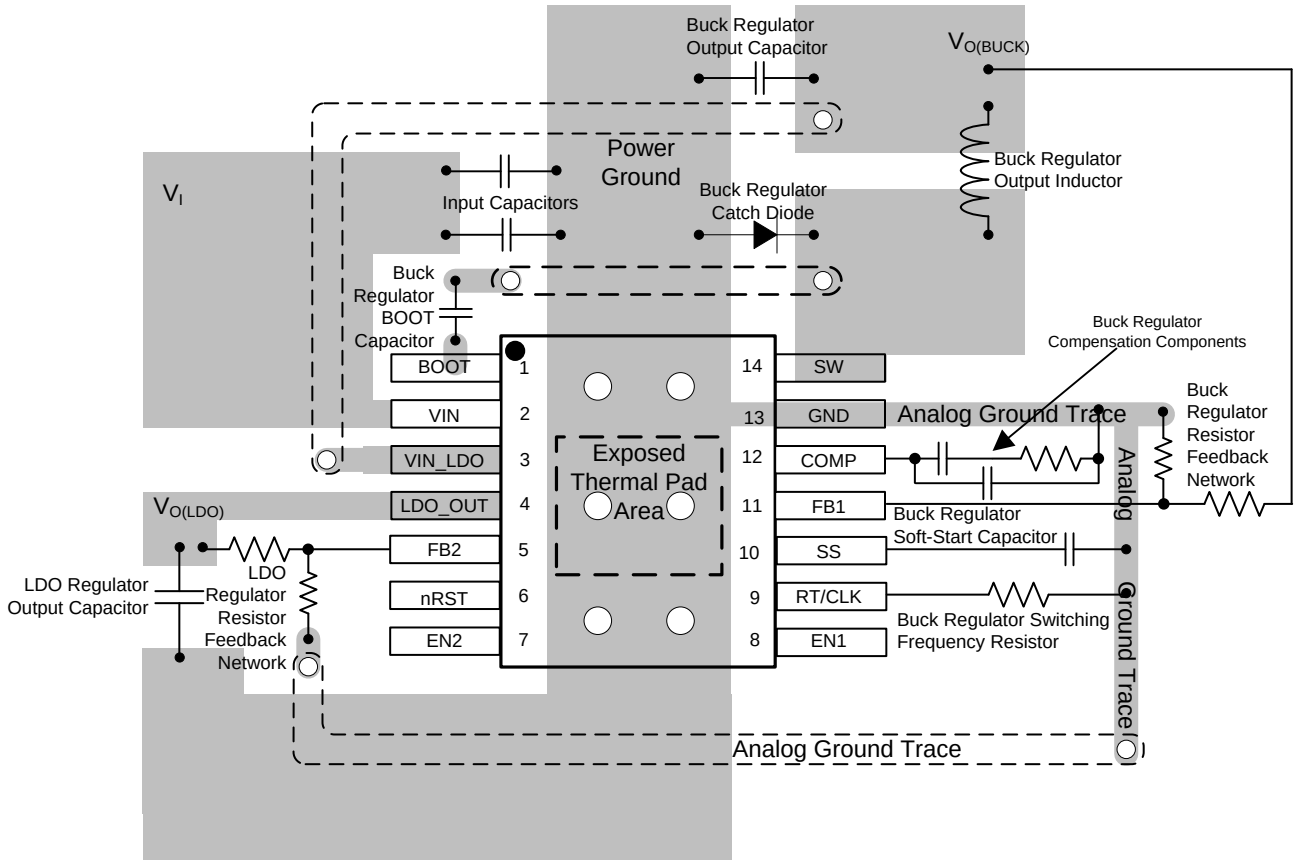


Figure 24. TPS65321-Q1 Layout Example

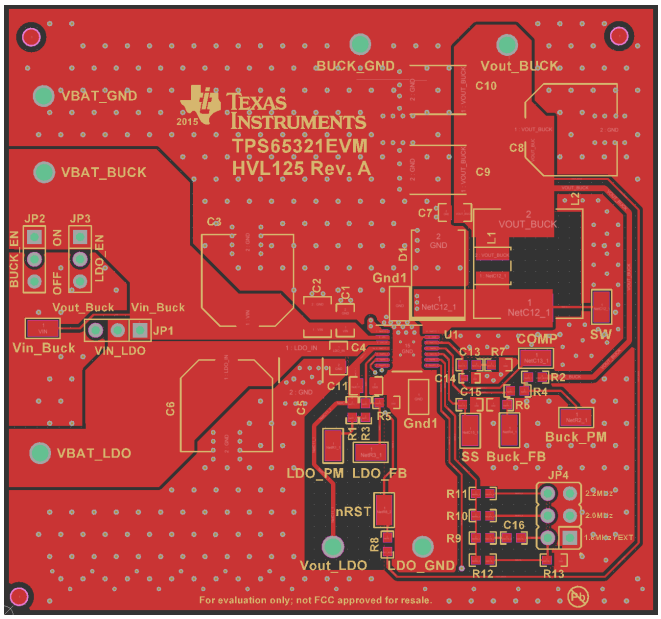


Figure 25. TPS65321-Q1 Layout Example Top Side

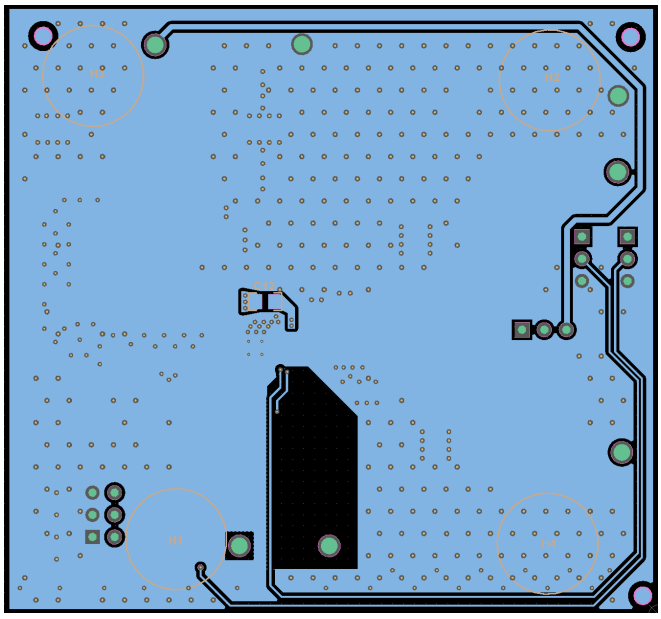


Figure 26. TPS65321-Q1 Layout Example Bottom Side

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TPS65321EVM (HVL125A) User Guide, SLVUAJ6

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

Eco-mode, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65321QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	T65321	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

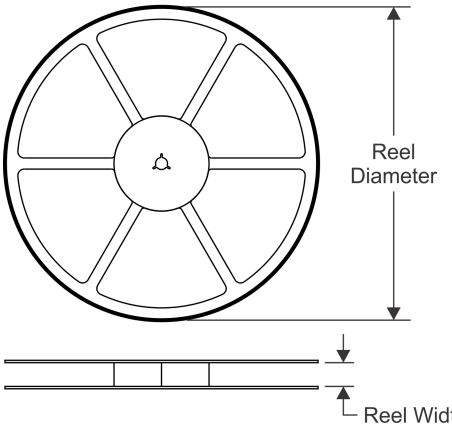
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

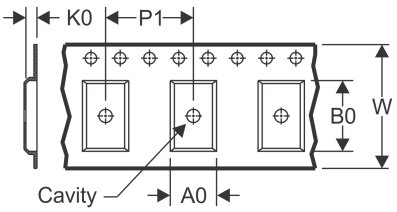
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

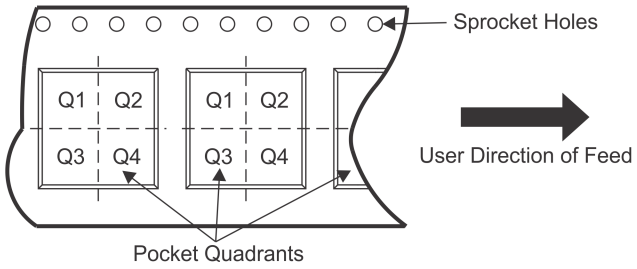


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

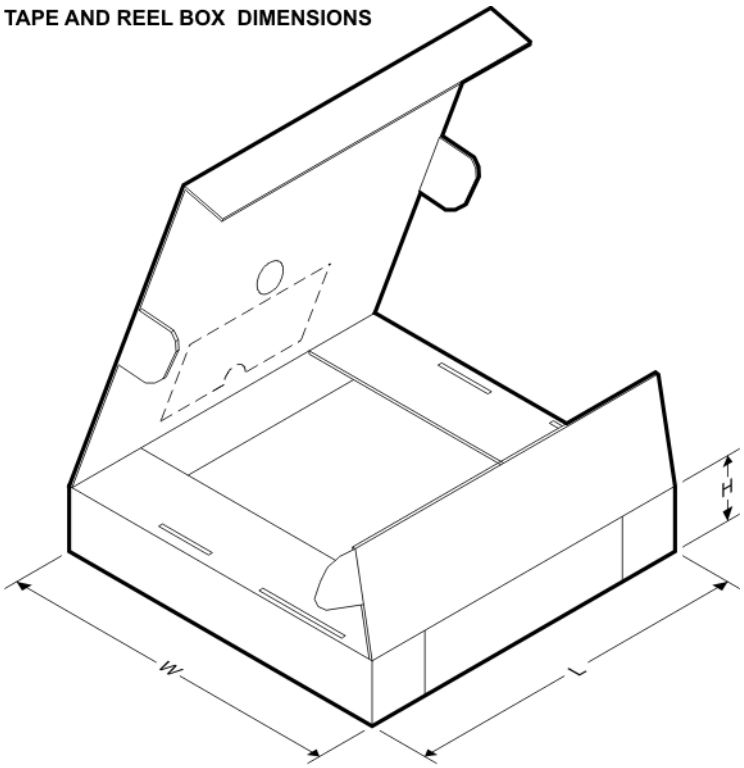
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65321QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

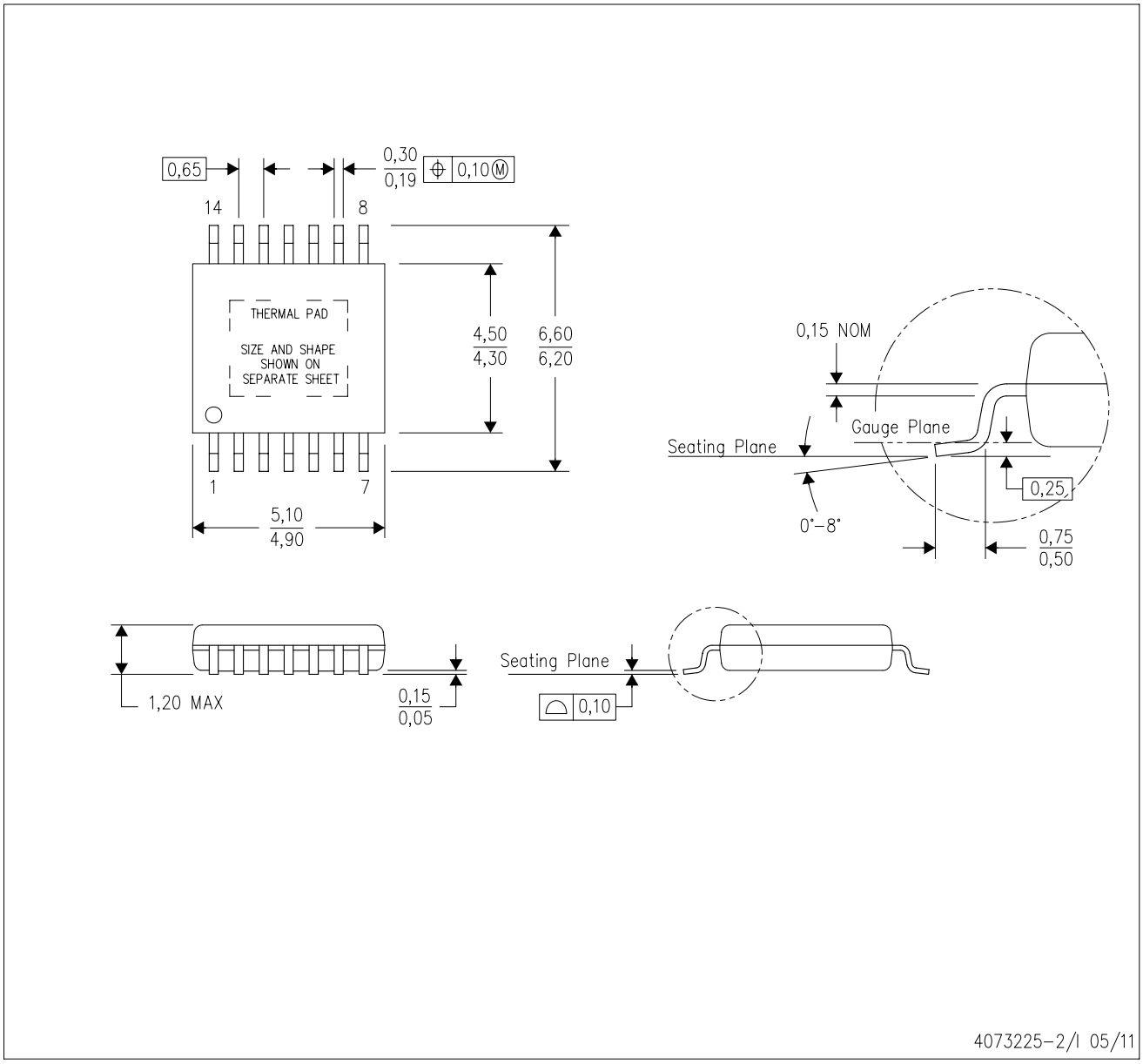
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65321QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	38.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

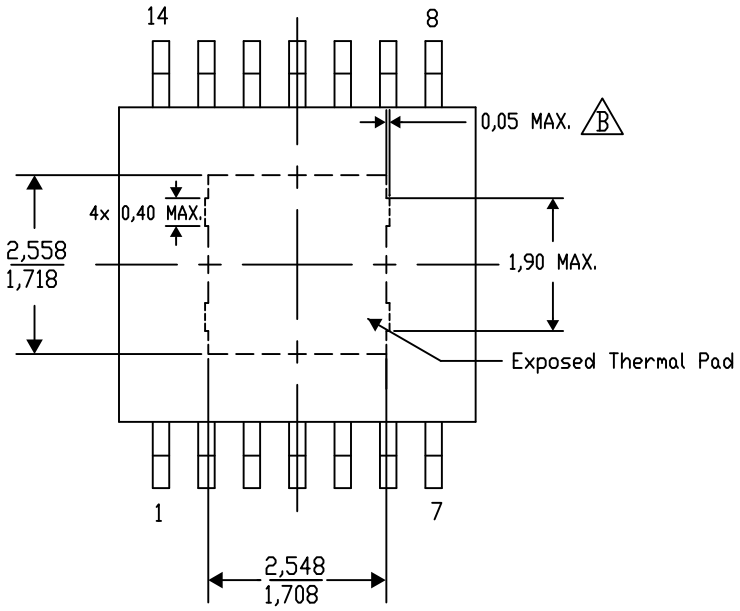
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–56/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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