

## 9-Channel Level Shifter With Gate Voltage Shaping and Discharge Functions

### FEATURES

- 9-Channel Level Shifter Supports 6 × CLK, VST, ODD, and EVEN Signals
- Organized as Two Groups of 7 + 2 Channels
- Separate Positive Supplies ( $V_{GHX}$ ) for Each Group
- $V_{GHX}$  Levels up to 38V
- $V_{GL}$  Levels Down to –13V
- Panel DISCHARGE Function
- Suitable for 4-Phase and 6-Phase Applications
- Gate Voltage Shaping on Channels 1 to 6
- Supports Single and Multiple Flicker Clocks
- Peak Output Currents greater than 500mA
- 28-Pin 5×5 mm QFN Package

### APPLICATIONS

- LCD Displays Using Gate-in-Panel (GIP) Technology

### DESCRIPTION

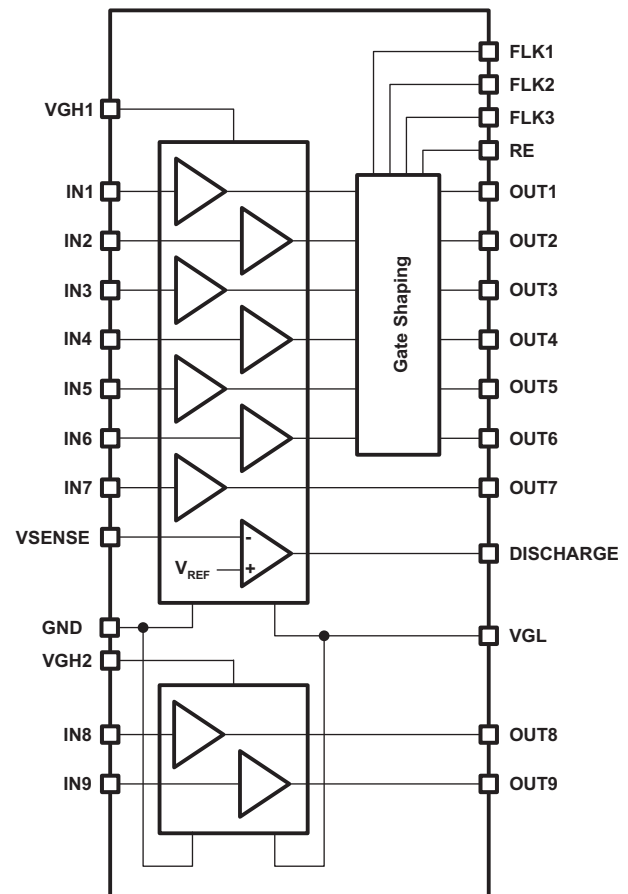
The TPS65192 is a 9 channel level-shifter intended for use in LCD display applications such as TVs and monitors. The device converts the logic-level signals generated by the Timing Controller (T-CON) to the high-level signals used by the display panel.

The 9 level shifter channels are organized as two groups. Channels 1 through 7 are powered from  $V_{GH1}$  and  $V_{GL}$ , and channels 8 and 9 are powered from  $V_{GH2}$  and  $V_{GL}$ . Each level-shifter channel features low impedance output stages that achieve fast rise and fall times even when driving the capacitive loading typically present in LCD display applications.

Level shifter channels 1 through 6 support gate voltage shaping, which can be used to improve picture quality by reducing image sticking. Novel decoding logic enables a single flicker clock signal to control gate voltage shaping for all CLK channels without the need for synchronization. The device also supports the use of multiple flicker clocks. The rate of decay is set by an external resistor or resistor network connected to the RE pin.

A tenth level shifter channel specially configured with a comparator input stage allows designers to implement panel discharging during power-down.

### BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65192RHDR	28-Pin QFN	TPS65192

(1) The device is supplied taped and reeled, with 3000 devices per reel.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
Supply voltage <sup>(2)</sup>	VGH1, VGH2	–0.3 to 45	V
	VGL	0.3 to –15	V
Input voltage <sup>(2)</sup>	IN1 through IN9, VSENSE, FLK1, FLK2, FLK3	–0.3 to 7.0	V
	RE	–0.3 to 45	V
Output current	RE	0.1	A
ESD rating	HBM	2	kV
	MM	200	V
	CDM	700	V
Continuous power dissipation		See Dissipation Rating Table	
Operating ambient temperature range		–40 to 85	°C
Operating junction temperature range		–40 to 150	°C
Storage temperature range		–65 to 150	°C
Lead temperature (soldering, 10 sec)		300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND pin.

**DISSIPATION RATINGS**

PACKAGE	θ <sub>JA</sub>	T <sub>A</sub> ≤25°C POWER RATING	T <sub>A</sub> =70°C POWER RATING	T <sub>A</sub> =85°C POWER RATING
28-Pin QFN <sup>(1)</sup>	35°C/W	3.57W	2.29W	1.86W

(1) This data is based on using a JEDEC High-K board with the exposed die pad connected to a Cu pad on the board connected to the ground plane by a 2x3 thermal via matrix.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
V <sub>GH1</sub> , V <sub>GH2</sub>	Positive supply voltage range	12	30	38	V
V <sub>GL</sub>	Negative supply voltage range	–13	–7	–2	V
T <sub>A</sub>	Operating ambient temperature	–40		85	°C
T <sub>J</sub>	Operating junction temperature	–40		125	°C

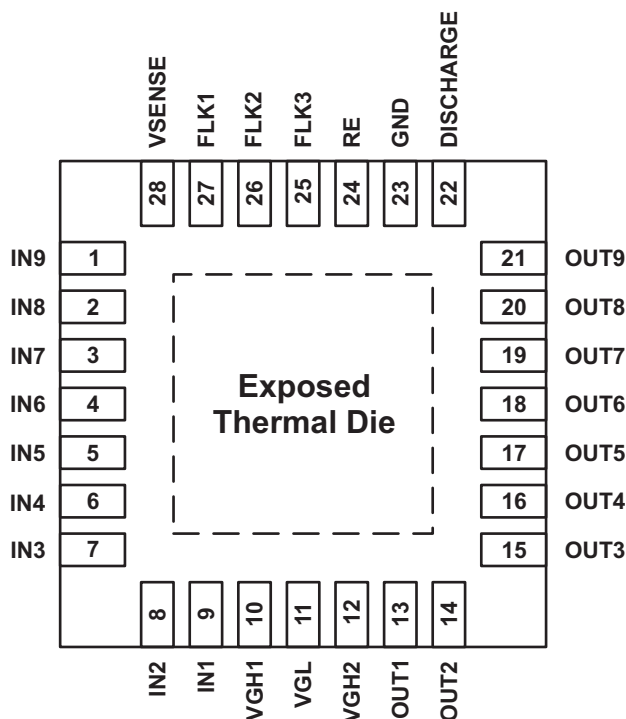
**ELECTRICAL CHARACTERISTICS**
 $V_{GH1} = V_{GH2} = 30V$ ;  $V_{GL} = -7V$ ;  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ ; typical values are at  $25^{\circ}C$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$I_{GH1}$	$V_{GH1}$ Supply current	IN1 to IN7 = GND; $V_{SENSE} = 0V$		0.35	3	mA
$I_{GH2}$	$V_{GH2}$ Supply current	IN8 and IN9 = GND; $V_{SENSE} = 0V$		0.012	1	mA
$I_{GL}$	$V_{GL}$ Supply current	IN1 to IN9 = GND; $V_{SENSE} = 0V$		0.144	4	mA
$V_{UVLO}$	Undervoltage lockout threshold	$V_{GH1}$ rising	10.5		13.5	V
$V_{HYS}$	Undervoltage lockout hysteresis	$V_{GH1}$ falling		450		mV
<b>LEVEL SHIFTERS</b>						
$I_{OUTX}$	Output current	Continuous; OUT1 to OUT7	±15			mA
		Peak; OUT1 to OUT7	±300	±650		
		Continuous; OUT8 and OUT9, DISCHARGE	±15			mA
		Peak; OUT8 and OUT9, DISCHARGE	±150	±250		
$I_{INX}$	Input current	IN1 to IN9 = GND			±1	µA
		IN1 to IN9 = 3.3 V			±1	
$V_{IH}$	High level input voltage	IN1 to IN9			2.0	V
$V_{IL}$	Low level input voltage	IN1 to IN9	0.5			V
$V_{DROPH}$	Output voltage drop high	OUT1 to OUT7; $I_{LOAD} = 10\text{ mA}$		0.12	0.4	V
		OUT8 and OUT9, DISCHARGE; $I_{LOAD} = 10\text{ mA}$		0.36	1.0	
$V_{DROPL}$	Output voltage drop low	OUT1 to OUT7; $I_{LOAD} = -10\text{ mA}$		0.07	0.3	V
		OUT8 and OUT9, DISCHARGE; $I_{LOAD} = -10\text{ mA}$		0.17	1.0	
$t_R$	Rise time	OUT1 to OUT7; $C_{LOAD} = 4.7\text{ nF}^{(1)}$		275	520	ns
		OUT8 and OUT9; $C_{LOAD} = 4.7\text{ nF}^{(1)}$		761	1000	
$t_F$	Fall time	OUT1 to OUT7; $C_{LOAD} = 4.7\text{ nF}^{(1)}$		220	370	ns
		OUT8 and OUT9; $C_{LOAD} = 4.7\text{ nF}^{(1)}$		526	850	
$t_{PH}$	Propagation delay	Rising edge, $C_L = 150\text{ pF}$			60	ns
$t_{PL}$		Falling edge, $C_L = 150\text{ pF}$			60	
<b>GATE VOLTAGE SHAPING</b>						
$t_{PH}$	Propagation delay – gate voltage shaping enabled	FLK falling			100	ns
$t_{SU}$	Set-up time	Time active IN signals must be stable before falling edge of FLK			70	ns
$r_{DS(on)}$	Resistance between OUT and RE pins			70	100	Ω
$I_{LEAK}$	Leakage current from RE pin				±10	µA
<b>DISCHARGE</b>						
$V_{SENSE}$	Discharge voltage sense threshold	$V_{SENSE}$ falling	1.275	1.5	1.725	V
$I_{SENSE}$	Discharge voltage sense input current	$V_{SENSE} = 2V$			±1	µA
$V_{HYS}$	Discharge voltage sense hysteresis	$V_{SENSE}$ rising		40		mV

(1) Rise and fall times are measured between 10% and 90% of the waveform's amplitude.

## DEVICE INFORMATION

### PIN ASSIGNMENT



### PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN9	1	I	Level shifter channel 9 input. Connect this pin to GND, if not used.
IN8	2	I	Level shifter channel 8 input. Connect this pin to GND, if not used.
IN7	3	I	Level shifter channel 7 input. Connect this pin to GND, if not used.
IN6	4	I	Level shifter channel 6 input. Connect this pin to GND, if not used.
IN5	5	I	Level shifter channel 5 input. Connect this pin to GND, if not used.
IN4	6	I	Level shifter channel 4 input. Connect this pin to GND, if not used.
IN3	7	I	Level shifter channel 3 input. Connect this pin to GND, if not used.
IN2	8	I	Level shifter channel 2 input. Connect this pin to GND, if not used.
IN1	9	I	Level shifter channel 1 input. Connect this pin to GND, if not used.
VGH1	10	P	Positive supply voltage for level shifter channels 1 through 7 and discharge function. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors.
VGL	11	P	Negative supply voltage. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors.
VGH2	12	P	Positive supply voltage for level shifter channels 8 and 9. Bypass this pin with a parallel combination of 10µF and 100nF ceramic capacitors.
OUT1	13	O	Level shifter channel 1 output. Leave this pin floating, if not used.
OUT2	14	O	Level shifter channel 2 output. Leave this pin floating, if not used.
OUT3	15	O	Level shifter channel 3 output. Leave this pin floating, if not used.
OUT4	16	O	Level shifter channel 4 output. Leave this pin floating, if not used.
OUT5	17	O	Level shifter channel 5 output. Leave this pin floating, if not used.
OUT6	18	O	Level shifter channel 6 output. Leave this pin floating, if not used.
OUT7	19	O	Level shifter channel 7 output. Leave this pin floating, if not used.

**PIN FUNCTIONS (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT8	20	O	Level shifter channel 8 output. Leave this pin floating, if not used.
OUT9	21	O	Level shifter channel 9 output. Leave this pin floating, if not used.
DISCHARGE	22	O	Panel discharge output. Leave this pin floating, if not used.
GND	23	P	Ground.
RE	24	O	Gate voltage shaping discharge resistor connection. Leave this pin floating, if not used.
FLK3	25	I	Gate voltage shaping flicker clock input for channels 3 and 6. Connect this pin to GND if not used.
FLK2	26	I	Gate voltage shaping flicker clock input for channels 2 and 5. Connect this pin to GND if not used.
FLK1	27	I	Gate voltage shaping flicker clock input for channels 1 and 4. Connect this pin to GND if not used.
VSENSE	28	I	Panel discharge voltage sense. Connect this pin to GND, if not used.
Exposed Thermal Die	Pad	P	Connect to VGL

**TYPICAL CHARACTERISTICS**
**TABLE OF GRAPHS**

		FIGURE
Output Rise and Fall Time	Channels 1 to 7, $C_L = 4.7$ nF, rising edge	<a href="#">Figure 1</a>
	Channels 1 to 7, $C_L = 4.7$ nF, falling edge	<a href="#">Figure 2</a>
	Channels 8 to 9, $C_L = 4.7$ nF, rising edge	<a href="#">Figure 3</a>
	Channels 8 to 9, $C_L = 4.7$ nF, falling edge	<a href="#">Figure 4</a>
	Channels 1 to 7, $C_L = 8$ pF, rising edge	<a href="#">Figure 5</a>
	Channels 1 to 7, $C_L = 8$ pF, falling edge	<a href="#">Figure 6</a>
	Channels 8 to 9, $C_L = 8$ pF, rising edge	<a href="#">Figure 7</a>
	Channels 8 to 9, $C_L = 8$ pF, falling edge	<a href="#">Figure 8</a>
Propagation Delay	IN to OUT, channels 1 to 7, $C_L = 150$ pF, rising edge	<a href="#">Figure 9</a>
	IN to OUT, channels 1 to 7, $C_L = 150$ pF, falling edge	<a href="#">Figure 10</a>
	IN to OUT, channels 8 to 9, $C_L = 150$ pF, rising edge	<a href="#">Figure 11</a>
	IN to OUT, channels 8 to 9, $C_L = 150$ pF, falling edge	<a href="#">Figure 12</a>
	FLK to OUT, channels 1 to 6, $C_L = 150$ pF, RE = 1 k $\Omega$	<a href="#">Figure 13</a>
Output Current	Channels 1 to 7, $C_L = 10$ nF	<a href="#">Figure 14</a>
	Channels 8 to 9, $C_L = 10$ nF	<a href="#">Figure 15</a>
Panel Discharge	Power-on sequencing	<a href="#">Figure 16</a>
	Power-off-sequencing	<a href="#">Figure 17</a>

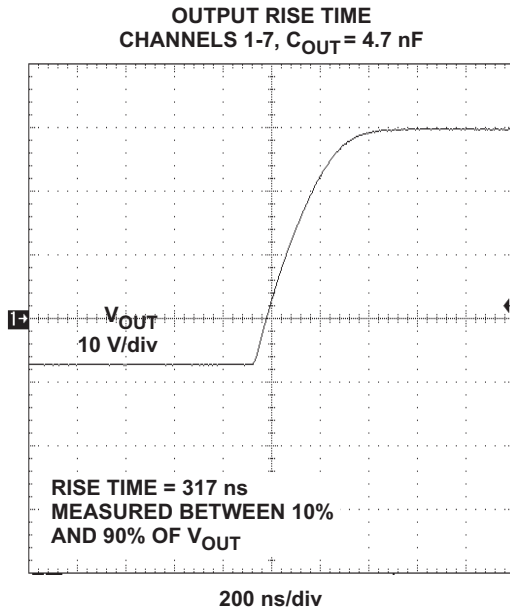


Figure 1.

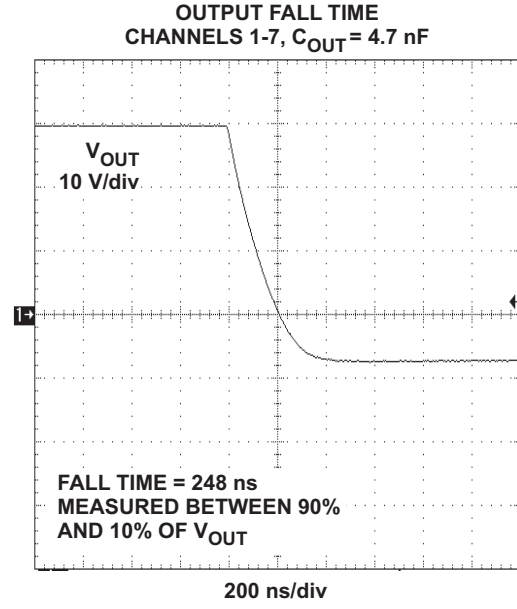


Figure 2.

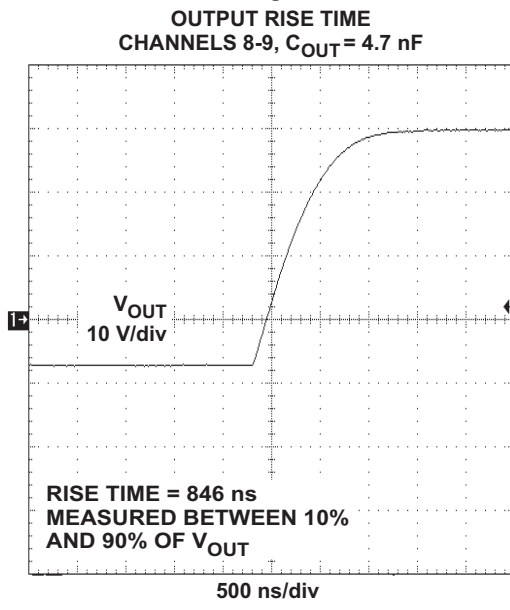


Figure 3.

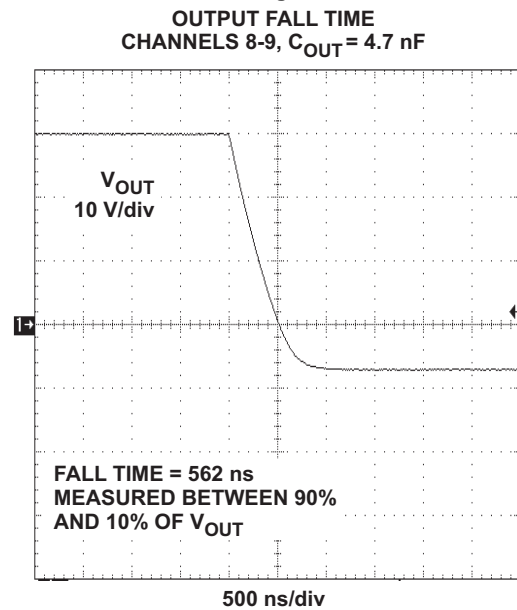


Figure 4.

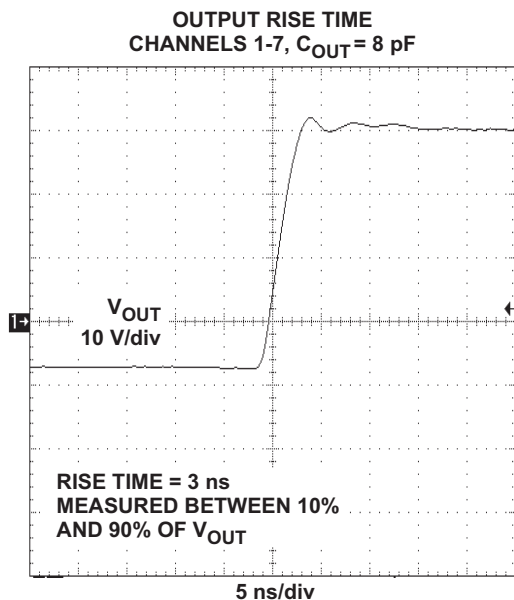


Figure 5.

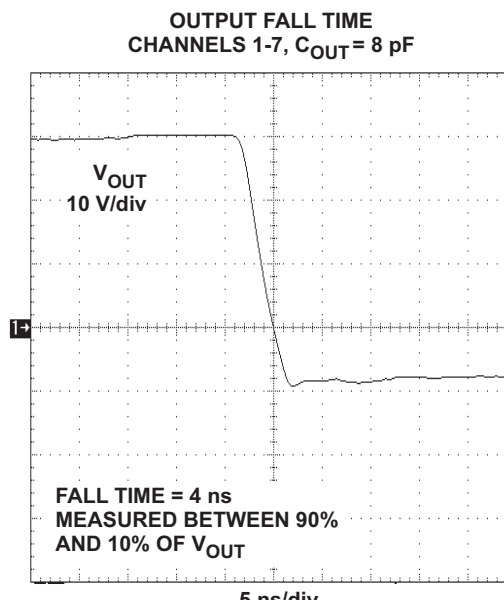


Figure 6.

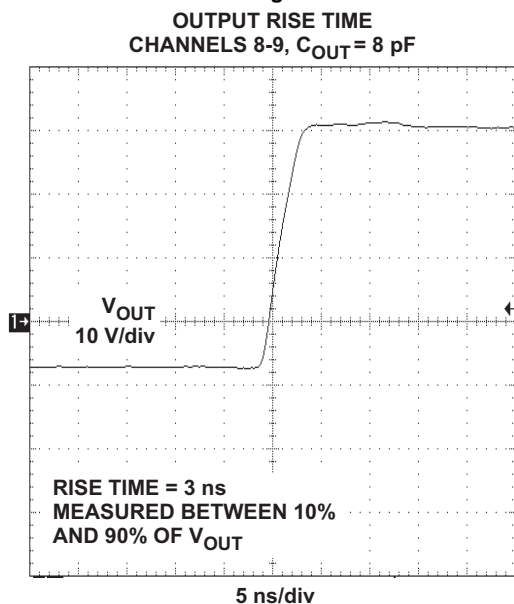


Figure 7.

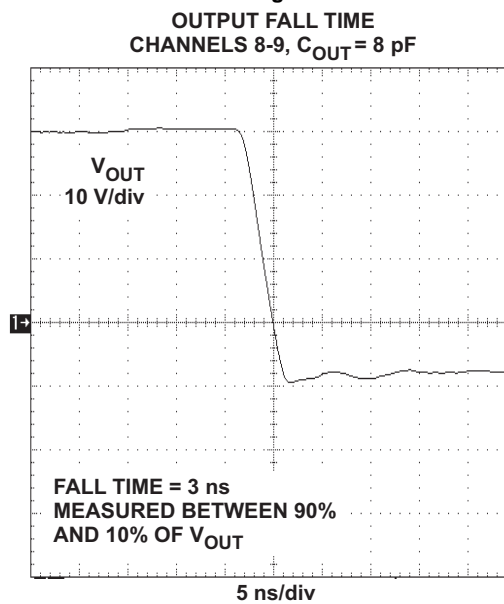
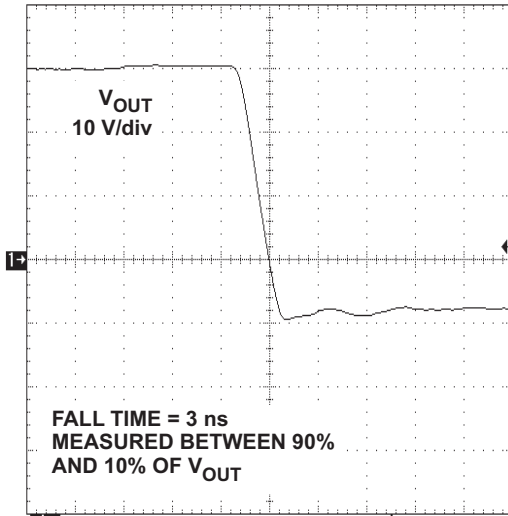


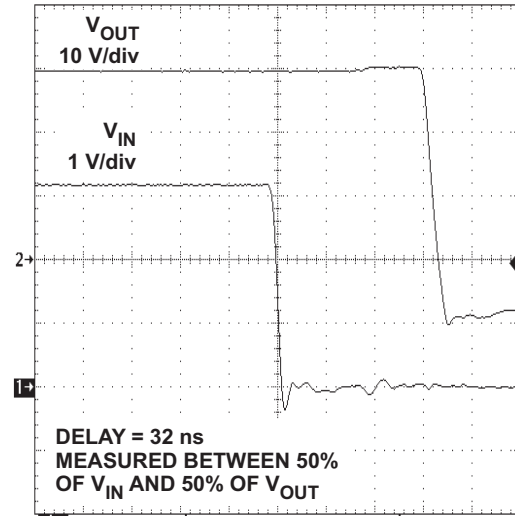
Figure 8.

**OUTPUT FALL TIME**  
CHANNELS 8-9,  $C_{OUT} = 8 \text{ pF}$



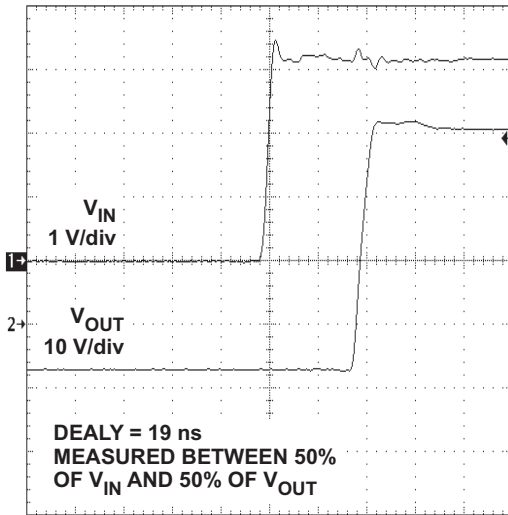
5 ns/div  
Figure 9.

**PROPAGATION DELAY – FALLING**  
IN-OUT, CHANNELS 1-7,  $C_{OUT} = 8 \text{ pF}$



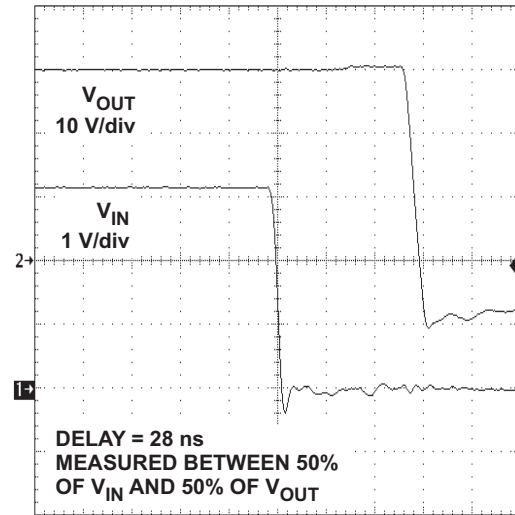
10 ns/div  
Figure 10.

**PROPAGATION DELAY – RISING**  
IN-OUT, CHANNELS 8-9,  $C_{OUT} = 8 \text{ pF}$



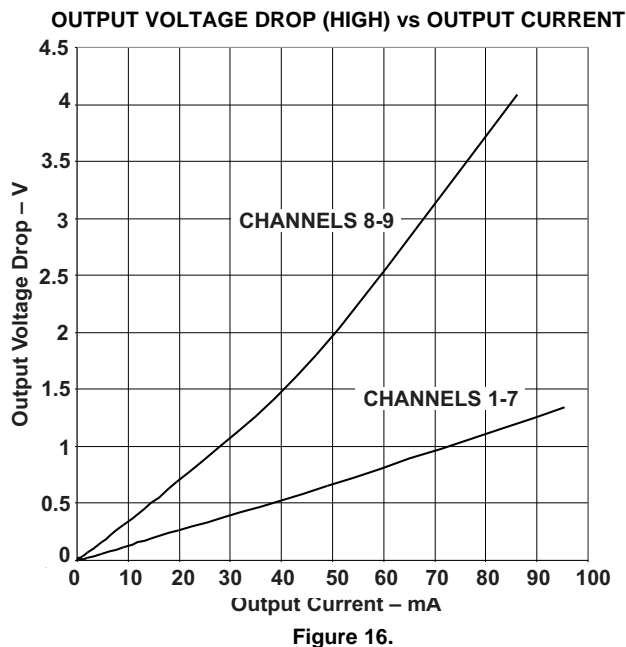
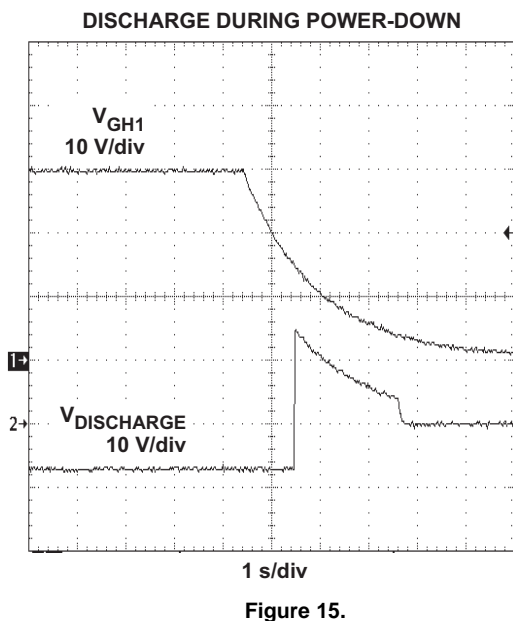
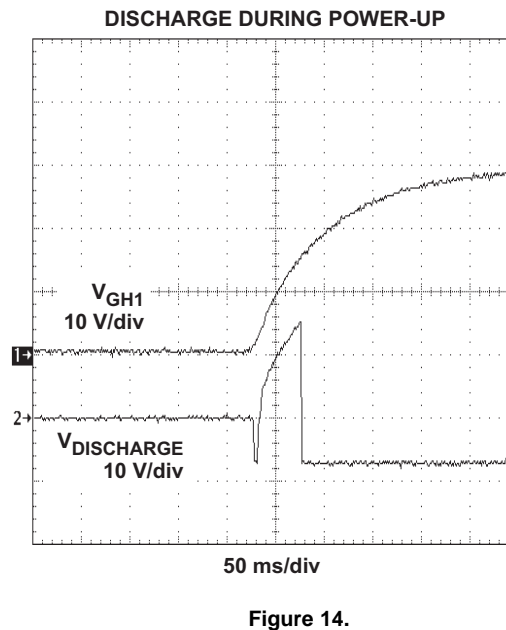
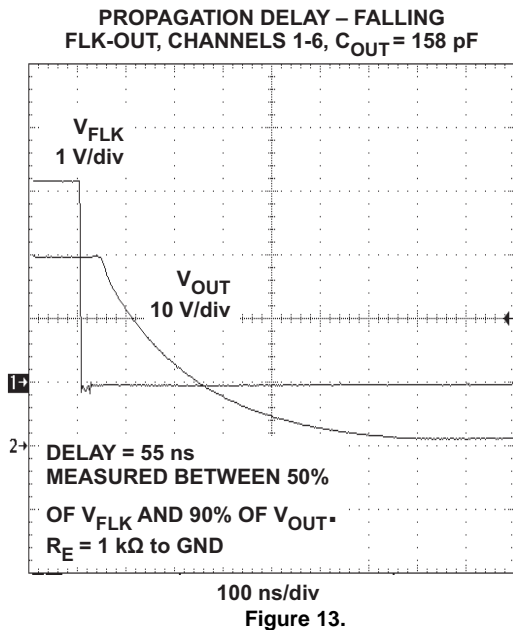
10 ns/div  
Figure 11.

**PROPAGATION DELAY – FALLING**  
IN-OUT, CHANNELS 8-9,  $C_{OUT} = 8 \text{ pF}$



100 ns/div  
Figure 12.





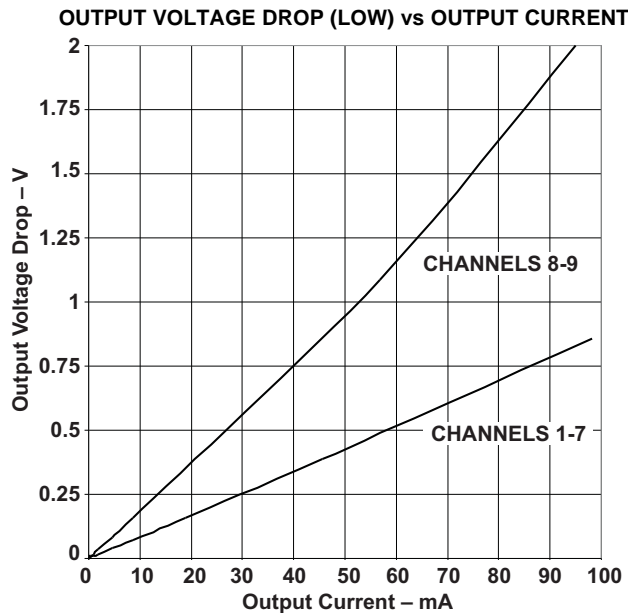


Figure 17.

DETAILED DESCRIPTION

LEVEL SHIFTERS

The 9 level shifter channels in the TPS65192 are divided into two groups. Channels 1 through 7 are powered from  $V_{GH1}$  and  $V_{GL}$ , channels 8 and 9 are powered from  $V_{GH2}$  and  $V_{GL}$ . Channels 1 to 6 support gate shaping and channels 7 through 9 do not (see the block diagram on page 1).

Figure 18 contains a simplified block diagram of one channel with gate voltage shaping.

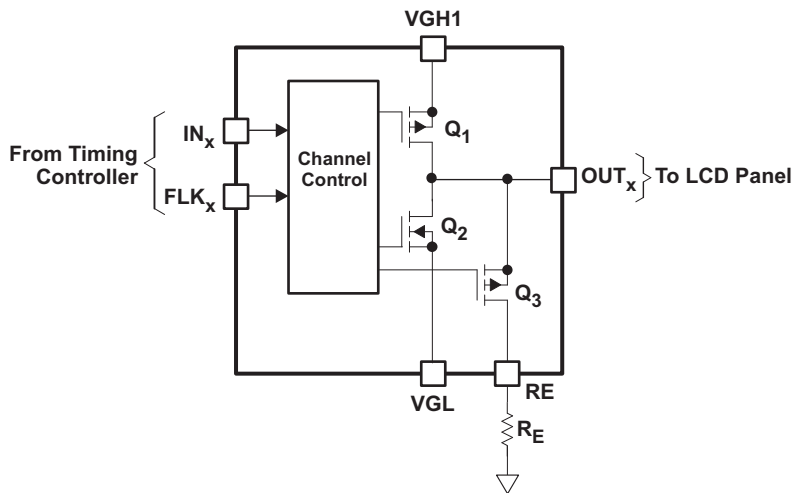


Figure 18. Level Shifter Channel With Gate Voltage Shaping

On the rising edge of IN,  $Q_1$  turns on,  $Q_2$  and  $Q_3$  turn off, and OUT is driven to  $V_{GH1}$ . On the falling edge of FLK,  $Q_1$  turns off,  $Q_3$  is turned on, and the panel now discharges through  $Q_3$  and  $R_E$  (see Figure 19). On the falling edge of IN,  $Q_2$  turns on and  $Q_3$  turns off, and OUT is driven to  $V_{GL}$ . This sequence is repeated in turn for each channel.

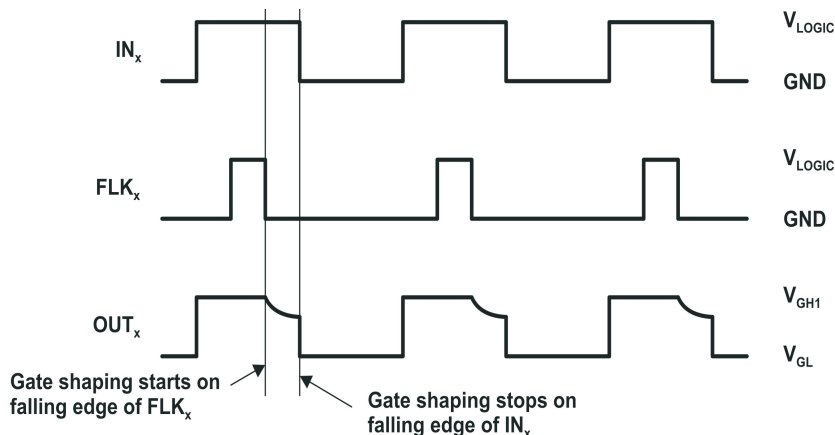


Figure 19. Gate Voltage Shaping Timing Diagram

The alternative configuration shown in Figure 20 can be used to define a minimum gate voltage reached during gate voltage shaping.

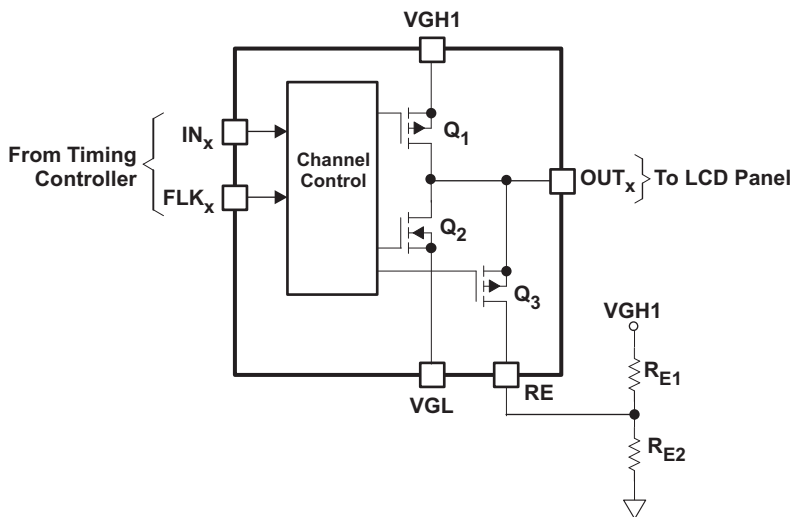


Figure 20. Alternative Gate Voltage Shaping Circuit Configuration

In this circuit, resistors  $R_{E1}$  and  $R_{E2}$  define both the rate of change of gate voltage decay and the minimum gate voltage  $V_{MIN}$ . Using the Thevenin equivalent, the operating parameters of Figure 20 are easily expressed as follows:

$$V_{MIN} = V_{VGH1} \times \left( \frac{R_{E2}}{R_{E1} + R_{E2}} \right)$$

$$R_E = \frac{R_{E1} \times R_{E2}}{R_{E1} + R_{E2}} \tag{1}$$

**FLICKER CLOCKS**

The gate voltage shaping control logic in the TPS65192 allows the device to be used with one, two or three flicker clock signals, according to the application requirements.

In 6-phase applications where one signal controls gate voltage shaping for six CLK channels, the flicker clock should be connected to FLK1 and the unused pins FLK2 and FLK3 connected to GND.

In 6-phase applications where three signals control gate voltage shaping for six CLK channels, the flicker clock for channels 1 and 4 should be connected to FLK1, the flicker clock for channels 2 and 5 connected to FLK2, and the flicker clock for channels 3 and 6 connected to FLK3.

In 4-phase applications where two signals control gate voltage shaping for four CLK channels, the flicker clock for phases 1 and 3 should be connected to FLK1, the flicker clock for phases 2 and 4 connected to FLK2, and the unused pin FLK3 connected to GND. The unused pins IN 3 and IN6 should be connected to  $V_{LOGIC}$ . Alternatively, IN3 can be connected to IN2 and IN6 connected to IN5; this arrangement can simplify PCB layout. Typical schematics for each of the above cases are included in the *Applications* section of this data sheet.

Gate voltage shaping is started by the falling edge of the FLK signal(s), which must occur during a valid part of the clock waveform. For 6-phase systems, this means the last 60° of the clock waveform; for 4-phase systems, this means the last 90° of the clock waveform (see [Figure 21](#) and [Figure 22](#)). Falling edges of the FLK signal(s) occurring outside the valid part of the clock waveform are ignored. The rising edge of the FLK signal(s) has no effect, regardless of when it occurs.

Note that gate voltage shaping is disabled when the voltage applied to the VSENSE pin is less than  $V_{REF}$ .

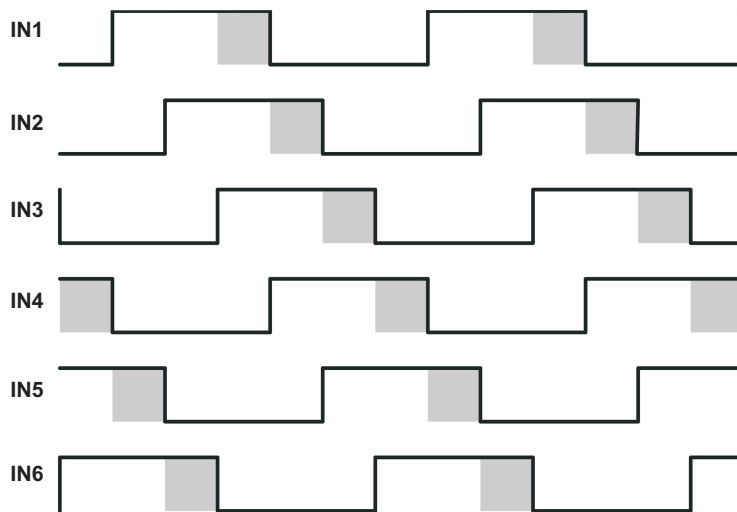


Figure 21. FLK Falling Edge Validity, 6-Phase Applications

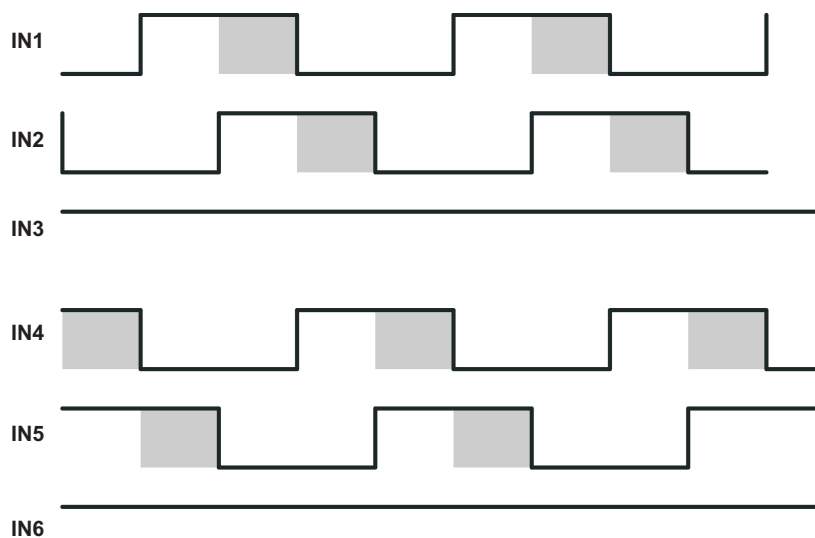


Figure 22. FLK Falling Edge Validity, 4-Phase Applications

## LEVEL SHIFTERS WITHOUT GATE VOLTAGE SHAPING

Channels 7 through 9 do not support gate voltage shaping and are controlled only by the logic level applied to their IN<sub>x</sub> pin. Figure 23 contains a block diagram of a channel that does not support gate voltage shaping.

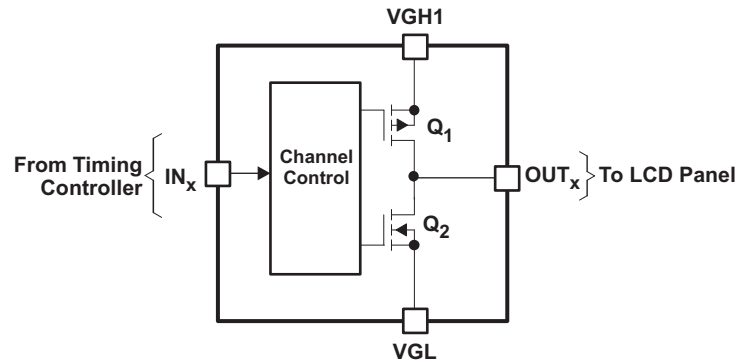


Figure 23. Block Diagram of Level Shifter Without Gate Voltage Shaping

## PANEL DISCHARGE

The TPS65192 contains a function for discharging the display panel during power-down. The discharge function comprises a comparator and a level shifter (see Figure 24). During normal operation, the voltage applied to the VSENSE pin is greater than V<sub>REF</sub>, the output of the level shifter is low, and the DISCHARGE signal is at V<sub>GL</sub>. During power-down, when the voltage applied to the VSENSE pin falls below V<sub>REF</sub>, the level shifter output goes high and the DISCHARGE signal tracks V<sub>GH1</sub> as it discharges (see Figure 16 and Figure 17). Note that gate voltage shaping is disabled when the voltage applied to the VSENSE pin is less than V<sub>REF</sub>.

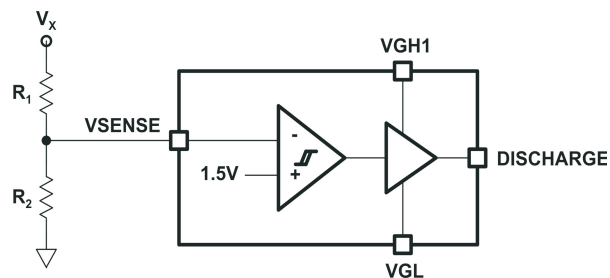


Figure 24. Panel Discharge Function Block Diagram

Suitable values for resistors R<sub>1</sub> and R<sub>2</sub> in Figure 24 can be calculated as follows:

$$R_1 = R_2 \times \left( \frac{V_x}{V_{REF}} - 1 \right) = R_2 \times \left( \frac{V_x}{1.5 \text{ V}} - 1 \right) \quad (2)$$

Where V<sub>x</sub> is the voltage used to activate/deactivate the discharge function.

For most applications, a value between 1kΩ and 10kΩ for R<sub>2</sub> can be used (R<sub>1</sub> depends on the value of R<sub>2</sub> and the value of V<sub>x</sub>).

## APPLICATION INFORMATION

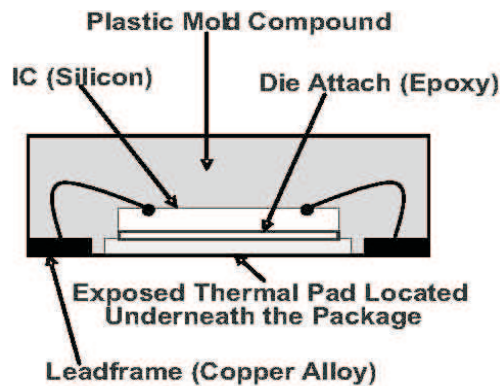
### Power Supply Decoupling

For proper performance, it is recommended that each power supply rail be decoupled with high quality ceramic decoupling capacitors placed as close to the IC supply pins as possible. The exact values used should be optimized for each application, but a parallel combination of 10 $\mu$ F and 100nF is a good place to start.

### PCB LAYOUT

The output stages of the TPS65192 are capable of sinking and sourcing high peak currents – greater than 500mA in typical applications – and care must be taken during PCB layout to ensure that this performance can be achieved in practice. In particular, the high rates of change of current occurring at the rising and falling edges of each output require stray inductance to be minimized. This is most easily achieved by routing the output signals using short, wide PCB tracks (as far as this is possible) and using a low impedance ground plane on the other side of the board to conduct return currents. Tracks between the decoupling capacitors and the corresponding power supply pins should also be kept short and wide as possible.

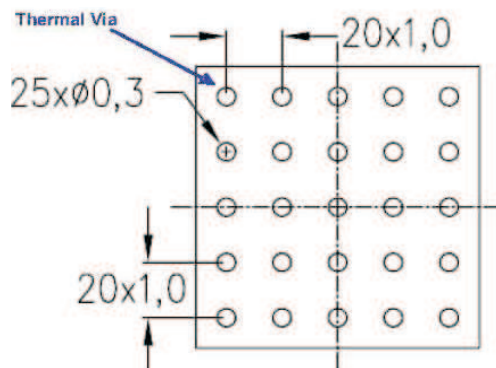
PCB layout must also be adequate from a thermal as well as electrical point of view. The TPS65192 is supplied in a 28-pin QFN package designed to eliminate the need for heat sinks to dissipate the power generated in the IC. The package, shown in [Figure 25](#), is designed so that the lead-frame die pad is exposed on the bottom of the IC, thereby providing an extremely low thermal resistance path between the die and the exterior of the package ( $R_{\theta JC}$ ).



**Figure 25. Section View of a QFN Package**

Copper areas in and on a PCB act as heat sinks for the QFN device; however, signal routing typically restricts access to the power pad on the top layer of the PCB. In typical applications, therefore, the main copper area used to conduct heat away from the IC is on the bottom layer.

TI recommends placing thermal vias in the solder mask defined thermal pad to transfer heat from the top layer of the PCB to the inner or bottom layer used for heat sinking. The recommended via diameter is 0.3mm or less, and via spacing 1mm (see [Figure 26](#)). For the 5 x 5 mm QFN package used for the TPS65192, five thermal vias are typically used.



**Figure 26. Recommended Thermal Via Spacing**

The thermal vias should make their connection to the bottom (or internal) copper plane with a complete connection around the entire circumference of the plated through hole, and a ring of exposed copper (0.05mm wide) around the vias at the bottom of the copper plane. It is not recommended to cover the vias with solder mask as this can cause excessive voiding, and nor is it recommended to use a thermal relief web or spoke connection as this impedes the conduction path to the other layers (see [Figure 27](#)).



**Figure 27. Thermal Via Connection at the Bottom Layer**

In any design, the copper areas used as heat sinks should be made as large as possible.

**The power pad of the TPS65192 is electrically connected to VGL and therefore must not be connected to the PCB's ground plane.**

For more detailed information concerning the thermal performance of QFN packages and recommendations about how to mount the ICs on a PCB, refer to the following application reports:

- SLOA122      *QFN Layout Guidelines*
- SLUA271A    *QFN/SON PCB Attachment*

APPLICATION CIRCUITS

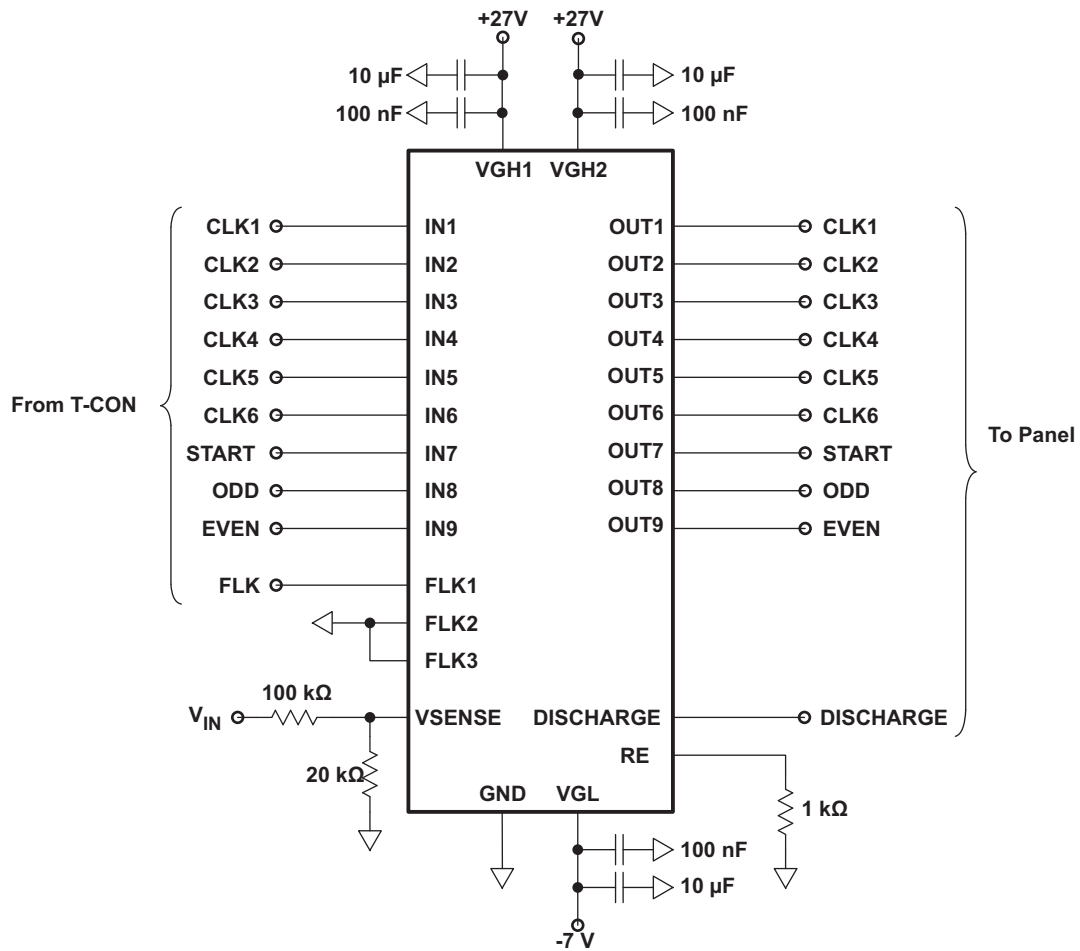


Figure 28. Typical 6-Phase HD TV Application with One Flicker Clock



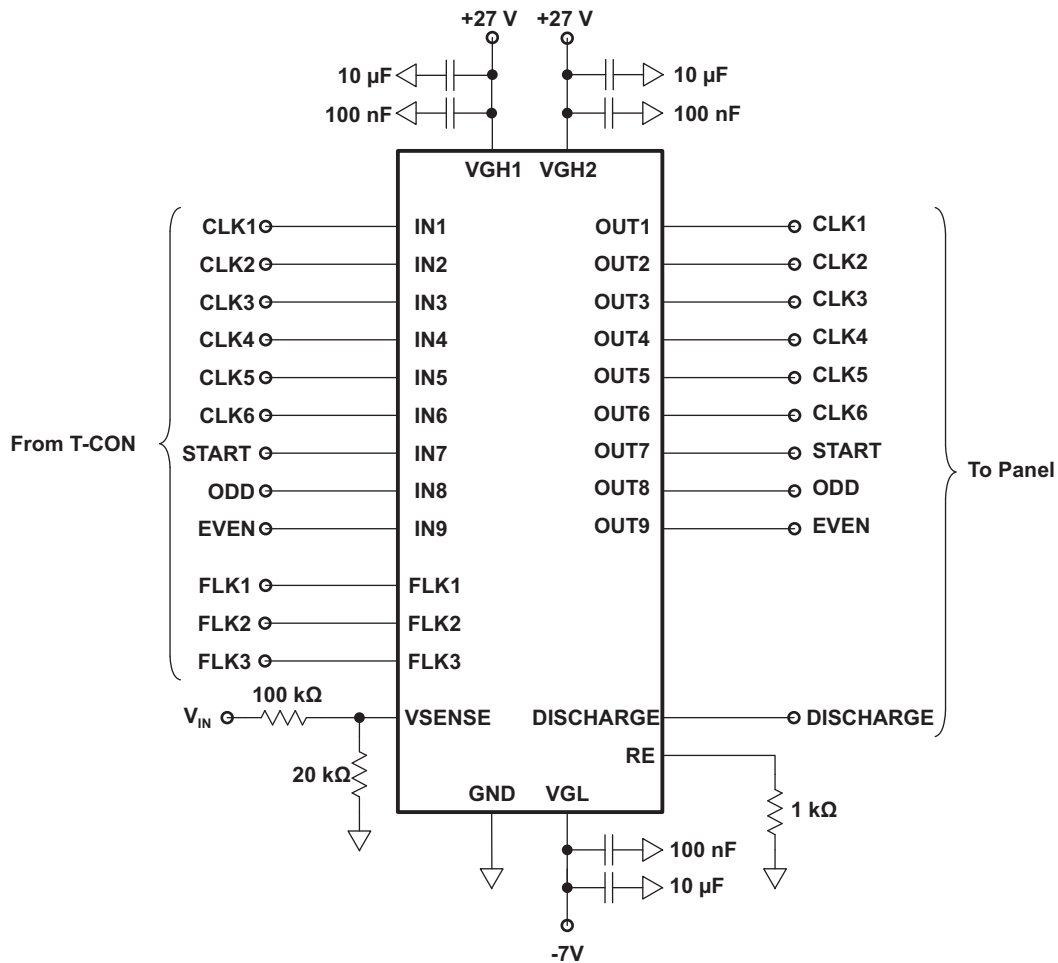


Figure 29. Typical 6-Phase F-HD TV Application with Three Flicker Clocks

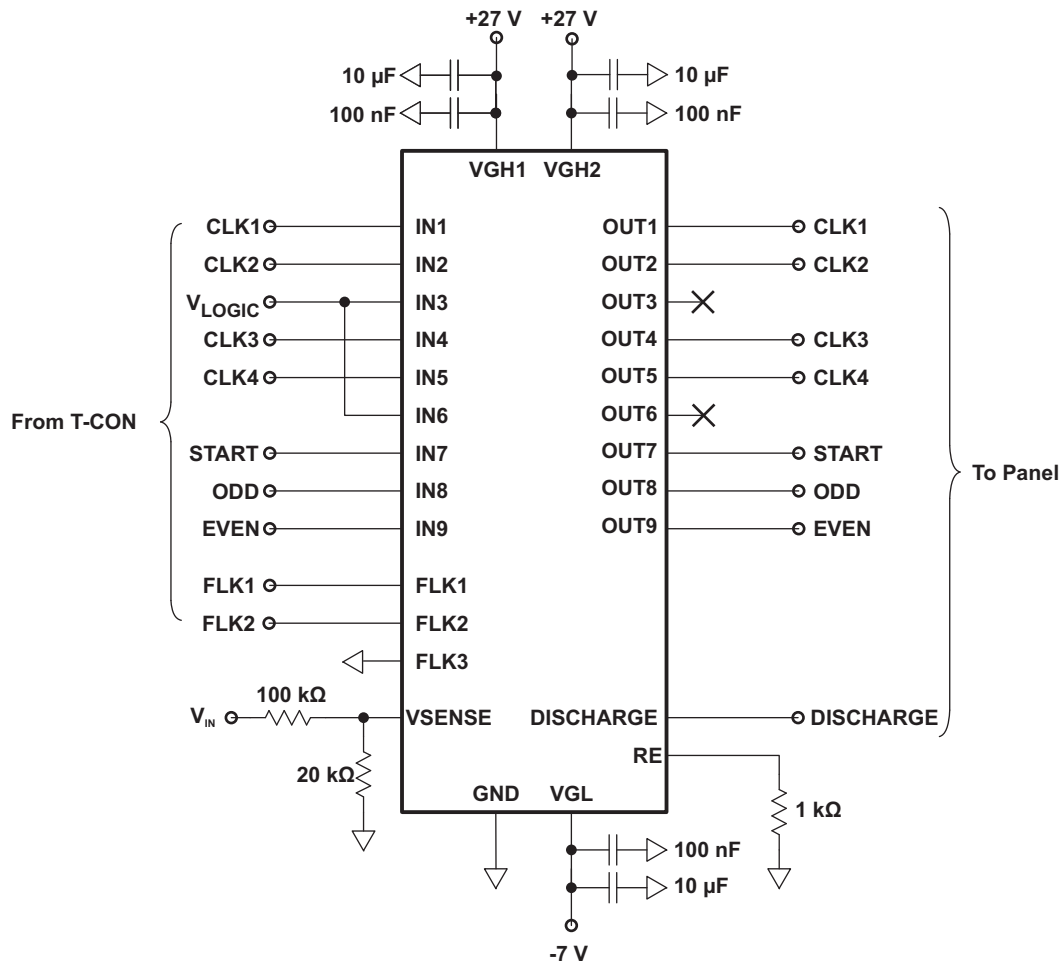


Figure 30. Typical 4-Phase Monitor Application with Two Flicker Clocks

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS65192RHDR	ACTIVE	QFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65192RHDT	PREVIEW	QFN	RHD	28		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65192RHDR	QFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

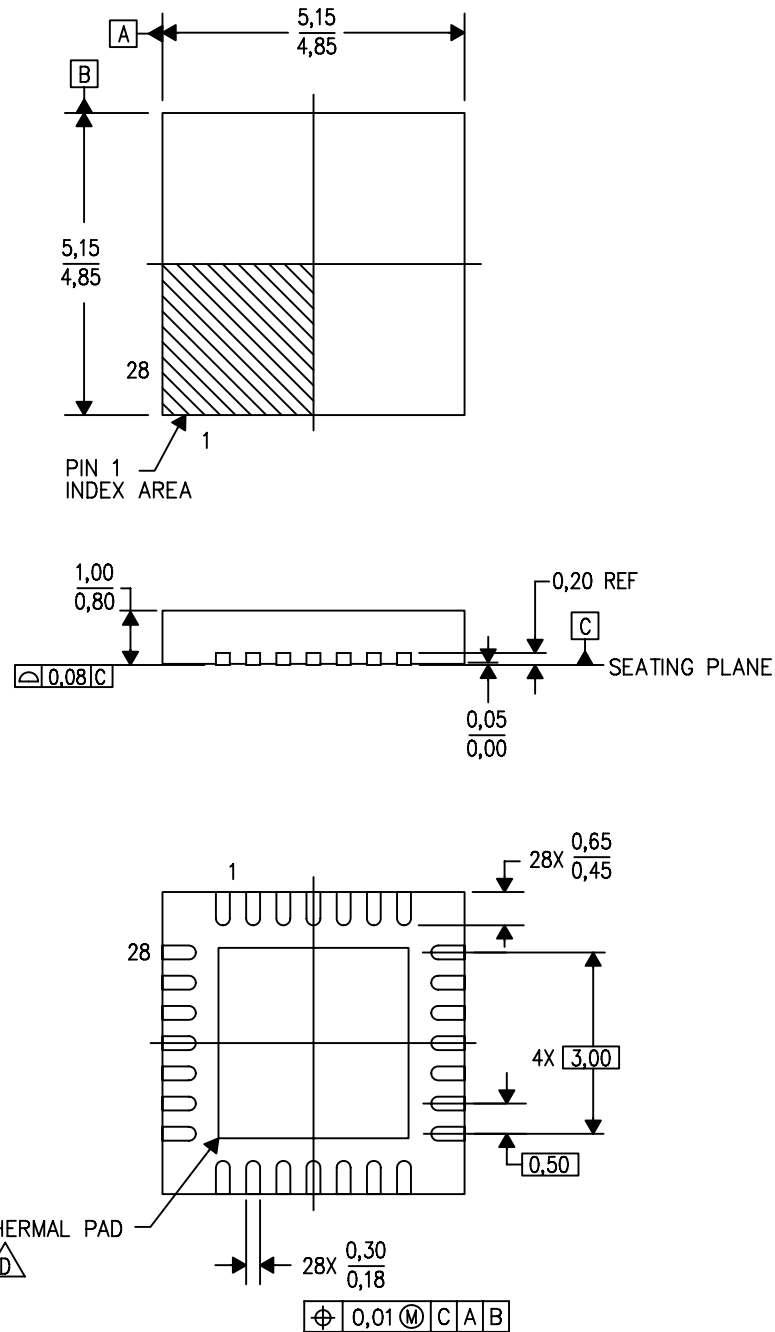


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65192RHDR	QFN	RHD	28	3000	346.0	346.0	29.0

RHD (S-PQFP-N28)

PLASTIC QUAD FLATPACK



4204400/C 07/07

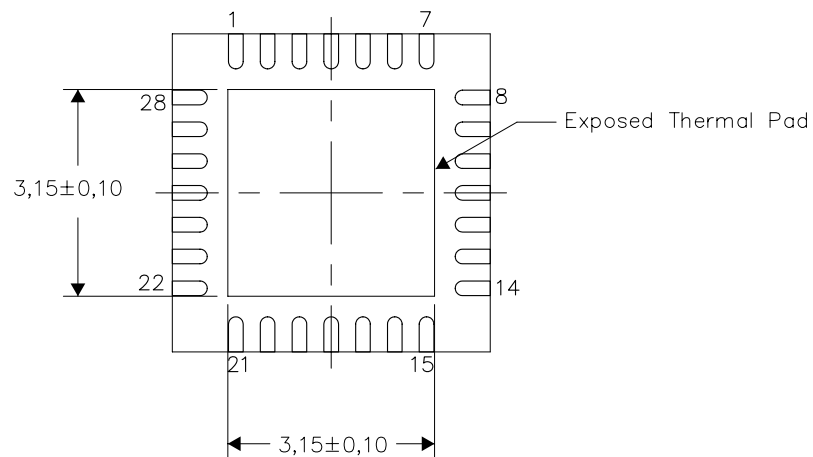
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

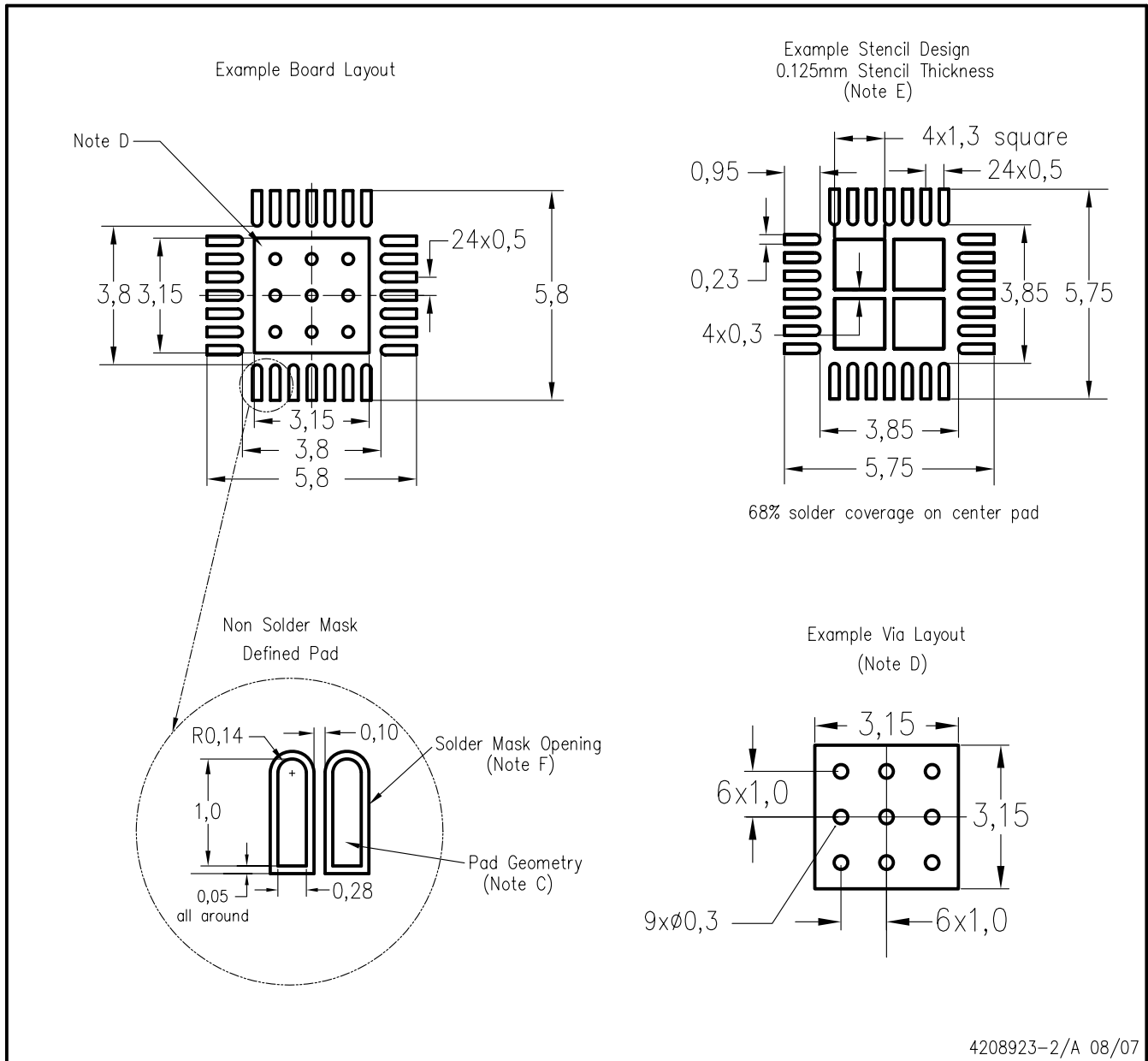


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHD (S-PQFP-N28)



4208923-2/A 08/07

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.



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