TPS62510 1.5-A, Low V_{IN} High Efficiency Step-Down Converter

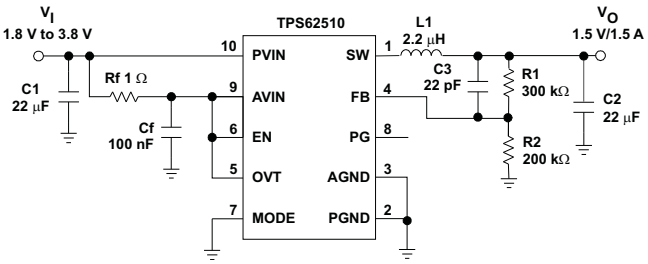
1 Features

- 1.8-V to 3.8-V Input Voltage Range
- Up to 96% High Efficiency Synchronous Step-Down Converter
- 1.5-MHz Fixed Frequency PWM Operation
- 1% Output Voltage Accuracy in Fixed Frequency PWM Mode
- Power Save Mode Operation for High Efficiency Over the Entire Load Current Range
- 22-µA Quiescent Current
- Adjustable Output Voltage
- Output Voltage Tracking (OVT) for Reliable Sequencing
- Available in a 3-mm × 3-mm 10-Pin VSON Package

2 Applications

- Portable Devices (Mobile Phone, Smartphone)
- 2-Cell NiMHd/Alkaline Applications
- Hard Disc Drives
- Point-of-Load Regulation
- Notebook Computers
- WiMAX and WLAN Applications

Typical Application Schematic



3 Description

The TPS62510 is a high-efficiency step-down converter targeted for operation from a 1.8-V to 3.8-V input voltage rail, ideally suited for 2-cell alkaline or NiMHd applications. The TPS62510 is also ideal as a point-of-load regulator running from a fixed 3.3-V, 2.5-V, or 1.8-V input voltage rail.

The converter operates in fixed frequency pulse width modulation (PWM) mode switching at 1.5 MHz with the MODE pin high. Pulling the MODE pin low enables the high efficiency mode. In high efficiency mode, the device operates with a 1.5-MHz fixed frequency PWM at nominal load current, and automatically enters the power save mode at light load currents. For maximum system reliability, the converter features *output voltage tracking* using the OVT pin to allow sequencing, and to allow for the output voltage to track an external voltage applied to this pin.

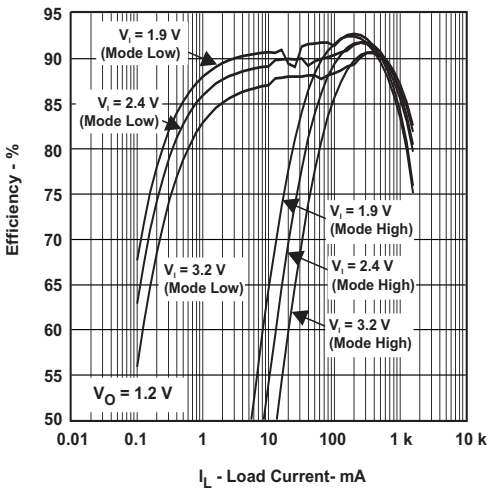
The TPS62510 is available in a 3-mm × 3-mm 10-pin VSON package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62510	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2009) to Revision B **Page**

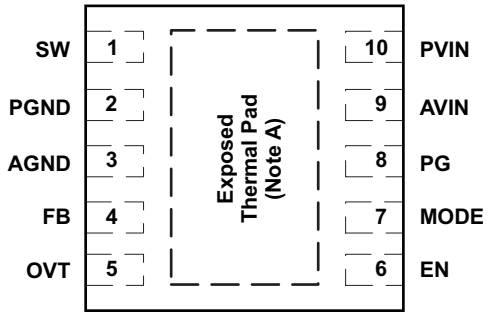
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (May 2006) to Revision A **Page**

- Changed V_{FB} - Feedback voltage inputs ... 5
- Added Note 4 to the Electrical Characteristics Table - Min/Max values established by characterization and not production tested. ... 5

5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



The exposed thermal pad is connected to AGND.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1	—	Switch pin of the converter. The inductor is connected here.
PGND	2	—	Power ground for the converter
AGND	3	—	Analog ground connection
FB	4	I	Feedback voltage sense input. Connect directly to V_{OUT} or to the midpoint of an external voltage divider for the adjustable version.
OVT	5	I	Output voltage tracking input. The signal applied to this pin is used as reference voltage overriding the internal reference voltage when it is below the internal 0.6-V reference. If this feature is not used, the OVT pin is connected to V_{IN}.
EN	6	I	Enable pin. A logic high enables the regulator, a logic low disables the regulator. This pin needs to be terminated and not left floating.
MODE	7	I	This pin is used to force fixed frequency PWM operation or to synchronize the device to an external clock signal. With MODE = High, the device is forced into 1.5-MHz fixed frequency PWM operation. With MODE = Low, the device automatically enters the power save mode at light load currents.
PG	8	O	Power good indication. This is a open drain output that is low when the device is disabled or the output voltage drops 10% below target.
AVIN	9	—	Power supply for control circuitry. Must be connected to the same voltage supply as PVIN through RC filter.
PVIN	10	—	Input voltage for the power stage. VIN must be connected to the same voltage supply as AVIN.
Exposed Thermal Pad	C2	—	Connect the exposed thermal pad to analog ground AGND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_S	Supply voltage at PVIN, AVIN	–0.3	4	V
	Voltage at EN, MODE, OVT, FB, PG (2)	–0.3	4	V
	Voltage at SW (2)	–0.3	V_{IN} + 0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage on pins PVIN and AVIN	1.8		3.8	V
V_{OUT}	Output voltage	0.6		V_{IN}	V
I_{OUT}	Output current, V_{IN} = 1.8 V to 3.6 V			1500	mA
L	Inductor value		2.2		µH
C_{IN}	Input capacitor value (1)		10		µF
C_{OUT}	Output capacitance value (1)		22		µF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See *Application and Implementation* for more information.

6.4 Thermal Information

THERMAL METRIC (1)		TPS62510 DRC [VSON] 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 3.3 V, OVT = EN = V_{IN}, MODE = GND, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{IN}	Input voltage			1.8		3.8	V
$I_{(q)}$	Power save mode quiescent current AVIN + PVIN		FB = FB nominal + 5%, MODE = Low		22	30	µA
	PWM Mode quiescent current into AVIN		MODE = High		4.4	5	mA
$I_{(SD)}$	Shutdown current into PVIN + AVIN		EN = Low, SW = GND		0.1	5	µA
UVLO	Undervoltage lockout threshold at AVIN		$V_{(AVIN)}$ falling (1)		1.55	1.58	V
	Undervoltage lockout hysteresis				150		mV
$T_{(SD)}$	Thermal shutdown threshold		Increasing junction temperature		160		°C
	Thermal shutdown hysteresis				20		°C
CONTROL SIGNALS EN, MODE							
V_{IH}	High level input voltage		V_{IN} = 1.8 V to 3.8 V	1.2			V
V_{IL}	Low level input voltage					0.4	V
I_{IB}	Input bias current				0.01	0.1	µA
$f_{(sync)}$	MODE synchronization range			1.15		2.25	MHz
	Duration of high or low level for synchronization signal (2)			75			ns
OUTPUT VOLTAGE TRACKING (OVT)							
I_{IB}	Input bias current				0.001	0.05	µA
V_{OS}	OVT offset voltage		V_{OS} = V(OVT) - V(FB), 0.1 V < V(OVT) < 0.5 V	–15		15	mV
POWER GOOD (PG)							
$V_{(th)}$	Power good threshold		Feedback voltage rising	–7% V_{OUT}	–5% V_{OUT}	–3% V_{OUT}	V
	Power good hysteresis			2% V_{OUT}		7% V_{OUT}	V
V_{OL}	Low level voltage		$I_{(PG)}$ = 1 mA			0.3	V
I_{lkg}	Power good leakage current		$V_{(PG)}$ = 3.8 V		1	100	nA
OUTPUT							
$R_{DS(on)}$	P-channel MOSFET on-resistance		V_{IN} = $V_{(GS)}$ = 1.8 V			330	mΩ
			V_{IN} = $V_{(GS)}$ = 3.3 V		120	170	
I_{lkg}	P-channel leakage current		V_{IN} = 3.6 V			10	µA
$R_{DS(on)}$	N-channel MOSFET on-resistance		V_{IN} = $V_{(GS)}$ = 1.8 V			200	mΩ
			V_{IN} = $V_{(GS)}$ = 3.3 V		80	130	
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 3.6 V			10	µA
I_F	Forward current limit (P- and N-channel)		1.8 V < V_{IN} < 3.8 V	1.75	2	2.25	A
f_s	Oscillator frequency		MODE = High	1.3	1.5	1.7	MHz
V_{ref}	Reference voltage				0.6		V
V_{FB}	Feedback voltage (3)	PFM operation	V_{IN} = (V_{OUT} + 0.3 V) to 3.8 V	–2%		5%	
			V_{IN} = (V_{OUT} + 0.2 V) to 3.8 V; V_{OUT}= 1.8 V, (4) C_2 = 15 µF, L_1= 2.1 µH (effective values), I_{OUT} = 0 mA to 150 mA	–2%		2.5%	
			V_{IN} = (V_{OUT} + 0.3 V) to 3.8 V; V_{OUT}= 2.5V, (4) C_2 = 15 µF, L_1= 2.1 µH (effective values), I_{OUT} = 0 mA to 150 mA	–1.3%		2.3%	
		PWM operation	V_{IN} = V_{OUT} + 0.3 V	–1%		1%	
I_{FB}	Feedback bias current		$V_{(FB)}$ = 0.6 V, EN = High		0.001	0.05	µA
	Line Regulation		V_{IN} = V_{OUT} + 0.3 V (minimum 1.8 V) to 3.8 V; I_{OUT} = 800 mA		0		%/V
	Load Regulation		I_{OUT} = 10 mA to 1500 mA, PWM mode		0.1		%/A
t_{SS}	Soft start time		V_{OUT} ramping from 5% to 95% of nominal value		750		µs

(1) The undervoltage lockout threshold is detected at the AVIN pin. Current through the RC filter causes a UVLO trip at higher V_{IN}
(2) The minimum and maximum duty cycle applied to the MODE pin is calculated as: D(min) = 75 ns × $f_{(sync)}$ and D(max) = 1 - 75 ns × $f_{(sync)}$.
(3) When using the output voltage tracking function, the feedback regulates to the voltage applied to OVT as long as the OVT < 0.6 V.
(4) Minimum and maximum values established by characterization and not production tested. Includes line and load regulation in PFM mode operation. For the measurements, a proper PCB layout and usage of recommended inductors and capacitors are essential.

Electrical Characteristics (continued)

V_{IN} = 3.3 V, OVT = EN = V_{IN}, MODE = GND, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Leakage resistance from SW pin to GND	$V_{IN} > V_{OUT}$, 0 V ≤ $V_{(SW)}$ ≤ V_{IN}	700	1000		kΩ
Leakage resistance from FB pin to GND	EN = Low	17	23		

6.6 Typical Characteristics

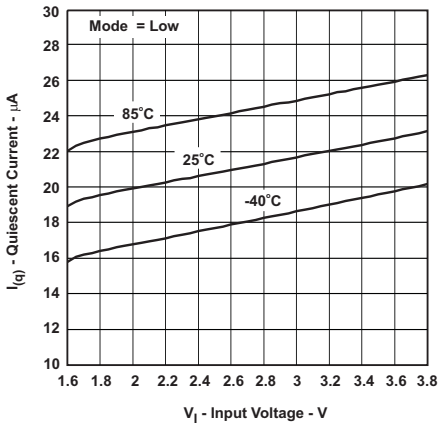


Figure 1. No Load Quiescent Current vs Input Voltage, MODE = Low

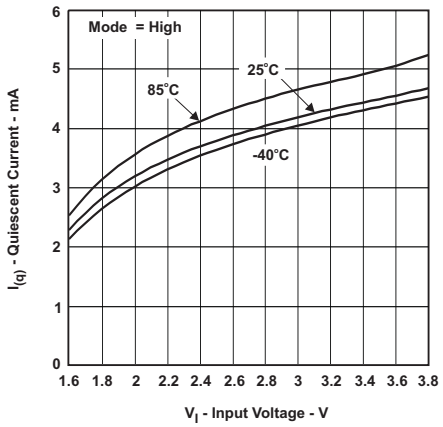


Figure 2. No Load Quiescent Current vs Input Voltage, MODE = High

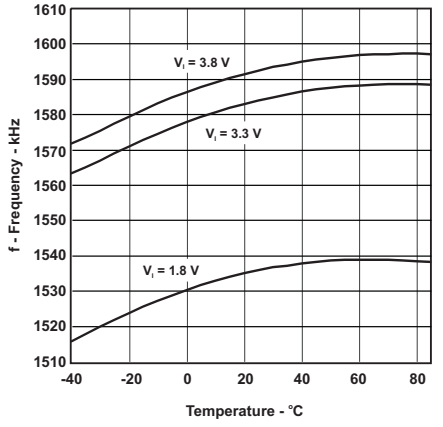


Figure 3. Frequency vs Temperature

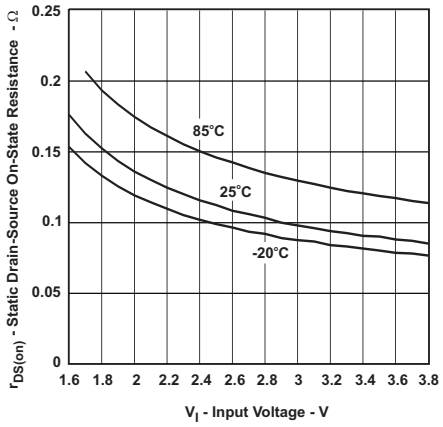


Figure 4. PMOS $R_{DS(on)}$ vs Input Voltage

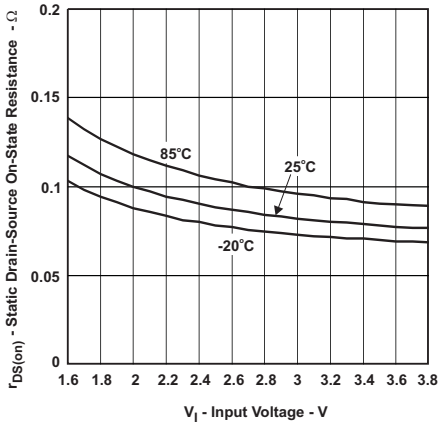


Figure 5. NMOS $R_{DS(on)}$ vs Input Voltage

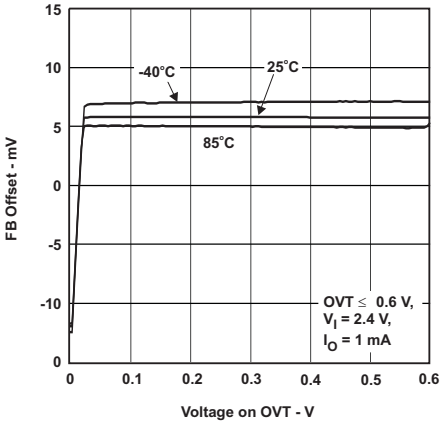


Figure 6. FB Offset vs Voltage ON V_{OUT}

7 Detailed Description

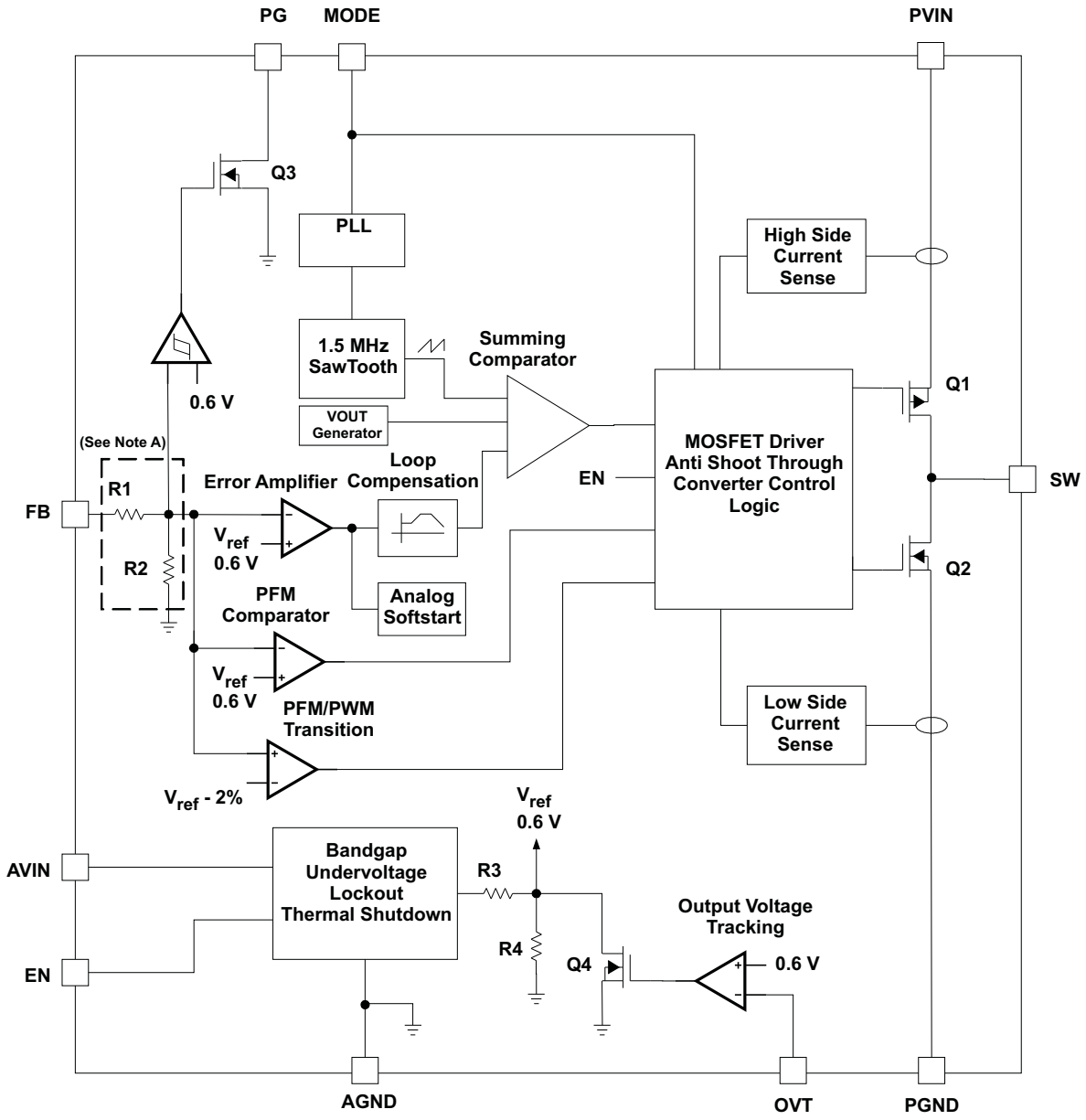
7.1 Overview

The TPS62510 has two target areas of operation. The high efficiency area is defined when the MODE pin is held low. In this condition, the converter operates at typically 1.5-MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters power save mode and operates with pulse frequency modulation (PFM) mode. Low noise operation is defined when the MODE pin is held high. In this condition, the converter is forced into fixed frequency PWM mode and runs at 1.5 MHz. The converter is capable of delivering 1.5-A output current.

The TPS62510 can also be synchronized to an external clock in the frequency range between 1.15 MHz and 2.25 MHz. Synchronization is aligned with the falling edge of the incoming clock signal. This allows simple synchronization of two step-down converters running 180° out of phase reducing overall input RMS current.

During PWM operation, the converters use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line, and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time, which is used to prevent shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the P-channel switch.

7.2 Functional Block Diagram



A. R1 and R2 are only used for the fixed output voltage version.

7.3 Feature Description

7.3.1 Output Voltage Tracking (OVT)

In applications where a processor or FPGA is powered, it is important that the I/O voltage and core voltage start-up in a controlled way to avoid possible processor and FPGA latch-up. To implement this, the TPS62510 has an output voltage tracking feature where the internal reference voltage for the error amplifier follows the voltage applied to OVT, until OVT reaches V_{ref}. V_{ref} is the nominal internal reference voltage, typically 0.6 V. Figure 7 shows a typical application where an external voltage (V1) is applied to OVT pin using a resistor divider.

Feature Description (continued)

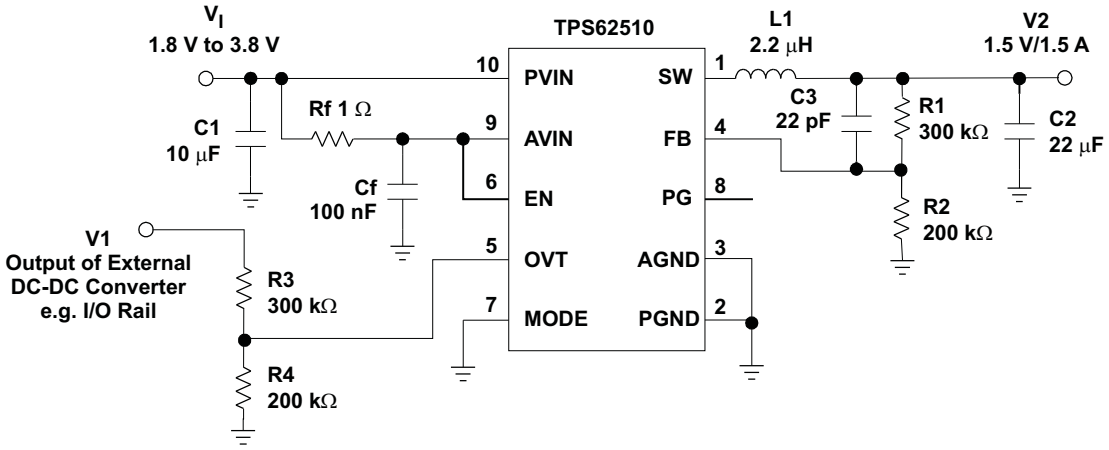


Figure 7. Output Voltage Tracking, V2 Tracks V1

In this application, the output voltage (V2) of the TPS62510 tracks the voltage (V1) as long as the OVT voltage is smaller than the internal device reference voltage, V_{ref} = 0.6 V. Depending on the resistor divider (R3, R4), the tracking can be adjusted. V2 can rise faster, at the same timer, or slower than V1.

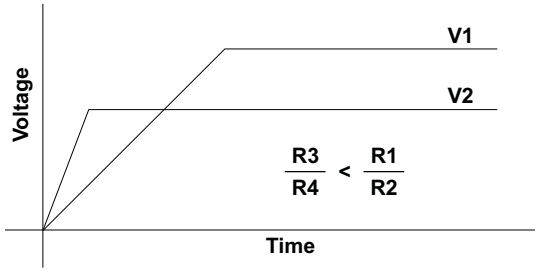


Figure 8. V2 Comes Up Before V1

Simultaneous tracking is achieved when the resistor divider (R3/R4) is equal to the resistor divider of the TPS65210.

$$\frac{R3}{R4} = \frac{V2 - V_{ref}}{V_{ref}} = \frac{1.5\ V - 0.6\ V}{0.6\ V} = 1.5 \quad (1)$$

$$V2_{(tracking)} = V_{(OVT)} \times \frac{V2}{V_{ref}} = V1 \times \frac{R4}{R3 + R4} \times \frac{V2}{V_{ref}} = V1 \frac{200\ k}{300\ k + 200\ k} \times \frac{1.5\ V}{0.6\ V} = V1 \quad (2)$$

If V2 needs to rise before V1, then R4 must be increased as shown in Figure 9.

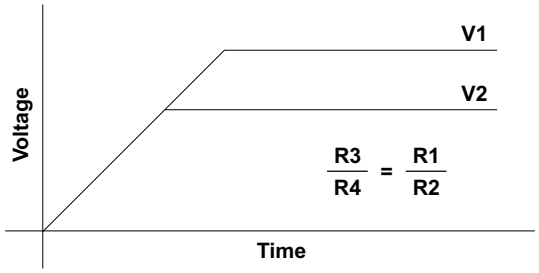


Figure 9. Simultaneous Tracking of V2 and V1

Feature Description (continued)

If V2 needs to rise after V1, then R4 must be decreased as shown in Figure 10.

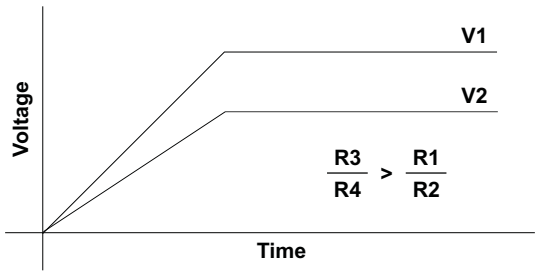


Figure 10. V2 Comes Up After V1

7.3.2 Power Good

The power good output can be used for sequencing purposes, enabling a separate regulator once the output voltage is reached, or to indicate that the output voltage is in regulation. When the device is disabled, the PG pin is pulled low by the internal open-drain output transistor. Internally, the TPS62510 compares the feedback voltage FB to the nominal reference voltage of typically 0.6 V. If the feedback voltage is more than 95% of this value then the power good output goes high impedance. If the feedback voltage is less than 90% of the reference voltage then PG pin is pulled low.

7.3.3 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages. It disables the converter. The UVLO circuit monitors the AVIN pin, the falling threshold is set internally to 1.55 V with 150-mV hysteresis. Note that when the DC/DC converter is running, there is an input current at the AVIN pin, which is up to 5 mA when in PWM mode. This current must be taken into consideration if an external RC filter is used at the AVIN pin to remove switching noise from the TPS62510 internal analog circuitry supply.

7.3.4 Thermal Shutdown

As soon as the device junction temperature exceeds 160°C (typical), all switching activity ceases and both high-side and low-side power transistors are off. The device continues operation once the temperature fall to 20°C (typical) below its thermal shutdown threshold of 160°C.

7.4 Device Functional Modes

7.4.1 Soft Start

The converter has an internal soft start circuit that limits the inrush current during start-up. The soft start is realized by using a low current to control the output of the error amplifier during start-up. The soft start time is typically 750 µs to ramp the output voltage to 95% of the final target value. There is a short delay of typically 120 µs between the converter being enabled and switching activity actually starting. See the typical soft start characteristic shown in Figure 20.

7.4.2 100% Duty Cycle Low Dropout Operation

The TPS62510 converter offers a low input to output voltage difference while maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage, as shown in Equation 3.

$$V_I\,min = V_O\,min + I_O\,max \times \left(r_{DS(on)}\,max + R_L\right)$$

where

- $I_O$max = Maximum load current (Note: ripple current in the inductor is zero under these conditions)
- $R_{DS(on)}$max = Maximum P-channel switch $R_{DS(on)}$

Device Functional Modes (continued)

- RL = DC resistance of the inductor
- $V_O$min = Nominal output voltage minus 2% tolerance limit (3)

7.4.3 Power Save Mode Operation (MODE)

When the MODE pin is connected to GND, the device automatically enters the power save mode when the average output current reaches the appropriate threshold. This reduces the switching frequency and minimum quiescent current, maintaining efficiency over the entire load current range. For low noise operation, the device can be forced into fixed frequency PWM mode operating at 1.5 MHz over the entire load current range. This is done by pulling the MODE pin high.

Many applications require a low output ripple voltage during power save mode. This is accomplished by a single threshold PFM comparator which allows control of the output voltage ripple in power save mode. The larger the output capacitor value, the smaller the output voltage ripple (see Figure 19). During power save mode, the device monitors the output voltage with the PFM comparator. As soon as the output voltage falls below the nominal output voltage, the device starts switching for a minimum of 1 µs (typical), or until the output voltage is above the nominal output voltage.

7.4.4 Power Save Mode Transition Thresholds

To achieve an accurate transition into and out of power save mode, the device monitors the average inductor current which is equal to the average output current. The device enters power save mode when the average output current is ≤ $I_{(PFM\ enter)}$ as calculated in Equation 4.

$$I_{(PFM\ enter)} = \frac{VIN}{22\ \Omega} \quad (4)$$

The device leaves the power save mode when the output current is ≥ $I_{(PFM\ enter)}$.

$$I_{(PFM\ leave)} = \frac{VIN}{17\ \Omega} \quad (5)$$

To minimize any delay times during a load transient, the device enters PWM mode when the output voltage is 2% below the nominal value, and the PFM/PWM transition comparator trips.

7.4.5 Short-Circuit Protection

The TPS62510 monitors the forward current through both the high-side and low-side power devices. This enables the converter to limit the short-circuit current, which helps to protect the device and other circuits connected to its output.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS62510 is a high-efficiency step-down converter targeted for operation from a 1.8-V to 3.8-V input voltage rail, ideally suited for 2-cell alkaline or NiMHd applications. The TPS62510 is also ideal as a point-of-load regulator running from a fixed 3.3-V, 2.5-V or 1.8-V input voltage rail.

8.2 Typical Application

Figure 11 shows the adjustable version programming to 1.5 V.

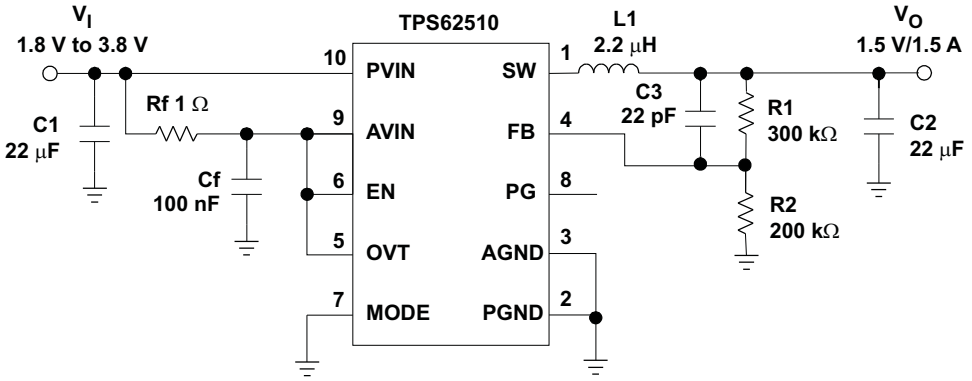


Figure 11. Adjustable Version Programmed to 1.5 V Example

8.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. The output voltage tracking is not used and the output voltage is programmed using the external voltage divider. The connection of the power good output is shown in one of the system examples.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. The converter needs a ceramic input capacitor of 22 µF. The input capacitor may be increased without any limit for better input voltage filtering. The AVIN pin is separated from the power input of the converter. Note that the filter resistor may affect the undervoltage lockout threshold since up to 5 mA can flow via this resistor into the AVIN pin when the converter runs in PWM mode.

Table 1. Input Capacitor Selection

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	1206	TDK C3216X5R0J226M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic

8.2.2.2 Output Filter Design (Inductor and Output Capacitor)

The TPS62510 step-down converter has an internal loop compensation. Therefore, the external L-C filter must be selected to work with the internal compensation.

The internal compensation is optimized to operate with an output filter of L = 2.2 µH with an output capacitor of C_{OUT} = 22 µF. The output filter has its corner frequency per Equation 6:

$$f_c = \frac{1}{2\pi \times \sqrt{L \times C_O}} = \frac{1}{2\pi \times \sqrt{2.2\ \mu H \times 22\ \mu F}} = 22.8\ kHz \quad (6)$$

where

- L = 2.2 µH
- C_O = 22 µF

As a general rule of thumb, the product L x C should not move over a wide range when selecting a different output filter. This is because the internal compensation is designed to work with a certain output filter corner frequency, as calculated in Equation 6. This is especially important when selecting smaller inductor or output capacitor values that move the corner frequency to higher frequencies. However, when selecting the output filter a low limit for the inductor value exists due to other internal circuit limitations. The minimum inductor value for the TPS62510 should be kept at 2.2 µH. Selecting a larger capacitor value is less critical because the corner frequency drops, causing fewer stability issues.

Table 2. Output Capacitor Selection

L	C_O
2.2 µH	≥22 µF (ceramic capacitor)
3.3 µH	≥22 µF (ceramic capacitor)(1)

(1) For output currents <800 mA, a 10-µF output capacitor is sufficient.

8.2.2.3 Setting the Output Voltage Using the Feedback Resistor Divider

The external resistor divider sets the output voltage of the converter.

The output voltage is calculated as:

$$V_O = 0.6\ V \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

where

- R1 + R2 ≤ 1 MΩ
- The internal reference voltage is V_{ref} typical = 0.6 V

To keep the operating quiescent current to a minimum, a high impedance feedback divider is selected with R1 + R2 ≤ 1 MΩ. The sum of R1 and R2 should not be greater than 1 MΩ to avoid possible noise related regulation issues. A feedforward capacitor is needed across the upper feedback resistor to place a zero at a frequency of 25 kHz in the control loop. After selecting the feedback resistor values, the feedforward capacitor is calculated as:

$$C_{ff} = \frac{1}{2\pi \times f_z \times R1} = \frac{1}{2\pi \times 25\ kHz \times R1} \quad (8)$$

where

- R1 = upper resistor of voltage divider
- C_{ff} = upper capacitor of voltage divider

Select the capacitor value that is closest to the calculated value.

8.2.2.4 Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high switching frequencies where the core material has a higher impact on the efficiency. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. However, larger inductor values cause slower load transient response. Usually, the inductor ripple current as calculated in Equation 9, should be around 20% of the average output current.

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current calculated in Equation 9:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L\,max = I_O\,max + \frac{\Delta I_L}{2} \tag{9}$$

where

- f = Switching frequency (1.5 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current

The highest inductor current occurs at maximum V_{IN}.

A more conservative approach is to select the inductor current rating just for the maximum typical switch current limit of the converter of 2 A. See Table 3 for inductor recommendations.

Table 3. Inductor Recommendations

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS	$I_{(SAT)}$ / $R_{(DC)}$
2.2 µH	Sumida CDRH2D18/HP 4R7	3.2 mm × 3.2 mm × 2 mm	1.6 A / 60 mΩ
2.2 µH	Wuerth 744045002	4.5 mm × 3.2 mm × 2.6 mm	1.6 A / 110 mΩ
2.2 µH	Sumida CDRH3D14	4 mm × 4 mm × 1.8 mm	1.75 A / 69 mΩ
2.2 µH	Sumida CDRH4D22	5 mm × 5 mm × 2.4 mm	1.8 A / 25.4 mΩ
2.2 µH	Sumida CDRH4D28	5 mm × 5 mm × 3 mm	2 A / 31.3 mΩ
2.2 µH	Coilcraft MSS5131	5.1 mm x 5.1 mm × 3.1 mm	1.9 A / 23 mΩ
2.2 µH	Coilcraft DO1608	6.6 mm × 4.45 mm × 2.92 mm	2.3 A / 28 mΩ
2.2 µH	Wuerth 74455022	6.6 mm × 4.45 mm × 2.92 mm	2.3 A / 28 mΩ

8.2.3 Application Curves

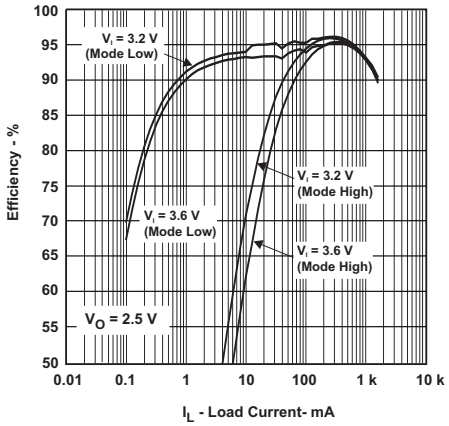


Figure 12. Efficiency vs Load Current, V_{OUT} = 2.5 V

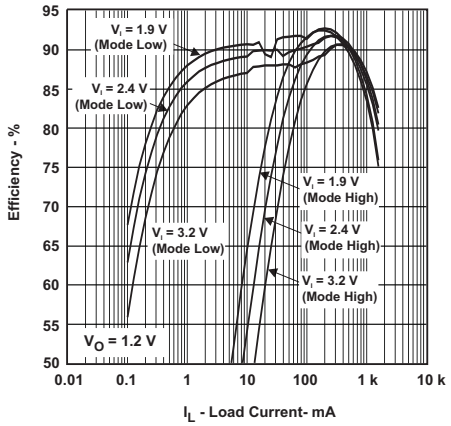


Figure 13. Efficiency vs Load Current, V_{OUT} = 1.2 V

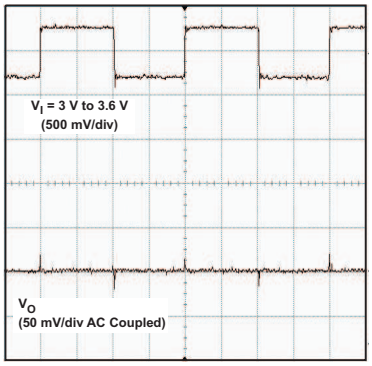


Figure 14. Line Transient Response

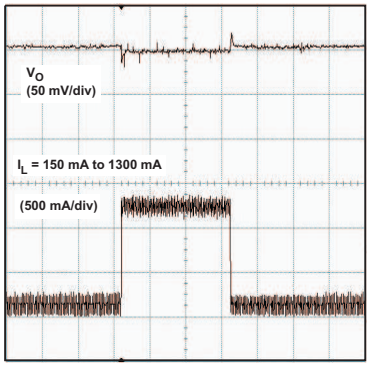


Figure 15. Load Transient Response, MODE = High

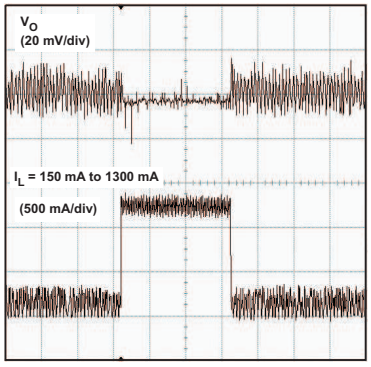


Figure 16. Load Transient, MODE = Low

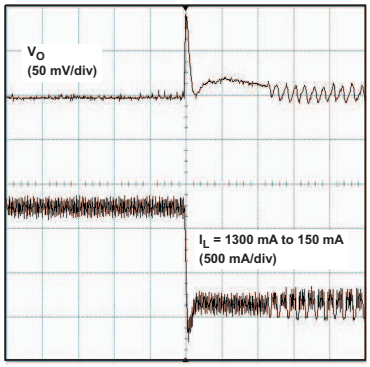


Figure 17. Falling Load Transient Response, MODE = Low

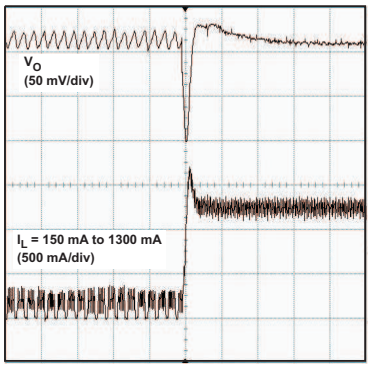


Figure 18. Rising Load Transient Response, MODE = Low

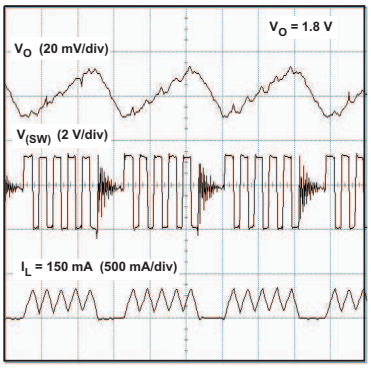


Figure 19. Power Save Mode Operation

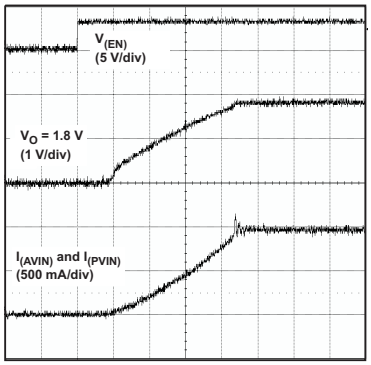


Figure 20. Soft Start-Up

8.3 System Example

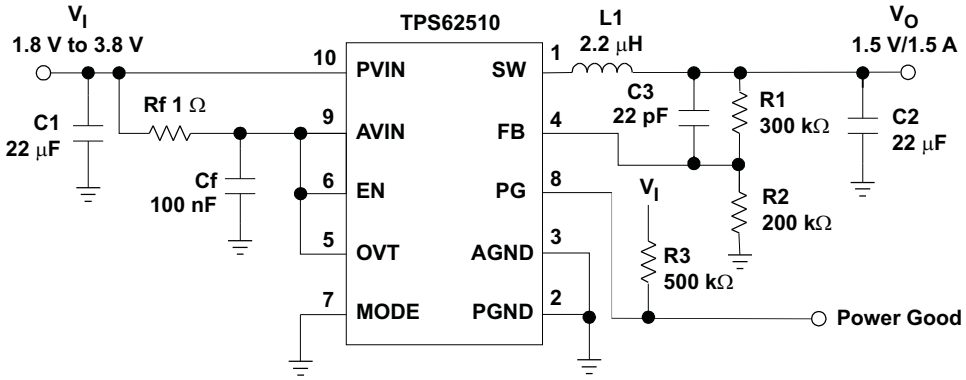


Figure 21. Adjustable Version Programmed to 1.5 V Using Power Good Example

9 Power Supply Recommendations

The TPS62510 has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS62510.

10 Layout

10.1 Layout Guidelines

1. Place and route the power components first (C1, L1, C2).
2. The input capacitor (C1) must be placed as close as possible from PVIN to PGND.
3. The inductor must be placed as close as possible to the switch pin.
4. All ground connections (shown in bold) must be on a common ground plane or form a star ground.
5. Analog ground (AGND) and power ground (PGND), as well as the exposed thermal pad, must be tight together.
6. The feedback network (R1, C3, R2) must be routed away from the inductor (L1) and should be grounded to the exposed thermal pad.
7. The feedback network must sense and regulate the output voltage across the output capacitor to minimize load regulation.

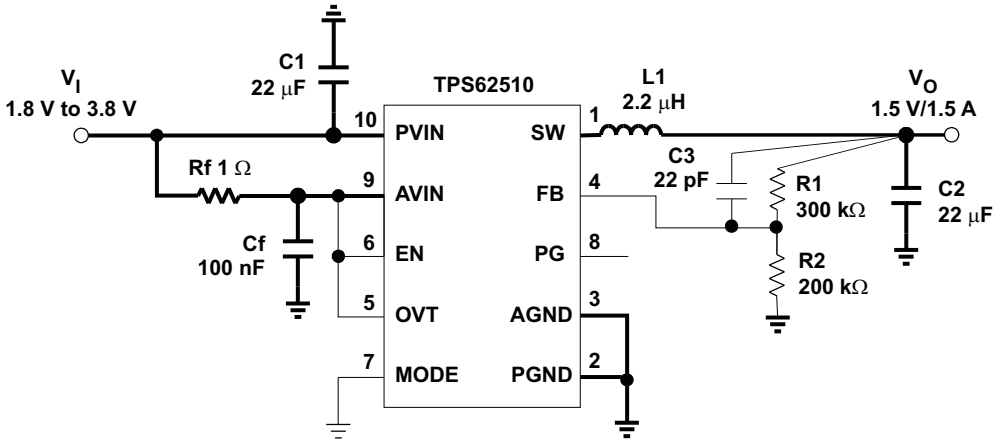


Figure 22. Layout Guidelines

10.2 Layout Example

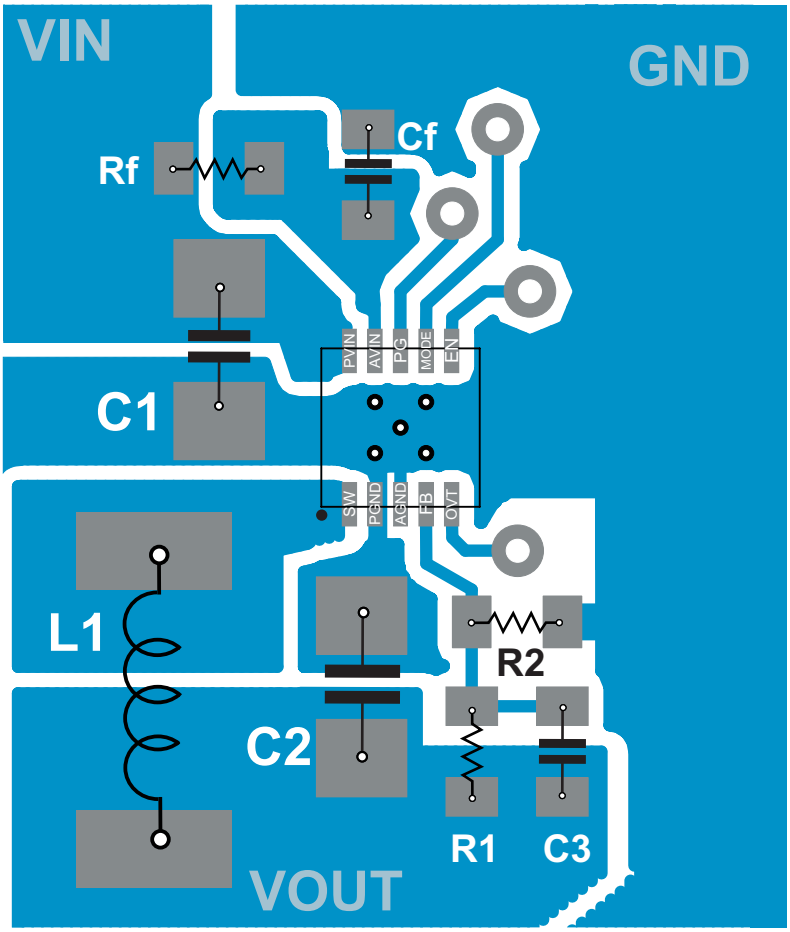


Figure 23. Recommended Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62510DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQA	Samples
TPS62510DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQA	Samples
TPS62510DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQA	Samples
TPS62510DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

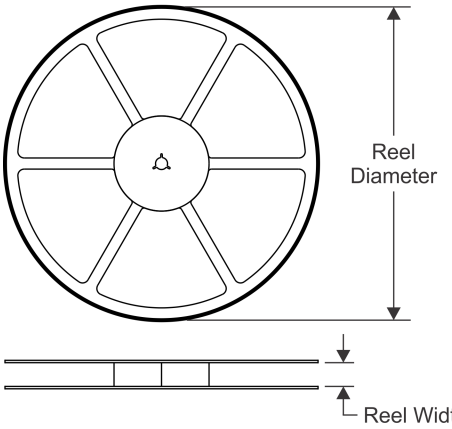
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

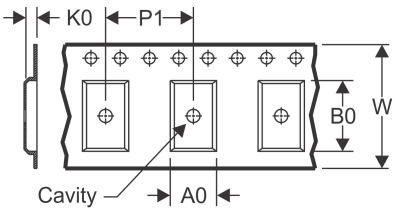
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

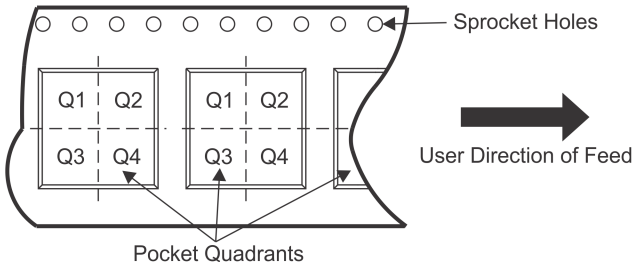


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

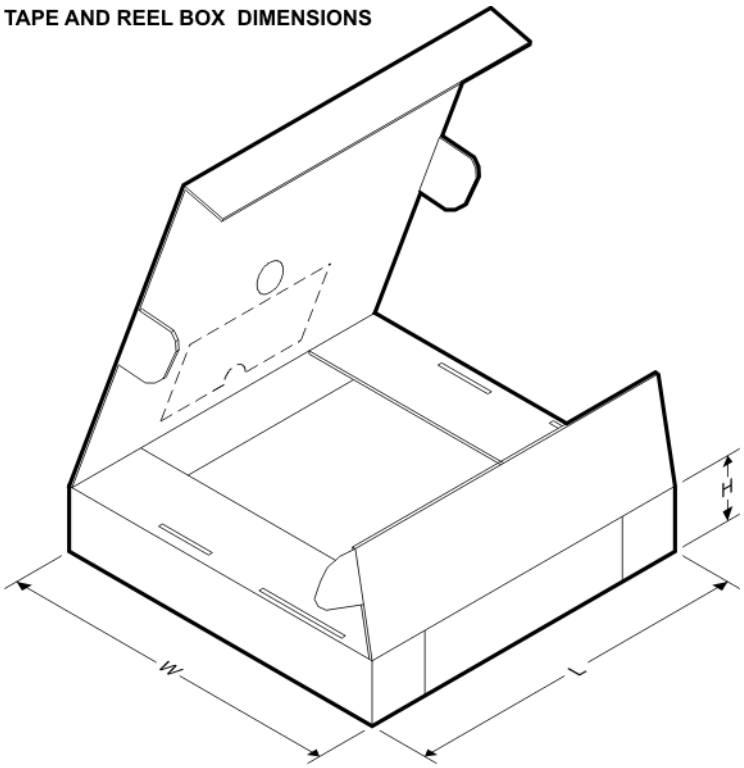
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62510DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62510DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62510DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62510DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

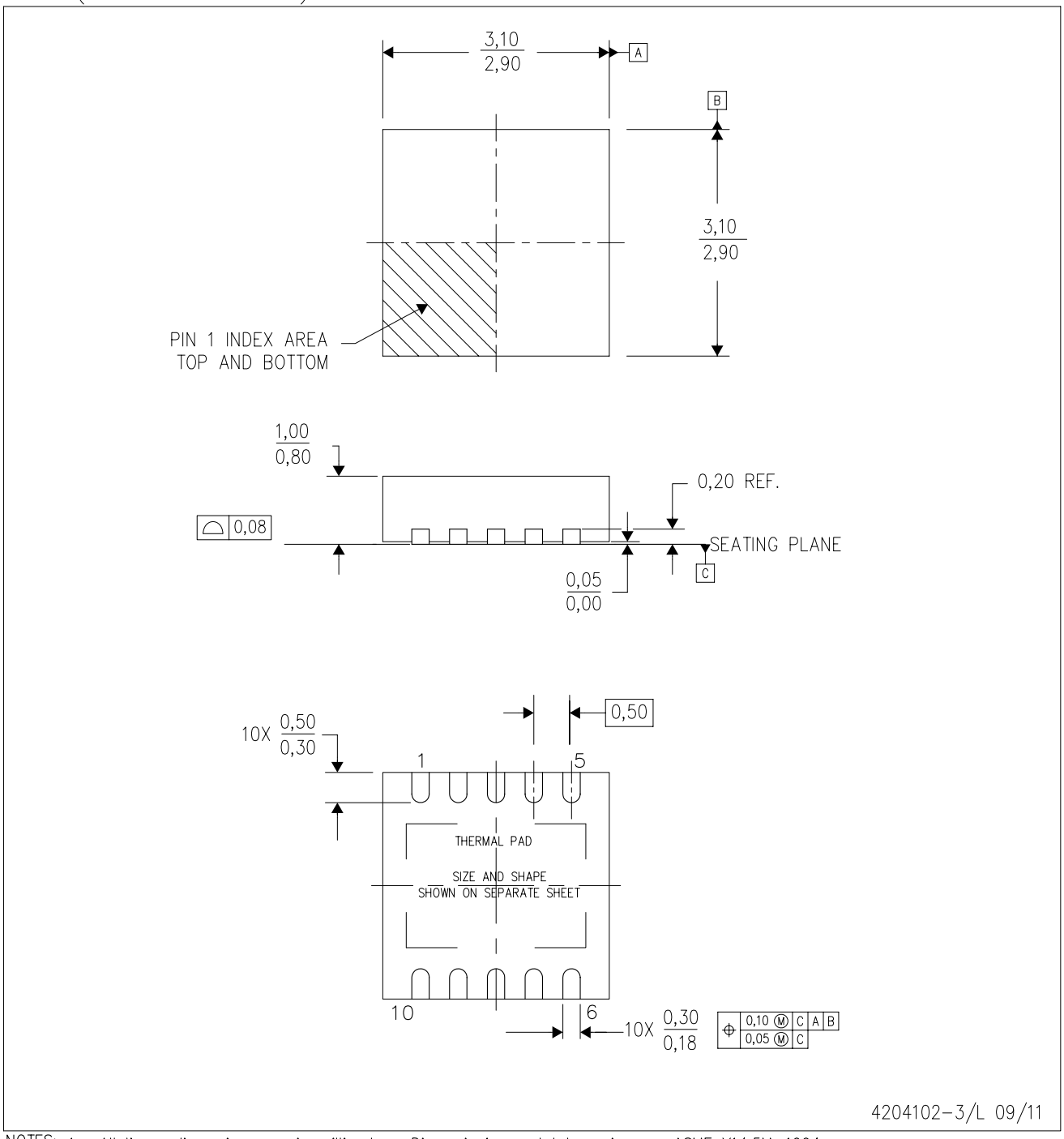
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62510DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62510DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62510DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS62510DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

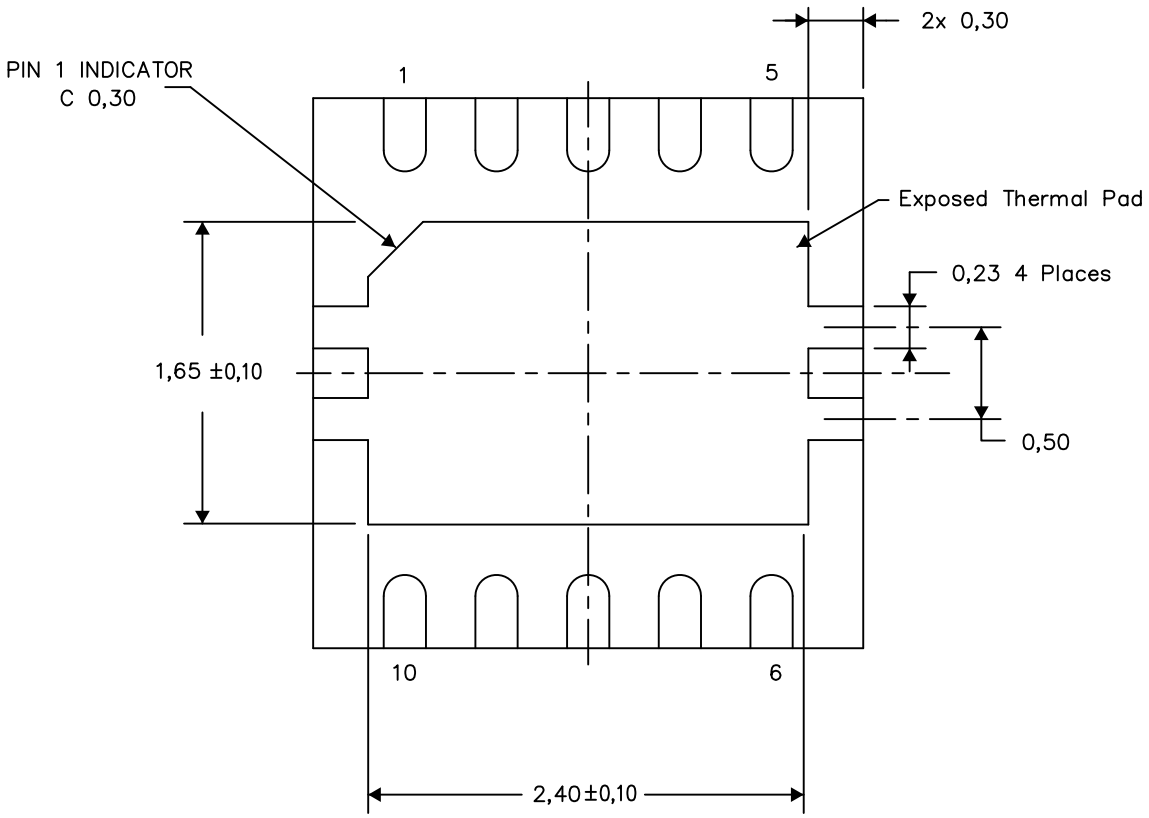
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



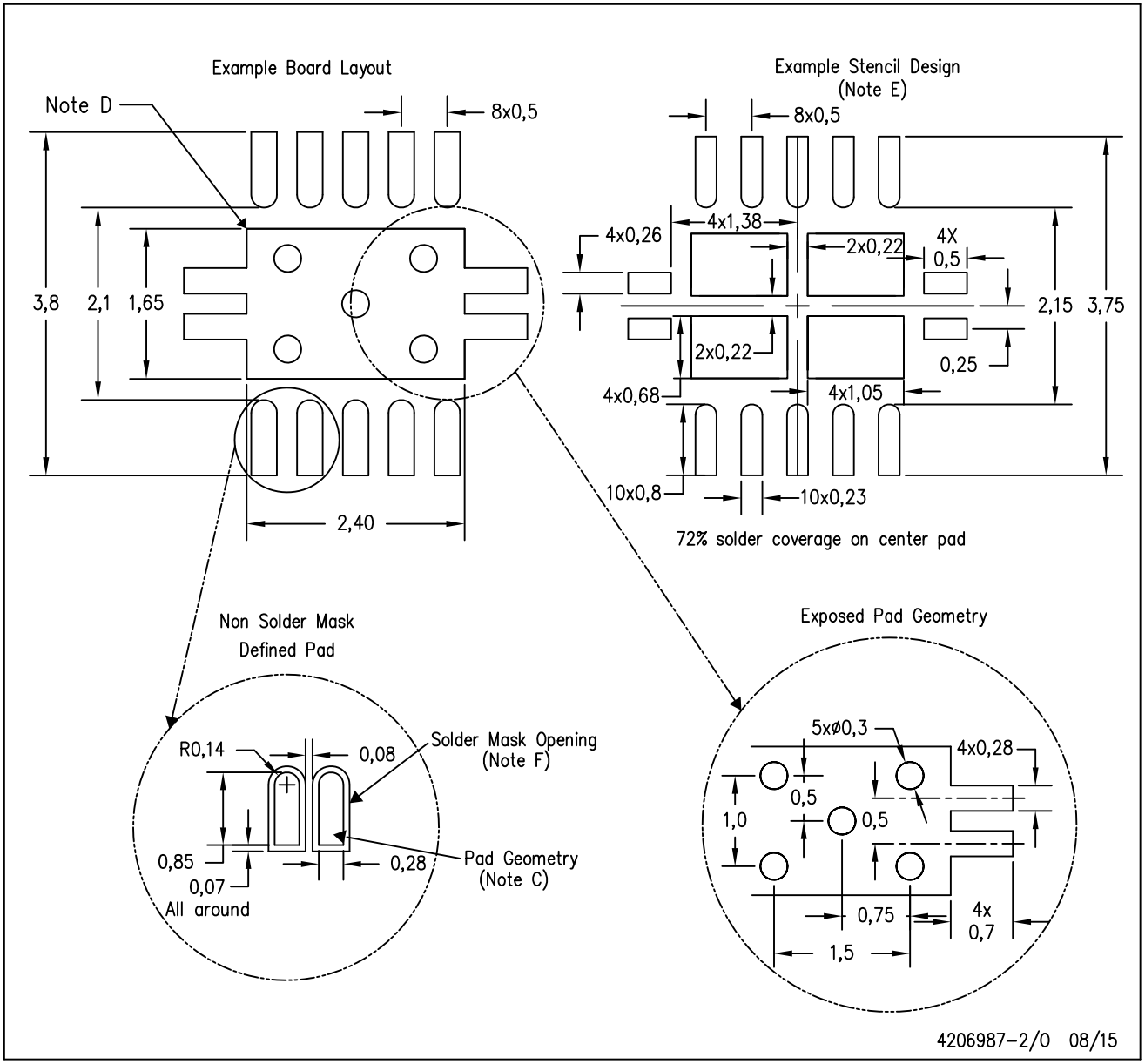
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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