TPS62134x, 17-V Input, Step-down Converter With Low-Power Mode Input for Intel Skylake Platform

1 Features

- DCS-Control™ Architecture
- Supports Low-Power Mode for System Standby Mode
- Power Save Mode for Light Load Efficiency
- Selectable Fixed Output Voltage (0.7 V to 1.05 V)
- Low Power Mode Logic Input
- Quiescent Current of 20 µA
- Input Voltage Range: 3 V to 17 V
- Output Current: up to 3.2 A
- Programmable Soft Start
- Power Good Output
- Short Circuit Protection
- Single-ended Remote Sense
- Thermal Shutdown Protection
- Available in a 3-mm × 3-mm, VQFN-16 Package

2 Applications

- Intel Skylake™ Platform Ultrabook, Notebook, PC
- Standard 12-V Rail Supply
- POL Supply from 1 to 4 Cells Li-Ion Battery
- Solid-State Disk Drive
- Embedded System

3 Description

The TPS62134x family of devices is an easy-to-use, synchronous step-down DC-DC converter, compatible with Intel Skylake platform applications such as Ultrabooks™ and notebooks. The high performance DCS-Control™ architecture provides fast transient response as well as high output voltage accuracy.

With a wide operating input-voltage range of 3 to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other batteries as well as from 12-V intermediate power rails. The devices have a low-power mode where the output voltage is reduced by using the LPM pin. In addition, the devices support dynamic output-voltage change by using the VIDx pins. The LPM and VIDx pins help the system minimize power consumption in different operating modes.

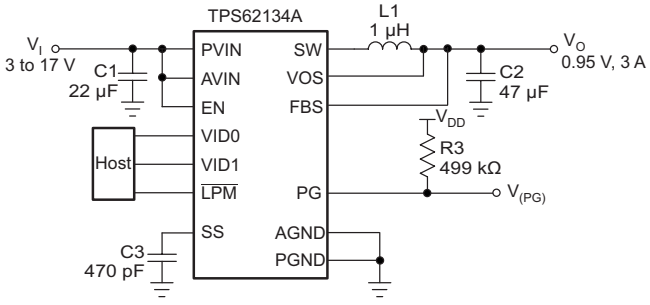
The output-voltage startup ramp is controlled by the SS pin. The power sequencing is configurable by the enable (EN) and power good (PG) pins. In power-save mode, the devices show quiescent current of approximately 20 µA which maintains high efficiency over the entire load range. Short circuit protection and thermal shutdown protect the IC and external components from heavy current when the output is shorted to ground. The device is available in a 3-mm × 3-mm 16-pin VQFN package with thermal pad.

Device Information(1)

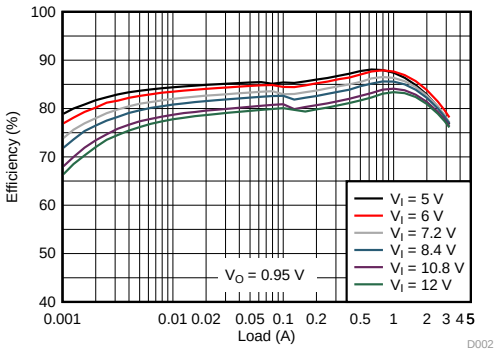
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62134A	VQFN	3.00mm x 3.00mm
TPS62134B		
TPS62134C		
TPS62134D		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Circuit



TPS62134A Efficiency



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- Added the *Program Output Voltage with External Resistor Divider* section ... 13

Changes from Revision B (August 2014) to Revision C — **Page**

- Changed the *Device Information* table ... 1
- Added the Device Comparison Table ... 3
- Moved the Storage temperature From the *Handling Ratings* table to the *Absolute Maximum Ratings*(1) table ... 4
- Changed the *Handling Ratings* table to the *ESD Ratings* table ... 4
- Changed the Output voltage accuracy, PSM mode MAX value From: 2% To: 3%, Add test condition: $\overline{\text{LPM}}$ = High. ... 5

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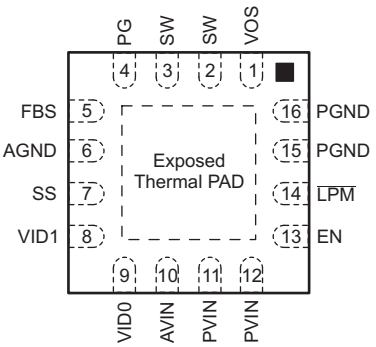
- Switched the pin names of pin 8 and 9 in the *Pin Functions* table ... 3

6 Device Comparison Table

PART NUMBER	PACKAGE MARKING	OUTPUT VOLTAGE
TPS62134A	134A	See Table 1
TPS62134B	134B	
TPS62134C	134C	
TPS62134D	134D	

7 Pin Configuration and Functions

RGT Package
16-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOS	I	Output voltage sense pin and connection for the control loop circuitry. The VOS pin must be connected directly at the output capacitor.
2	SW	PWR	This pin is a switch node and is connected to the internal MOSFET switches. Connect an inductor between the SW pin and output capacitor.
3			
4	PG	O	Output power-good pin. The PG pin is an open drain and requires a pullup resistor. If this pin is not in use, leave it floating.
5	FBS	I	Output-voltage feedback pin. This pin is used for a positive remote sense of the load voltage. The FBS pin must be connected close to the load-supply node on the output bus.
6	AGND	—	Analog ground pin. The AGND pin must be connected directly to the exposed thermal pad and common ground plane.
7	SS	O	Soft-start pin. An external capacitor connected to this pin sets the soft-start time.
8	VID1	I	Output-voltage selection pins (VIDx).
9	VID0		
10	AVIN	I	Supply-voltage pin for the internal control circuitry. Connect the AVIN pin to the same source as the PVIN pin.
11	PVIN	PWR	Supply-voltage pins for the internal power stage.
12			
13	EN	I	Enable and disable input pin. An internal pulldown resistor maintains logic-level low if the pin is floating.
14	$\overline{\text{LPM}}$	I	Low-power-mode input pin.
15	PGND	—	Power ground. The PGND pin must be connected directly to the exposed thermal pad and common ground plane.
16			
—	Exposed Thermal Pad	—	The exposed thermal pad must be connected to the AGND (6) pin, PGND (15 and 16) pins, and common ground plane. The thermal pad must be soldered to achieve appropriate power dissipation and mechanical reliability.

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage at pins(2)	AVIN, PVIN	–0.3	20	V
	EN, SW	–0.3	V_I + 0.3	
	SS, PG, VOS, VID0, VID1, $\overline{LPM}$	–0.3	7	
	FBS	–0.3	3	
Sink current	PG	0	2	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommend Operating Conditions

over operating junction temperature range, unless otherwise noted.

			MIN	MAX	UNIT
V_I	Input voltage (AVIN, PVIN)		3	17	V
$V_{(PG)}$	PG pin pullup resistor voltage		0	6	V
I_O	Output current	3 V ≤ V_I < 5 V	0	3	A
		5 V ≤ V_I ≤ 17 V	0	3.2	
T_J	Operating junction temperature		–40	125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS62134x RGT Package	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	16.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953

8.5 Electrical Characteristic

T_J = –40 °C to 125 °C and V_I = 3 V to 17 V. Typical values at V_I = 12 V and T_J = 25 °C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_I	Input voltage range		3		17	V
I_Q	Operating quiescent current	EN = High, no load, device not switching T_J = –40 °C to 85 °C		20	35	µA
		T_J = 125 °C			58	
I_{SD}	Shutdown current into AVIN and PVIN	EN = Low T_J = –40 °C to +85 °C		2	9	µA
		T_J = 125 °C			18	
$V_{(UVLO)}$	Undervoltage lockout threshold	V_I falling	2.6	2.7	2.8	V
		V_I rising	2.8	2.9	3	
$T_{SD(th)}$	Thermal shutdown threshold	T_J rising		160		°C
$T_{SD(hys)}$	Thermal shutdown hysteresis	T_J falling		20		
CONTROL (EN, SS, PG, VIDx, $\overline{LPM}$)						
V_{IH}	High-level input threshold voltage (EN, VIDx, $\overline{LPM}$)		0.8	0.54		V
V_{IL}	Low-level input threshold voltage (EN, VIDx, $\overline{LPM}$)			0.47	0.3	V
$R_{(PD)}$	Pull down resistor at EN, VIDx, $\overline{LPM}$	EN, VIDx, $\overline{LPM}$ = low		400		kΩ
$R_{(DIS)}$	Output discharge resistor	EN = Low, V_O = 1 V		20		kΩ
I_{lkg}	Input leakage current at EN, VIDx, $\overline{LPM}$	EN, VIDx, $\overline{LPM}$ = 3.3 V		0.01	1	µA
$V_{TH(PG)}$	Power good threshold DC voltage	V_O rising	736	760	784	mV
		V_O falling	696	720	752	
$V_{OL(PG)}$	Power good output low voltage	$I_{(PG)}$ = –2 mA		0.07	0.3	V
$I_{lkg(PG)}$	Input leakage current at PG	$V_{(PG)}$ = 1.8 V		1	400	nA
$t_{d(PG)}$	Power good delay time	PG rising		140		µs
		PG falling		20		
$I_{(SS)}$	SS pin source current		2.3	2.5	2.7	µA
POWER SWITCH						
$r_{DS(on\_H)}$	High-side MOSFET on-resistance	V_I ≥ 6 V		90	170	mΩ
$r_{DS(on\_L)}$	Low-side MOSFET on-resistance	V_I ≥ 6 V		40	70	
I_L	High-side MOSFET DC current-limit	V_I ≥ 5 V, T_J = 25 °C	3.6	4.4	5.4	A
$I_{L(LOW)}$	High-side MOSFET DC current-limit at low output voltage	V_O ≤ 0.3 V		1.6		
OUTPUT						
$I_{lkg(FBS)}$	Input leakage current at FBS	$V_{(FBS)}$= 1.1 V		1	100	nA
$V_{O(A)}$	Output voltage accuracy	PWM mode	–1%		1%	
		PSM mode, $\overline{LPM}$ = High(1)	–1%		3%	
$\Delta V_{O(\Delta IO)}$	Load regulation(2)	V_I = 7.2 V, I_O = 0.5 A to 3.2 A		0.01		%/A
$\Delta V_{O(\Delta VI)}$	Line regulation(2)	3 V ≤ V_I ≤ 17 V, I_O = 1 A		0.003		%/V

(1) This is the accuracy provided by the device itself (line and load regulation effects are not included). External components effective value: L = 1 µH and $C_{(OUT)}$ = 47 µF.
(2) Line and load regulation depend on external component selection and layout.

8.6 Typical Characteristics

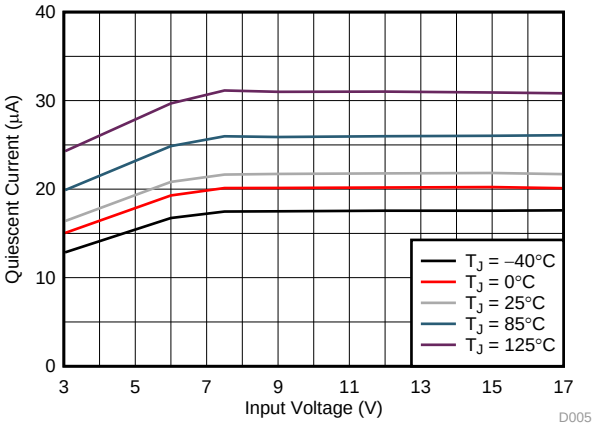


Figure 1. Quiescent Current into PVIN and AVIN

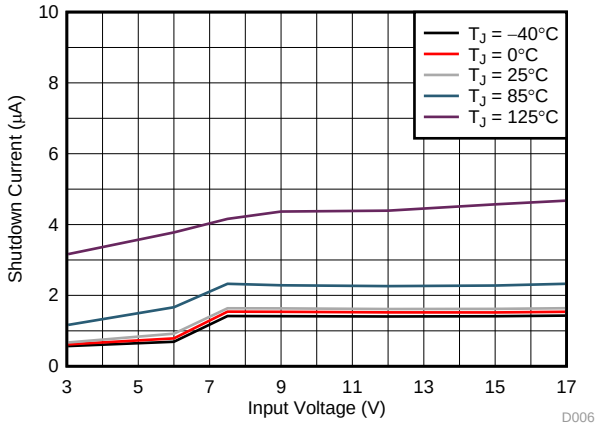


Figure 2. Shutdown Current into PVIN and AVIN

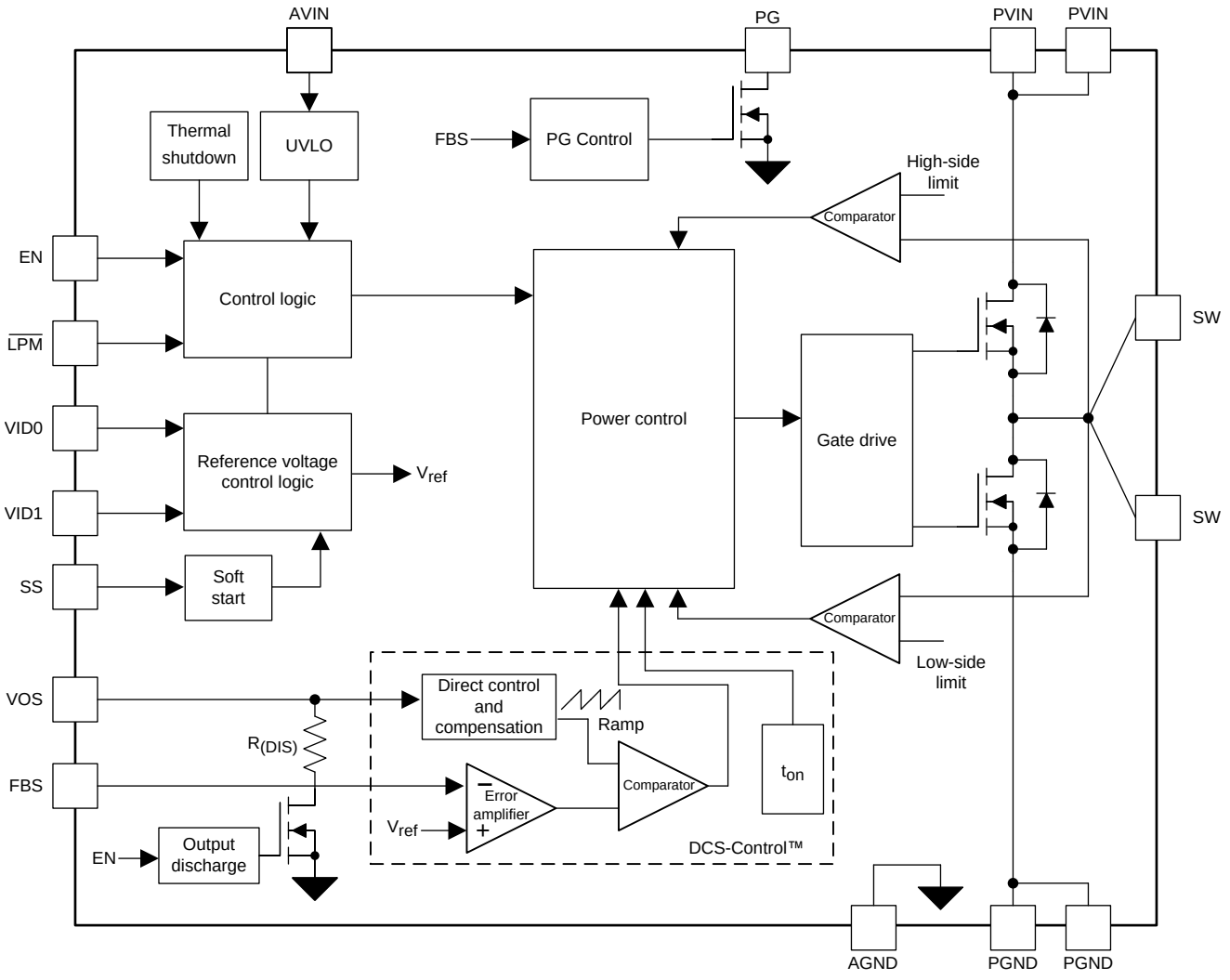
9 Detailed Description

9.1 Overview

The TPS62134x synchronous switched-mode power converters are based on DCS-Control™ (direct control with seamless transition into power-save mode), an advanced regulation topology that combines the advantages of hysteretic, voltage-mode, and current-mode control including an AC loop that is directly associated to the output voltage. This control loop uses information about output voltage changes and feeds the information directly to a fast comparator stage. The control loop provides immediate response to dynamic load changes. For accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (pulse width modulation) mode for medium and heavy load conditions and a power-save mode (PSM) at light loads. During PWM mode, the devices operate at the nominal switching frequency in continuous conduction mode (CCM). This frequency is approximately 1 MHz (typical) with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters PSM to sustain high efficiency down to very light loads. In PSM, the switching frequency decreases linearly with the load current. Because DCS-Control™ supports both operation modes within one single building block, the transition from PWM to PSM is seamless without effects on the output voltage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Enable and Shutdown (EN)

When the EN pin is set high, the device begins operation. The EN pin allows sequencing from a host or power-good output of another device.

The devices enter shutdown mode if the EN pin is pulled low with a shutdown current of 2 µA (typical). During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The output capacitor is smoothly discharged by a 20-kΩ internal resistor through the VOS pin. An internal pulldown resistor of approximately 400 kΩ is connected and maintains EN logic low, if the pin is floating. The pulldown resistor is disconnected if the EN pin is high.

9.3.2 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both power MOSFETs. The UVLO threshold is set to 2.7 V (typical). The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 200 mV (typical).

9.3.3 Soft-Start (SS) Circuitry

The internal soft-start circuitry controls the output-voltage slope during startup. This control avoids excessive inrush current and ensures a controlled output-voltage rise time. The control also prevents unwanted voltage drops from high-impedance power sources or batteries. When the EN pin is set high to begin device operation, the device begins switching after a delay of approximately 50 µs and V_O rises up to the nominal value set by the VIDx pins with a slope controlled by an external capacitor connected to the SS pin. Leave the SS pin floating for the fastest startup.

The device can startup into a pre-biased output. During monotonic pre-biased startup, both power MOSFETs are not allowed to turn on until the internal ramp of the device sets an output voltage above the pre-bias voltage.

If the device is in shutdown mode, undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS pin down to ensure a proper low level. Returning from those states causes a new startup sequence.

9.3.4 Switch Current-Limit and Short Circuit Protection

The TPS62134x family of devices is protected against heavy load and short circuit events. If an output short circuit is detected (V_O drops below 0.3 V), the switch current limit is reduced to 1.6 A (typical). If the output voltage rises above 0.4 V, the device operates in normal operation again.

At heavy loads, the current-limit determines the maximum output current. The current-limit supports output currents of 3 A with input voltages below 5 V and 3.2 A with higher input voltages. If the peak current-limit (I_L) is reached, the high-side MOSFET is turned off. Avoiding shoot-through current, the low-side MOSFET is switched on to sink the inductor current. The high-side MOSFET turns on again, only if the current in the low-side MOSFET has decreased below the low-side current-limit threshold of 3.2 A (typical).

Because of the internal propagation delay, the actual peak current of the high-side switch typically occurs above the DC value listed in the *Electrical Characteristic* table, especially in low duty-cycle applications. Use *Equation 1* to calculate the dynamic current-limit.

$$I_{L(dynamic)} = I_L + \frac{V_I - V_O}{L} \times 30\ ns \quad (1)$$

9.3.5 Output Voltage and LPM Logic Selection (VIDx and $\overline{LPM}$)

The output voltage of the TPS62134x family of devices is selected by two VIDx pins and one $\overline{LPM}$ pin as listed in Table 1. A pulldown resistor of 400 kΩ is internally connected to the VIDx pins and $\overline{LPM}$ pin to ensure a proper logic level if the pin is high impedance or floating. The pulldown resistors are disconnected if the pins are pulled High.

Feature Description (continued)

The device has a low power mode (LPM) where the output voltage is reduced or disabled by using the $\overline{\text{LPM}}$ pin. While the $\overline{\text{LPM}}$ pin is asserted, the PG output remains high impedance. The device also achieves a dynamic output-voltage change by using the VIDx pins. This feature helps the system to minimize power consumption in standby or idle mode. The TPS62134B/D devices provide the full current even if the output voltage is set at 0.7 V in LPM mode.

Table 1. Output Voltage Selection

PART NUMBER (INTEL SKYLAKE VRs)	$\overline{\text{LPM}}$ LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE (V)
TPS62134A ($V_{CC(IO)}$ Rail)	0	x	x	**0 (LPM)**
	1	0	0	0.850
	1	0	1	0.875
	1	1	0	0.950
	1	1	1	0.975
TPS62134B ($V_{CC(PRIM\_CORE)}$ Rail)	0	x	x	**0.7 (LPM)**
	1	0	0	0.80
	1	0	1	0.85
	1	1	0	0.90
	1	1	1	0.95
TPS62134C ($V_{CC(EDRAM)}$ / $V_{CC(EOPIO)}$ Rail)	0	x	x	**0 (LPM)**
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05
TPS62134D ($V_{CC(PRIM\_CORE)}$ Rail)	0	x	x	**0.7 (LPM)**
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

9.3.6 Power-Good Output (PG)

The TPS62134x family of devices has a built-in power-good indicator. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage below 6 V. The device has a fixed power-good threshold of 760 mV (rising edge) and 720 mV (falling edge). The PG rising edge has a delay time of 140 µs (typical) and a falling edge has a delay time of 20 µs (typical). The PG pin can sink 2-mA of current and maintain the specified logic low level. Table 2 lists the PG logic status in different operation conditions. The PG pin can be left floating if not used.

In LPM, the PG signal is latched as high impedance. When the device exits LPM, the PG has a 500-µs blanking time to ensure that the output voltage returns to the nominal value.

Table 2. Power Good Logic

CONDITIONS		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	EN = high, $\overline{\text{LPM}}$ = high, V_O > 760 mV	√	
	EN = high, $\overline{\text{LPM}}$ = high, V_O < 720 mV		√
LPM	EN = high, $\overline{\text{LPM}}$ = low	√	
LPM, TPS62134B/D	EN = high, $\overline{\text{LPM}}$ = Low, V_O < 0.3 V		√
Shutdown	EN = Low		√
Thermal shutdown			√
UVLO	0.5 V < $V_{(AVIN)}$ < $V_{(UVLO)}$		√
Power supply removal	$V_{(AVIN)}$ < 0.5 V	√	

9.3.7 Single-Ended Remote Sense (FBS)

The devices allow a single-ended remote sense by connecting the FBS pin at the load. This function overcomes the parasitic resistance of the PCB traces and achieves an improved output-voltage regulation at the load. Avoid any noise coupled into the FBS trace. Use a solid ground plane to connect the ground return of the load with the AGND and PGND pins of the device. Connect the AGND and PGND pins directly to exposed thermal pad of the device. Figure 3 shows an example.

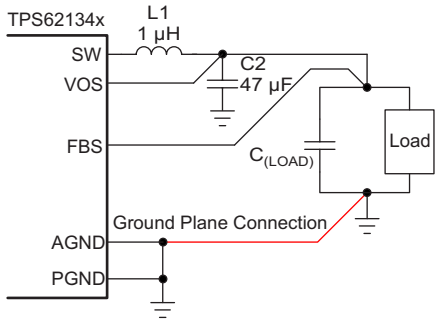


Figure 3. Remote Sense Connection

9.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power MOSFETs are turned off. When T_J decreases below the hysteresis of 20°C, the converter resumes normal operation, beginning with a soft start.

9.4 Device Functional Modes

9.4.1 PWM Operation and Power Save Mode

The device operates with pulse width modulation (PWM) in medium and heavy load with a fixed on-time circuitry (t_{on}). Use Equation 2 to calculate the on-time in steady-state operation.

$$t_{on} = 1\,\mu s \times \frac{V_O}{V_I} \tag{2}$$

The typical PWM switching frequency is 1 MHz. The frequency variation in PWM is controlled and depends on V_I, V_O, and the inductance. The switching frequency decreases with the input voltage to improve the efficiency in small duty-cycle applications.

To maintain high efficiency at light loads, the device enters PSM at the boundary to discontinuous conduction mode (DCM). In PSM, the switching frequency decreases linearly with the load current maintaining high efficiency. Use Equation 3 to calculate the switching frequency in PSM mode.

$$f_{S(PSM)} = \frac{2 \times I_O}{t_{on}^2 \times \frac{V_I}{V_O} \times \frac{V_I - V_O}{L}} \tag{3}$$

See Figure 12 for the switching frequency variation over load and input voltage.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS62134x family of devices are synchronous step-down converters based on the DCS-Control™ topology. The following section discusses the design of the external components to complete the power-supply design for power rails in the Intel Skylake platform.

10.2 Typical Application

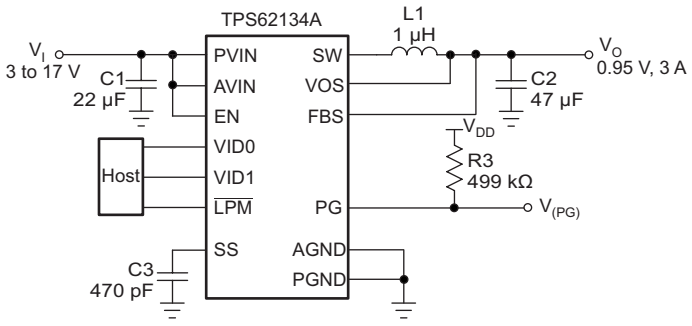


Figure 4. TPS62134A Typical Application

10.2.1 Design Requirements

The design guideline provides component selection to operate the device within the values listed in the *Recommend Operating Conditions* section. Meanwhile, the design meets the time and slew rate requirements of the Intel Skylake platform for $V_{CC(IO)}$, $V_{CC(PRIM\_CORE)}$, $V_{CC(EDRAM)}$, and $V_{CC(EOPIO)}$ rails. Table 3 lists the components used for the curves in the *Application Curves* section.

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TPS62134x	High efficiency step down converter	TI
L1	Inductor, 1 µH, XFL4020-102ME	Coilcraft
C1	Ceramic capacitor, 22 µF, GRM21BR61E226ME44L	Murata
C2	Ceramic capacitor, 47 µF, GRM21BR60J476ME15L	Murata
C3	Ceramic capactor, 470 pF, GRM188R71H471KA01D	Murata
R3	Resistor, 499 kΩ	Standard

10.2.2 Detailed Design Procedure

10.2.2.1 Output Filter Selection

The first step of the design procedure is the selection of the output-filter components. The combinations listed in Table 4 are used to simplify the output filter component selection.

Table 4. Recommended LC Output Filter Combinations(1)

INDUCTOR	OUTPUT CAPACITOR				
	22 µF	47 µF	100 µF	200 µF	400 µF
0.47 µH					
1 µH		√(2)	√	√	
2.2 µH					

(1) The values in the table are nominal values, including device tolerances.
(2) This LC combination is the standard value and recommended for most applications.

10.2.2.2 Inductor Selection

The inductor selection is affected by several effects such as inductor-ripple current, output-ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the selected inductor must be rated for appropriate saturation current and DC resistance (DCR). Use Equation 4 to calculate the maximum inductor current under static load conditions.

$$I_{(L)}max = I_O max + \frac{\Delta I_{(L)}max}{2}$$

$$\Delta I_{(L)}max = \frac{V_O}{L_{min} \times f_S} \times \left(1 - \frac{V_O}{V_I}\right)$$

where

- $I_{(L)}max$ is the maximum inductor current
- $\Delta I_{(L)}max$ is the maximum peak-to-peak inductor ripple current
- L_{min} is the minimum effective inductor value
- f_S is the actual PWM switching frequency (4)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of approximately 20% is recommended to be added. The inductor value also determines the load current at which power save mode is entered:

$$I_{O(PSM)} = \frac{\Delta I_{(L)}}{2} \quad (5)$$

Table 5 lists inductors that are recommended to use with the TPS62134x device.

Table 5. List of Inductors

TYPE	INDUCTANCE (µH)	CURRENT (A)	DIMENSIONS (L × B × H, mm)	MANUFACTURER
XFL4020-102ME	1 µH	4.7	4 × 4 × 2	Coilcraft
DFE252012F	1 µH	5.0	2.5 × 2 × 1.2	Toko
DFE201612E	1 µH	4.1	2 × 1.6 × 1.2	Toko
PISB25201T	1 µH	3.9	2.5 × 2 × 1	Cyntec
PIME031B	1 µH	5.4	3.1 × 3.4 × 1.2	Cyntec

10.2.2.3 Output Capacitor

The recommended value for the output capacitor is 47 µF. The architecture of the TPS62134x family of devices allows the use of tiny ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are recommended. Using an X7R or X5R dielectric is recommended to maintain low resistance up to high frequencies and to achieve narrow capacitance variation with temperature. Using a higher value can have some advantages such as smaller voltage ripple and a tighter DC output accuracy in PWM. See *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463 for additional information.

Note that in power save mode, the output voltage ripple depends on the output capacitance, ESR, and peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

10.2.2.4 Input Capacitor

For most applications, using a capacitor with a value of 22 µF is a recommended. Larger values further reduce input-current ripple. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A ceramic capacitor which has low ESR is recommended for best filtering and should be placed between the PVIN and PGND pins and as close as possible to those pins.

10.2.2.5 Soft-Start Capacitor

A capacitor connected between the SS pin and the AGND pin allows a user programmable startup slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. Use Equation 6 to calculate the capacitor value required for a given soft-start time.

$$C_{(SS)} = t_{(SS)} \times \frac{2.5\ \mu A}{V_O} \quad (6)$$

where

- $C_{(SS)}$ is the capacitance (F) required at the SS pin
- $t_{(SS)}$ is the desired soft-start time (s)

Leave the SS pin floating for fastest startup.

10.2.2.6 Program Output Voltage with External Resistor Divider

The TPS62134x family of devices extends the output voltage range by an external resistor divider, shown in Figure 5. The output voltage is then set by Equation 7.

$$V_O = V_{FBS} \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

where

- V_{FBS} is the FBS pin voltage setting by the VIDx pins, as shown in Table 1

The maximum output voltage must be less than 1.9 V. The required feed forward capacitor, C4, improves the loop stability performance. 5 pF is sufficient for most of applications with the R1 and R2 values shown. R1, R2 and C4 must be located close to the IC.

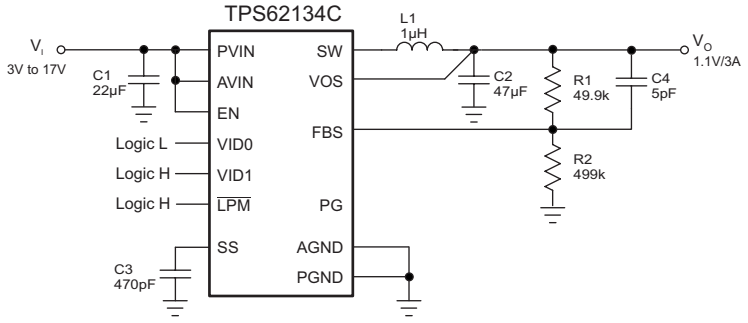
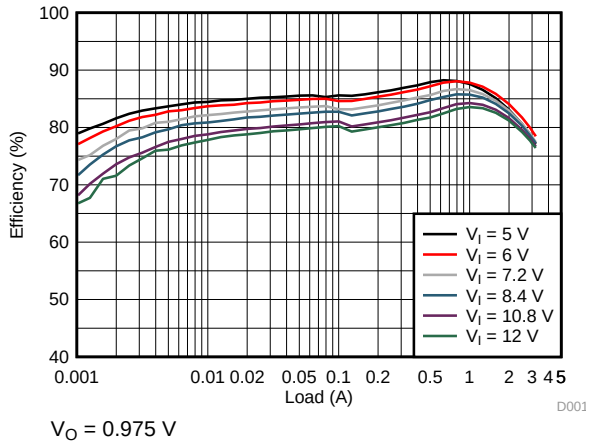


Figure 5. TPS62134C 1.1-V Output

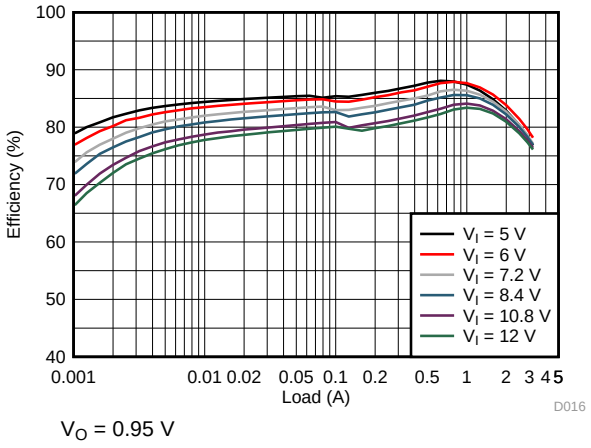
10.2.3 Application Curves

T_A = 25°C and V_I = 7.2 V, unless otherwise noted.



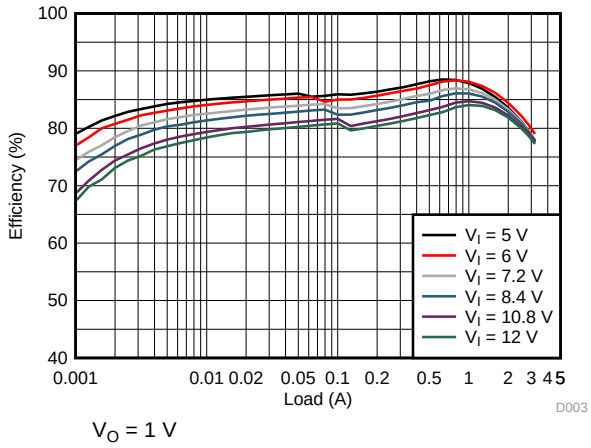
V_O = 0.975 V

Figure 6. TPS62134A Efficiency



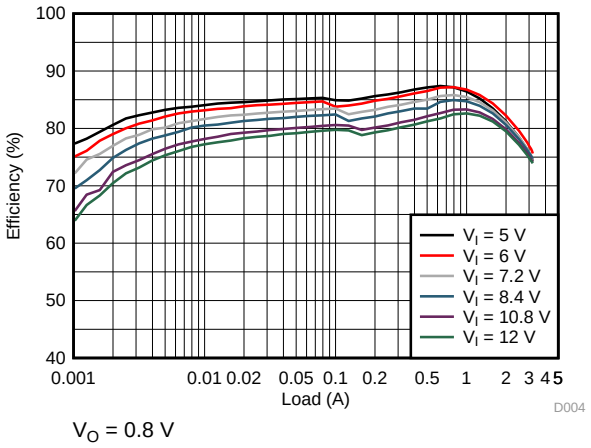
V_O = 0.95 V

Figure 7. TPS62134B Efficiency



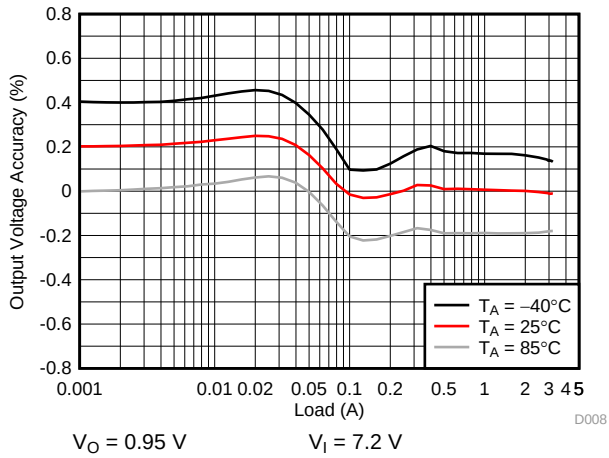
V_O = 1 V

Figure 8. TPS62134C Efficiency



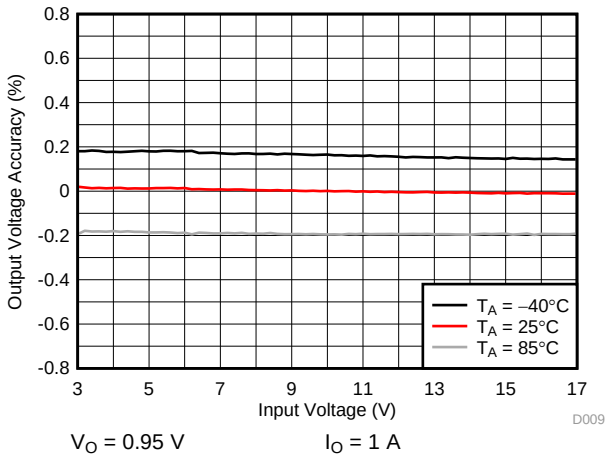
V_O = 0.8 V

Figure 9. TPS62134C Efficiency



V_O = 0.95 V V_I = 7.2 V

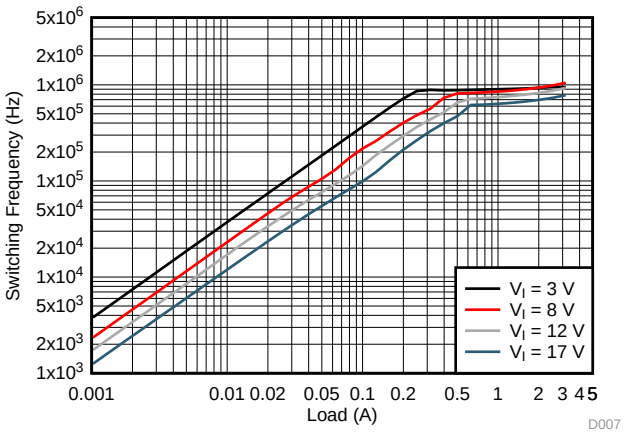
Figure 10. TPS62134A Load Regulation



V_O = 0.95 V I_O = 1 A

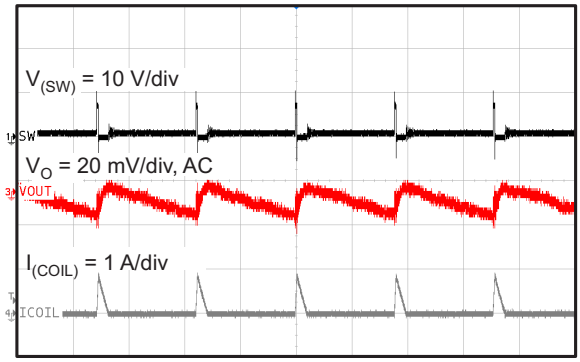
Figure 11. TPS62134A Line Regulation

T_A = 25°C and V_I = 7.2 V, unless otherwise noted.



V_O = 0.975 V

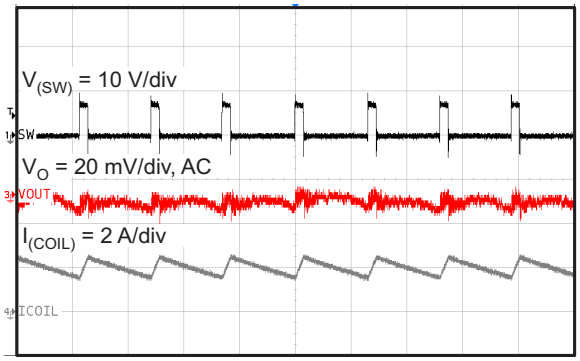
Figure 12. TPS62134A Switching Frequency



Time = 5 µs/div

V_O = 0.95 V I_O = 50 mA

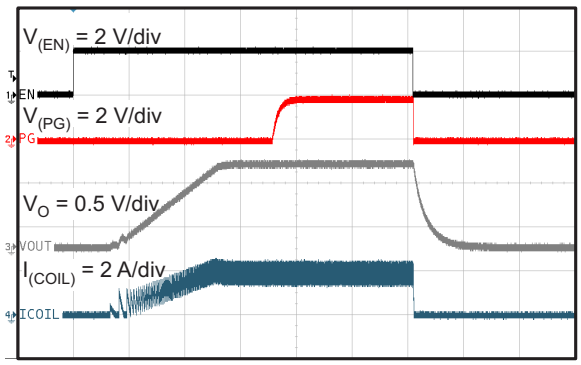
Figure 13. TPS62134A Output Ripple



Time = 1 µs/div

V_O = 0.95 V I_O = 2 A

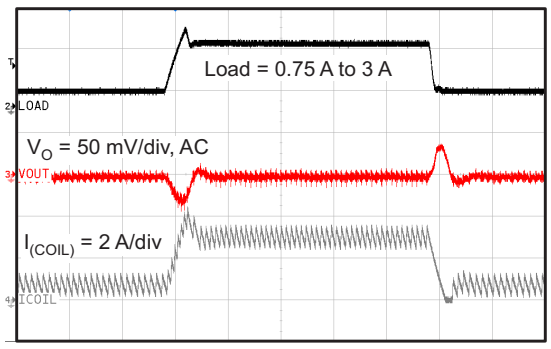
Figure 14. TPS62134A Output Ripple



Time = 100 µs/div

V_O = 0.95 V $R_{(LOAD)}$ = 0.47 Ω

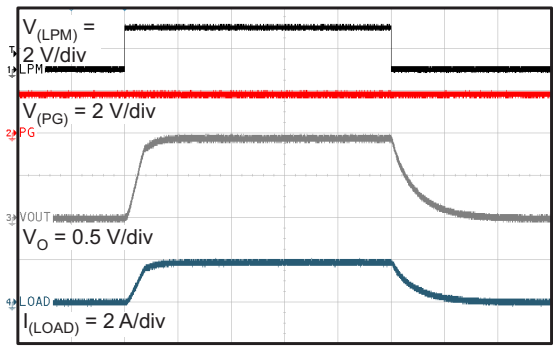
Figure 15. TPS62134A Startup and Shutdown



Time = 10 µs/div

V_O = 0.95 V

Figure 16. TPS62134A Load Transient



Time = 50 µs/div

$R_{(LOAD)}$ = 0.47 Ω

Figure 17. TPS62134C LPM Entry and Exit

T_A = 25°C and V_I = 7.2 V, unless otherwise noted.

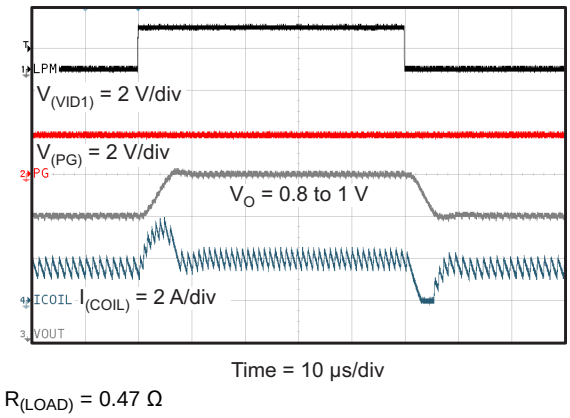


Figure 18. TPS62134C Minimum Speed Mode (MSM) Entry and Exit

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3 V and 17 V. Use Equation 8 to calculate the average input current of the TPS62134x device.

$$I_I = \frac{1}{\eta} \times \frac{V_O \times I_O}{V_I} \quad (8)$$

Ensure that the input power supply has a sufficient current rating for the application.

12 Layout

12.1 Layout Guidelines

- TI recommends to place all components as close as possible to the device. Ensure that the input capacitor placement is as close as possible to the PVIN and PGND pins of the device.
- The VOS pin is noise sensitive and must be routed short and directly to the output of the output capacitor. This routing minimizes switch node jitter and ensures reliability.
- The direct common-ground connection of the AGND and PGND pins to the exposed thermal pad and the system ground (ground plane) is mandatory. To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- The capacitor on the SS pin should be placed close to the device and connected directly to those pins and the AGND pin.
- The inductor should be placed close to the SW pins, keeping this area small.
- Finally, the ground of the output capacitor should be located close to the PGND pins of the device.
- See Figure 19 for an example of component placement, routing, and thermal design.

12.2 Layout Example

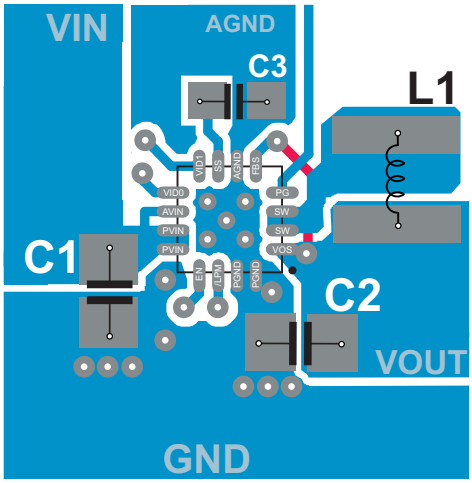


Figure 19. TPS62134x Layout Example

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The following lists three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), and *Semiconductor and IC Package Thermal Metrics* (SPRA953).

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

- *Optimizing the TPS62130/40/50/60/70 Output Filter*, SLVA463
- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, SZZA017

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62134A	Click here	Click here	Click here	Click here
TPS62134B	Click here	Click here	Click here	Click here
TPS62134C	Click here	Click here	Click here	Click here
TPS62134D	Click here	Click here	Click here	Click here

13.4 Trademarks

DCS-Control, the DCS-Control are trademarks of Texas Instruments.
Skylake, Ultrabooks are trademarks of Intel.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62134ARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134A	Samples
TPS62134ARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134A	Samples
TPS62134BRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134B	Samples
TPS62134BRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134B	Samples
TPS62134CRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134C	Samples
TPS62134CRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134C	Samples
TPS62134DRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134D	Samples
TPS62134DRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	134D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

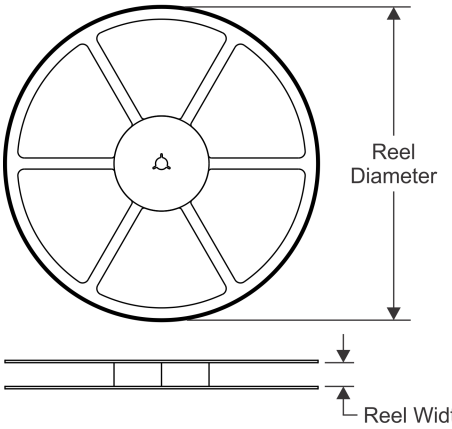
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

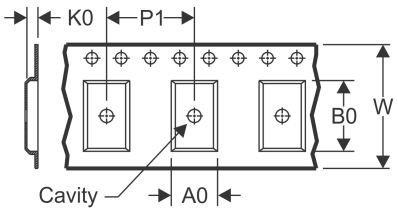
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

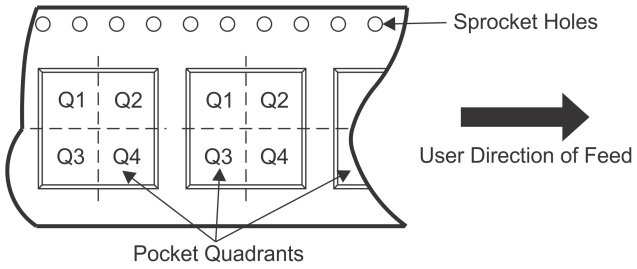


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

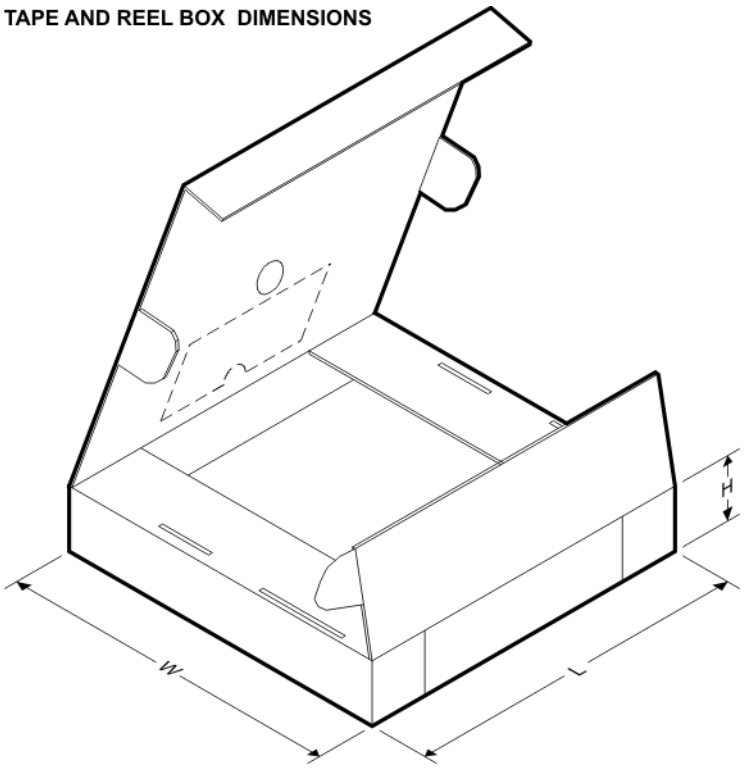
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62134ARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134ARGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134BRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134BRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134BRGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134BRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134CRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134CRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134DRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62134DRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

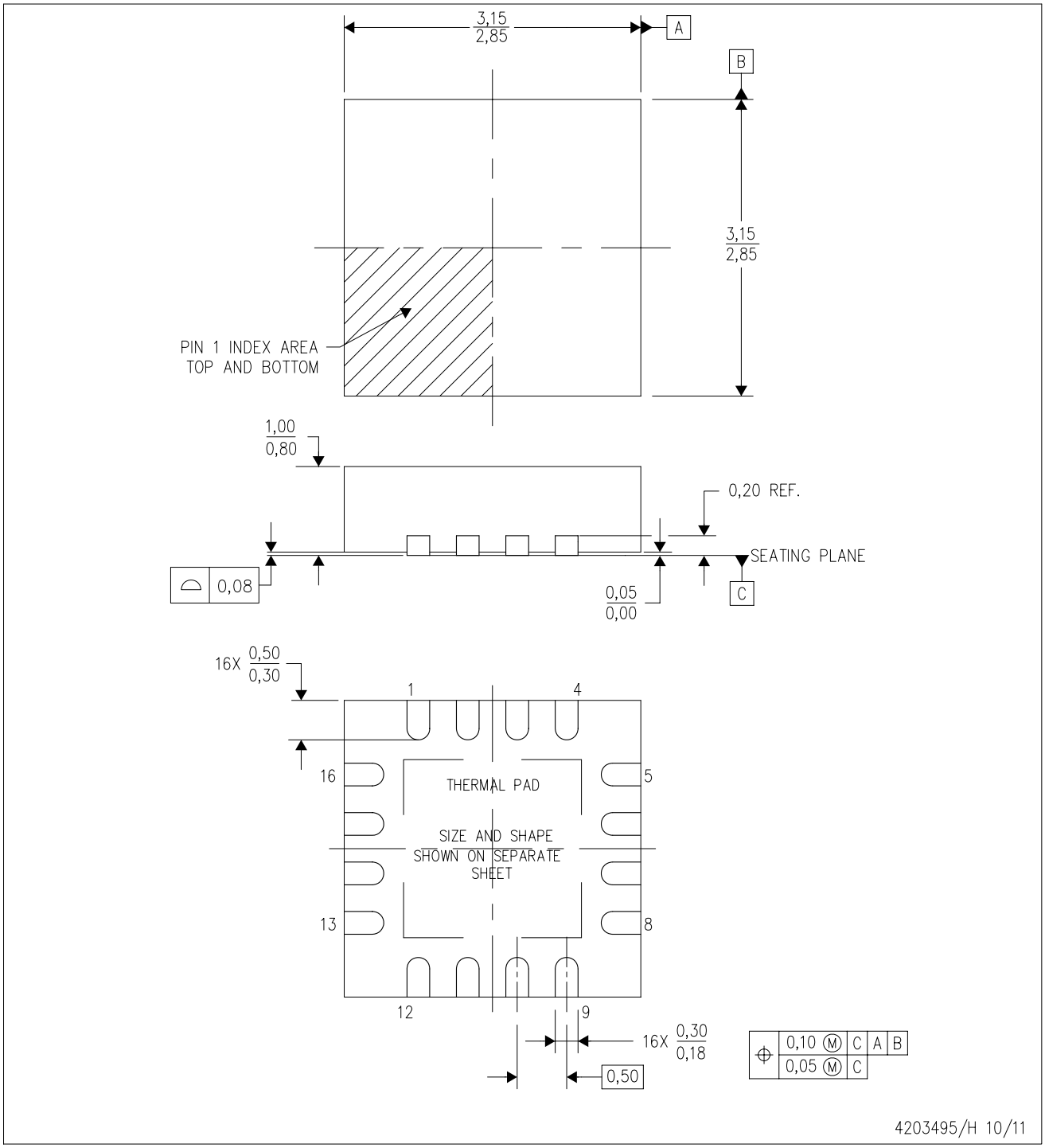
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62134ARGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62134ARGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62134BRGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62134BRGTR	QFN	RGT	16	3000	338.0	355.0	50.0
TPS62134BRGTT	QFN	RGT	16	250	338.0	355.0	50.0
TPS62134BRGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62134CRGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62134CRGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62134DRGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62134DRGTT	QFN	RGT	16	250	552.0	185.0	36.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

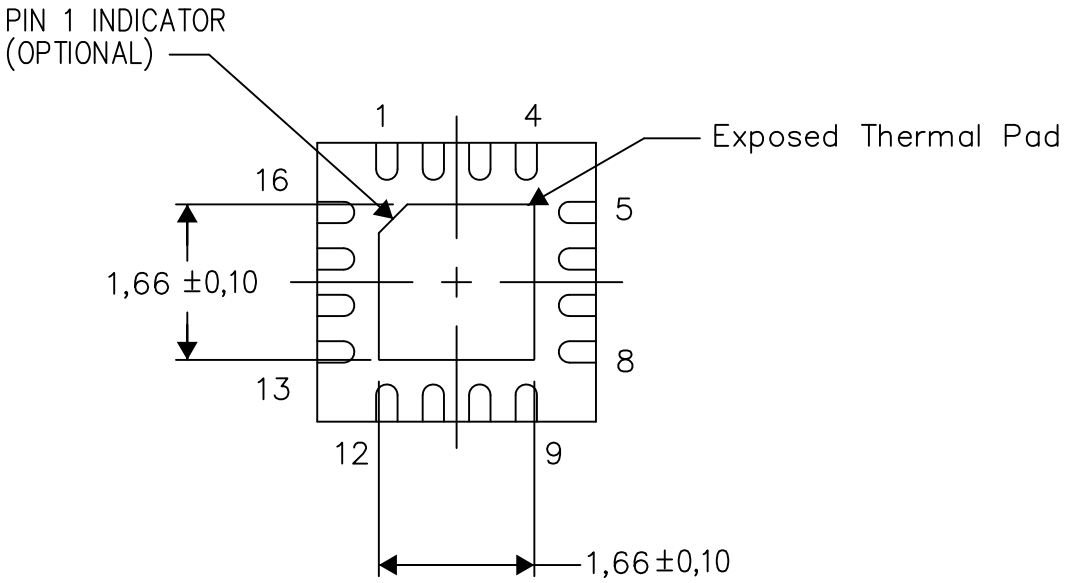
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



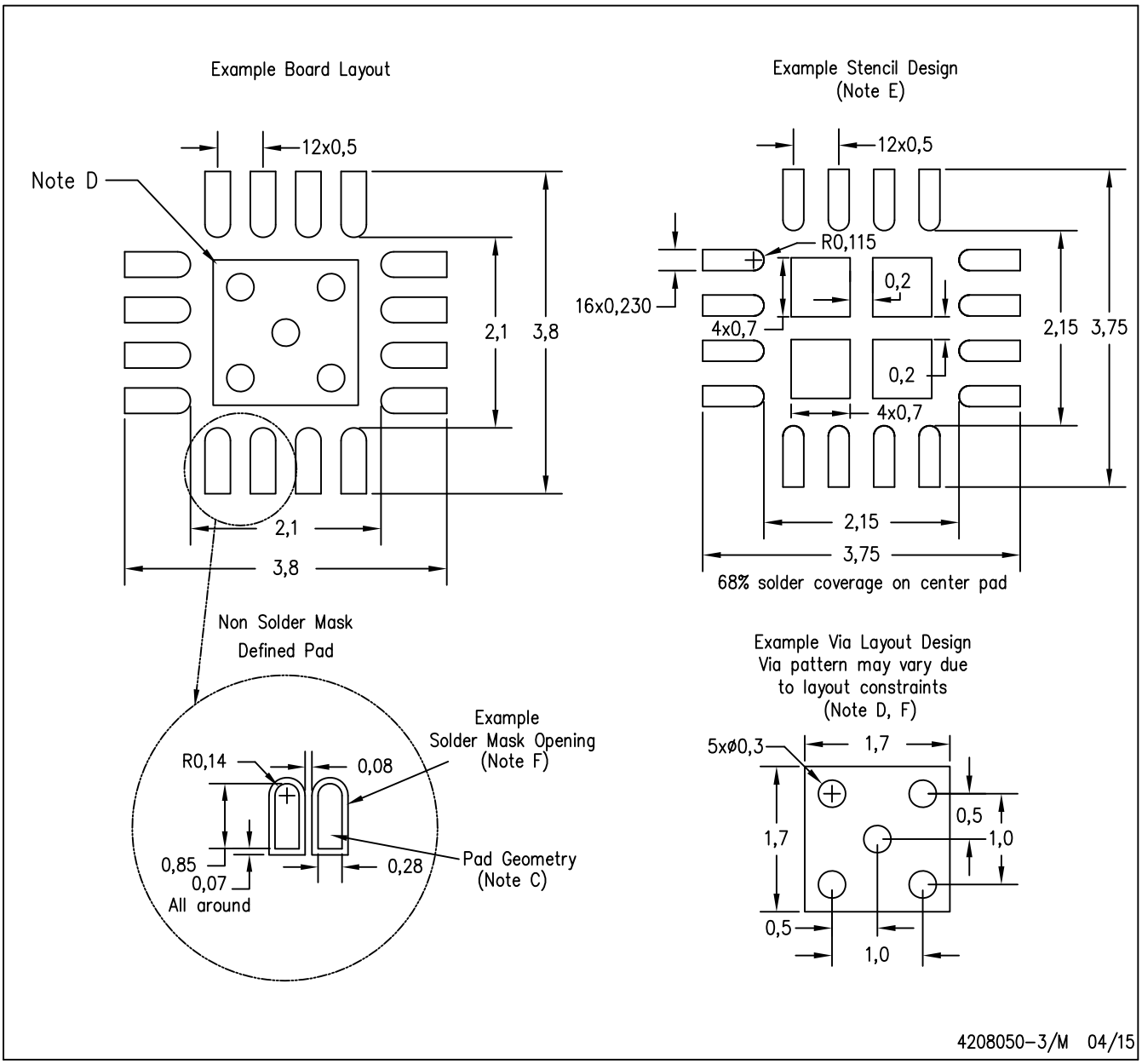
Bottom View

Exposed Thermal Pad Dimensions

4206349–10/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

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