WLED Driver for Notebooks with PWM Control Interface

Check for Samples: TPS61185

FEATURES

- **4.2 V to 24 V Input Voltage**
- **Integrated 2 A/40 V MOSFET**
- **600 kHz to 2 MHz Programmable Switching Frequency**
- **Adaptive Boost Output for Best Efficiency**
- **Design to Use Small L-C Components**
- **Integrated Loop Compensation**
- **Eight 25 mA Current Sinks**
- **Up to 10 WLED in Series**
- **1% Current Matching and Accuracy**
- **PWM Brightness Interface Control**
- **200 mV Ripple Under PWM Dimming**
- **Driver for Input/Output Isolation PFET**
- **Programmable Over Voltage Threshold**
- **100 Hz to 5 kHz Programmable PWM Dimming Frequency**
- **Up to 20 kHz Direct PWM Dimming Frequency**
- **Enhanced Electrostatic Discharge Immunity Level**
- **Built-in WLED Open/Short Protection**
- **Over Temperature Protection**
- **24 Pin 4 mm × 4 mm QFN Package**

APPLICATIONS

- **Notebook LCD Display Backlight**

DESCRIPTION

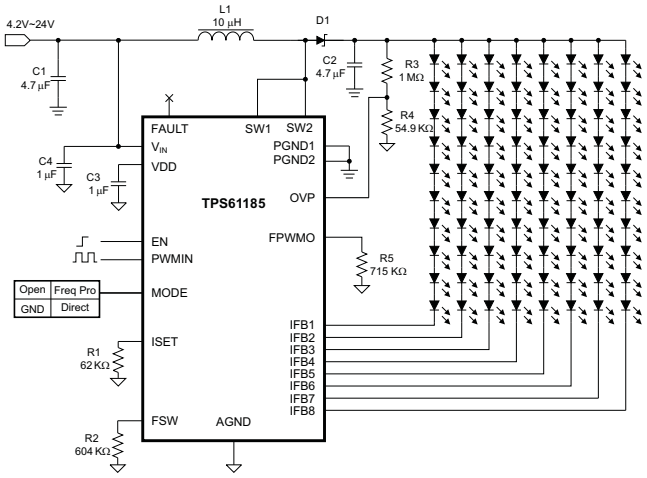
The TPS61185 IC provides highly integrated solutions for large-size LCD backlighting. This device has a built-in high efficiency boost regulator with integrated 2 A/40 V power MOSFET. The eight current sink regulators provide high precision current regulation and matching. In total, the device can support up to 80 LEDs. In addition, the boost output automatically adjusts its voltage to the WLED forward voltage to improve efficiency.

The TPS61185 supports the PWM method for brightness dimming. Simply tie the unused current sinks to ground if fewer than eight are needed. During PWM dimming, each of the eight current regulators is turned on/off at the duty cycle determined by an external pulse width modulation (PWM) signal input to the PWM pin. The frequency at which each current regulator turns on/off follows the input PWM signal on the PWMIN pin if the MODE pin is grounded. If the MODE pin is left floating or tied high, the regulators turn on/off at the frequency programmed by an external resistor on the FPWMO pin.

The TPS61185 IC supports boost switch frequency programming from 600kHz to 2MHz by an external resistor on the FSW pin. The device also provides a driver output for an optional external PFET connected between the input and inductor for truly disconnecting the battery from LED during the shutdown or fault protection. The device integrates resistor programmable over-voltage protection, soft-start, and thermal shutdown.

The TPS61185 IC has a built-in linear regulator to power the internal circuits of the IC. The device is in a 4 mm × 4 mm QFN package.

Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE INFORMATION(1)

PACKAGE	PACKAGE MARKING
TPS61185RGE	TPS61185

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Voltage range(2)	V_{IN} and FAULT		–0.3	24	V
	MODE		–0.3	7	V
	SW		–0.3	40	V
	EN, PWM, IFB1 to IFB8		–0.3	20	V
	On all other pins		–0.3	3.6	V
Continuous power dissipation			See Thermal Information Table		
Temperature range	Operating junction, T_j		–40	150	°C
	Storage, T_{stg}		–65	150	°C
ESD rating(3)	Human Body Model (HBM)	IFB1 to IFB8		5	kV
		On all other pins		2	
	Machine Model (MM)			200	V
	Charge Device Model (CDM)			1	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61185 RGE 24	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	16.9	
θ_{JB}	Junction-to-board thermal resistance (4)	7.4	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter (6)	7.1	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery input voltage range	4.2		24	V
V_{OUT}	Output voltage range	V_{IN}		38	V
L	Inductor	4.7		10	µH
C_I	Input capacitor	1.0			µF
C_O	Output capacitor	2.2		10	µF
F_{PWMO}	Internal, programmable PWM dimming frequency	0.1		5	kHz
F_{PWMIN}	Input PWM Frequency	0.1		20	kHz
T_{ON}	Minimum on time in one dimming cycle		5		µs
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 10.8 V, EN = Logic High, IFB Current = 20 mA, IFB Voltage = 500 mV, T_A = –40°C to 85°C, Typical Values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Battery input voltage range		4.2		24	V
I_{q_VIN}	Operating quiescent current into V_{IN}	Device enable, V_{IN} = 24 V, No load, No switch	0.5		3	mA
V_{DD}	VDD pin output voltage	V_{IN} > 5.5 V, ILoad = 3 mA	2.7	3.15	3.6	V
I_{SD}	Shutdown current	V_{IN} = 10.8 V, EN = low	2		10	µA
		V_{IN} = 21 V, EN = Low	4		15	
V_{in_UVLO}	V_{IN} under-voltage lockout threshold	V_{IN} ramp down	3.7	3.9	4.1	V
		V_{IN} ramp up	3.8		4.2	
V_{in_hys}	V_{IN} under-voltage lockout hysterisis		100	150	200	mV
EN, PWM and MODE						
V_H	EN logic high threshold		2.1		20	V
V_L	EN logic Low threshold		0		0.8	V
V_H	PWM logic high threshold		2.1		20	V
V_L	PWM logic low threshold		0		0.8	V
V_H	MODE logic high threshold		2.1		7	V
V_L	MODE logic low threshold		0		0.8	V
R_{PD_EN}	Pull down resistor on EN	V_{EN} = 2.5 V	400	800	1600	kΩ
R_{PD_PWM}	Pull down resistor on PWM	V_{PWM} = 2.5 V	400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage	ISET current = 20 µA	1.204	1.229	1.253	V
K_{ISET}	Current multiple Iout/ISET	ISET current = 20 µA, D = 100%		980		
I_{FB_AVG}	Average current accuracy	ISET current = 20 µA, D = 100%	–1.4%		1.4%	mA
K_m	$(I_{max}-I_{min})/I_{AVG}$	ISET current = 20 µA, D = 100%	0%	1%	3%	
I_{leak}	IFB pin leakage current	IFB voltage = 20 V on all pins	0		3	µA
I_{IFB_MAX}	Current sink max output current	IFB = 500 mV	25			mA
f_{dim}	PWM dimming frequency	R_{FPWM} = 715 kΩ	190	210	230	Hz
BOOST OUTPUT REGULATION						
V_{IFB_L}	V_O dial up threshold	Measure on IFB		400		mV
V_{IFB_H}	V_O dial down threshold	Measure on IFB		900		mV
V_{reg_L}	Min Vout regulation voltage			0.72 × (1+R3/R4)		V

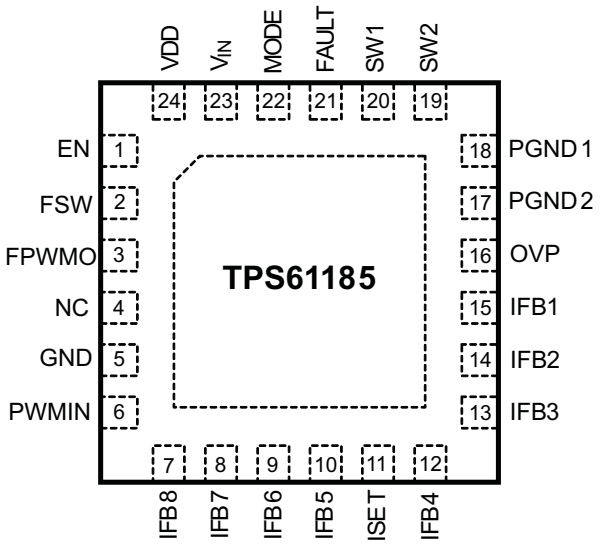
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 10.8 V, EN = Logic High, IFB Current = 20 mA, IFB Voltage = 500 mV, T_A = –40°C to 85°C, Typical Values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
R_{PWM_SW}	PWM FET on-resistance		0.1	0.15	0.38	Ω
I_{LN_NFET}	PWM FET leakage current	V_{SW} = 35 V, T_A = 25°C	0		2	µA
OSCILLATOR						
f_S	Oscillator frequency	R_{FSW} = 604 kΩ	0.8	1.0	1.2	MHz
D_{max}	Maximum duty cycle	IFBx = 0 V, F_{SW} = 600 kHz	89%	94%		
D_{min}	Minimum duty cycle	F_{SW} = 600 kHz	0.1%		7%	
OC, SC, OVP AND SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	2		3.1	A
V_{CLAMP_TH}	V_O clamp threshold	Measured on OVP pin	1.90	1.95	2.00	V
V_{OVP_TH}	V_O overvoltage threshold	Measured on OVP pin (rise)	1.97	2.03	2.09	V
V_{ovp_IFB}	IFB overvoltage threshold	Measured on the IFBx pin, IFB on	4.4	4.8	5.2	V
V_{ovp2_IFB}	2nd level IFB overvoltage threshold	Measured on the IFBx pin, IFB on and off	18			
V_{IFB_nouse}	IFB no use detection threshold during start up	IFB voltage rising		0.6		V
I_{IFB_low}	Low current detection threshold	As percentage of normal current		50%		
V_{OL}	OVP pin overload detection	Output voltage drop		60%		
FAULT OUTPUT						
V_{fault_high}	FAULT high voltage	Measured as V_{IN}-V_{FAULT}	0.03	0.07	0.13	V
V_{fault_low}	FAULT low voltage	Measured as V_{IN}-V_{FAULT}, Sink 10 µA, V_{IN} = 12 V	6	8	10	V
I_{fault}	FAULT pull-down current	V_{IN} = 12 V	10	20	30	µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			170		°C

DEVICE INFORMATION

24 PIN RGE PACKAGE
TOP VIEW



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin.
FSW	2	I	Switching frequency program pin. Use a resistor from this pin to GND to set the boost switch frequency from 600 kHz to 2 MHz.
FPWMO	3	O	Dimming frequency program pin. When the mode pin is open or pulled high, the resistor on this pin to GND programs the PWM dimming frequency between 100 Hz to 5 kHz.
NC	4	I	No connection pin.
GND	5	I	Signal ground of the IC. Tie the ground of noise sensitive components to GND.
PWMIN	6	I	Dimming control logic input. The dimming frequency range is 100 Hz to 20 kHz.
IFB8-IFB5 IFB4-IFB1	7–10 12–15	O	Current sink regulation inputs. They are connected to the cathode of the WLEDs. Connect any unused IFB pins to GND or leave open. The PWM loop regulates the lowest V_{IFB} to 400 mV. Each channel is limited to 25 mA current.
ISET	11	O	The resistor on this pin programs WLED output current. Tie resistor ground to GND.
OVP	16	I	Over voltage programming pin. The OVP voltage threshold is set through an external resistor divider combination according to equation 4.
PGND2	17	I	Power grounds of the IC. Internally connect to the source of the PWM switch. Tie the ground of power stage components to these grounds.
PGND1	18	I	
SW2	19	I	Drain connections of the internal PWM switch MOSFET and external Schottky diode.
SW1	20	I	
FAULT	21	O	Gate driver output for an external PFET used for fault protection. It can also be used as signal output for system fault report.
MODE	22	I	Dimming mode select pin. When MODE is high or open, the internal dimming frequency is programmable by a resistor on pin 3 (FPWMO pin); when MODE is low, the internal dimming frequency is the same as the PWM input signal on pin 6 (PWMIN pin).
V_{IN}	23	I	This pin is connected to the battery supply. It also provides the pull-up voltage for the FAULT pin.
VDD	24	O	The supply rail of internal logic. Connect a 1-µF capacitor from VDD to GND.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURES
Load efficiency of TPS61185	V_{IN} = 10.8 V; V_O = 29 V, 31 V, 33 V and 36 V; L = 10 µH	Figure 1
Load efficiency of TPS61185	V_{IN} = 7 V, 10.8 V and 24 V; V_O = 31 V; L = 10 µH	Figure 2
PWM dimming efficiency	V_{IN} = 7 V, 10.8 V and 24 V; V_O = 36 V; L = 10 µH; R_{ISET} = 62 kΩ	Figure 3
PWM dimming efficiency	V_{IN} = 7 V, 10.8 V and 24 V; V_O = 30 V; L = 10 µH; R_{ISET} = 62 kΩ	Figure 4
Dimming linearity	V_{IN} = 10.8 V; V_O = 36 V; F_{PWMO} = 210 Hz; R_{ISET} = 62 kΩ; MODE = OPEN	Figure 5
Dimming linearity	V_{IN} = 10.8 V; V_O = 36 V; F_{PWMO} = 1 kHz; R_{ISET} = 62 kΩ; MODE = OPEN	Figure 6
Dimming linearity	V_{IN} = 10.8 V; V_O = 36 V; F_{PWMO} = 210 Hz; R_{ISET} = 62 kΩ; MODE = GND	Figure 7
Dimming linearity	V_{IN} = 10.8 V; V_O = 36 V; F_{PWMO} = 20 kHz; R_{ISET} = 62 kΩ; MODE = GND	Figure 8
Boost switching frequency	V_{IN} = 10.8 V; V_O = 36 V; R_{ISET} = 62 kΩ; MODE = OPEN	Figure 9
Programmable PWM dimming frequency	V_{IN} = 10.8 V; V_O = 36 V; R_{ISET} = 62 kΩ; MODE = OPEN	Figure 10
Switching waveform	V_{IN} = 5 V; V_O = 36 V; L = 10 µH; R_{ISET} = 62 kΩ	Figure 11
Switching waveform	V_{IN} = 21 V; V_O = 36 V; L = 10 µH; R_{ISET} = 62kΩ	Figure 12
Startup waveform	V_{IN} = 10.8 V; V_O = 36 V; R_{ISET} = 62 kΩ	Figure 13
Shutdown waveform	V_{IN} = 10.8 V; V_O = 36 V; R_{ISET} = 62kΩ	Figure 13
PWM dimming	V_{IN} = 10.8 V; V_O = 36 V; ISET = 20 µA; F_{PWMO} = 210 Hz; D = 1%	Figure 15
PWM dimming	V_{IN} = 10.8 V; V_O = 36 V; ISET = 20 µA; F_{PWMO} = 20 kHz; D = 10%	Figure 16

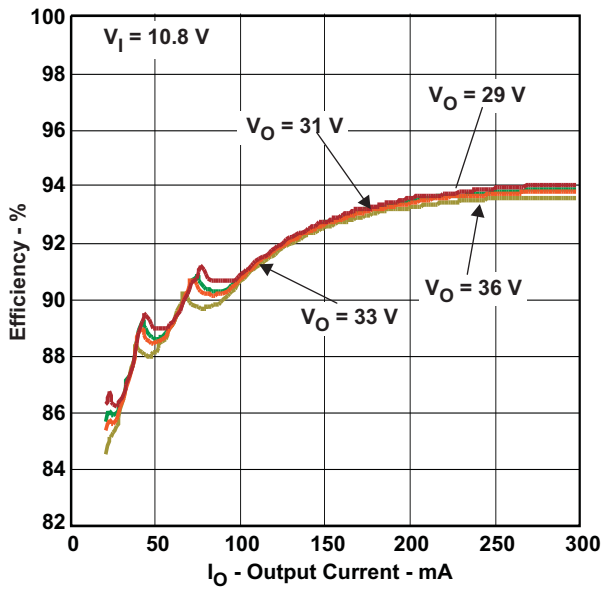


Figure 1. Efficiency vs. Output Current

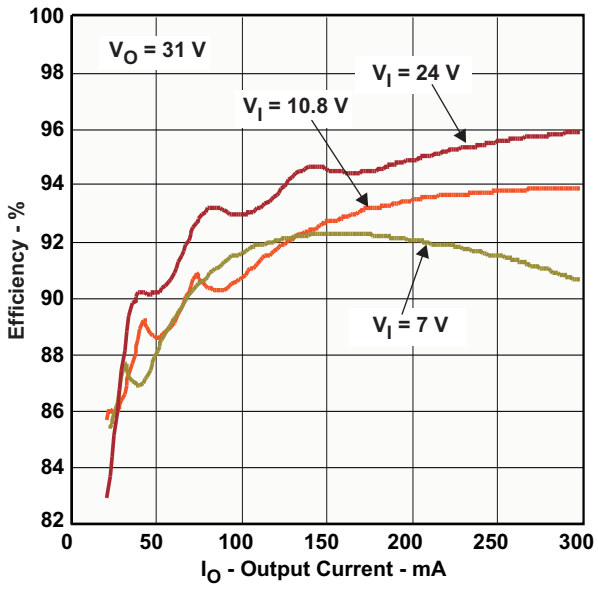


Figure 2. Efficiency vs. Output Current

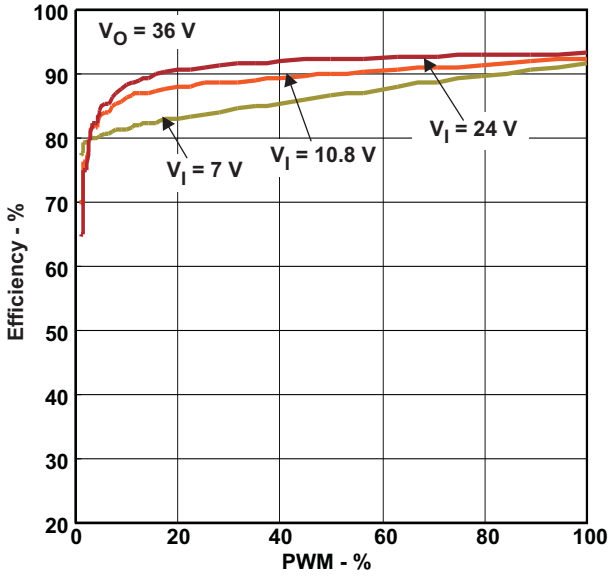


Figure 3. Efficiency vs. PWM Dimming %

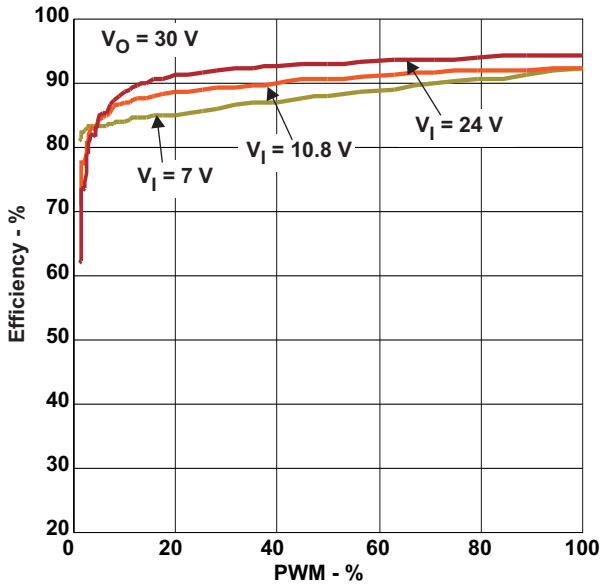


Figure 4. Efficiency vs. PWM Dimming %

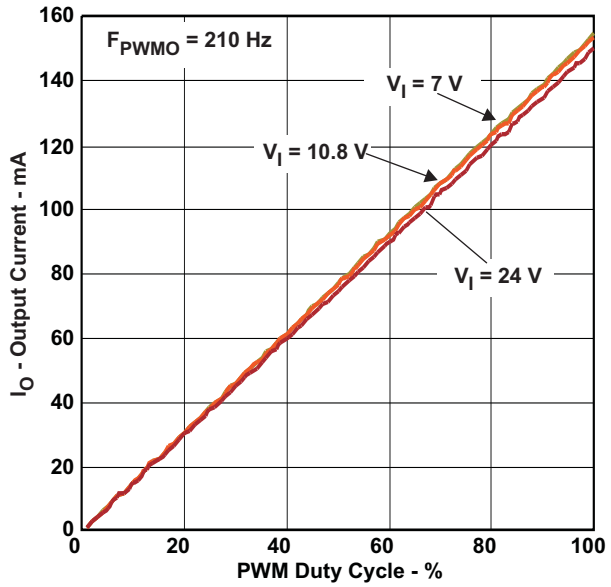


Figure 5. Output Current vs. PWM Duty Cycle

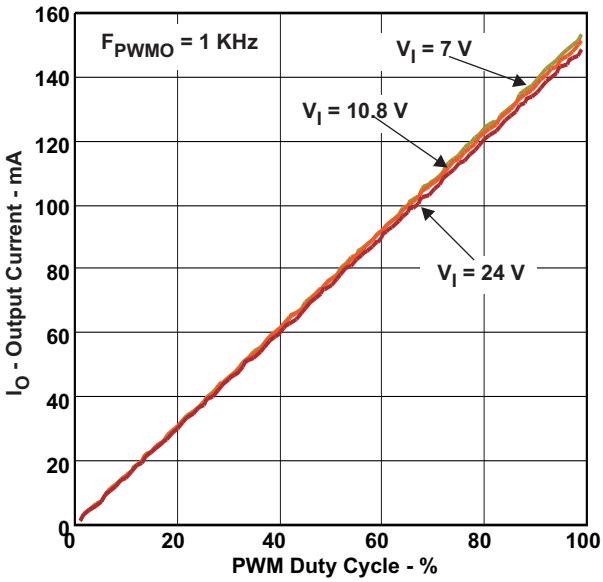


Figure 6. Output Current vs. PWM Duty Cycle

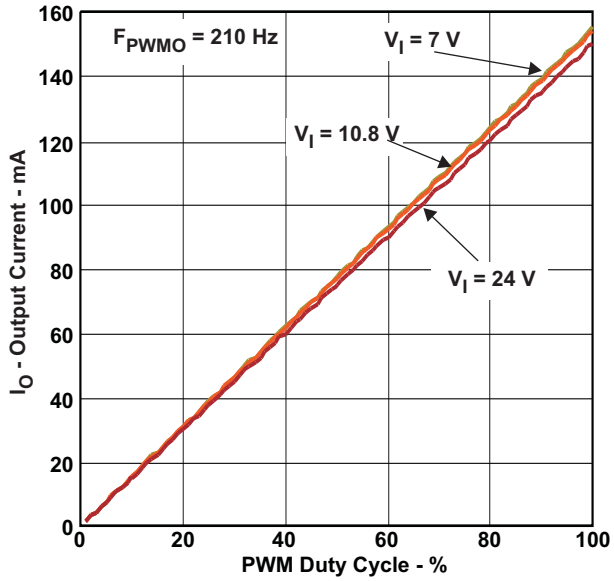


Figure 7. Output Current vs. PWM Duty Cycle

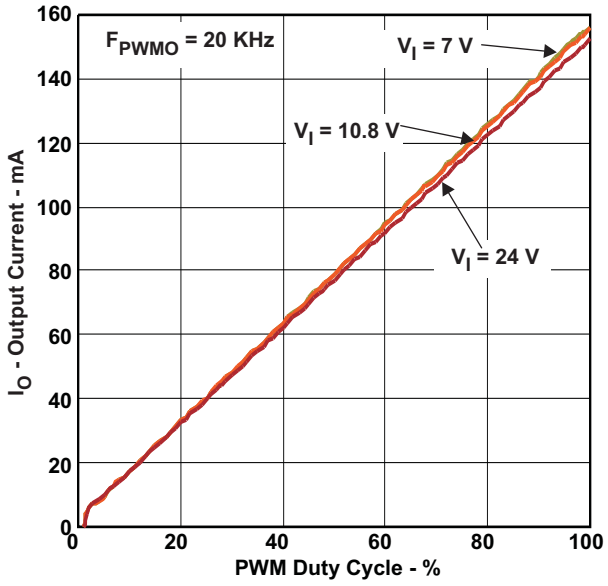


Figure 8. Output Current vs. PWM Duty Cycle

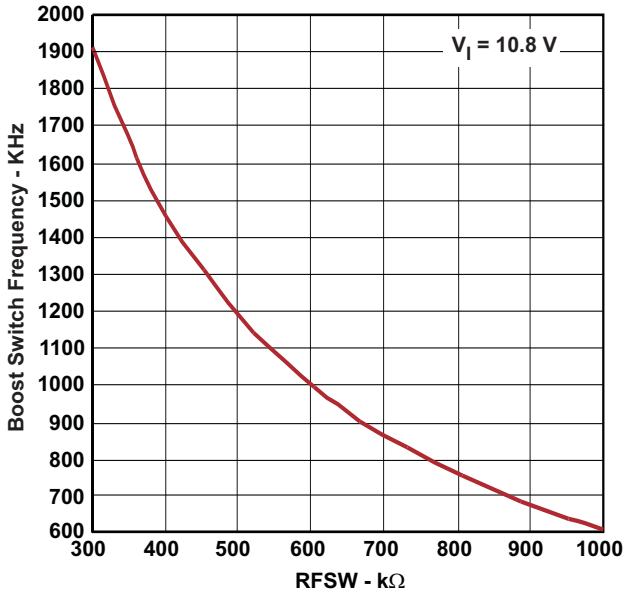


Figure 9. Boost Switch Frequency vs. R_{FSW}

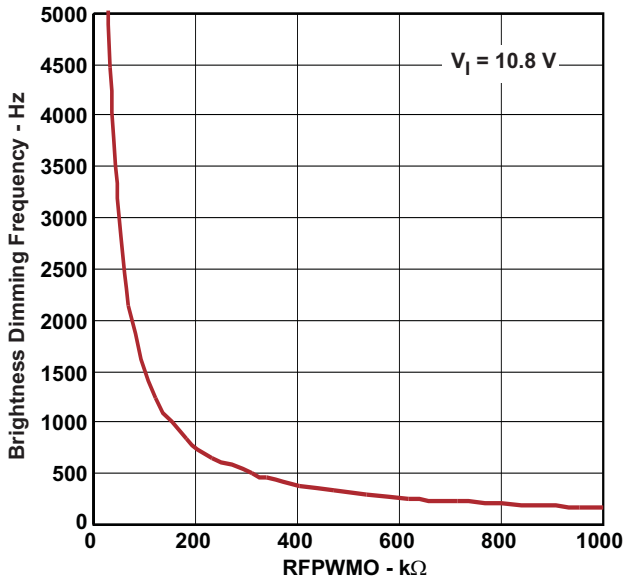


Figure 10. Brightness Dimming Frequency vs. R_{FPWMO}

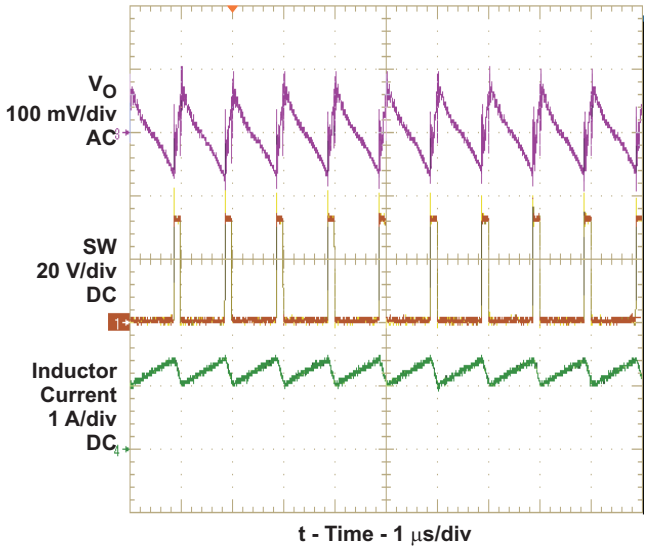


Figure 11. Switching Waveform

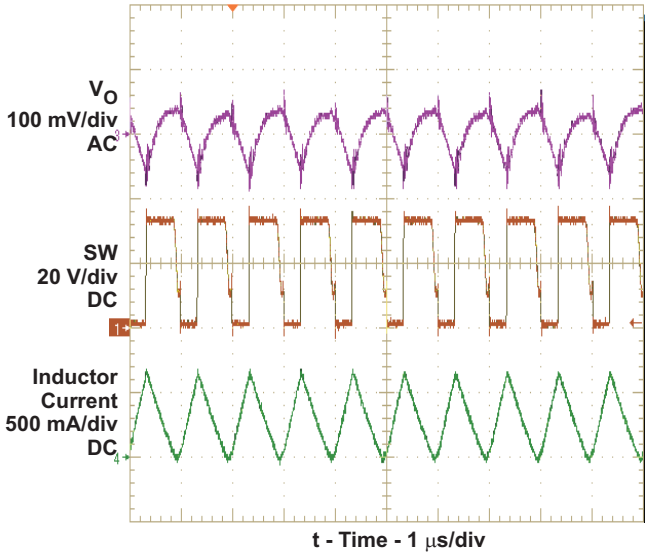


Figure 12. Switching Waveform

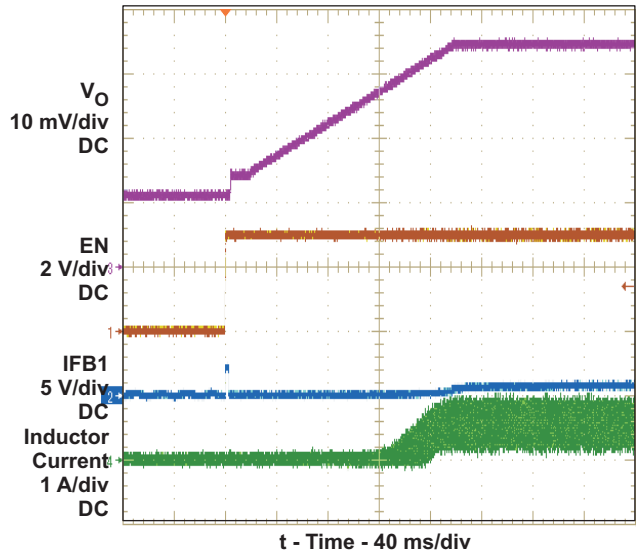


Figure 13. Startup Waveform

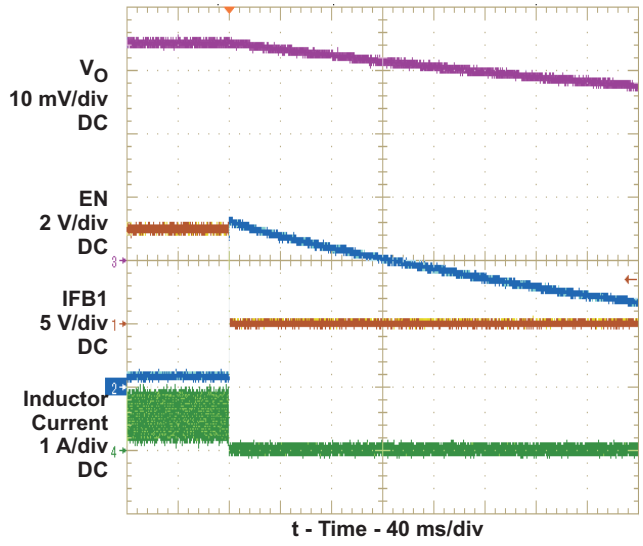


Figure 14. Shutdown Waveform

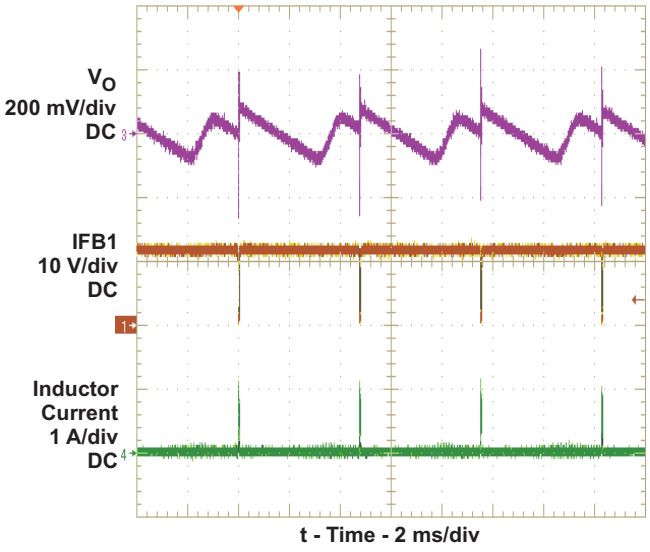


Figure 15. Dimming Waveform

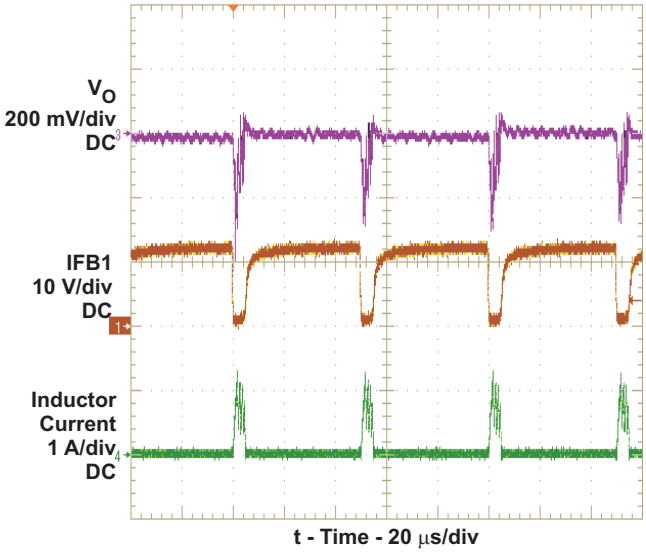
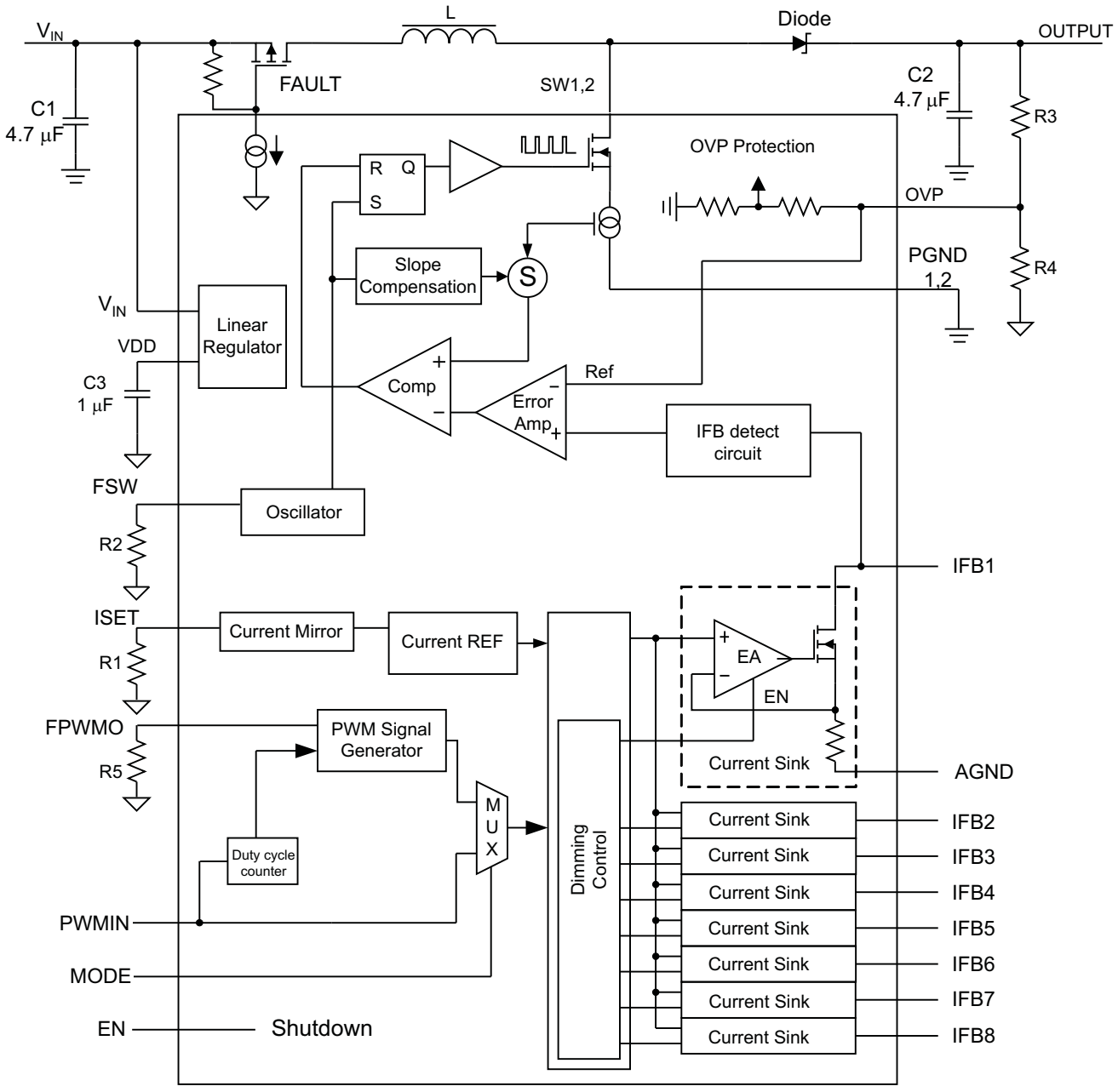


Figure 16. Dimming Waveform

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

NORMAL OPERATION

The TPS61185 is a high efficiency, high output voltage white LED driver for notebook panel backlighting applications. The advantages of white LEDs compared to CCFL backlights are higher power efficiency and lower profile design. Due to the large number of white LEDs required to provide backlighting for medium to large display panels, the LEDs must be arranged in parallel strings of several LEDs in series. Therefore, the backlight driver for battery powered systems is almost always a boost regulator with multiple current sink regulators. Having more white LEDs in series reduces the number of parallel strings and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there must be enough white LEDs in series to ensure the output voltage stays above the input voltage range.

The TPS61185 IC has integrated all of the key functional blocks to power and control up to 80 white LEDs. The device includes a 2 A/40 V boost regulator, eight 25 mA current sink regulators, and protection circuitry for over-current, over-voltage, and short circuit failures.

The TPS61185 provides a PMW interface to control the current of each regulator to realize the LED brightness dimming.

SUPPLY VOLTAGE

The TPS61185 IC has a built-in LDO linear regulator to supply the IC analog and logic circuit. The LDO is powered up when the EN pin is high. The output of the LDO is connected to the VDD pin. A 1 µF bypass capacitor on the VDD pin is required for the LDO control loop to be stable. While possible to enable the IC by tying EN to the VDD for evaluation purposes, it is recommended to use a separate digital signal to enable and disable the IC in a real system.

The voltage on the V_{IN} pin is the input of the internal LDO and powers the IC. There is an under-voltage lockout on the V_{IN} pin which disables the IC when its voltage falls to 4.0 V (maximum). The IC restarts when the V_{IN} pin voltage recovers by 200 mV.

BOOST REGULATOR AND PROGRAMMABLE SWITCH FREQUENCY (FSW)

The fixed-frequency PWM boost converter uses current-mode control and has integrated loop compensation. The internal compensation ensures stable output over the full input and output voltage ranges assuming the recommended values of inductor and output capacitor on page 3 are used. The output voltage of the boost regulator is automatically set by the IC to minimize the voltage drop across the IFB pins. The IC regulates the lowest IFB pin to 400 mV and consistently adjusts the boost output voltage to account for any changes in LED forward voltages. If the input voltage is higher than the sum of the white LED forward voltage drops (e.g., at low duty cycles), the boost converter is not able to regulate the output due to its minimum duty cycle limitation. In this case, increase the number of LEDs in series or include series ballast resistors in order to provide enough headroom for the converter to boost the output voltage. Since the TPS61185 integrates a 2 A/40 V power MOSFET, the boost converter can provide up to a 38 V output voltage.

The TPS61185 switch frequency is programmable between 600 kHz to 2.0MHz by the resistor value on the FSW pin and approximately follows Equation 1:

$$F_{SW} \approx \frac{6 \times 10^{11}}{R_{FSW}} \quad (1)$$

Where: R_{FSW} = FSW pin resistor

See Figure 9 for boost converter switching frequency adjustment resistor R_{FSW} selection.

The adjustable switching frequency feature provides the user with the flexibility of choosing a faster switching frequency, and therefore, an inductor with smaller inductance and footprint, or a slower switching frequency, and therefore, potentially higher efficiency due to lower switching losses.

LED CURRENT SINKS

The eight current sink regulators embedded in the TPS61185 can be collectively configured to provide up to a maximum of 25 mA. These eight specialized current sinks are accurate to within ±1% typical maximum for currents above 5 mA, with a string-to-string difference of ±1% . The IFB current must be programmed to the highest LED current expected using the ISET pin resistor and Equation 2.

$$I_{FB} = \frac{V_{ISET}}{R_{ISET}} \times K_{ISET} \quad (2)$$

Where:

K_{ISET} = Current multiple (980 typical)
V_{ISET} = ISET pin voltage (1.229 V typical)
R_{ISET} = ISET pin resistor

ENABLE AND SOFT STARTUP

A logic high signal on the EN pin turns on the internal LDO linear regulator which provides VDD to activate the IC. After the device is enabled, the TPS61185 checks the status of all current feedback channels and shuts down any unused feedback channels.

After the device is enabled, if the PWMIN pin is left floating or logic low input, the output voltage of the TPS61185 regulates to the minimum output voltage. Once the IC detects a voltage on the PWMIN pin, the TPS61185 begins to regulate the IFB pin current, as pre-set per the ISET pin resistor, times the duty cycle of the signal on the PWMIN pin. The boost converter's output voltage rises to the appropriate level to accommodate the sum of the white LED string with the highest forward voltage drop plus 400 mV typical at that current.

The TPS61185 has integrated soft-start circuitry to avoid any inrush current during startup. During the startup period, the TPS61185 output voltage rises step by step from the minimum output voltage in 100 mV increments, over a 1 ms interval. After startup, the output voltage continues to rise until all of the IFB pin voltages exceed 400 mV and all IFB current is regulated under the pre-set value.

Pulling the EN pin low immediately shuts down the IC, resulting in the IC consuming less than 50 µA in shutdown mode.

IFB PIN UNUSED

If the application requires less than 8 WLED strings, those IFB pins not required can be easily disabled. The TPS61185 simply requires leaving the unused IFB pin open or shorting it to ground. If the IFB pin is open, the boost output voltage ramps up to the pre-set over-voltage threshold on the V_{OVP} pin during start up. The IC then detects the zero current string and removes it from the feedback loop. If the IFB pin is shorted to ground, the IC detects the voltage less than the V_{IFB_nouse} threshold typically 0.6V and immediately disables the string after the IC is enabled. Thus, the boost output voltage ramps to the regulation voltage immediately following soft start and does not go up to the over-voltage threshold.

BRIGHTNESS DIMMING (MODE)

The TPS61185 adopts PWM dimming technology for output LED brightness control. All output current strings are turned on and off together at the duty cycle which is determined by the PWM signal input to the PWMIN pin.

However, the TPS61185 has two PWM dimming methods to control LED brightness. The voltage level of the MODE pin determines the PWM dimming method. Direct PWM dimming mode is selected with the MODE pin tied to GND. The frequency programmable dimming mode is selected by either leaving the MODE pin open or pulling it high to VDD. In direct PWM dimming mode, the dimming frequency is synchronized to the PWM signal input on the PWMIN pin, while in frequency programmable dimming mode, the internal PWM dimming frequency is set by the resistor on the FPWMO pin.

DIRECT PWM DIMMING

In direct PWM dimming mode, all used IFB channels turn on and off together at the same frequency and duty cycle as the input PWM on the PWMIN pin. Figure 17 shows the timing diagram for direct PWM dimming.

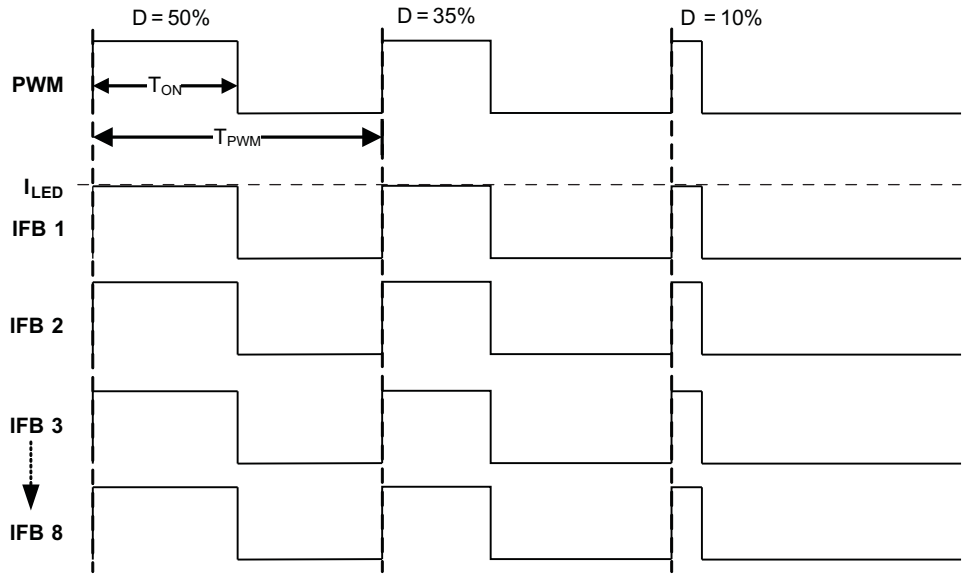


Figure 17. Direct PWM Dimming Timing Diagram

FREQUENCY PROGRAM PWM DIMMING

In this mode, all used IFB channels are turned on and off together at the internal oscillator frequency as set by the resistor on the FPWMO pin. Figure 18 shows the timing diagram for each channel when running in frequency program PWM dimming mode.

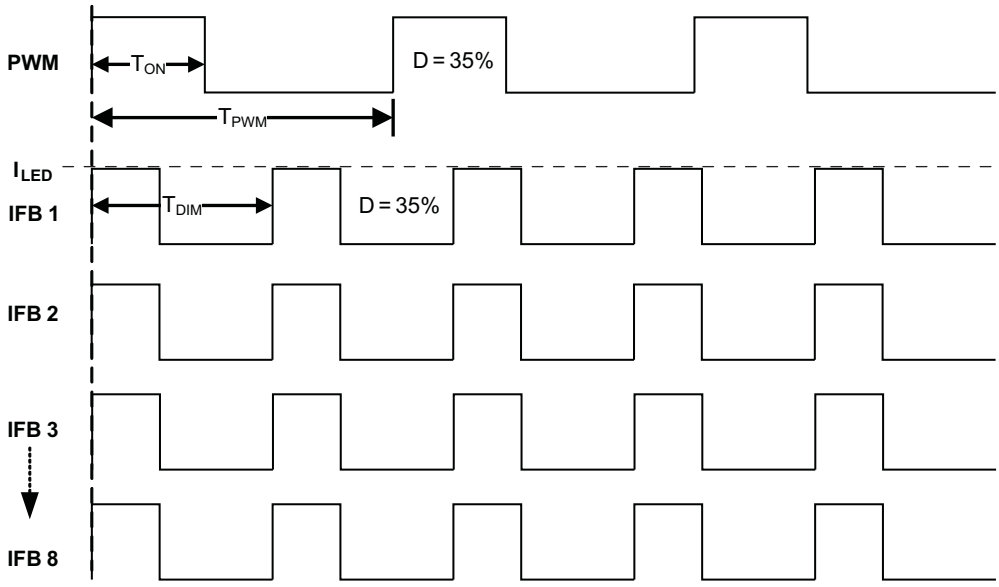


Figure 18. Frequency Program PWM Dimming Timing Diagram

The built-in oscillator is adjustable by an external resistor R_{FPWMO} on the FPWMO pin and is in the range of 100 Hz to 5 kHz approximately following Equation 3:

$$F_{PWMO} \approx \frac{1.5 \times 10^8}{R_{FPWMO}} \quad (3)$$

Where: R_{FPWMO} = FPWMO pin resistor

The adjustable range of the R_{FPWMO} resistor is from 27 kΩ to 1.5 MΩ, corresponding to the dimming frequency, F_{PWMO}, of 100 Hz to 5 kHz. See Figure 10 for PWM dimming frequency adjustment resistor R_{FPWMO} selection and Table 1 for the resistor value recommendation list.

Table 1. Resistor Value Recommendation List

RFPWMO	FPWMO
715 kΩ	210 Hz
309 kΩ	500 Hz
150 kΩ	1000 Hz
72.3 kΩ	2000 Hz

During PWM dimming, minimum on time in each dimming cycle is 5 µs typical. This means the minimum duty cycle of PWM dimming can be down to 1% when the dimming frequency is less than 2 kHz.

OVER VOLTAGE PROTECTION (OVP)

The TPS61185 has two levels of protection to prevent the output, and therefore the SW pins, from exceeding a certain voltage. The output voltage clamp circuit limits the output voltage to the user selected value by limiting the internal feedback loop reference level. The clamp circuit response time is not fast enough to protect against output voltage transients or high-voltage noise spikes that couple from external circuits. So, if the over voltage (OV) circuit detects the output going 80 mV higher than the clamp voltage, it turns off the boost switch until the output voltage drops below the clamp voltage. Resistors R3 and R4 in Typical Application Circuit set the output voltage clamp threshold and OV threshold as computed by Equation 4 and Equation 5.

$$V_{OUT\_CLAMP} = V_{CLAMP\_TH} \times \left(1 + \frac{R3}{R4}\right) \quad (4)$$

$$V_{OUT\_OV} = V_{OV\_TH} \times \left(1 + \frac{R3}{R4}\right) \quad (5)$$

Where:

V_{CLAMP_TH} = 1.95 V typically
V_{OV_TH} = 2.03 V typically

In the Typical Application Circuit, the output OVP voltage is set to:

$$V_{OUT\_CLAMP} = 1.95 \times \left(1 + \frac{1\ M}{54.9\ K}\right) = 37.5\ V \quad (6)$$

$$V_{OUT\_OV} = 2.03 \times \left(1 + \frac{1M}{54.9K}\right) = 39.0\ V \quad (7)$$

CURRENT SINK OPEN AND SHORT PROTECTION

For the TPS61185, if one of the WLED strings is open, the boost output rises to the output voltage clamp threshold. The IC detects the open WLED string by sensing no current on the corresponding IFB pin. As a result, the IC deactivates the open IFB pin and removes it from the voltage feedback loop. Subsequently, the output voltage returns to the minimum voltage required for the connected WLED strings. The IFB pin currents of the connected WLED strings remain in regulation during this process.

If any IFB pin voltage exceeds the IFB over voltage threshold (5 V typical), the IC turns off the corresponding current sink and removes this IFB pin from the output voltage regulation loop. Current regulation of the remaining IFB pins is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create such a large voltage difference among WLED strings.

The IC only shuts down if it detects that all of the WLED strings are open. If any open WLED string is reconnected, it is reactivated automatically.

OVER CURRENT AND SHORT CIRCUIT PROTECTION

The TPS61185 pulse by pulse over-current limit is 2.0 A (min). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the IC and external components under over-load conditions. When there is a sustained over-current condition, the IC turns off and requires a POR or EN pin toggling to restart.

Under severe over-load and/or short circuit conditions, the boost output voltage can be pulled below the required regulated voltage to keep all of the white LEDs operating with all IFB voltage higher than 400 mV. Under this condition, the current flows directly from input to output through the inductor and schottky diode. To protect the TPS61185, the device shuts down immediately. The IC restarts after input POR or EN pin logic toggling.

SKIP PULSE OPERATION

When the input voltage on the V_{IN} pin is less than 1 V higher than the total LED forward voltage, the TPS61185 boost regulator operates in skip pulse mode. In pulse skip mode, the main switch turns on/off for several cycles to charge the inductor and output capacitor and continues to regulate the output voltage and current sinks continue to regulate the IFB pin current.

If the input voltage is more than 1 V higher than the output total LED forward voltage, the boost regulator shuts down. The output voltage follows the V_{IN} voltage with a diode forward voltage drop and the current sinks continue to regulate the IFB pin current.

Once the input voltage is approximately 5 V higher than the total LED forward voltage, the IFB voltage exceeds the 5 V IFB over-voltage threshold and the LED current sinks are disabled.

THERMAL PROTECTION

When the junction temperature of the TPS61185 is over 170°C (typ), the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature is back to less than 170°C with about 15°C hysteresis.

APPLICATION INFORMATION

INDUCTOR SELECTION

Because the selection of an inductor affects power supply steady state operation, transient behavior, and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, dc resistance, and saturation current. The TPS61185 is designed to work with inductor values between 4.7 µH and 10 µH. A 4.7 µH inductor is typically available in a smaller or lower profile package, while a 10 µH inductor may produce higher efficiency due to slower switching frequency and/or lower inductor ripple. If boost output current is limited by the over-current protection of the IC, using a 10 µH inductor and the highest switching frequency maximizes the controller's output current capability.

Internal loop compensation for PWM control is optimized for the external component values, including typical tolerances, recommended on page 3. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0 A value depending on how the inductor vendor defines saturation.

In a boost regulator, the inductor dc current can be calculated as:

$$I_{dc} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (8)$$

Where:

V_{out} = Boost output voltage
I_{out} = Boost output current
V_{in} = Boost input voltage
η = Power conversion efficiency, use 90% for TPS61185 applications

Inductor current peak-to-peak ripple can be calculated as:

$$I_{pp} = \frac{1}{L \times \left(\frac{1}{V_{out} - V_{in}} + \frac{1}{V_{in}} \right) \times F_{sw}} \quad (9)$$

Where:

I_{pp} = Inductor peak-to-peak ripple
L = Inductor value
F_{SW} = Switching frequency
V_{out} = Boost output voltage
V_{in}= Boost input voltage

Therefore, the peak current seen by the inductor is:

$$I_p = I_{dc} + \frac{I_{pp}}{2} \quad (10)$$

Select an inductor with a saturation current at least 30% higher the calculated peak current to account for the load transient steps that occur during startup and dimming. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage, and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and the switching losses associated with the PWM switch and power diode. Although the TPS61185 IC has optimized internal switch resistances, overall efficiency is affected by the inductor's dc resistance (DCR); lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 2 lists recommended inductor models.

Table 2. Recommended Inductors for the TPS61185

	L (µH)	DCR (mΩ)	I_{sat} (A)	Size (L×W×H mm)
TOKO				
A915AY-4R7M	4.7	38	1.87	5.2×5.2×3.0

Table 2. Recommended Inductors for the TPS61185 (continued)

	L (µH)	DCR (mΩ)	I_{sat} (A)	Size (L×W×H mm)
A915AY-100M	10	75	1.24	5.2×5.2×3.0
TDK				
VLF5014ST-4R7M1R7	4.7	98	1.7	4.6×4.8×1.4
VLF5014ST-100M1R2	10	210	1.2	4.6×4.8×1.4

OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{out} = \frac{(V_{out} - V_{in}) \times I_{out}}{V_{out} \times F_{boost} \times V_{ripple}} \quad (11)$$

Where,

V_{ripple} = Peak-to-peak output ripple. The additional part of ripple caused by the ESR is calculated using:
$V_{ripple\_ESR} = I_{out} \times R_{ESR}$

Due to its low ESR, V_{ripple_ESR} can be neglected for a ceramic capacitor, but must be considered if a tantalum or electrolytic capacitor is used.

The output voltage of the controller also ripples due to the load transient that occurs during PWM dimming. The TPS61185 adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. In a typical application, the output ripple is less than 250 mV during PWM dimming with a 4.7 µF output capacitor. However, the output ripple decreases with higher output capacitances. An output capacitance value in the range of 4.7 µF to 10 µF is required for loop stability.

The popular vendors for high value ceramic capacitors are:

- TDK (http://www.component.tdk.com/components.php)
- Murata (http://www.murata.com/products/capacitor/index.html)

ISOLATION MOSFET SELECTION

The TPS61185 IC provides a gate drive to an external P channel MOSFET which is turned off during a device shutdown or fault condition. This MOSFET provides a true shutdown function and also protects the battery from output short circuit conditions. The source of the PMOS should be connected to the input, and a pull up resistor is required between the source and the gate of the FET to keep the FET off during IC shutdown. To turn on the isolation FET, the FAULT pin is pulled low and clamped to 8 V below the Vbat pin voltage.

During a device shutdown or fault condition, the isolation FET is turned off and input voltage is applied on the isolation MOSFET. During a short circuit condition, the catch diode (D2 in the Typical Application Circuit) is forward biased when the isolation FET is turned off. Drain of the isolation FET swings below ground. Voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30 V PMOS for a 24 V maximum input. The FETs on resistance, $R_{DS(on)}$, has a large impact on power conversion efficiency since the input current flows through the FET. Select a MOSFET with $R_{DS(on)}$ less than 100 mΩ to limit power losses.

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C4 in the Typical Application Circuit, needs not only to be close to the V_{IN} pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The input capacitor, C1 in the Typical Application Circuit, should be also placed close to the inductor. C3 is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VDDIO and AGND pins to prevent any noise insertion to digital circuits. The SW pin carries high current with fast rising and falling edges. Therefore, the

connection between the pin to the inductor and the schottky diode should be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin since there is large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separate from power ground traces and connect them together at a single point, for example on the thermal pad.

Resistors R1, R2, and R5 in the Typical Application Circuits are current setting and frequency programming resistors. To avoid unexpected noise coupling into the pins and affecting current or frequency accuracy, these resistors need to be close to the pins with short and wide traces to GND.

The thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. Additional thermal via can significantly improve power dissipation of the IC.

ADDITIONAL APPLICATION CIRCUITS

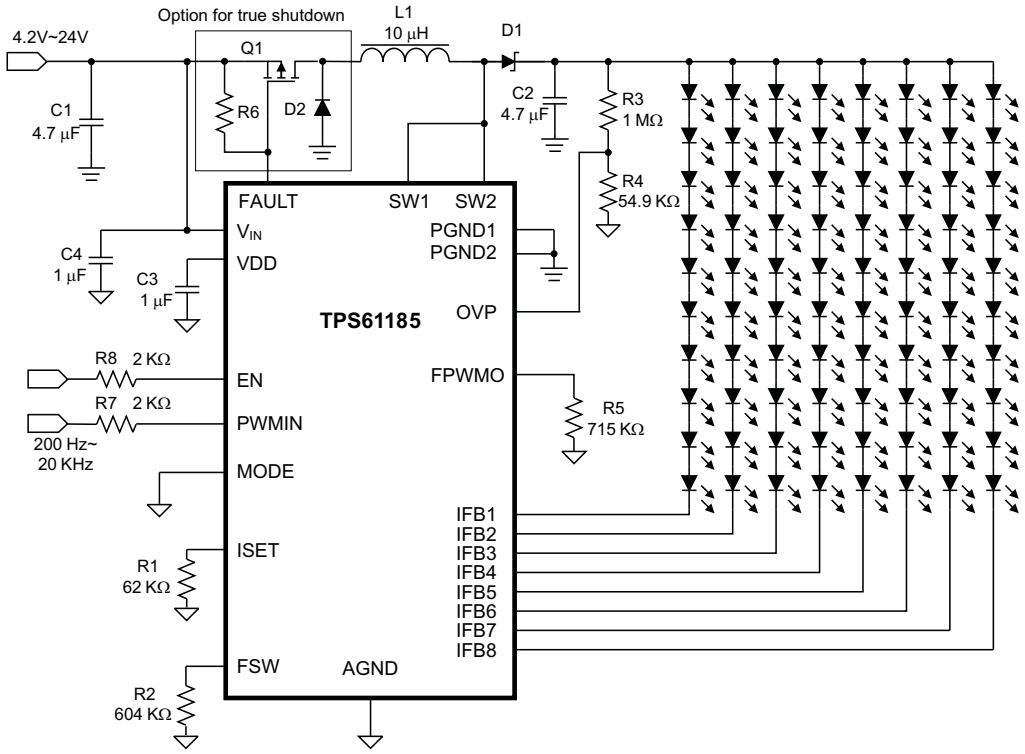


Figure 19. Typical Application Circuit with True Shutdown ISO-FET

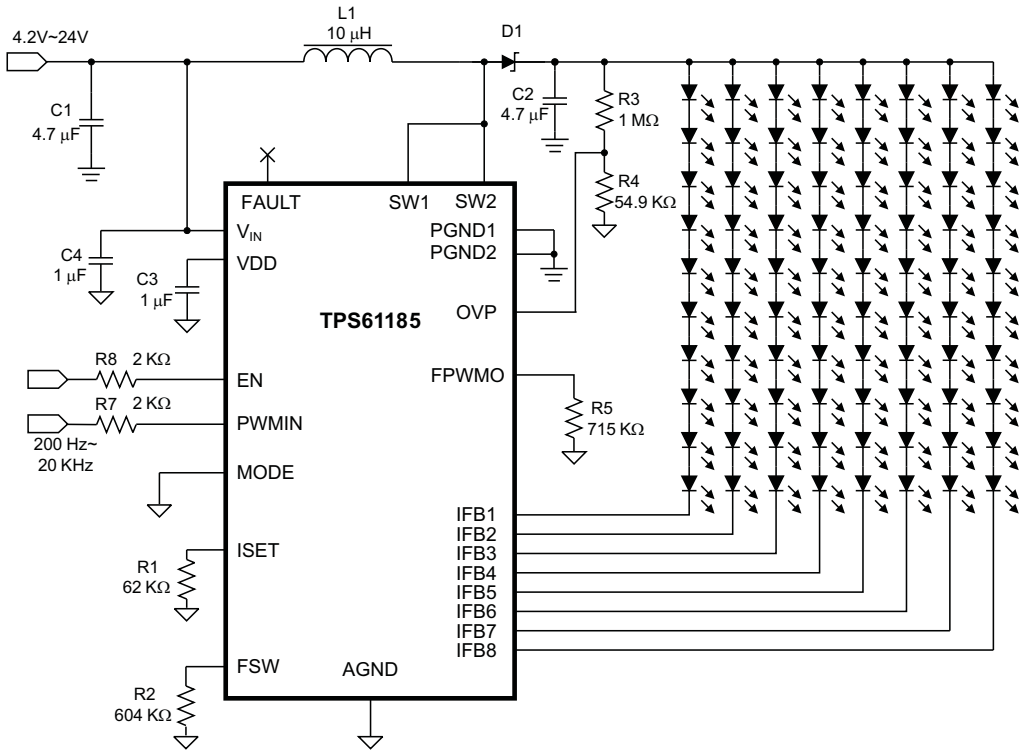


Figure 20. Typical Application Circuit for Direct PWM Dimming

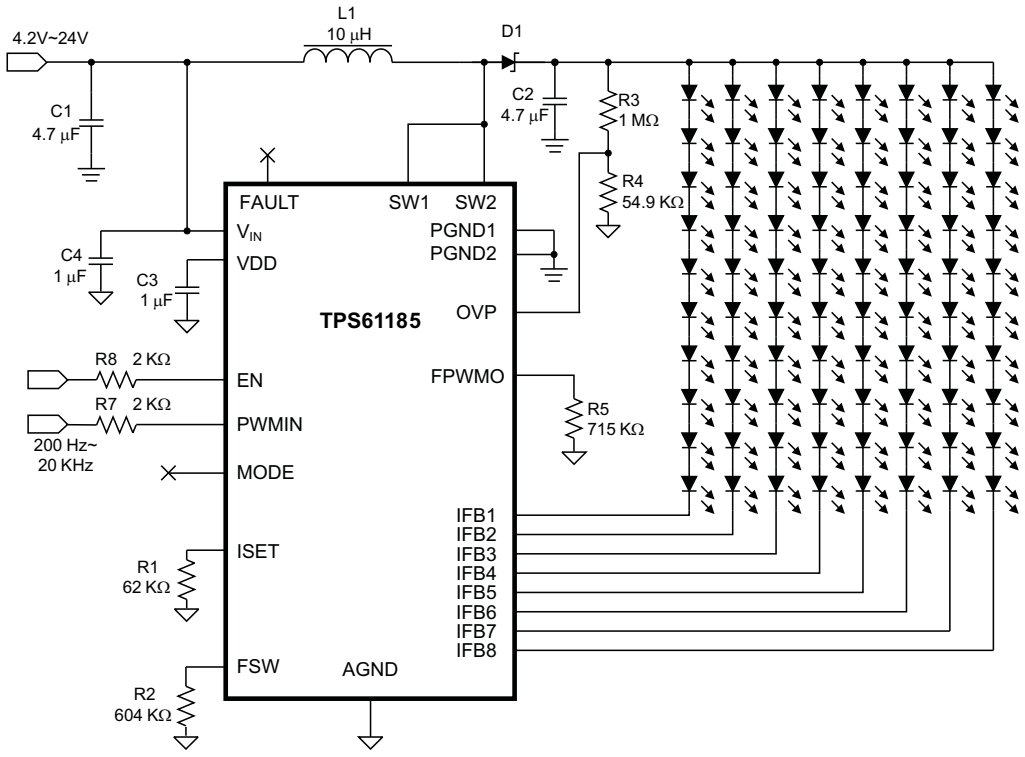


Figure 21. Typical Application Circuit for Programmable Frequency Dimming

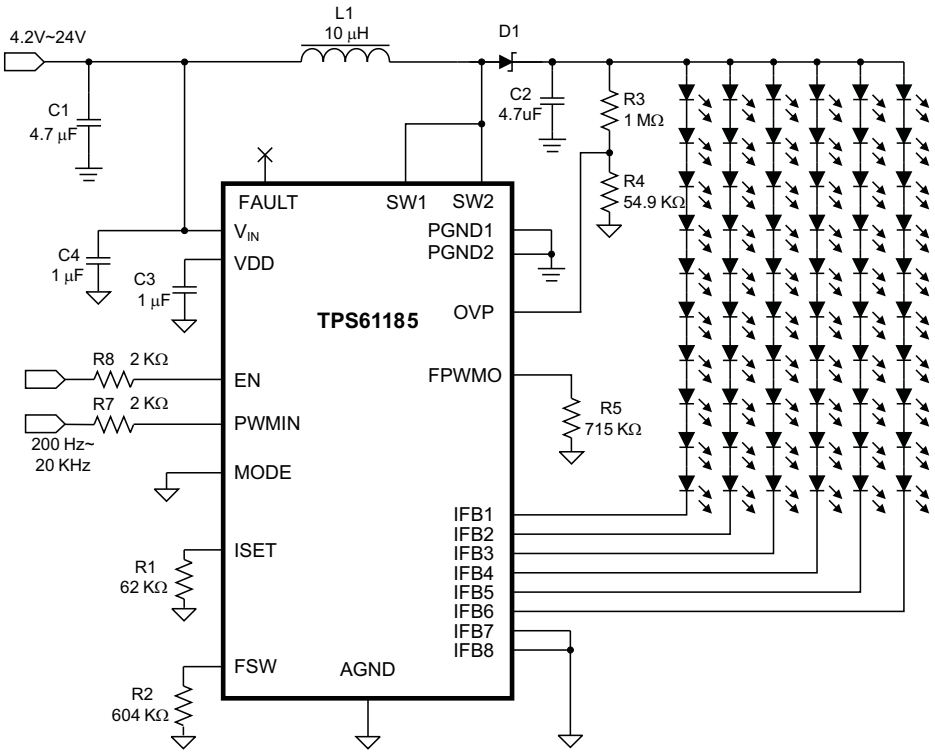


Figure 22. Typical Application Circuit for Six Strings of LEDs

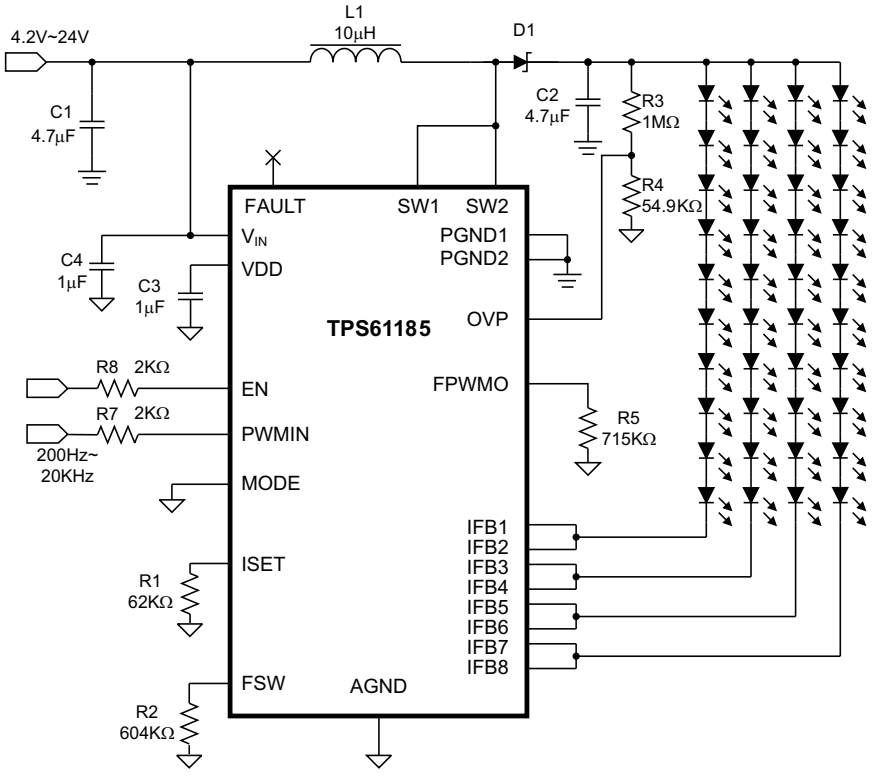


Figure 23. Typical Application Circuit for Four Strings of 40 mA LEDs

PACKAGING INFORMATION

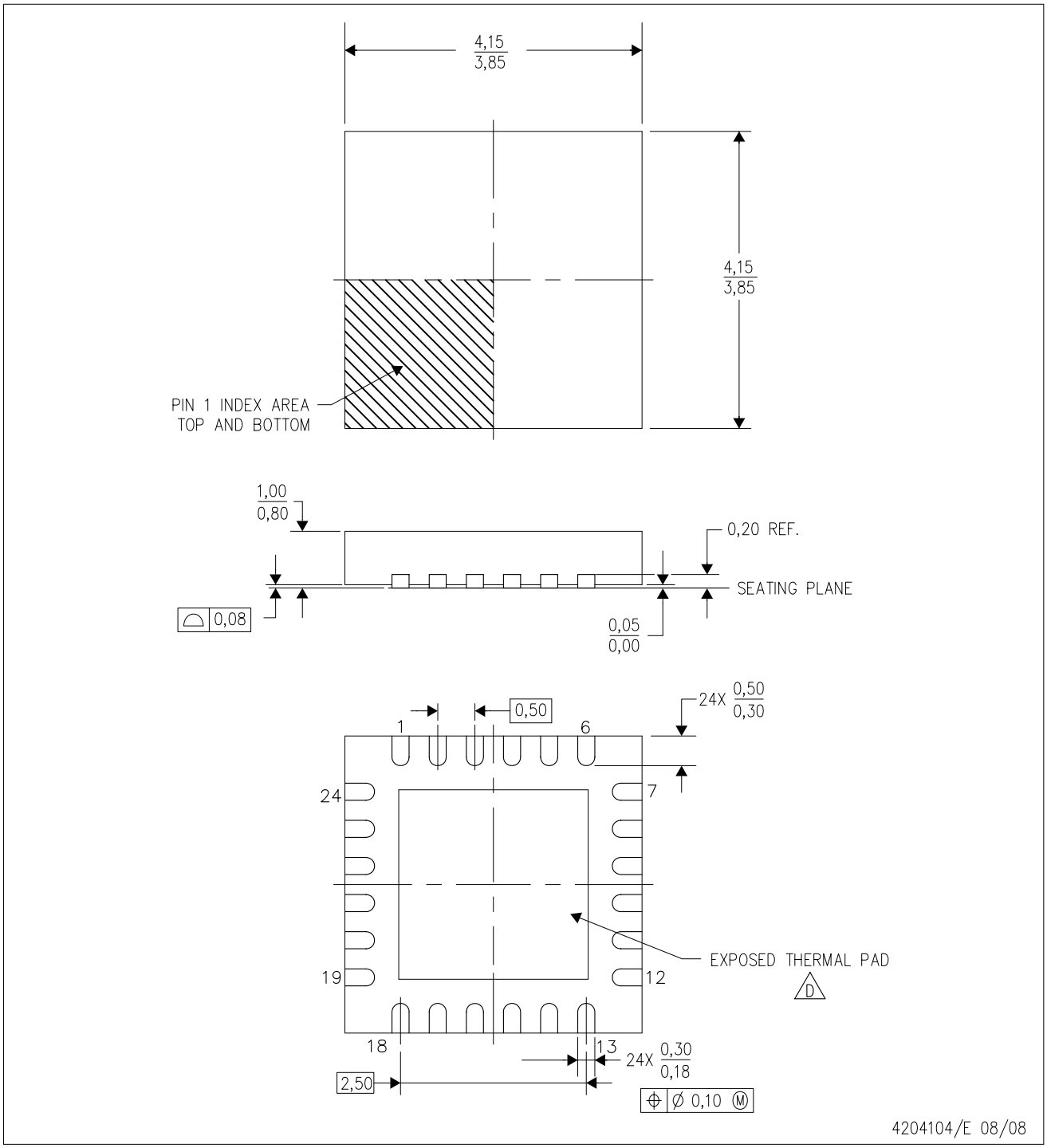
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS61185RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TPS61185RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



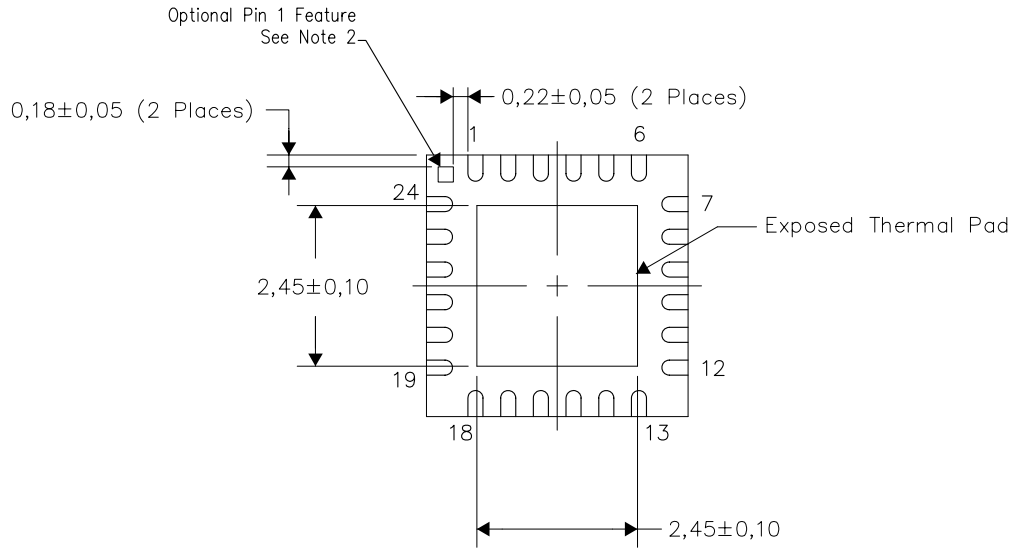
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



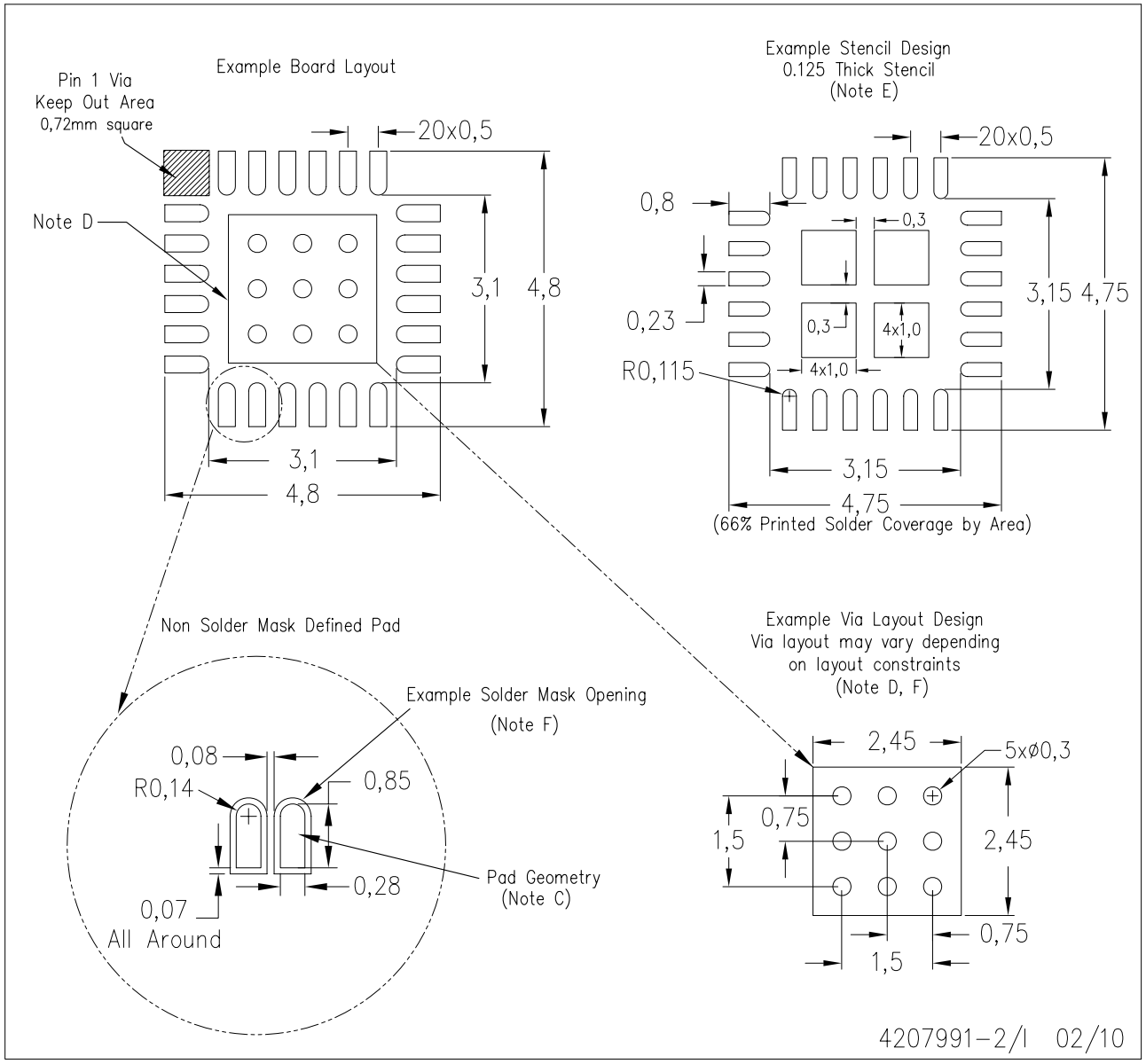
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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