White LED Driver With PWM Brightness Control in 2mm x 2mm QFN Package for up to 10 LEDs in Series

FEATURES

- **2.7V to 18V Input Voltage Range**
- **26V Open LED Protection for 6 LEDs (TPS61160A)**
  38V Open LED Protection for 10 LEDs (TPS61161A)
- **200mV Reference Voltage With ±2% Accuracy**
- **PWM Interface for Brightness Control**
- **Built-in Soft Start**
- **Up to 90% Efficiency**
- **2mm × 2mm × 0.8mm 6-pin QFN Package With Thermal Pad**

APPLICATIONS

- **Cellular Phones**
- **Portable Media Players**
- **Ultra Mobile Devices**
- **GPS Receivers**
- **White LED Backlighting for Media Form Factor Display**

DESCRIPTION

With a 40-V rated integrated switch FET, the TPS61160A/61A is a boost converter that drives up to 10 LEDs in series. The boost converter runs at 600kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200mV, as shown in the typical application. During the operation, the LED current can be controlled by a pulse width modulation (PWM) signal applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In PWM dimming mode, the TPS61160A/61A does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS61160A/61A to prevent the output from exceeding the absolute maximum ratings during open LED conditions.

The TPS61160A/61A is available in a space-saving, 2mm × 2mm QFN package with thermal pad.

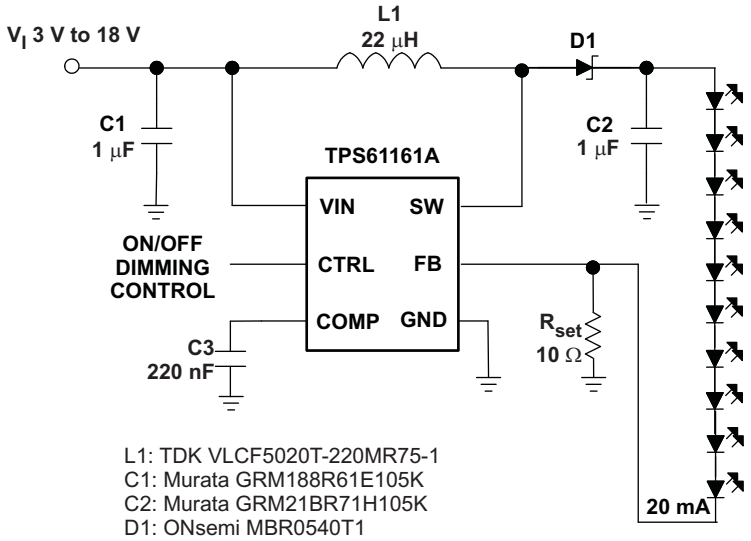

Figure 1. Typical Application of TPS61161A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	OPEN LED PROTECTION	PACKAGE(2)	PACKAGE MARKING
–40°C to 85°C	26V (typical)	TPS61160ADRV	OBV
	38V (typical)	TPS61161ADRV	OBT

(1) For the most current package and ordering information, see the TI Web site at www.ti.com.
(2) The DRV package is available in tape and reel. Add R suffix (TPS61160ADRVR) to order quantities of 3000 parts per reel or add T suffix (TPS61160ADRVT) to order 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_I	Supply Voltages on VIN (2)	–0.3 to 20	V
	Voltages on CTRL(2)	–0.3 to 20	V
	Voltage on FB and COMP(2)	–0.3 to 3	V
	Voltage on SW(2)	–0.3 to 40	V
P_D	Continuous Power Dissipation	See Dissipation Rating Table	
T_J	Operating Junction Temperature Range	–40 to 150	°C
T_{STG}	Storage Temperature Range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

BOARD PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
Low-K(1)DRV	20°C/W	140°C/W	7.1 mW/°C	715 mW	395 mW	285 mW
High-K (2)DRV	20°C/W	65°C/W	15.4 mW/°C	1540 mW	845 mW	615 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in×3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in×3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_I	Input voltage range, VIN	2.7		18	V
V_O	Output voltage range	VIN		38	V
L	Inductor(1)	10		22	µH
f_{dim}	PWM dimming frequency(2)	5		100	kHz
Duty	PWM duty cycle resolution at 10kHz	0.5			%
	at 30kHz	1.5			
C_{IN}	Input capacitor	1			µF
C_O	Output capacitor(1)	0.47		10	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.
(2) The device can support the frequency range from 1kHz to 5kHz based on the specification, t_{off}. The output ripple needs to be considered in the range of 1kHz to 5kHz.

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ELECTRICAL CHARACTERISTICS

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range, VIN		2.7		18	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load			1.8	mA
I_{SD}	Shutdown current	CRTL=GND, VIN = 4.2 V			1	µA
UVLO	Undervoltage lockout threshold	VIN falling		2.2	2.5	V
V_{hys}	Undervoltage lockout hysterisis			70		mV
ENABLE AND REFERENCE CONTROL						
$V_{(CTRLh)}$	CTRL logic high voltage	VIN = 2.7 V to 18 V	1.2			V
$V_{(CTRLl)}$	CTRL logic low voltage	VIN = 2.7 V to 18 V			0.4	V
$R_{(CTRL)}$	CTRL pull down resistor		400	800	1600	kΩ
t_{off}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		196	200	204	mV
$V_{(REF_PWM)}$	Voltage feedback regulation voltage under brightness control	V_{FB} = 50 mV	47	50	53	mV
		V_{FB} = 20 mV	17	20	23	
I_{FB}	Voltage feedback input bias current	V_{FB} = 200 mV			2	µA
f_S	Oscillator frequency		500	600	700	kHz
D_{max}	Maximum duty cycle	V_{FB} = 100 mV	90	93		%
t_{min_on}	Minimum on pulse width			40		ns
I_{sink}	Comp pin sink current			100		µA
I_{source}	Comp pin source current			100		µA
G_{ea}	Error amplifier transconductance		240	320	400	µmho
R_{ea}	Error amplifier output resistance			6		MΩ
f_{ea}	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6 V		0.3	0.6	Ω
		VIN = 3.0 V			0.7	
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA
OC and OLP						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	0.56	0.7	0.84	A
I_{LIM_Start}	Start up current limit	D = D_{max}		0.4		A
t_{Half_LIM}	Time step for half current limit			5		ms
V_{ovp}	Open LED protection threshold	Measured on the SW pin, TPS61160A TPS61161A	25 37	26 38	27 39	V
$V_{(FB_OVP)}$	Open LED protection threshold on FB	Measured on the FB pin, percentage of Vref, Vref = 200 mV and 20 mV		50%		
t_{REF}	V_{REF} filter time constant			180		µs
t_{step}	V_{REF} ramp up time			213		µs
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

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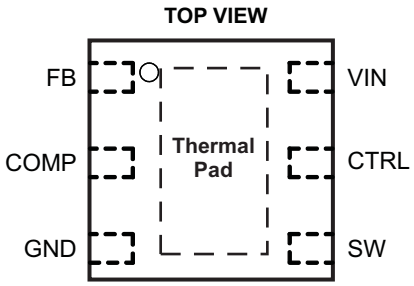
DEVICE INFORMATION



6-PIN 2mm x 2mm x 0.8mm QFN

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	6	I	The input supply pin for the IC. Connect VIN to a supply voltage between 2.7V and 18V.
SW	4	I	This is the switching node of the IC. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection
GND	3	O	Ground
FB	1	I	Feedback pin for current. Connect the sense resistor from FB to GND.
COMP	2	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the regulator.
CTRL	5	I	Control pin of the boost regulator. Enable and disable IC. PWM signal can be applied to the pin for LED brightness dimming as well.
Thermal Pad			The thermal pad should be soldered to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

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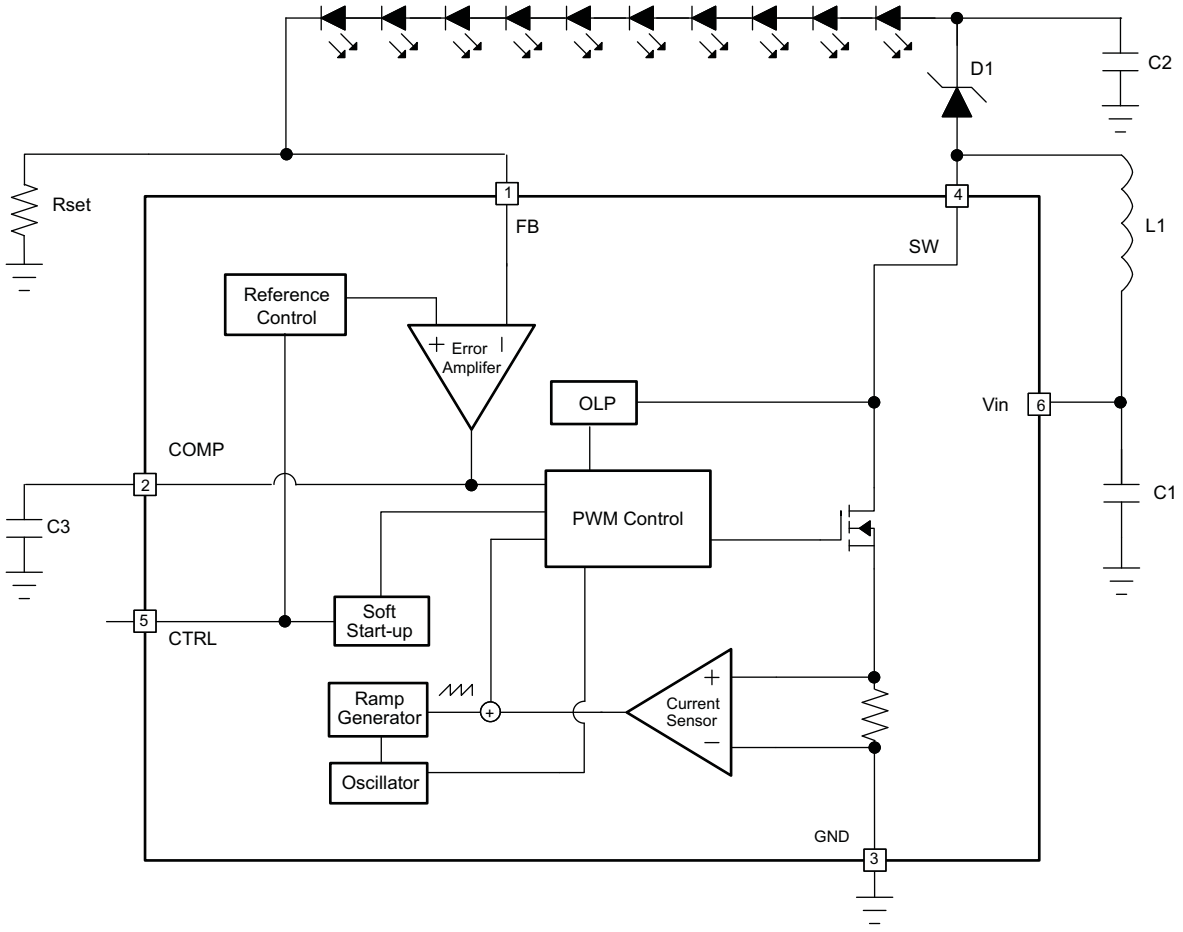
FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency TPS61160A/61A	VIN = 3.6 V; 4, 6, 8, 10 LEDs; L = 22 µH	Figure 2
Efficiency TPS61160A		Figure 3
Efficiency TPS61161A		Figure 4
Current limit	T_A = 25°C	Figure 5
Current limit		Figure 6
PWM dimming linearity	VIN = 3.6 V; PWM Freq = 10 kHz and 40 kHz	Figure 7
Output ripple at PWM dimming	8 LEDs; VIN = 3.6 V; I_{LOAD} = 20 mA; PWM Freq = 10 kHz	Figure 8
Switching waveform	8 LEDs; VIN = 3.6 V; I_{LOAD} = 20 mA; L = 22 µH	Figure 9
Start-up	8 LEDs; VIN = 3.6 V; I_{LOAD} = 20 mA; L =22 µH	Figure 10
Open LED protection	8 LEDs; VIN = 3.6 V; I_{LOAD} = 20 mA; L = 22 µH	Figure 11

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EFFICIENCY VS OUTPUT CURRENT

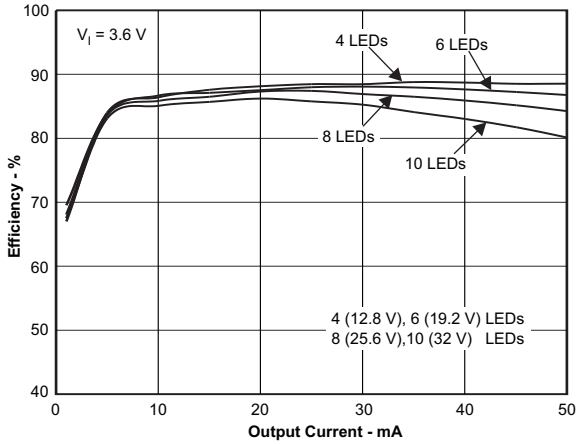

Figure 2.

EFFICIENCY VS OUTPUT CURRENT

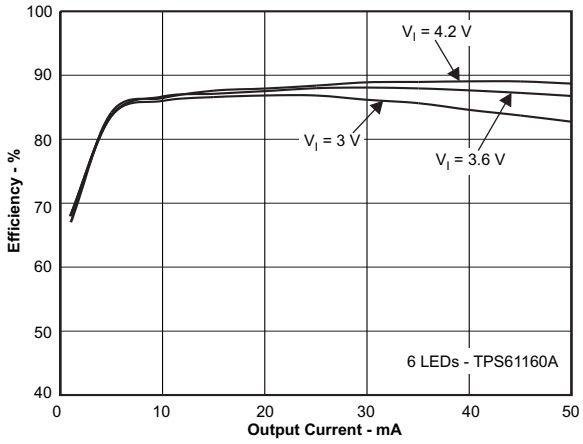

Figure 3.

EFFICIENCY VS OUTPUT CURRENT

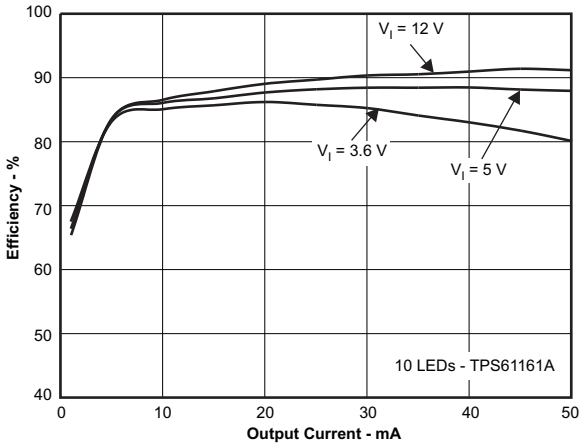

Figure 4.

SWITCH CURRENT LIMIT VS DUTY CYCLE

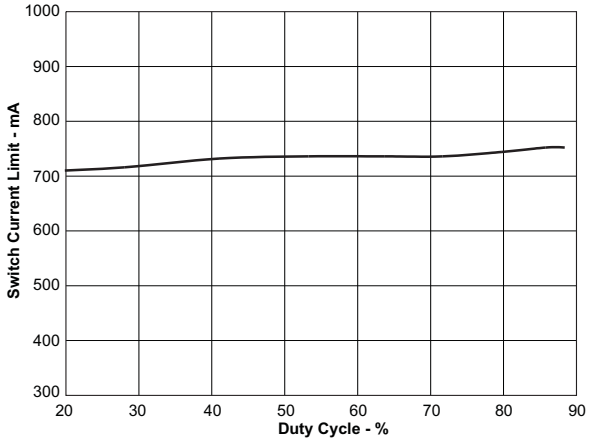

Figure 5.

SWITCH CURRENT LIMIT VS TEMPERATURE

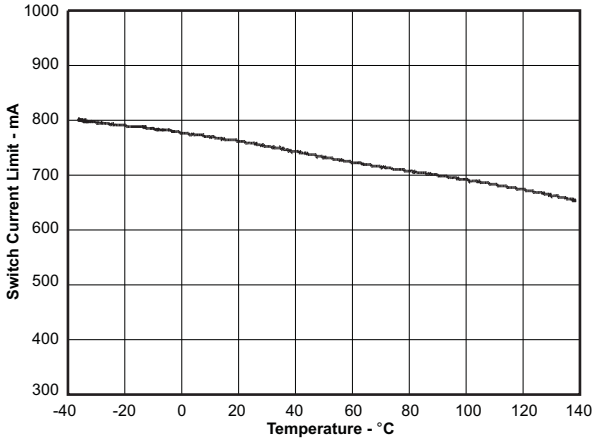

Figure 6.

FB VOLTAGE VS PWM DUTY CYCLE

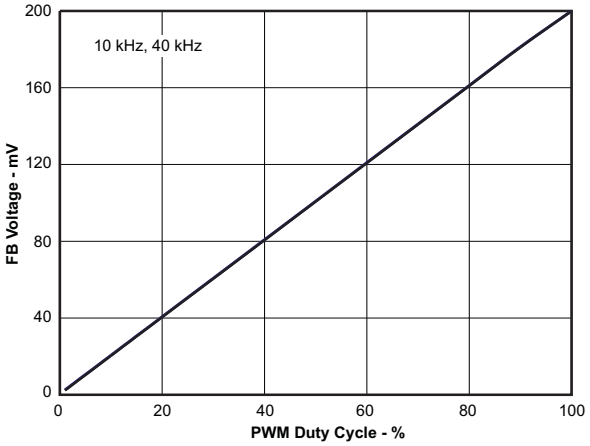

Figure 7.

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OUTPUT RIPPLE at PWM DIMMING

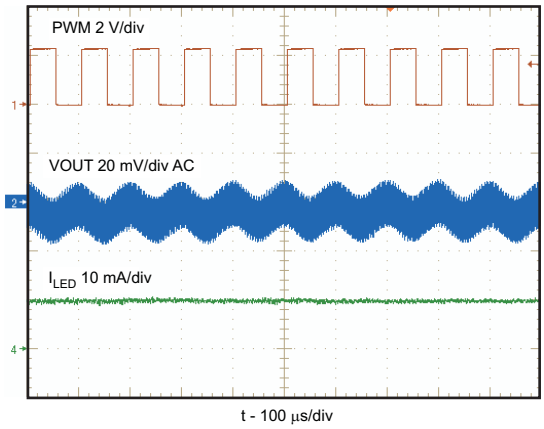

Figure 8.

SWITCHING WAVEFORM

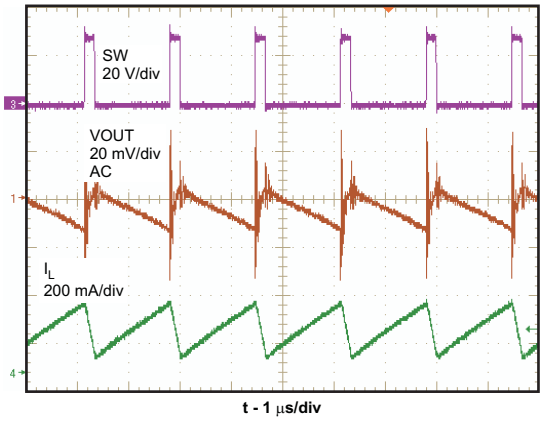

Figure 9.

START-UP

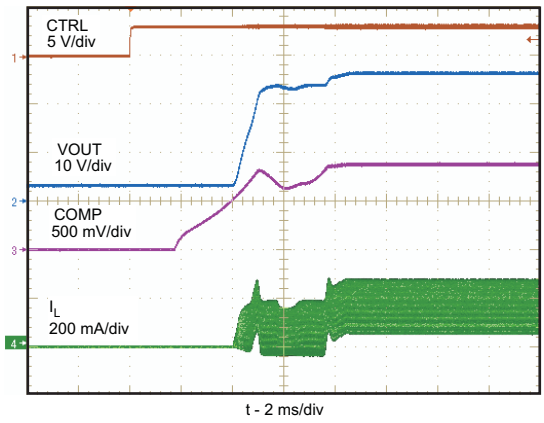

Figure 10.

OPEN LED PROTECTION

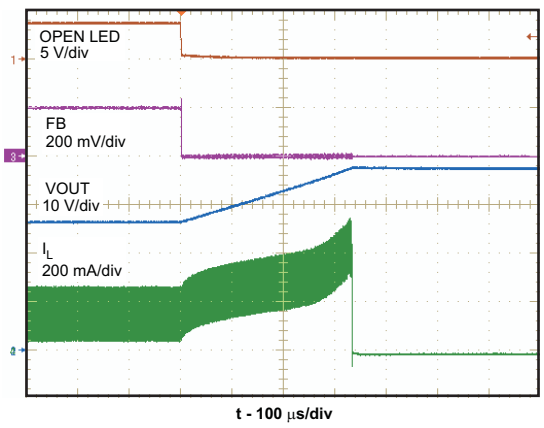

Figure 11.

DETAILED DESCRIPTION

OPERATION

The TPS61160A/61A is a high efficiency, high output voltage boost converter in small package size that is ideal for driving up to 10 white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40V/0.7A switch FET and operates in pulse width modulation (PWM) with 600kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, a slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

SOFT START-UP

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps, each step takes 213µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5msec after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 400mA (typical). See the start-up waveform of a typical example, Figure 10.

OPEN LED PROTECTION

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61160A/61A monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC as soon as the SW voltage exceeds the Vovp threshold and the FB voltage is less than half of regulation voltage for 8 clock cycles. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin logic. To allow the use of inexpensive low-voltage output capacitor, the TPS61160A/61A has different open lamp protection thresholds to prevent the internal 40V FET from breaking down. The threshold is set at 26V for the TPS61160A and 38V for the TPS61161A. The devices can be selected according to the number of external LEDs and their maximum forward voltage.

SHUTDOWN

The TPS61160A/61A enters shutdown mode when the CTRL voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is less than 1µA (max). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown; however, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

CURRENT PROGRAM

The FB voltage is regulated by a low 0.2V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the RSET is calculated using Equation 1:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

Where

I_{LED} = output current of LEDs
V_{FB} = regulated voltage of FB
R_{SET} = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

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PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = \text{Duty} \times 200\ \text{mV} \quad (2)$$

Where

Duty = duty cycle of the PWM signal
200 mV = internal reference voltage

As shown in Figure 12, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, TPS61160A/61A regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz. The requirement of minimum dimming frequency comes from the output ripple. Low frequency causes high output ripple. Since the CTRL pin is logic only pin, applying an external RC filter to the pin does not work.

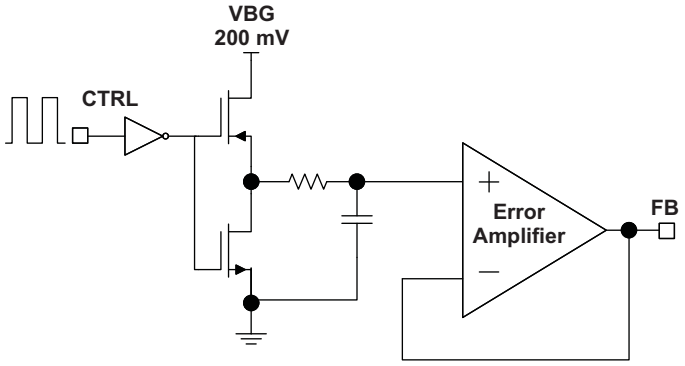

Figure 12. Block Diagram of Programmable FB Voltage Using PWM Signal

To use lower PWM dimming, add an external RC network connected to the FB pin as shown in the additional typical application (Figure 15).

UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

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APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{\left[L \times F_s \times \left(\frac{1}{V_{out} + V_f - V_{in}} + \frac{1}{V_{in}}\right)\right]} \quad (3)$$

Where:

I_p = inductor peak to peak ripple
L = inductor value
V_f = Schottky diode forward voltage
Fs = switching frequency
V_{out} = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

$$I_{out_max} = \frac{Vin \times \left(I_{lim} - I_P/2\right) \times \eta}{Vout} \quad (4)$$

Where:

I_{out_max} = maximum output current of the boost converter
I_{lim} = over current limit
η = efficiency

For instance, when VIN is 3.0V, 8 LEDs output equivalent to VOUT of 26V, the inductor is 22µH, the Schottky forward voltage is 0.2V; and then the maximum output current is 65mA in typical condition. When VIN is 5V, 10 LEDs output equivalent to VOUT of 32V, the inductor is 22µH, the Schottky forward voltage is 0.2V; and then the maximum output current is 85mA in typical condition.

INDUCTOR SELECTION

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor DC current given by:

$$I_{in_DC} = \frac{Vout \times Iout}{Vin \times \eta} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10µH to 22µH inductor value range is recommended. A 22µH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. Table 1 lists the recommended inductor for the TPS61160A/61A. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

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TPS61160A/61A has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10µH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 1. Recommended Inductors for TPS61160A/61A

PART NUMBER	L (µH)	DCR MAX (Ω)	SATURATION CURRENT (mA)	SIZE (L × W × H mm)	VENDOR
LQH3NPN100NM0	10	0.3	750	3×3×1.5	Murata
VLCF5020T-220MR75-1	22	0.4	750	5×5×2.0	TDK
CDH3809/SLD	10	0.3	570	4×4×1.0	Sumida
A997AS-220M	22	0.4	510	4×4×1.8	TOKO

SCHOTTKY DIODE SELECTION

The high switching frequency of the TPS61160A/61A demands a high-speed rectification for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for TPS61160A/61A.

COMPENSATION CAPACITOR SELECTION

The compensation capacitor C3 (see the block diagram), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61160A/61A. Use a 220nF ceramic capacitor for C3.

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{\left(V_{out} - V_{in}\right) I_{out}}{V_{out} \times Fs \times V_{ripple}} \quad (6)$$

where, V_{ripple} = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple_ESR} = I_{out} \times R_{ESR}$$

Due to its low ESR, Vripple_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1µF to 4.7µF is recommended for input side. The output requires a capacitor in the range of 0.47µF to 10µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. For example, if use the output capacitor of 0.1µF, a 470nF compensation capacitor has to be used for the loop stable.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

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LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the IC supply ripple. Figure 13 shows a sample layout.

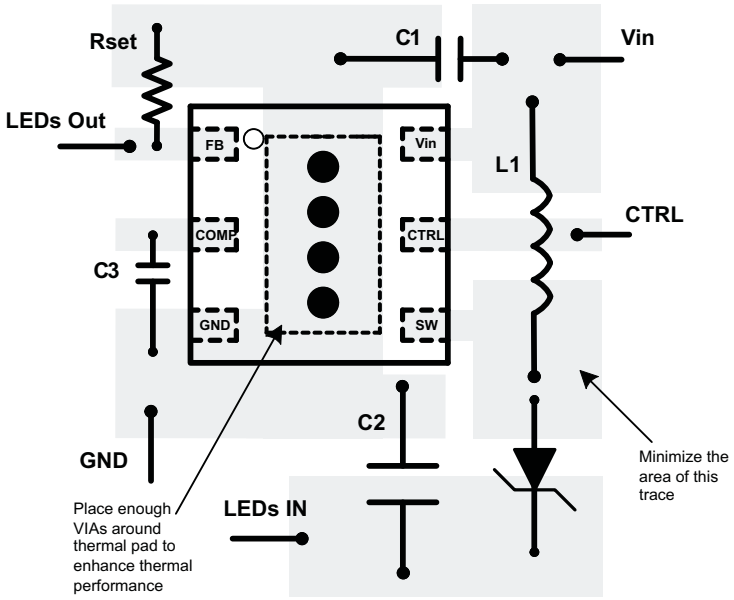

Figure 13. Sample Layout

THERMAL CONSIDERATIONS

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61160A/61A. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 7:

$$P_{D(max)} = \frac{125^{\circ}C - T_A}{R_{\theta JA}} \quad (7)$$

where, T_A is the maximum ambient temperature for the application. $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in Power Dissipation Table.

The TPS61160A/61A comes in a thermally enhanced QFN package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the QFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad as illustrated in the layout example. Also see the *QFN/SON PCB Attachment* application report (SLUA271).

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ADDITIONAL TYPICAL APPLICATIONS

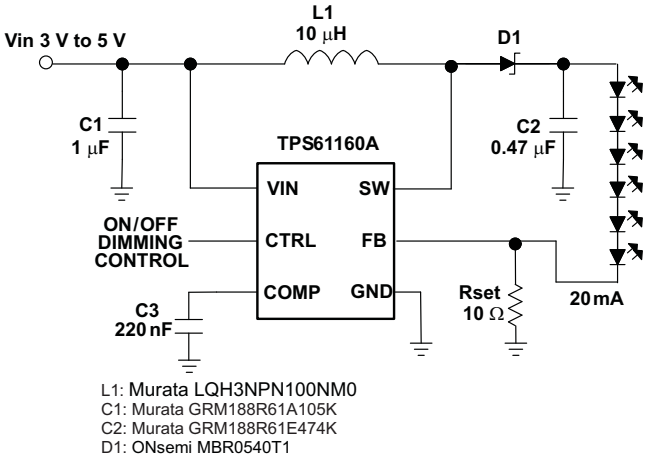

Figure 14. Li-Ion Driver for 6 White LEDs

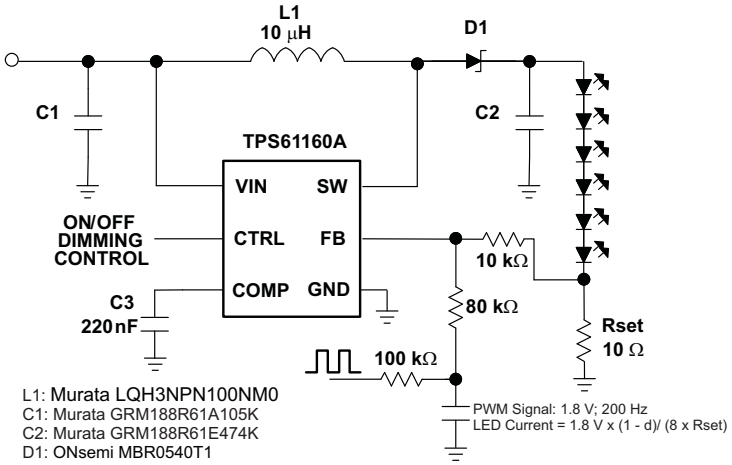

Figure 15. Li-Ion Driver for 6 White LEDs With External PWM Dimming Network

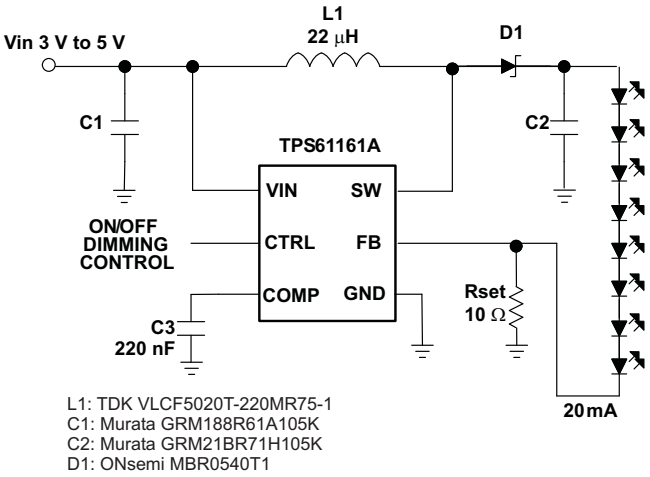

Figure 16. Li-Ion Driver for 8 White LEDs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS61160ADRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61160ADRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61161ADRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61161ADRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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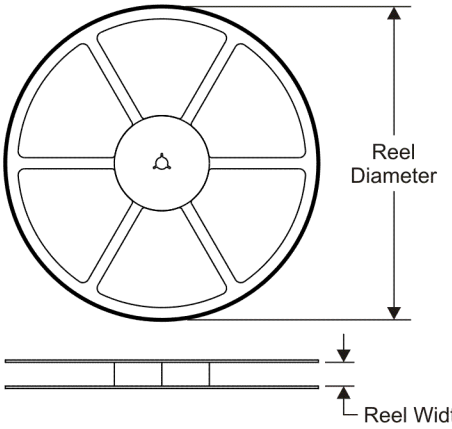
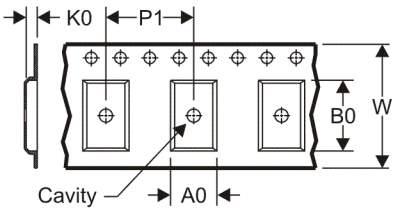
TAPE AND REEL INFORMATION

REEL DIMENSIONS

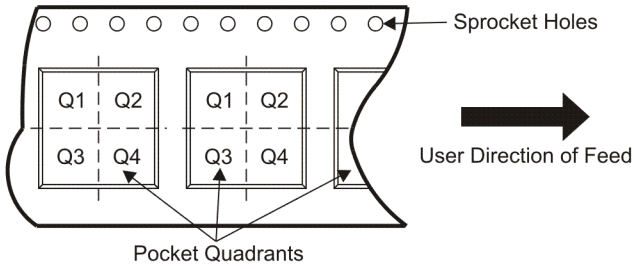


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

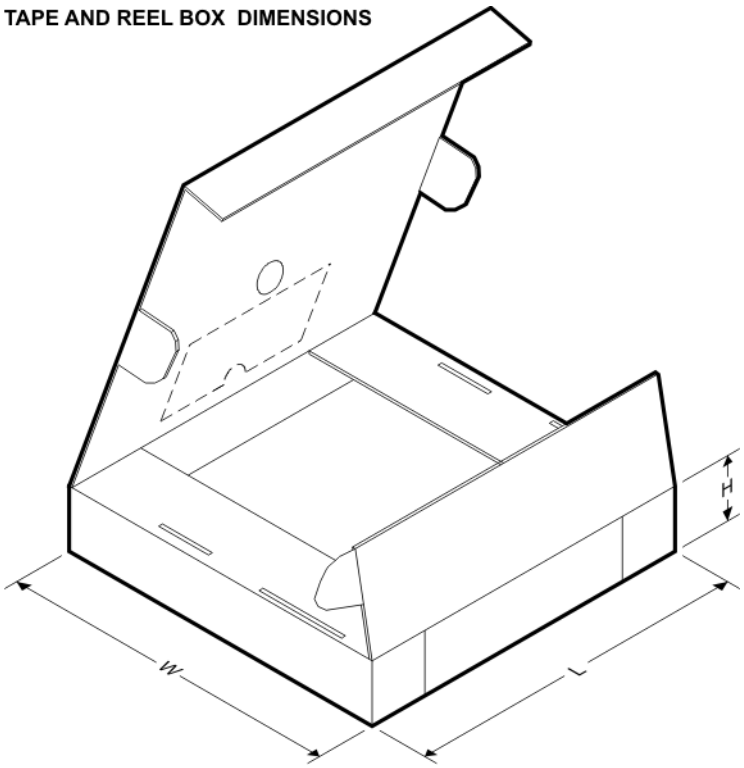
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61160ADRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
TPS61160ADRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
TPS61161ADRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
TPS61161ADRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2

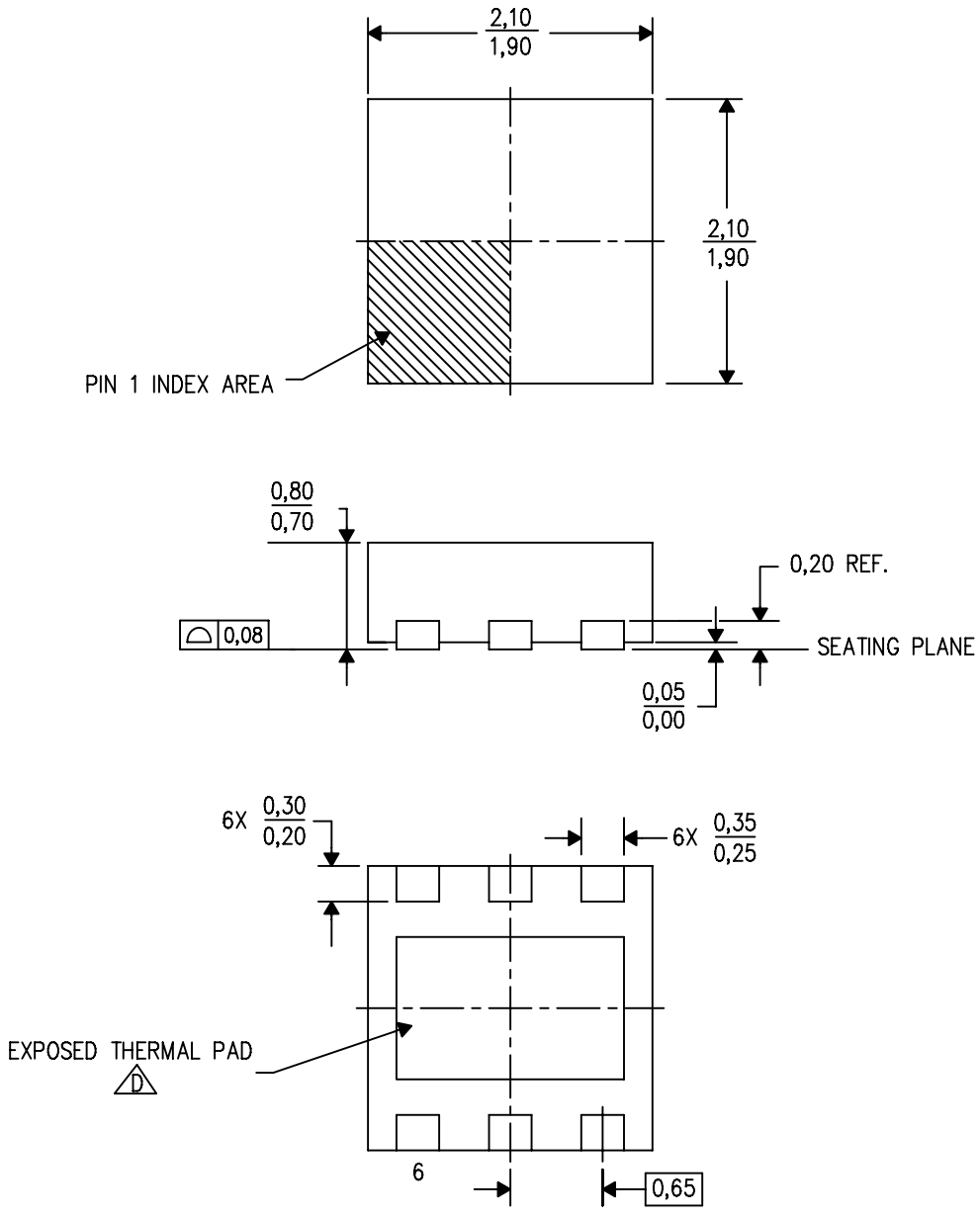
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61160ADRVR	SON	DRV	6	3000	346.0	346.0	29.0
TPS61160ADRVT	SON	DRV	6	250	190.5	212.7	31.8
TPS61161ADRVR	SON	DRV	6	3000	346.0	346.0	29.0
TPS61161ADRVT	SON	DRV	6	250	190.5	212.7	31.8

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



4206925/D 12/07

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

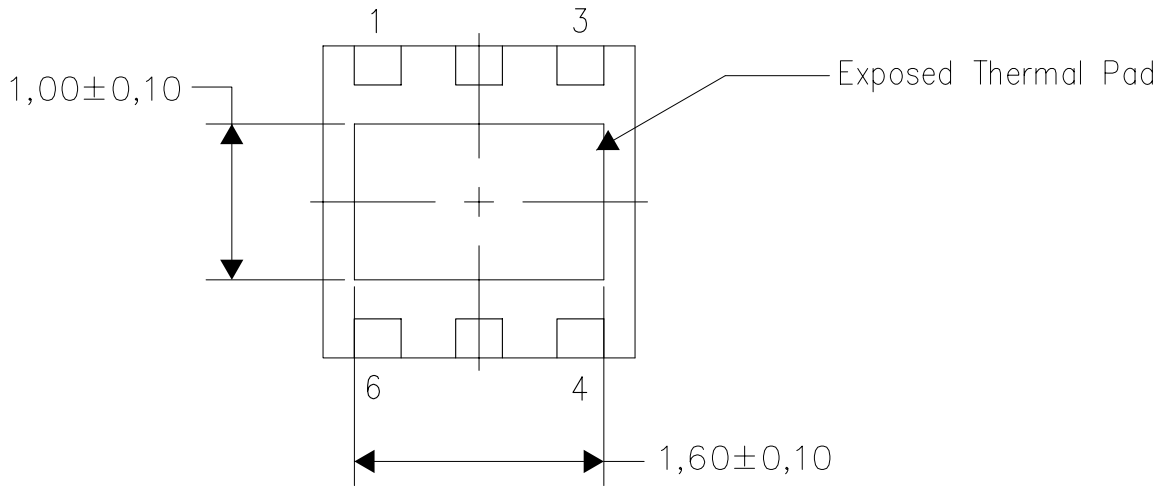
DRV (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

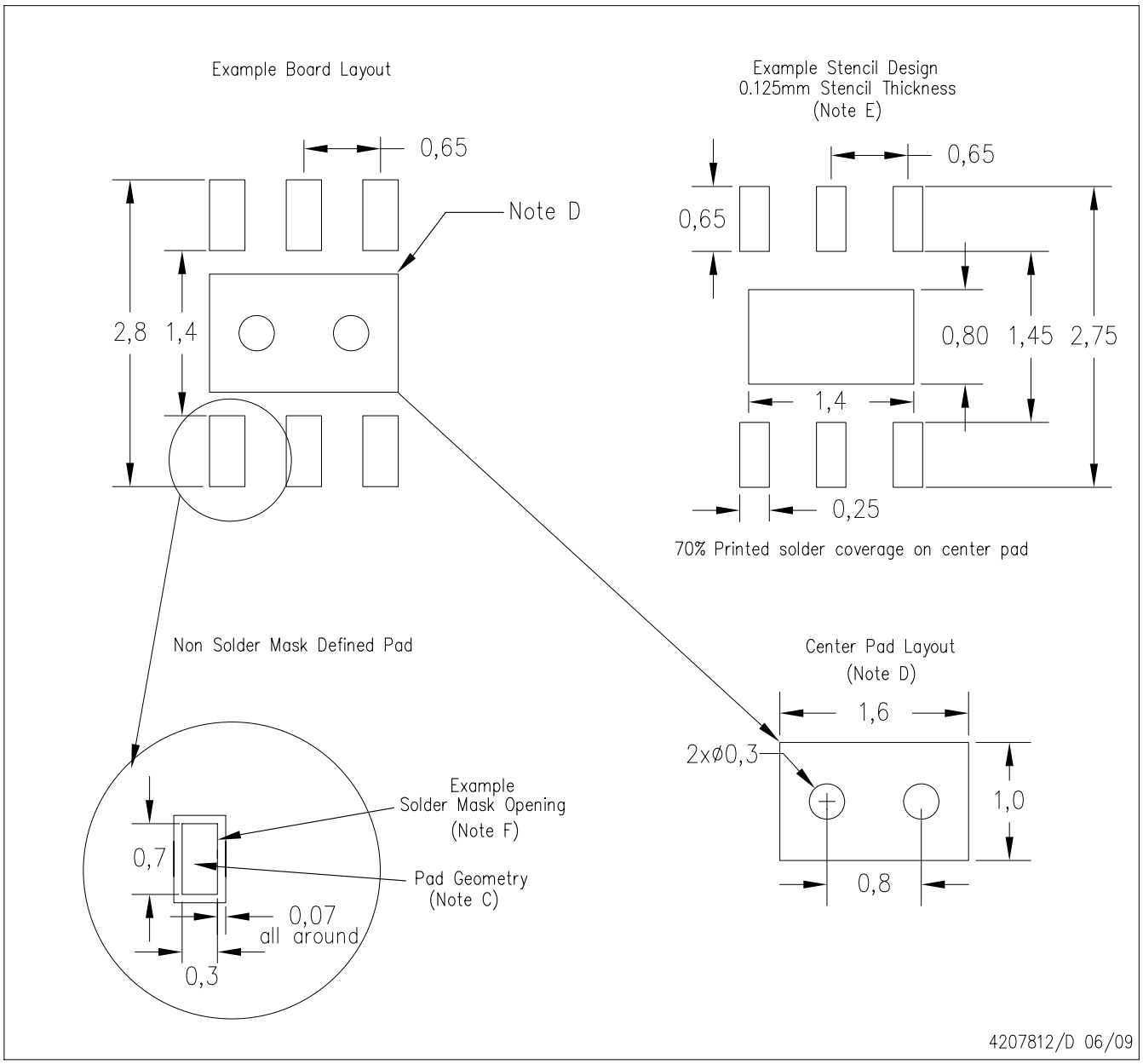


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRV (S–PWSON–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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