

# TPS56x219 4.5-V to 17-V Input, 2-A, 3-A Synchronous Step-Down Voltage Regulator in 8 Pin SOT-23

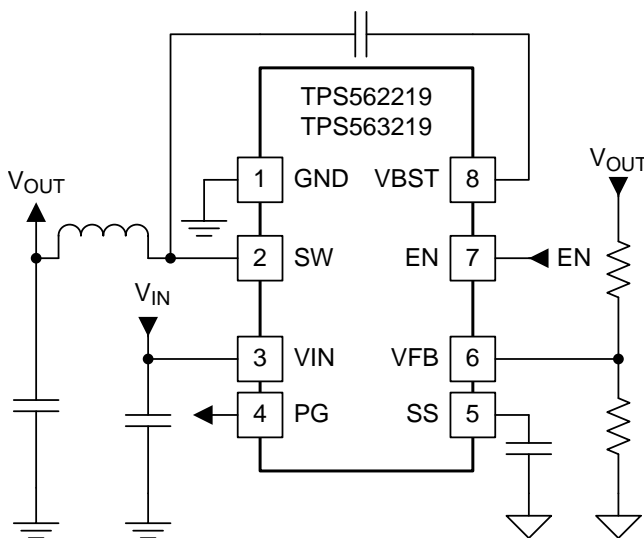
## 1 Features

- TPS562219: 2-A Converter With Integrated 133-m $\Omega$  and 80-m $\Omega$  FETs
- TPS563219: 3-A Converter With Integrated 68-m $\Omega$  and 39-m $\Omega$  FETs
- D-CAP2™ Mode Control with 650-kHz Switching Frequency
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650-kHz Switching Frequency
- Low Shutdown Current Less than 10  $\mu$ A
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle By Cycle Overcurrent Limit
- Hiccup-mode Under Voltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Adjustable Soft Start
- Power Good Output

## 2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

## 4 Simplified Schematic



## 3 Description

The TPS562219 and TPS563219 are simple, easy-to-use, 2-A, 3 -A synchronous step-down converters in 8 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2™ mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

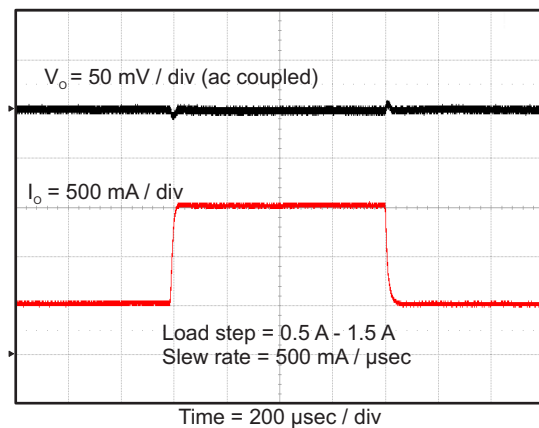
The devices always operate in continuous conduction mode, which reduces the output ripple voltage in light load compared to discontinuous conduction mode . The TPS562219 and TPS563219 are available in a 8-pin 1.6 × 2.9 (mm) SOT (DDF) package, and specified from –40°C to 85°C of ambient temperature.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS562219	DDF(8)	1.60 mm × 2.90 mm
TPS563219		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### TPS562219 Transient Response



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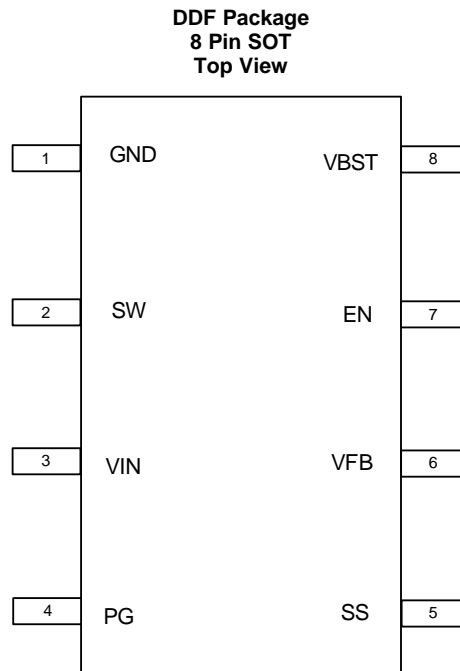
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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2015) to Revision A	Page
• Changed Thermal Metric data from 103.6, 47.0, 8.7, 7.4, 8.6 °C/W to 87.0, 41.6, 14.6, 4.7, 14.6 °C/W respectively, for TPS563219DDF .....	4
• Changed I <sub>VFB</sub> spec UNIT from "mA" to "µA" .....	5

## 6 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
PG	4	Power good open drain output
SS	5	Soft-start control. An external capacitor should be connected to GND.
VFB	6	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	7	Enable input control. Active high and must be pulled up to enable the device.
VBST	8	Supply input for the high-side NFET gate drive circuit. Connect 0.1 $\mu$ F capacitor between VBST and SW pins.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage range	VIN, EN	-0.3	19	V
	VBST	-0.3	25	V
	VBST (10 ns transient)	-0.3	27.5	V
	VBST (vs SW)	-0.3	6.5	V
	VFB, PG	-0.3	6.5	V
	SS	-0.3	5.5	V
	SW	-2	19	V
	SW (10 ns transient)	-3.5	21	V
Operating junction temperature, $T_J$		-40	150	$^{\circ}\text{C}$
Storage temperature, $T_{stg}$		-55	150	$^{\circ}\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{IN}$	Supply input voltage range	4.5	17	V	
$V_I$	Input voltage range	VBST	-0.1	23	V
		VBST (10 ns transient)	-0.1	26	
		VBST(vs SW)	-0.1	6	
		EN	-0.1	17	
		VFB, PG	-0.1	5.5	
		SS	-0.1	5	
		SW	-1.8	17	
		SW (10 ns transient)	-3.5	20	
$T_A$	Operating free-air temperature	-40	85	$^{\circ}\text{C}$	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS562219	TPS563219	UNIT
		DDF (8 PINS)		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.1	87.0	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	41.6	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	14.6	$^{\circ}\text{C}/\text{W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	8.6	4.7	$^{\circ}\text{C}/\text{W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	10.8	14.6	$^{\circ}\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{VIN}$	Operating – non-switching supply current	$V_{IN}$ current, $T_A = 25^\circ\text{C}$ , $EN = 5\text{ V}$ , $V_{FB} = 0.8\text{ V}$		650	900	$\mu\text{A}$
$I_{VNSDN}$	Shutdown supply current	$V_{IN}$ current, $T_A = 25^\circ\text{C}$ , $EN = 0\text{ V}$		3	10	$\mu\text{A}$
<b>LOGIC THRESHOLD</b>						
$V_{ENH}$	EN high-level input voltage	EN	1.6			V
$V_{ENL}$	EN low-level input voltage	EN			0.6	V
$R_{EN}$	EN pin resistance to GND	$V_{EN} = 12\text{ V}$	225	450	900	$\text{k}\Omega$
<b><math>V_{FB}</math> VOLTAGE AND DISCHARGE RESISTANCE</b>						
$V_{FBTH}$	$V_{FB}$ threshold voltage	$T_A = 25^\circ\text{C}$ , $V_O = 1.05\text{ V}$	757	765	773	mV
		$T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$ , $V_O = 1.05\text{ V}^{(1)}$	753		777	
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $V_O = 1.05\text{ V}^{(1)}$	751		779	
$I_{VFB}$	$V_{FB}$ input current	$V_{FB} = 0.8\text{ V}$ , $T_A = 25^\circ\text{C}$		0	$\pm 0.1$	$\mu\text{A}$
<b>MOSFET</b>						
$R_{DS(on)h}$	High side switch resistance	$T_A = 25^\circ\text{C}$ , $V_{BST} - SW = 5.5\text{ V}$ , TPS562219		133		m $\Omega$
		$T_A = 25^\circ\text{C}$ , $V_{BST} - SW = 5.5\text{ V}$ , TPS563219		68		
$R_{DS(on)l}$	Low side switch resistance	$T_A = 25^\circ\text{C}$ , TPS562219		80		m $\Omega$
		$T_A = 25^\circ\text{C}$ , TPS563219		39		
<b>CURRENT LIMIT</b>						
$I_{ocL}$	Current limit <sup>(1)</sup>	DC current, $V_{OUT} = 1.05\text{ V}$ , $L1 = 2.2\text{ }\mu\text{H}$ , TPS562219	2.5	3.2	4.3	A
		DC current, $V_{OUT} = 1.05\text{ V}$ , $L1 = 1.5\text{ }\mu\text{H}$ , TPS563219	3.5	4.2	5.3	
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold <sup>(1)</sup>	Shutdown temperature		155		$^\circ\text{C}$
		Hysteresis		35		
<b>SOFT START</b>						
$I_{SS}$	SS charge current	$V_{SS} = 0.5\text{ V}$	4.2	6	7.8	$\mu\text{s}$
	SS discharge current	$V_{SS} = 0.5\text{ V}$ , $EN = L$	0.75	1.3		mA
<b>POWER GOOD</b>						
$V_{THPG}$	PG threshold	VFB rising (Good)	85%	90%	95%	
		VFB falling (Fault)		85%		
IPG	PG sink current	$PG = 0.5\text{ V}$	0.5	1		mA
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$V_{OVP}$	Output OVP threshold	OVP Detect		125% $\times$ $V_{fbth}$		
$V_{UVP}$	Output UVP threshold	Hiccup detect		65% $\times$ $V_{fbth}$		
$T_{HiccupOn}$	Hiccup Power On Time			1		ms
$T_{HiccupOff}$	Hiccup Power Off Time			7		
<b>UVLO</b>						
UVLO	UVLO threshold	Wake up $V_{IN}$ voltage	3.45	3.75	4.05	V
		Hysteresis $V_{IN}$ voltage	0.13	0.32	0.55	

(1) Not production tested.

## 7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
<b>ON-TIME TIMER CONTROL</b>						
$t_{ON}$	On time	$V_{IN} = 12\text{ V}, V_O = 1.05\text{ V}$		150		ns
$t_{OFF(MIN)}$	Minimum off time	$T_A = 25^\circ\text{C}, V_{FB} = 0.5\text{ V}$		260	310	ns

### 7.7 Typical Characteristics: TPS562219

$V_{IN} = 12V$  (unless otherwise noted)

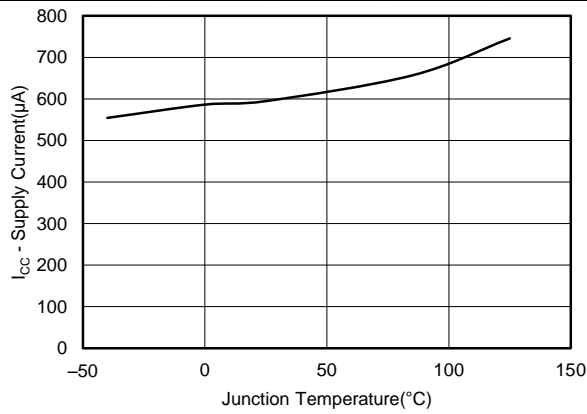


Figure 1. Supply Current vs Junction Temperature

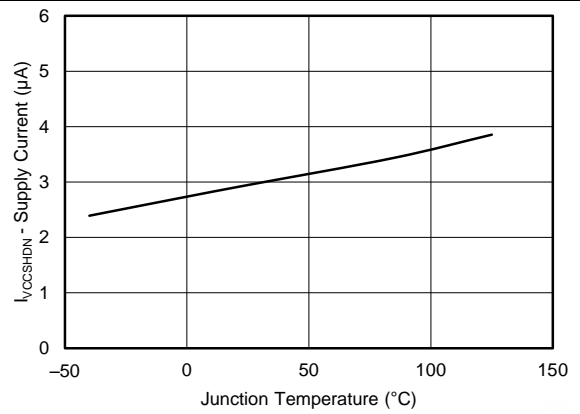


Figure 2. VIN Shutdown Current vs Junction Temperature

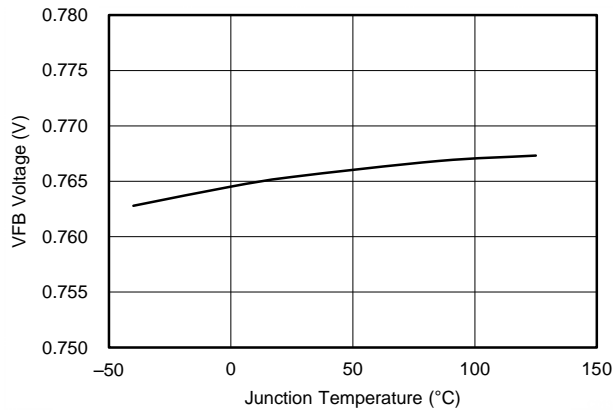


Figure 3. VFB Voltage vs Junction Temperature

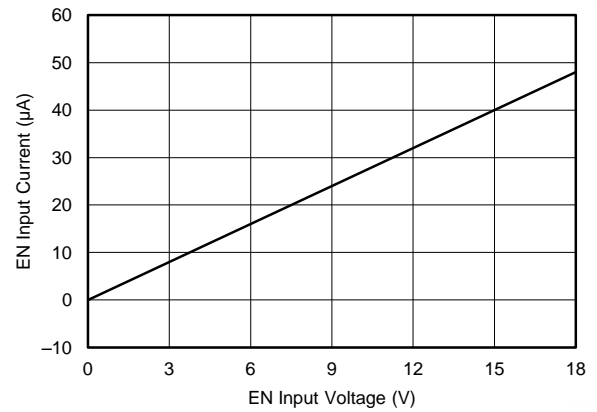


Figure 4. EN Current vs EN Voltage

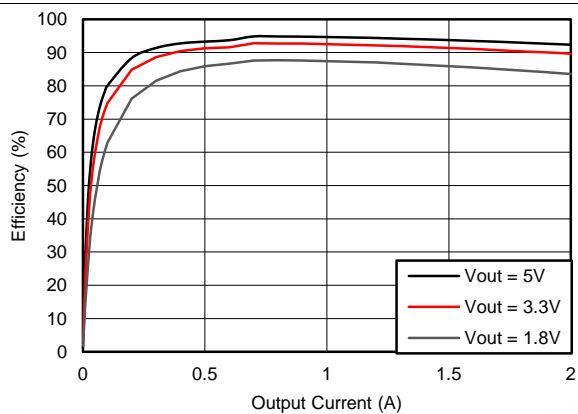


Figure 5. Efficiency vs Output Current

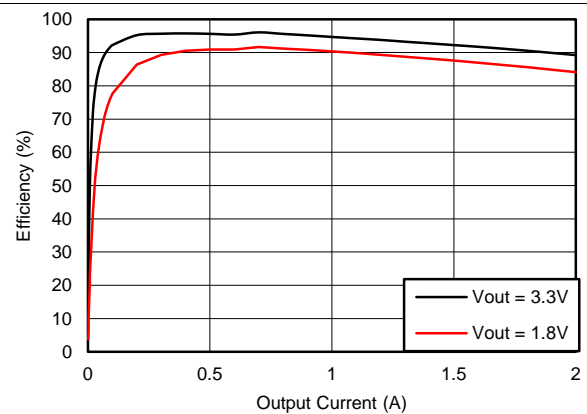
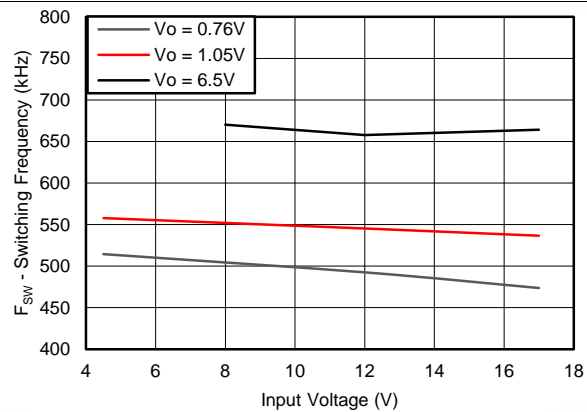
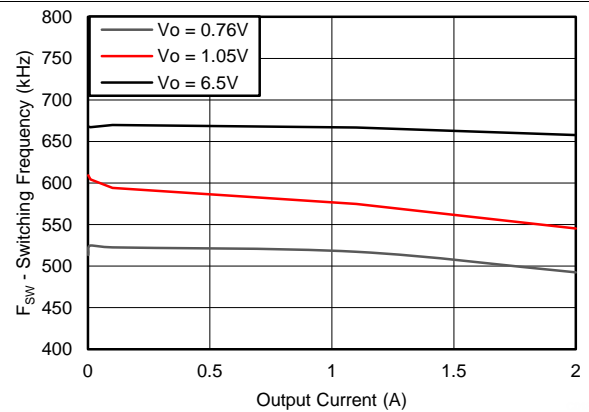


Figure 6. Efficiency vs Output Current ( $V_i = 5V$ )

**Typical Characteristics: TPS562219 (continued)**
 $V_{IN} = 12V$  (unless otherwise noted)

**Figure 7. Switching Frequency vs Input Voltage**

**Figure 8. Switching Frequency vs Output Current**



### 7.8 Typical Characteristics: TPS563219

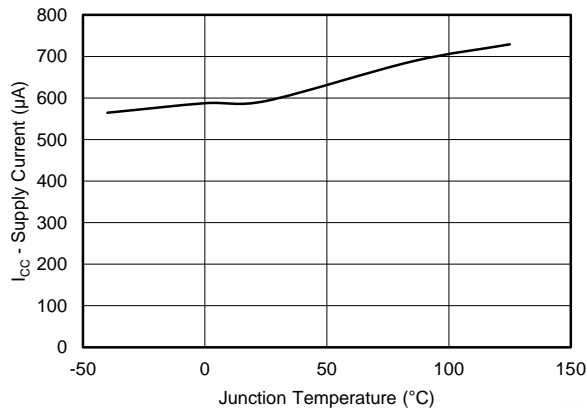


Figure 9. Supply Current vs Junction Temperature

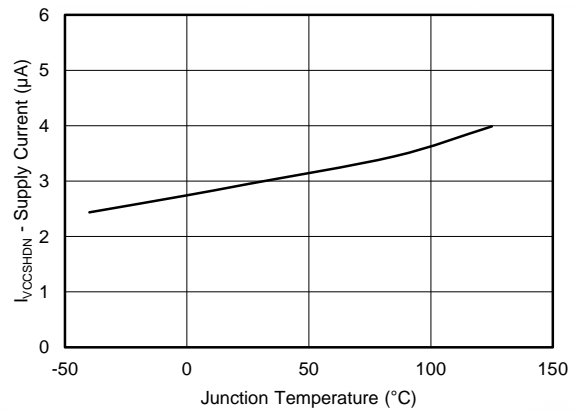


Figure 10. VIN Shutdown Current vs Junction Temperature

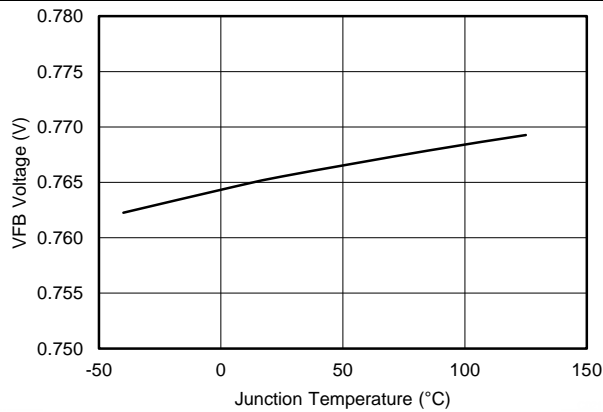


Figure 11. VFB Voltage vs Junction Temperature

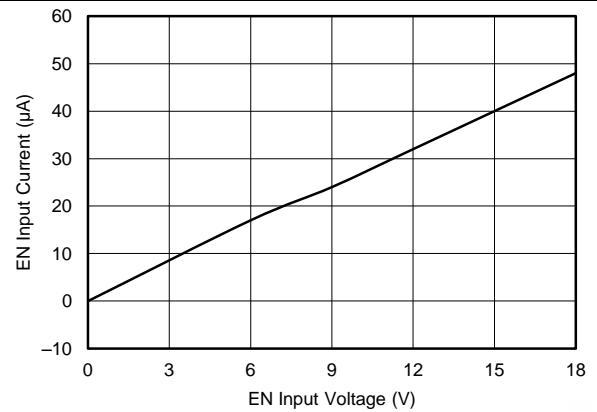


Figure 12. EN Current vs EN Voltage

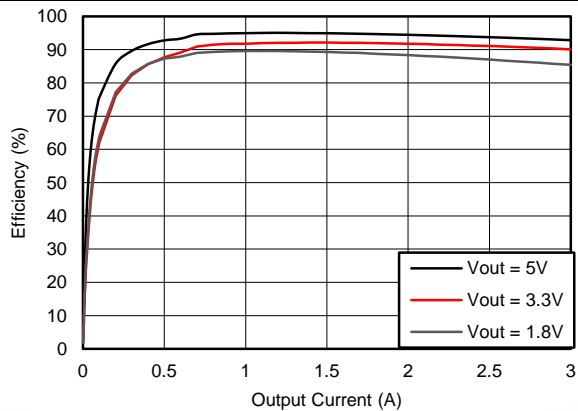


Figure 13. Efficiency vs Output Current

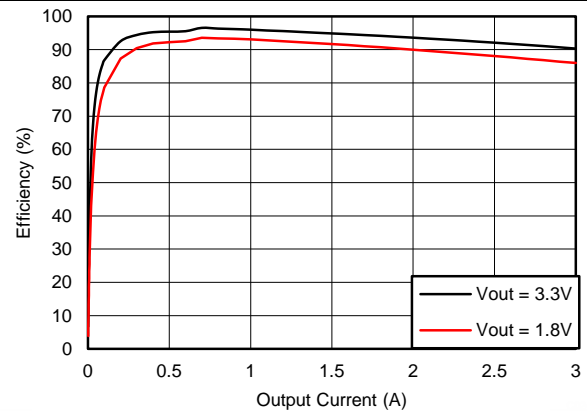
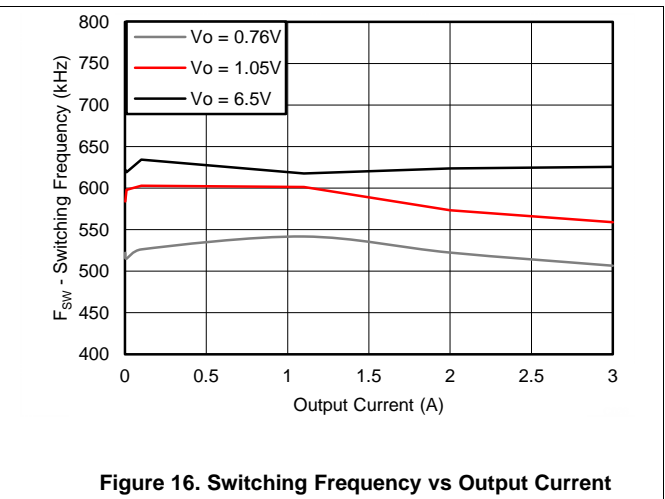
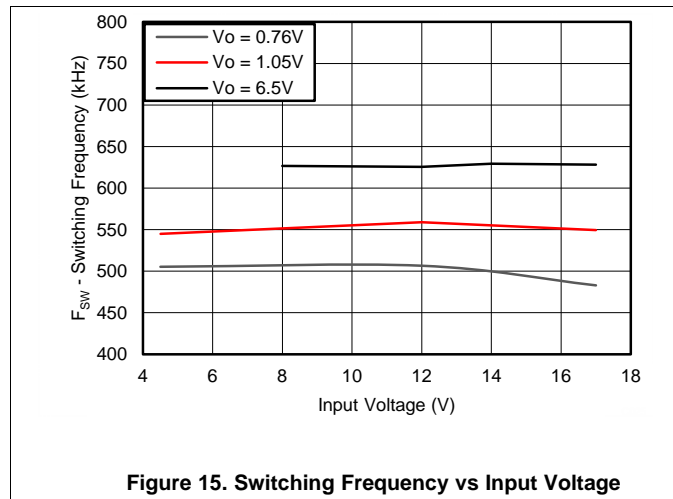


Figure 14. Efficiency vs Output Current (V<sub>I</sub> = 5V)

**Typical Characteristics: TPS563219 (continued)**

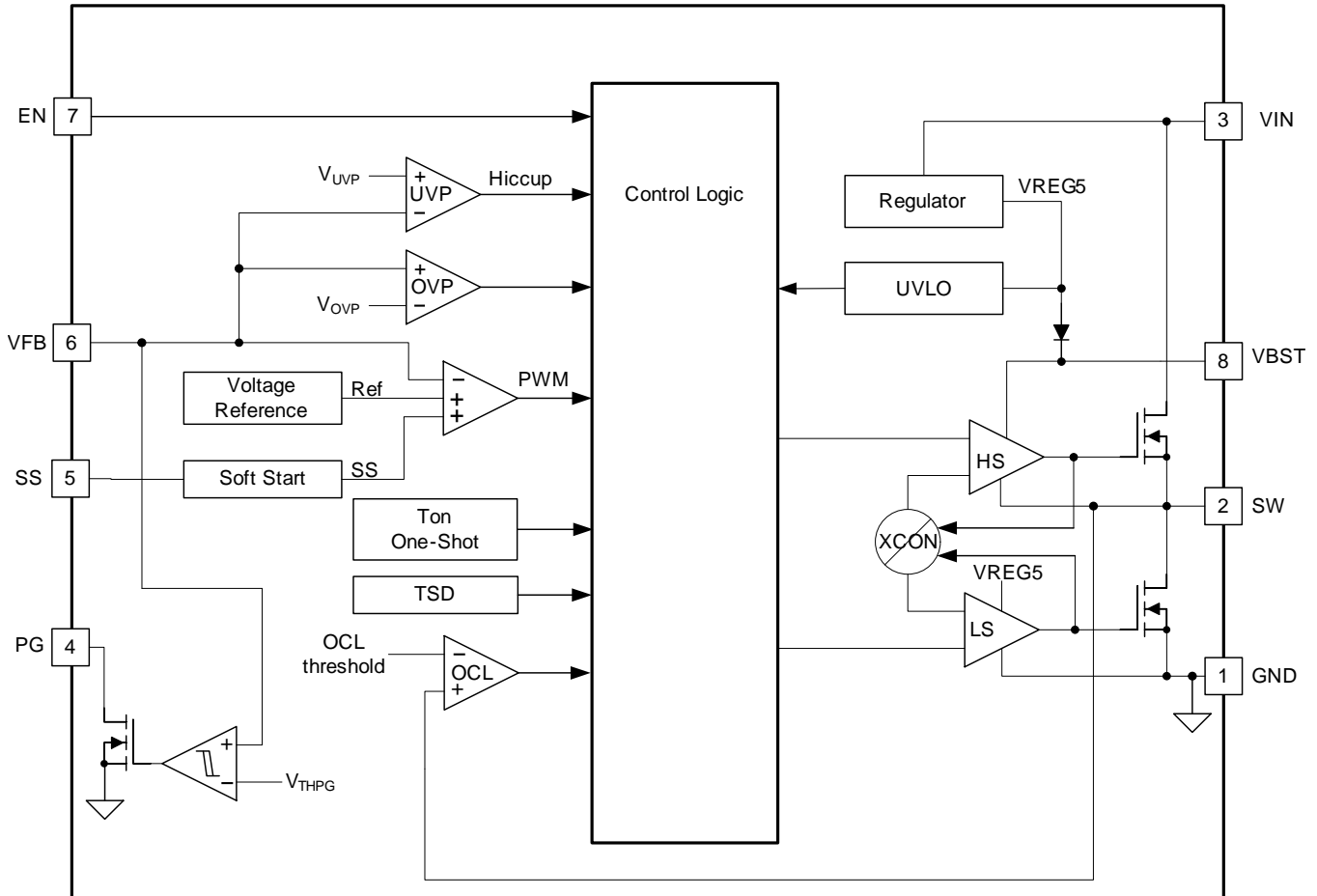


## 8 Detailed Description

### 8.1 Overview

The TPS562219 and TPS563219 are 2-A, 3-A synchronous step-down converters. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562219 and TPS563219 are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage,  $V_{IN}$ , and inversely proportional to the output voltage,  $V_O$ , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

## Feature Description (continued)

### 8.3.2 Soft Start and Pre-Biased Soft Start

The TPS562219 and TPS563219 have adjustable soft-start. When the EN pin becomes high, the SS charge current ( $I_{SS}$ ) begins charging the capacitor which is connected from the SS pin to GND ( $C_{SS}$ ). Smooth control of the output voltage is maintained during start up. The equation for the soft start time,  $T_{SS}$  is shown in [Equation 1](#).

$$T_{SS}(\text{ms}) = \frac{C_{SS} \times V_{FBTH} \times 1.1}{I_{SS}} \quad (1)$$

where  $V_{FBTH}$  is 0.765V and  $I_{SS}$  is 6 $\mu$ A.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage  $V_{FB}$ . This scheme ensures that the converters ramp up smoothly into regulation point.

### 8.3.3 Power Good

The power good output, PG is an open drain output. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

### 8.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{in}$ ,  $V_{out}$ , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{out}$ . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the  $V_{FB}$  voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14 $\mu$ s) and re-start after the hiccup time.

When the over current condition is removed, the output voltage returns to the regulated value.

### 8.3.5 Over Voltage Protection

TPS562219 and TPS563219 detect over voltage condition by monitoring the feedback voltage ( $V_{FB}$ ). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the high-side MOSFET turns off. This function is non-latch operation.

### 8.3.6 UVLO Protection

Under voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

### 8.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

## **8.4 Device Functional Modes**

### **8.4.1 Normal Operation**

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562219 and TPS563219 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562219 and TPS563219 operate at a quasi-fixed frequency of 650 kHz.

### **8.4.2 Forced CCM Operation**

When the TPS562209 and TPS563209 are in the normal CCM operating mode and the switch current falls below 0 A, the TPS562219 and TPS563219 begin operating in forced CCM.

### **8.4.3 Standby Operation**

When the TPS562219 and TPS563219 are operating in either normal CCM or forced CCM, they may be placed in standby by asserting the EN pin low.

## 9 Application and Implementation

### NOTE

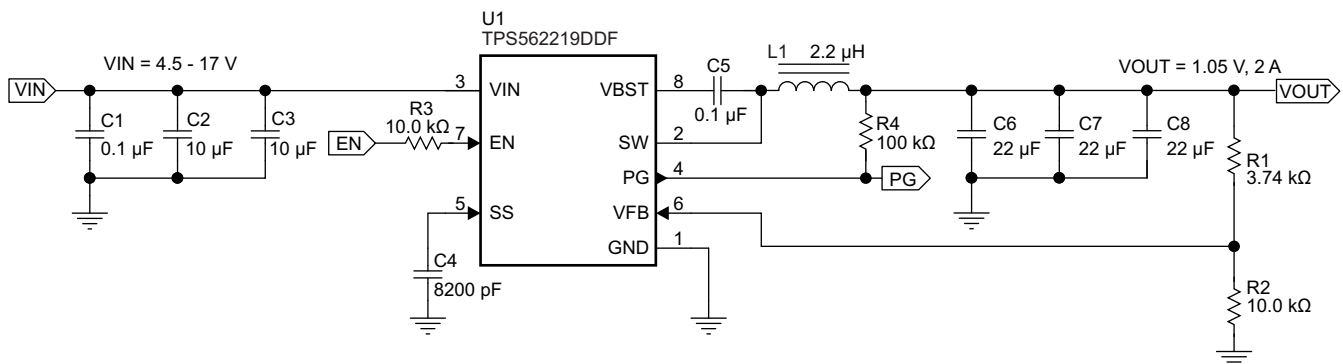
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS562219 and TPS563219 are typically used as step down converters, which convert a voltage from 4.5V - 17V to a lower voltage. Webench software is available to aid in the design and analysis of circuits.

### 9.2 Typical Application

#### 9.2.1 TPS562219 4.5-V to 17-V Input, 1.05-V output Converter



**Figure 17. TPS562219 1.05V/2A Reference Design**

#### 9.2.1.1 Design Requirements

For this design example, use the parameters shown in [Table 1](#).

**Table 1. Design Parameters**

PARAMETER	VALUES
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVpp

#### 9.2.1.2 Detailed Design Procedure

##### 9.2.1.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate  $V_{OUT}$ .

To improve efficiency at light loads consider using larger value resistors, too high of resistance are more susceptible to noise and voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left( 1 + \frac{R1}{R2} \right) \quad (2)$$

##### 9.2.1.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

**Table 2. TPS562219 Recommended Component Values**

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1(μH)			C6 + C7 + C8(μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75	10.0	3.3	4.7	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for  $f_{SW}$ . Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562219 and TPS563219 are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

### 9.2.1.2.3 Input Capacitor Selection

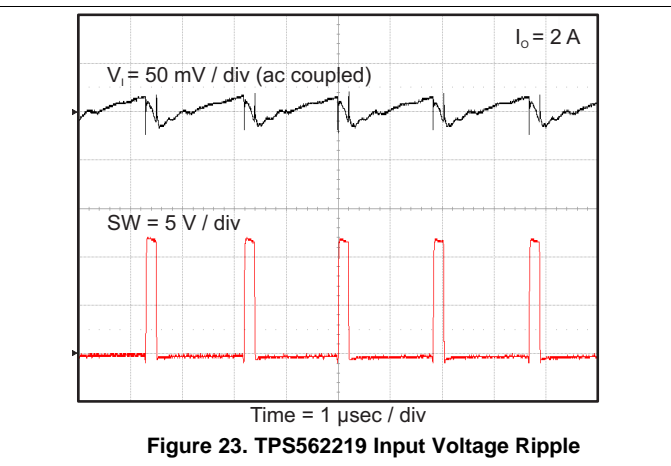
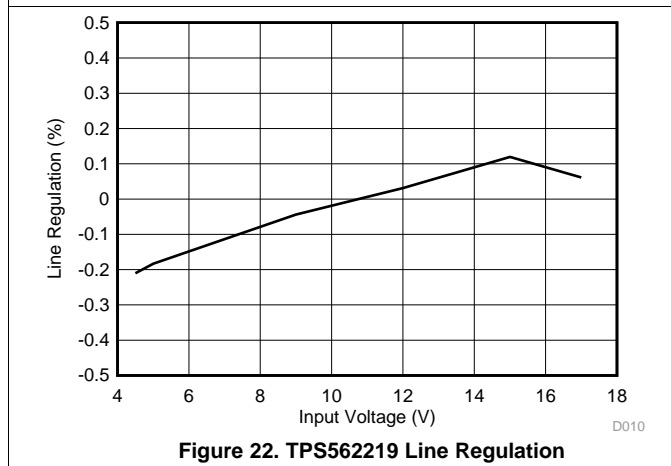
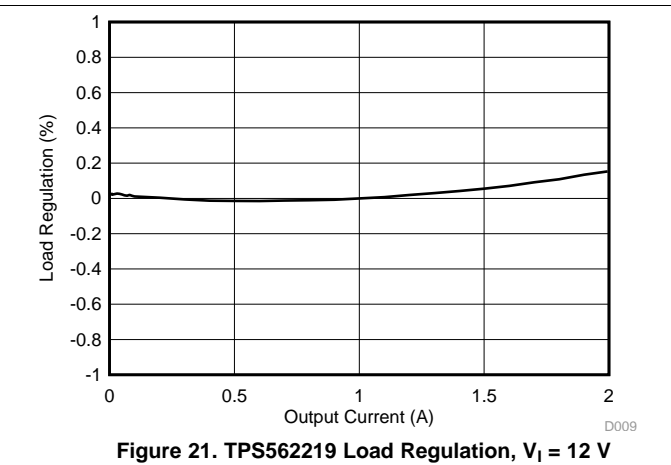
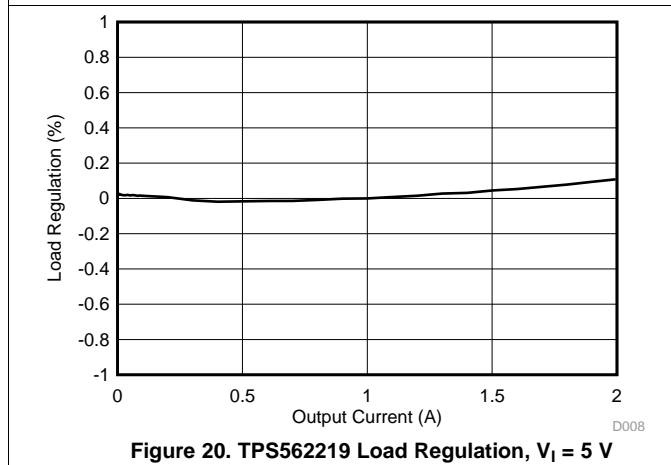
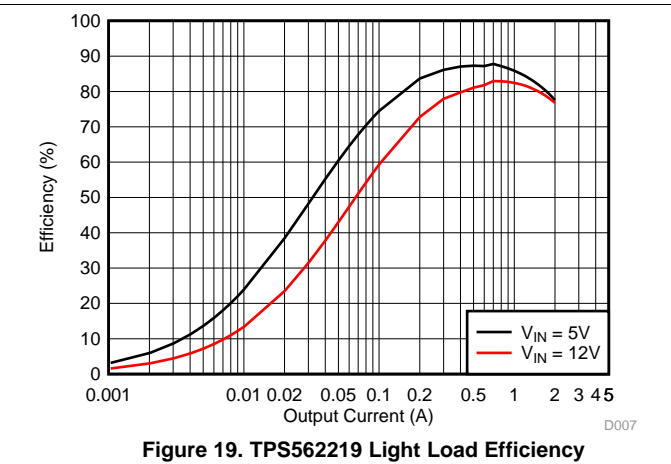
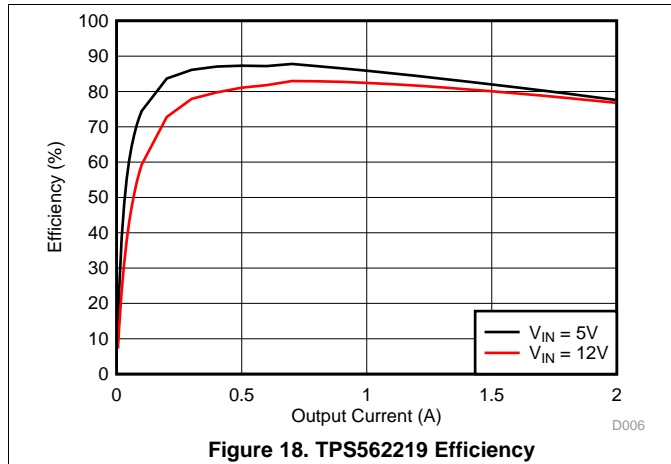
The TPS562219 and TPS563219 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

**9.2.1.2.4 Bootstrap capacitor Selection**

A 0.1µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

**9.2.1.3 Application Curves**

The following application curves were generated using the application circuit of [Figure 17](#).





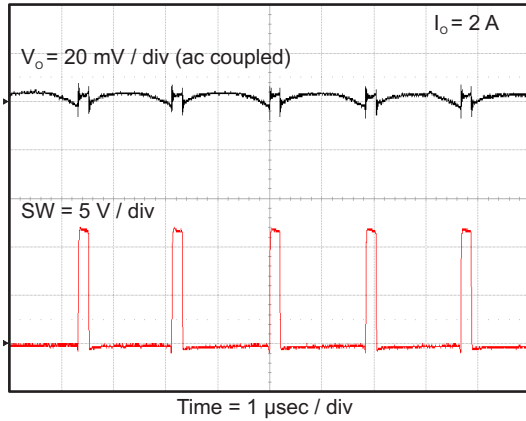


Figure 24. TPS562219 Output Voltage Ripple

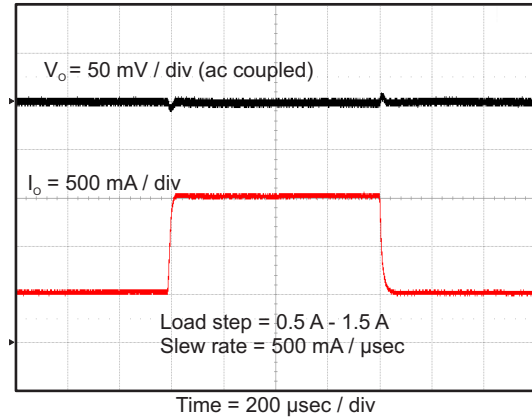


Figure 25. TPS562219 Transient Response

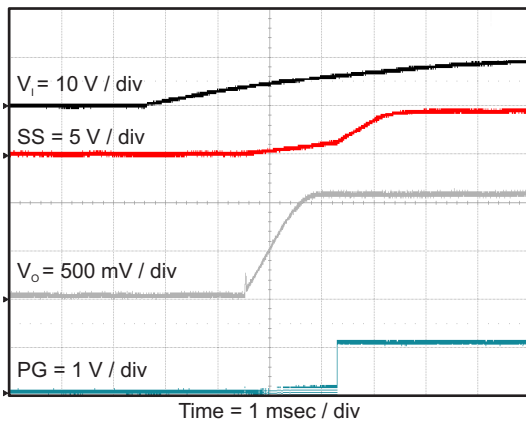


Figure 26. TPS562219 Start Up Relative To  $V_I$

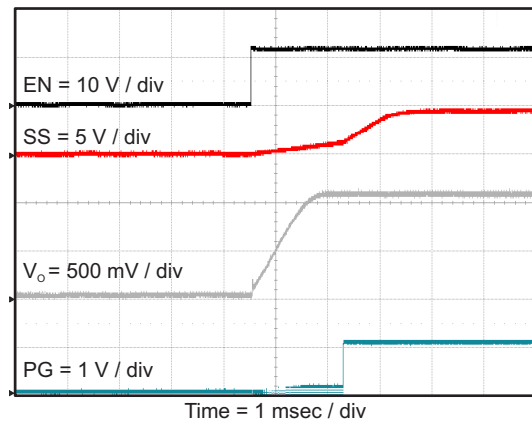


Figure 27. TPS562219 Start Up Relative To EN

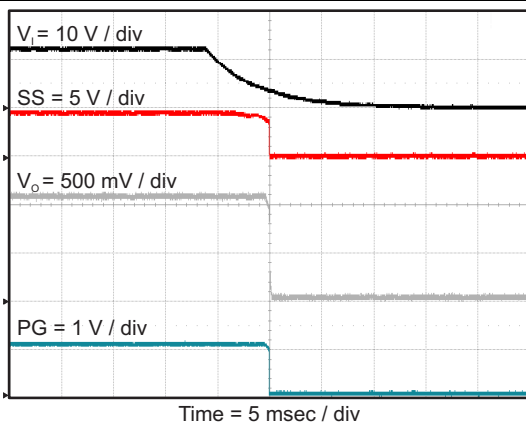


Figure 28. TPS562219 Shut Down Relative To  $V_I$

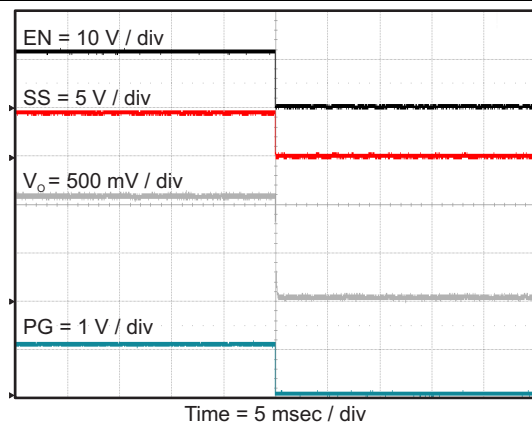


Figure 29. TPS562219 Shut Down Relative To EN

### 9.2.2 TPS563219 4.5-V To 17-V Input, 1.05-V Output Converter

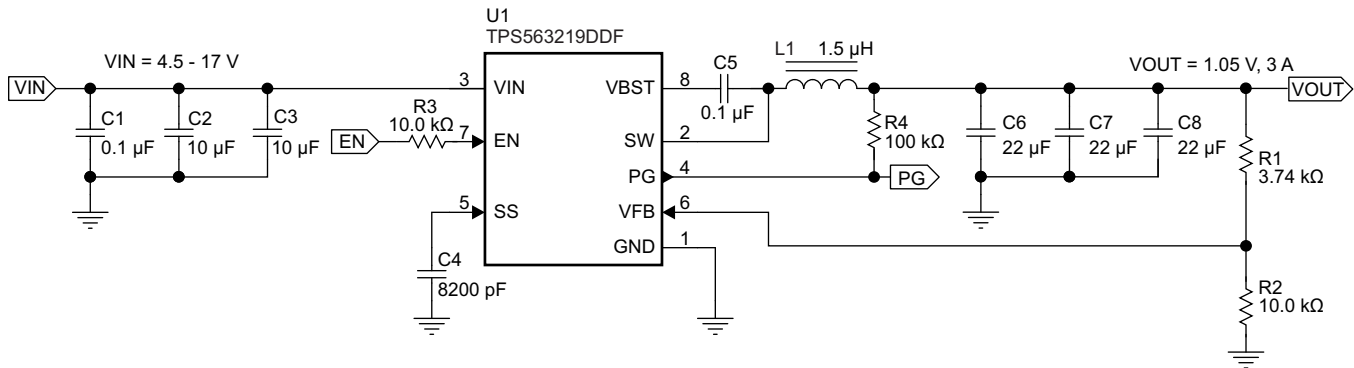


Figure 30. TPS563219 1.05V/3A Reference Design

#### 9.2.2.1 Design Requirements

For this design example, use the parameters shown in [Table 3](#).

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17V
Output voltage	1.05V
Output current	3A
Output voltage ripple	20mVpp

#### 9.2.2.2 Detailed Design Procedures

The detailed design procedure for TPS563219 is the same as for TPS562200 except for inductor selection.

##### 9.2.2.2.1 Output Filter Selection

Table 4. TPS563219 Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (μH)			C6 + C7 + C8 (μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 8](#), [Equation 9](#) and [Equation 10](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for  $f_{sw}$ .

Use 650 kHz for  $f_{sw}$ . Make sure the chosen inductor is rated for the peak current of [Equation 9](#) and the RMS current of [Equation 10](#).

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{8}$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \tag{9}$$

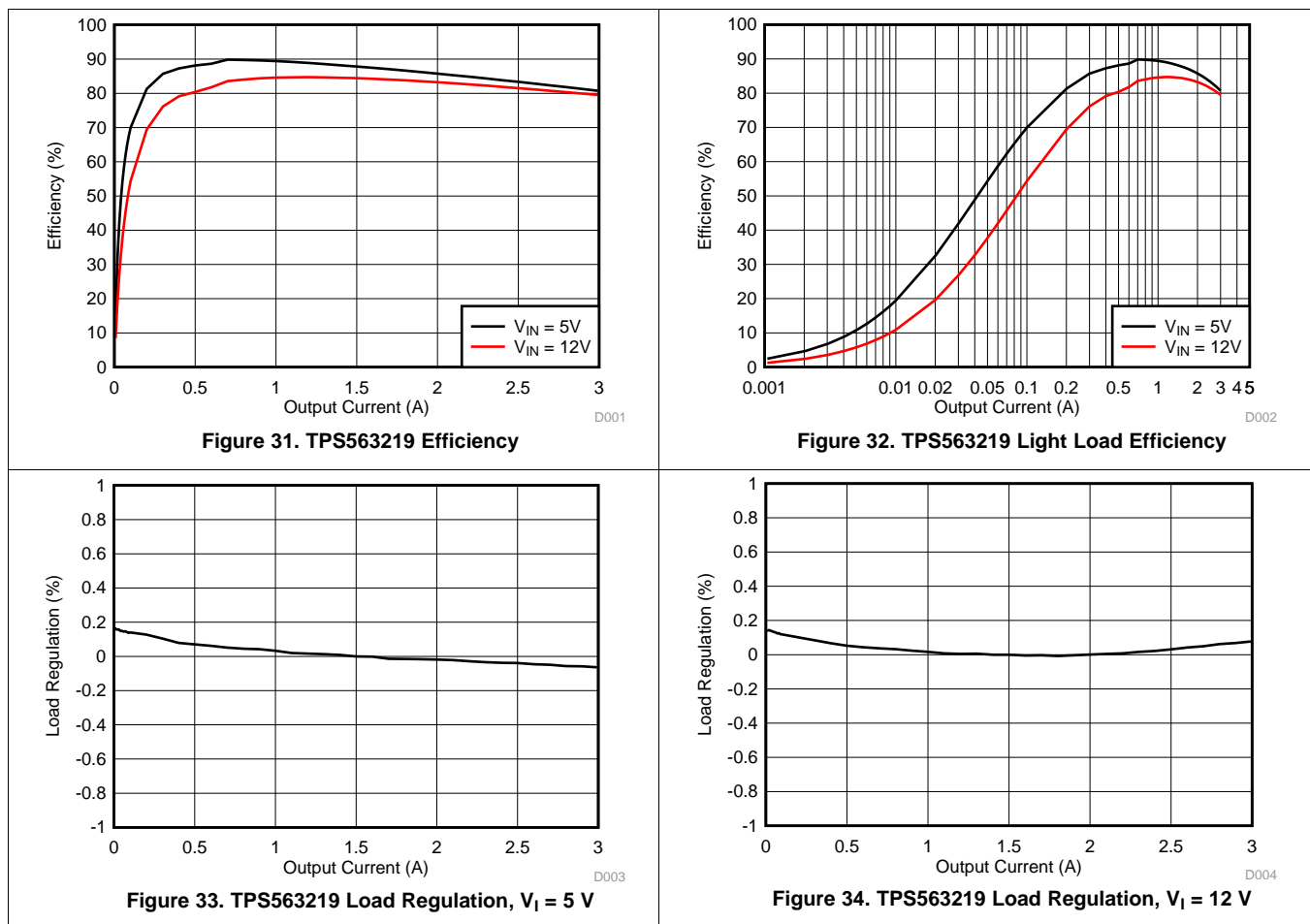
$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \tag{10}$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3-A and an RMS current rating of 4.9-A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use Equation 6 to determine the required RMS current rating for the output capacitor. For this design, three TDK C3216X5R0J226M 22 μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.292 A and each output capacitor is rated for 4 A.

### 9.2.2.3 Application Curves

The following application curves were generated using the application circuit of Figure 30.



The following application curves were generated using the application circuit of Figure 30.

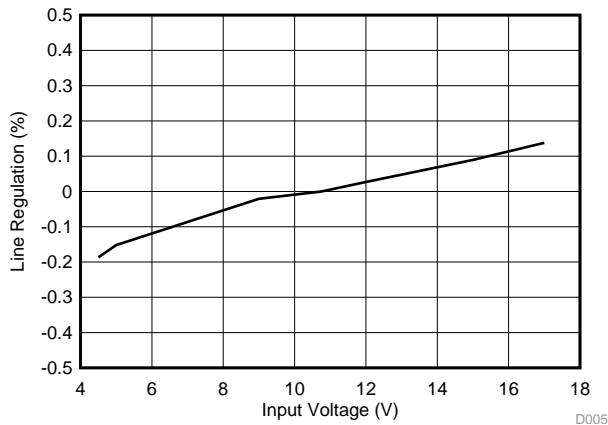


Figure 35. TPS563219 Line Regulation

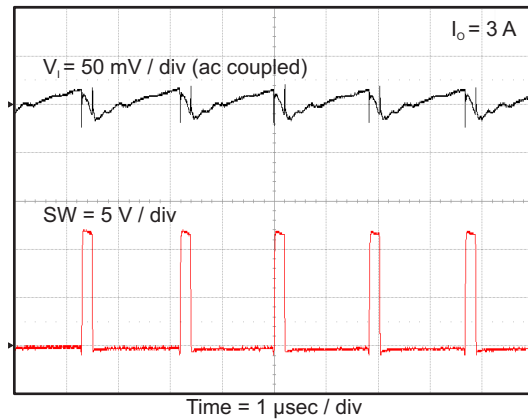


Figure 36. TPS563219 Input Voltage Ripple

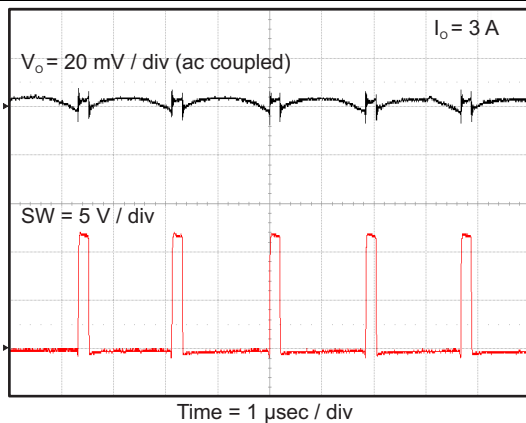


Figure 37. TPS563219 Output Voltage Ripple

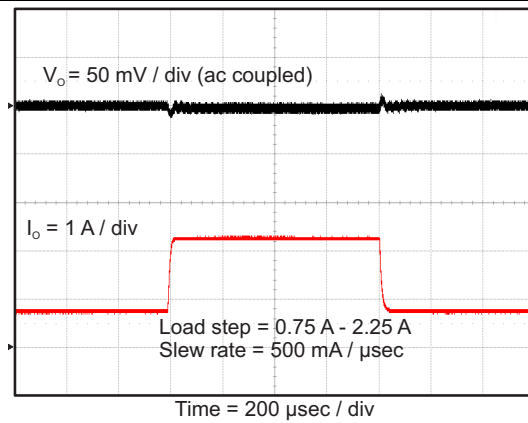


Figure 38. TPS563219 Transient Response

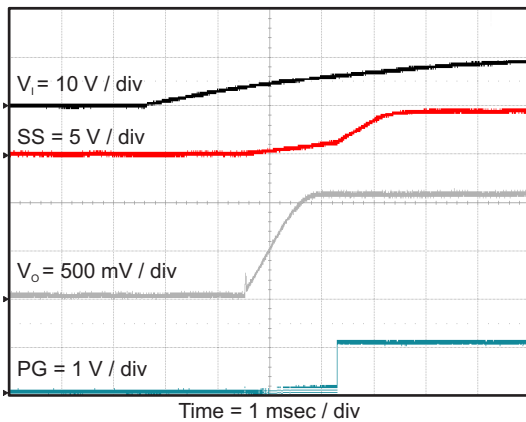


Figure 39. TPS563219 Start Up Relative To V<sub>1</sub>

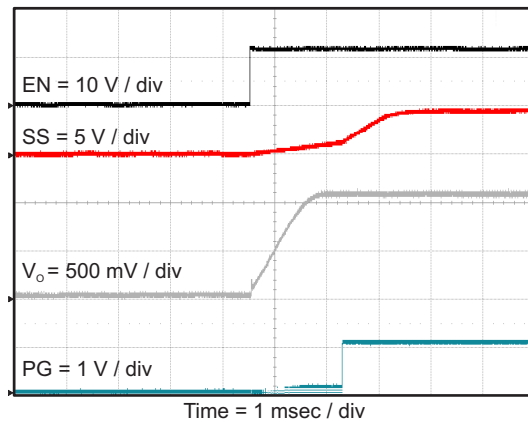
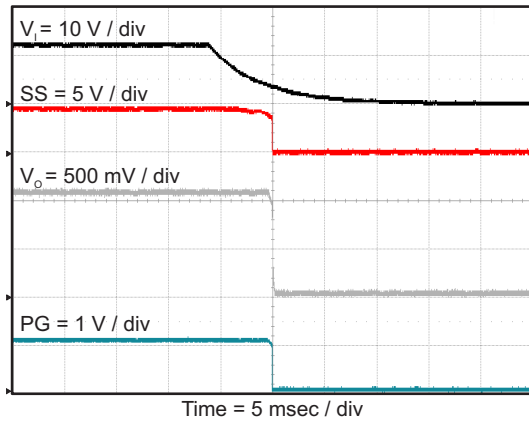
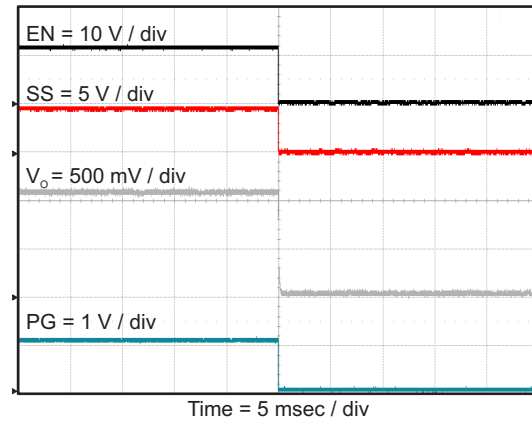


Figure 40. TPS563219 Start Up Relative To EN

The following application curves were generated using the application circuit of [Figure 30](#).



**Figure 41. TPS563219 Shut Down Relative To  $V_I$**



**Figure 42. TPS563219 Shut Down Relative To EN**

## 10 Power Supply Recommendations

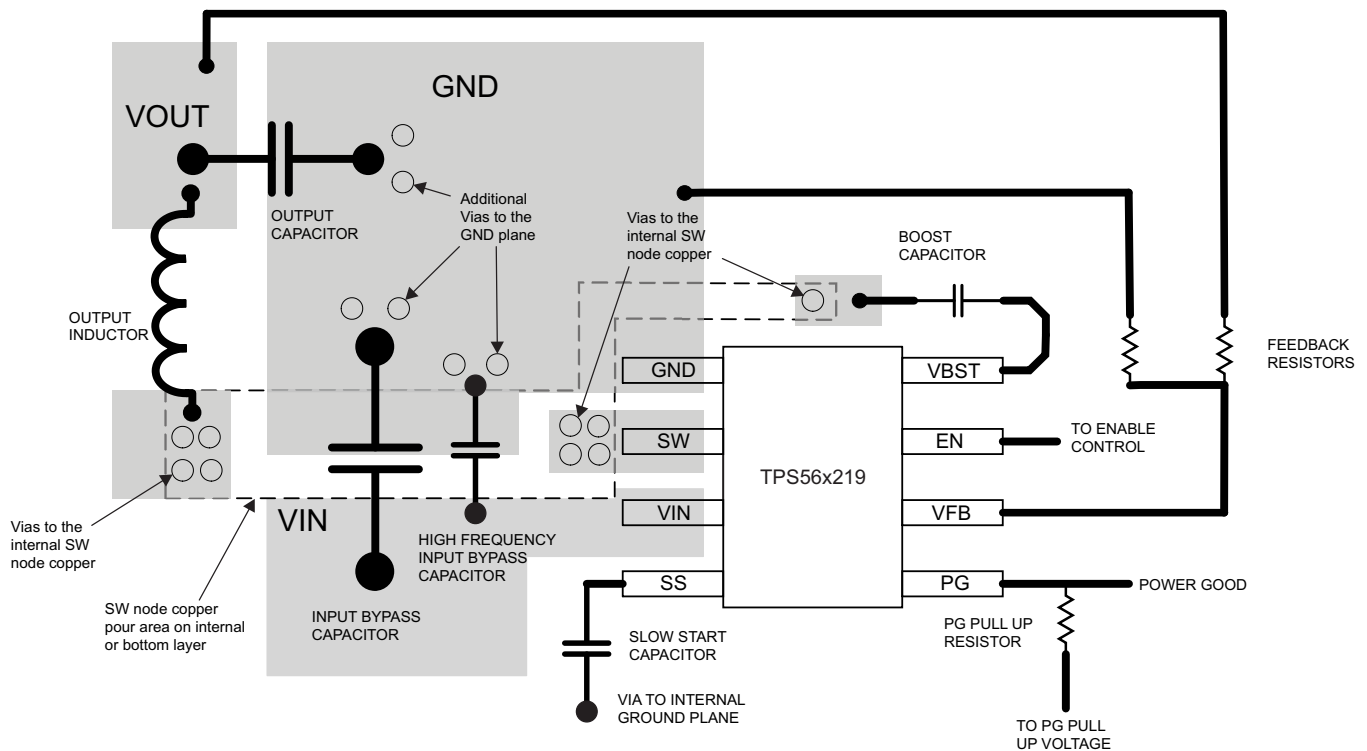
The TPS562209 and TPS563209 are designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is  $V_O / 0.65$ .

## 11 Layout

### 11.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS562219	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS563219	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Trademarks

D-CAP2 is a trademark of Texas Instruments.

Blu-ray Disc is a trademark of Blu-ray Disc Association.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562219DDFR	ACTIVE	SOT	DDF	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2219	<a href="#">Samples</a>
TPS562219DDFT	ACTIVE	SOT	DDF	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2219	<a href="#">Samples</a>
TPS563219DDFR	ACTIVE	SOT	DDF	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	3219	<a href="#">Samples</a>
TPS563219DDFT	ACTIVE	SOT	DDF	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	3219	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

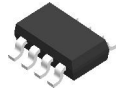
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS562219DDFR	SOT	DDF	8	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS562219DDFT	SOT	DDF	8	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS563219DDFR	SOT	DDF	8	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS563219DDFT	SOT	DDF	8	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS562219DDFR	SOT	DDF	8	3000	184.0	184.0	19.0
TPS562219DDFT	SOT	DDF	8	250	184.0	184.0	19.0
TPS563219DDFR	SOT	DDF	8	3000	184.0	184.0	19.0
TPS563219DDFT	SOT	DDF	8	250	184.0	184.0	19.0

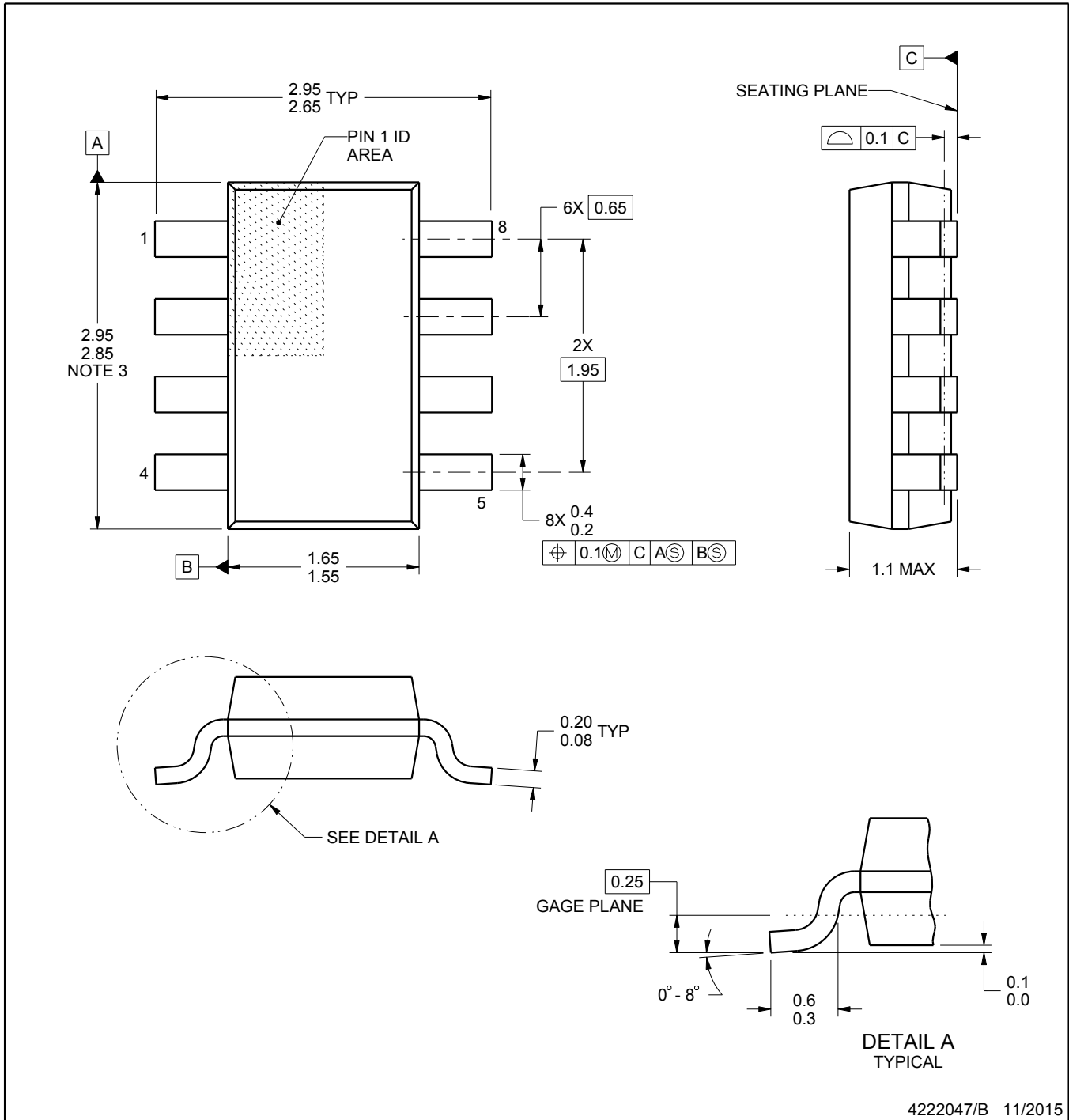
# DDF0008A



# PACKAGE OUTLINE

## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/B 11/2015

**NOTES:**

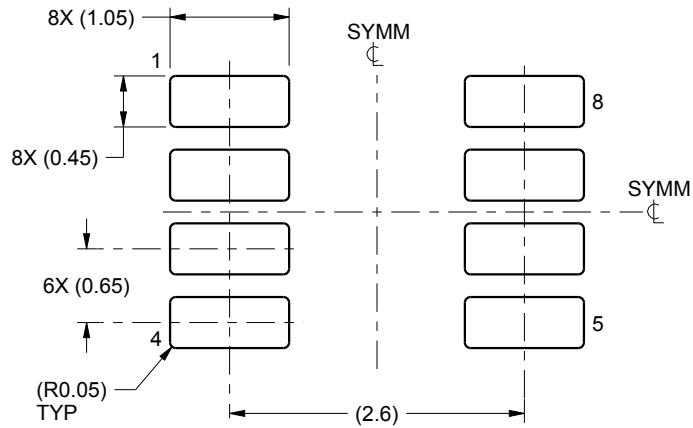
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

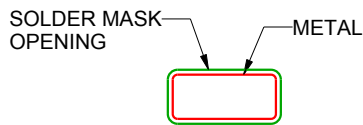
DDF0008A

SOT-23 - 1.1 mm max height

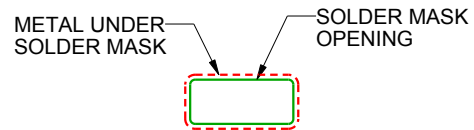
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

## SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

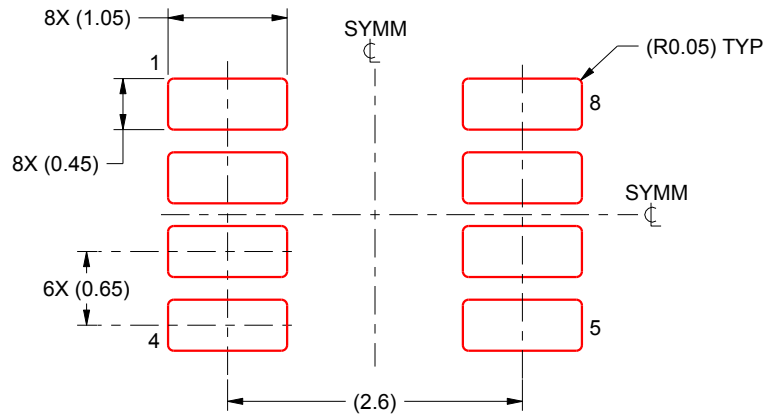
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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