TPS54200, TPS54201 4.5-V to 28-V Input Voltage, 1.5-A Output Current, Synchronous Buck WLED Driver

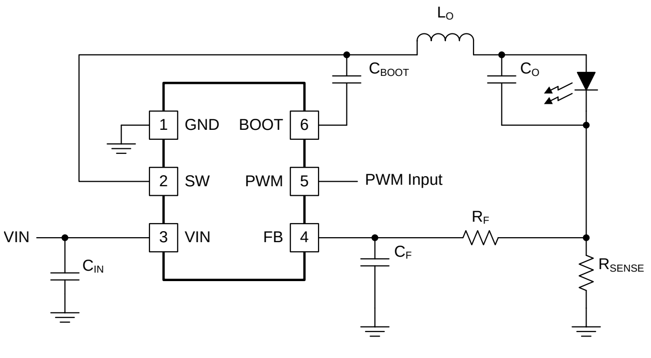
1 Features

- 4.5-V to 28-V Wide Input Range
- Integrated 150-mΩ and 70-mΩ MOSFETs for 1.5-A, Continuous Output Current
- Low, 2-μA Shutdown Current
- Fixed 600-kHz Frequency
- Peak Current Mode with Internal Compensation
- 200-mV and 100-mV Sense Voltage During Analog and PWM Dimming Mode
- Precision Analog Dimming by PWM Input
- LED Open and Short Protection
- Sense Resistor Open and Short Protection
- Shutdown-and-latch Mode Protection (TPS54200)
- Hiccup Mode Protection (TPS54201)
- Thermal Shutdown
- SOT23-6 Package

2 Applications

- General Purpose LED Driver
- Architecture Lighting
- Industrial and Commercial Illumination

Simplified Schematic



3 Description

The TPS54200 and TPS54201 are 1.5-A synchronous buck WLED drivers with 28-V maximum input voltage. Current mode operation provides fast transient response and eases loop stabilization.

By integrating the MOSFETs and employing the SOT23-6 package, TPS54200 and TPS54201 provide high-power density and only require a small footprint on the PCB.

The TPS54200 and TPS54201 implement analog dimming by changing the internal reference voltage proportional to the duty cycle of the PWM signal input in analog dimming mode. This device also supports PWM dimming mode, in which the internal reference voltage will be halved to 100 mV for higher efficiency.

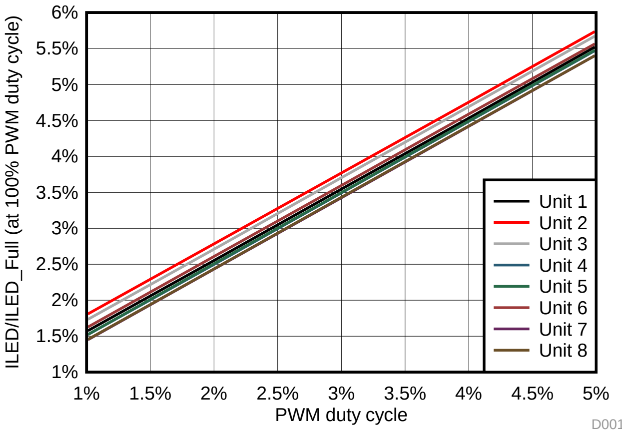
Cycle-by-cycle current limit in high-side MOSFET protects the converter in an over-load condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. There is a low-side MOSFET sinking current limit to prevent excessive reverse current. For safety and protection the TPS54200 and TPS54201 include LED open and short protection, sense resistor open and short protection, and device thermal protection. TPS54200 implements shutdown-and-latch mode protection, while TPS54201 adopts hiccup mode protection.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54200	SOT23(6)	1.6 mm x 2.9 mm
TPS54201	SOT23(6)	1.6 mm x 2.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Excellent Deep Dimming in ADIM



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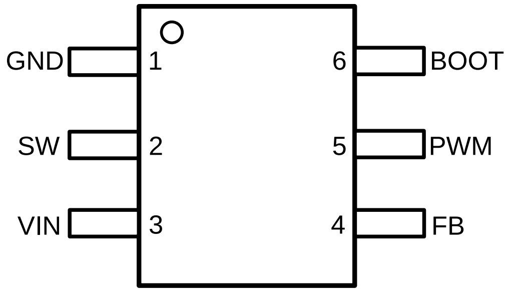
4 Revision History

Changes from Original (November 2016) to Revision A

Change	Page
Added initial release of the TPS54201 device.	1
Changed description to include protection modes.	1
Changed I_{LIM_HS1} and I_{LIM_HS2} CURRENT LIMIT.	5
Changed low side source current limit from (2.4/3.4/4.4) to (2.3/3.3/4.4),	5
Added TPS54201 $t_{HIC\_THERMAL}$, t_{HIC_OV} and t_{HIC_WAIT} Timing Requirements.	6
Added TPS54201 LED Short Protection image.	24
Added TPS54201 LED Open Protection image.	24
Added TPS54201 Sense Resistor Short Protection image.	24

5 Pin Configuration and Functions

TPS54200, TPS54201
DDC Package, 6-Pin SOT23
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
BOOT	6	O	A bootstrap capacitor is required between BOOT and SW.
FB	4	I	LED current detection feedback.
GND	1	G	Power ground.
PWM	5	I	Dimming input. Default low (internal pull low). In analog dimming mode, the internal reference will be proportional to the PWM duty input. In PWM dimming mode, LED current will be ON during the PWM high period in each PWM cycle.
SW	2	O	Switching node to external inductor.
VIN	3	P	Input supply voltage

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range, V_I	VIN	–0.3	30	V
	PWM	–0.3	7	V
	FB	–0.3	7	V
Output voltage range, V_O	BOOT-SW	–0.3	7	V
	SW	–0.3	30	V
	SW (20 ns transient)	–5	30	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range	VIN	4.5	28	V
		PWM	–0.1	6	V
		FB	–0.1	6	V
V_O	Output voltage range	BOOT-SW	–0.1	6.5	V
		SW	–0.1	28	V
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS5420x DDC (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +125°C, V_{IN} = 4.5 V to 28 V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		4.5		28	V
I_{OFF}	Shut down current	PWM = GND		2	8.6	µA
V_{IN_UVLO}	VIN under voltage lockout	Rising V_{IN}	3.83	4.2	4.47	V
		Falling V_{IN}	3.4	3.7	3.95	V
	Hysteresis			470		mV
DIMMING (PWM PIN)						
V_{ADIM}	Analog dimming mode threshold	Rising	1.97	2.07	2.17	V
		Falling		1.8		V
V_{PDIM}	PWM dimming mode threshold	Rising	0.9	1.0	1.1	V
		Falling		0.8		V
V_{PWM}	Threshold to identify PWM duty cycle	Rising	0.91	1.0	1.12	V
		Falling	0.5	0.63	0.72	V
$V_{PWM\_SHUTDOWN}$	Shutdown threshold		0.35	0.55		V
FEEDBACK AND ERROR AMPLIFIER						
V_{FB1}	Feedback voltage in analog dimming mode	PWM = 3.3 V, SW duty > 90%	201	205	210	mV
V_{FB2}	Feedback voltage in PWM dimming mode	PWM = 1.5 V, SW duty > 90%	96	100	104	mV
BOOT PIN						
V_{BOOT_UVLO}	BOOT-SW UVLO threshold	Rising		2.1	2.33	V
		Falling		2	2.2	V
POWER STAGE						
R_{HSD}	High-side FET on resistance	V_{BOOT} – SW = 6 V		150	259	mΩ
R_{LSD}	Low-side FET on resistance	V_{IN} > 6 V		70	120	mΩ
CURRENT LIMIT						
I_{LIM_HS1}	High side current limit 1	Either one of below conditions: 1. PWM dim mode 2. Analog dim mode and PWM duty >25%	2.4	3	3.6	A
I_{LIM_HS2}	High side current limit 2	Analog dim mode and PWM duty <25%	1	1.4	1.8	A
$I_{LIM\_LS\_SOURCE}$	Low side source current limit	V_{IN} > 6 V	2.3	3.3	4.4	A
$I_{LIM\_LS\_SINK}$	Low side sink current limit	V_{IN} > 6 V	1.25	1.7	2.2	A
FAULT PROTECTION						
Thermal shutdown(1)	Rising temperature		150	160	170	°C
	Hysteresis			10		°C
V_{OVP}	Over voltage protection			1		V
V_{OCP}	Over current protection			120%		

(1) Not production tested

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
$t_{HIC\_THERMAL}$	TPS54200 and TPS54201 Thermal shutdown hiccup time		32768		Cycles
OVER VOLTAGE PROTECTION					
t_{HIC_OV}	TPS54201 hiccup time for over voltage protection		32768		Cycles
OVER CURRENT AND OPEN LOOP PROTECTION					
$t_{SHUTDOWN\_DELAY}$	TPS54200 shutdown delay time for open loop and over current protection		512		Cycles
t_{HIC_WAIT}	TPS54201 Hiccup wait time for open loop and over current protection		512		Cycles
t_{HIC_OC}	TPS54201 Hiccup time for open loop and over current protection		16384		Cycles
SOFT START					
t_{SS}	Internal soft-start time		0.6		ms

6.7 Switching Characteristics

T_J = –40°C to +125°C, V_{IN} = 4.5 V to 28 V, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
F_{sw}	Switching frequency		480	600	700	kHz
ON TIME CONTROL						
t_{MIN_ON}	Minimum on time	Measured at 90% to 90% and 1A loading		90	105	ns

6.8 Typical Characteristics

V_{IN} = 12V, unless otherwise specified

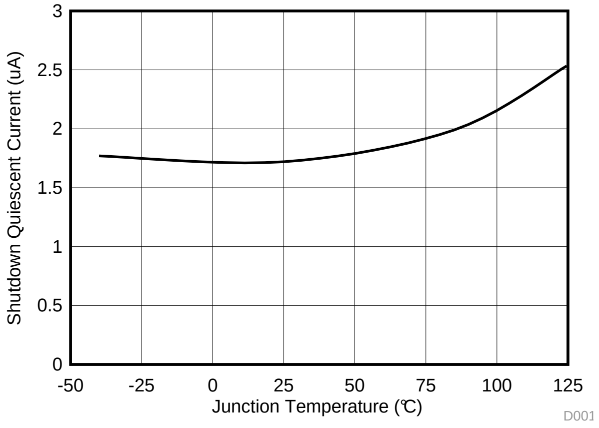


Figure 1. Shutdown Quiescent Current vs Junction Temperature

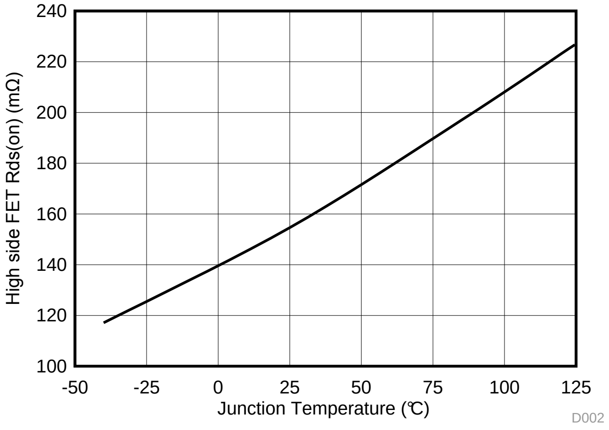


Figure 2. High-Side FET On Resistance vs Junction Temperature

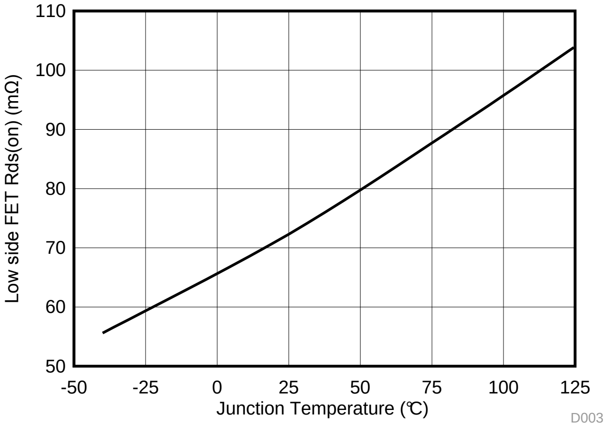


Figure 3. Low-Side FET On Resistance vs Junction Temperature

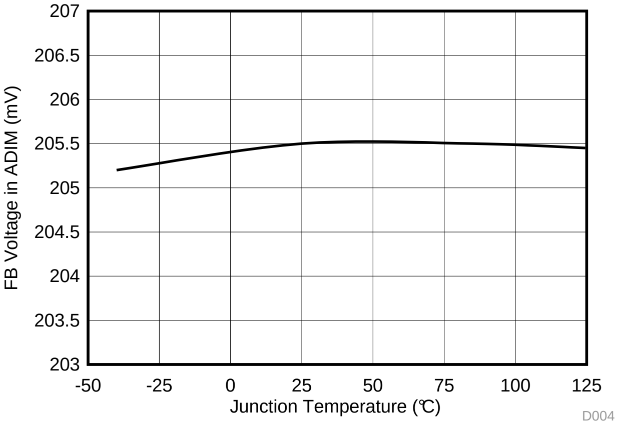


Figure 4. FB Voltage in ADIM vs Junction Temperature

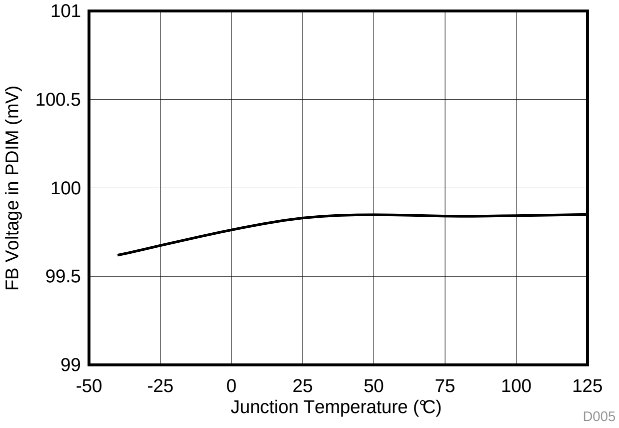


Figure 5. FB Voltage in PDIM vs Junction Temperature

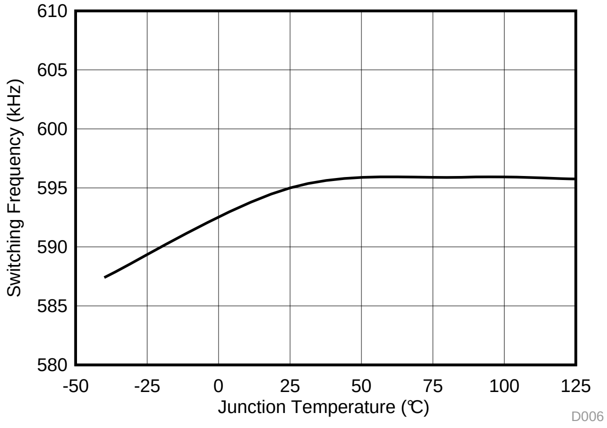


Figure 6. Switching Frequency vs Junction Temperature

Typical Characteristics (continued)

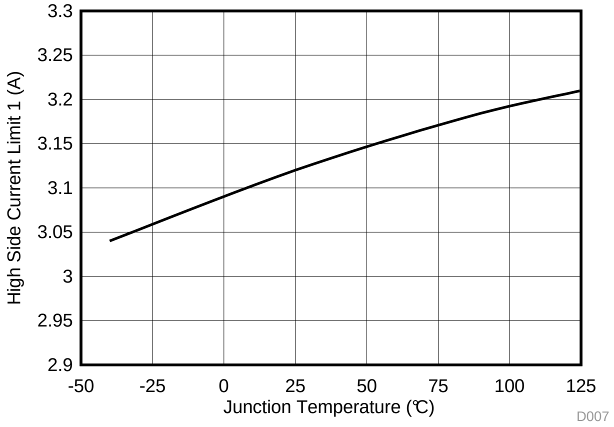


Figure 7. High-Side Source Current Limit 1 Threshold vs Junction Temperature

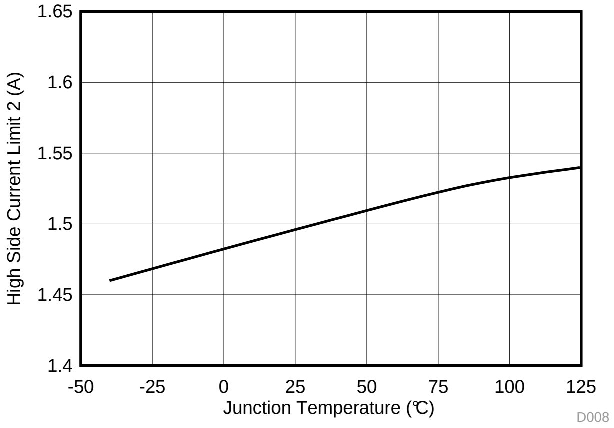


Figure 8. High-Side Source Current Limit 2 Threshold vs Junction Temperature

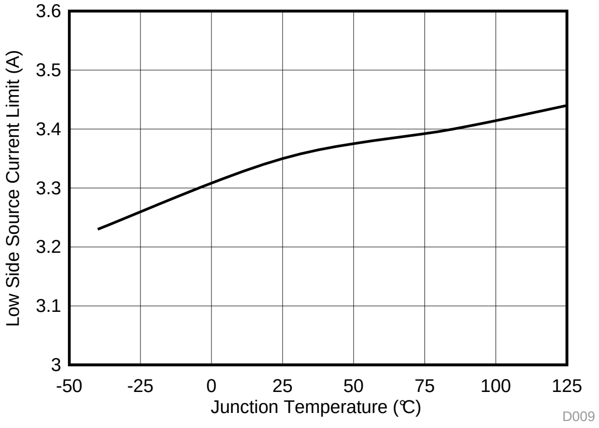


Figure 9. Low-Side Source Current Limit Threshold vs Junction Temperature

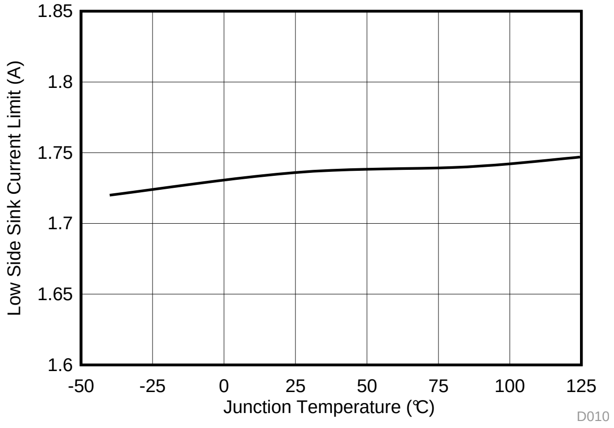


Figure 10. Low-Side Sink Current Limit Threshold vs Junction Temperature

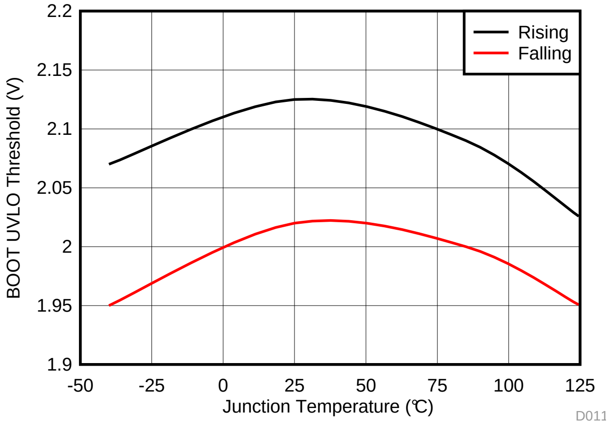


Figure 11. BOOT-SW UVLO Threshold vs Junction Temperature

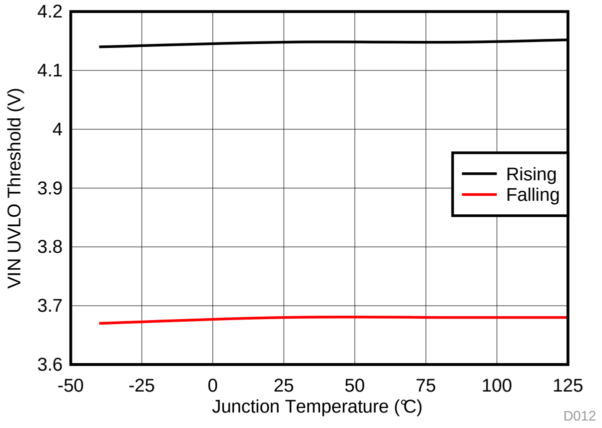


Figure 12. VIN UVLO Threshold vs Junction Temperature

Typical Characteristics (continued)

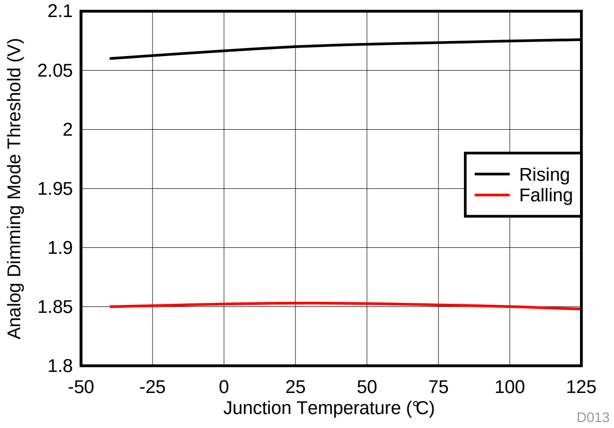


Figure 13. Analog Dimming Mode Threshold vs Junction Temperature

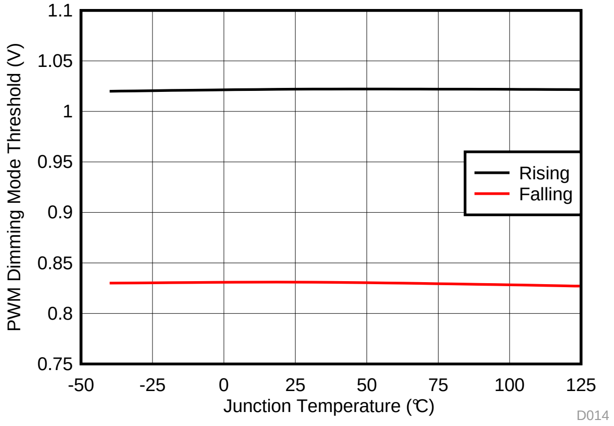


Figure 14. PWM Dimming Mode Threshold vs Junction Temperature

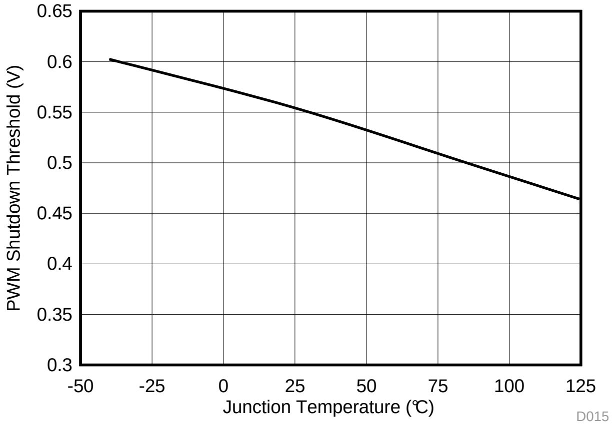


Figure 15. PWM Shutdown Threshold vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS5420x is a 1.5-A synchronous buck LED driver up to 28-V input. Current-mode operation provides fast transient response. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Fixed 600-kHz switching frequency is chosen for a good tradeoff between efficiency and size.

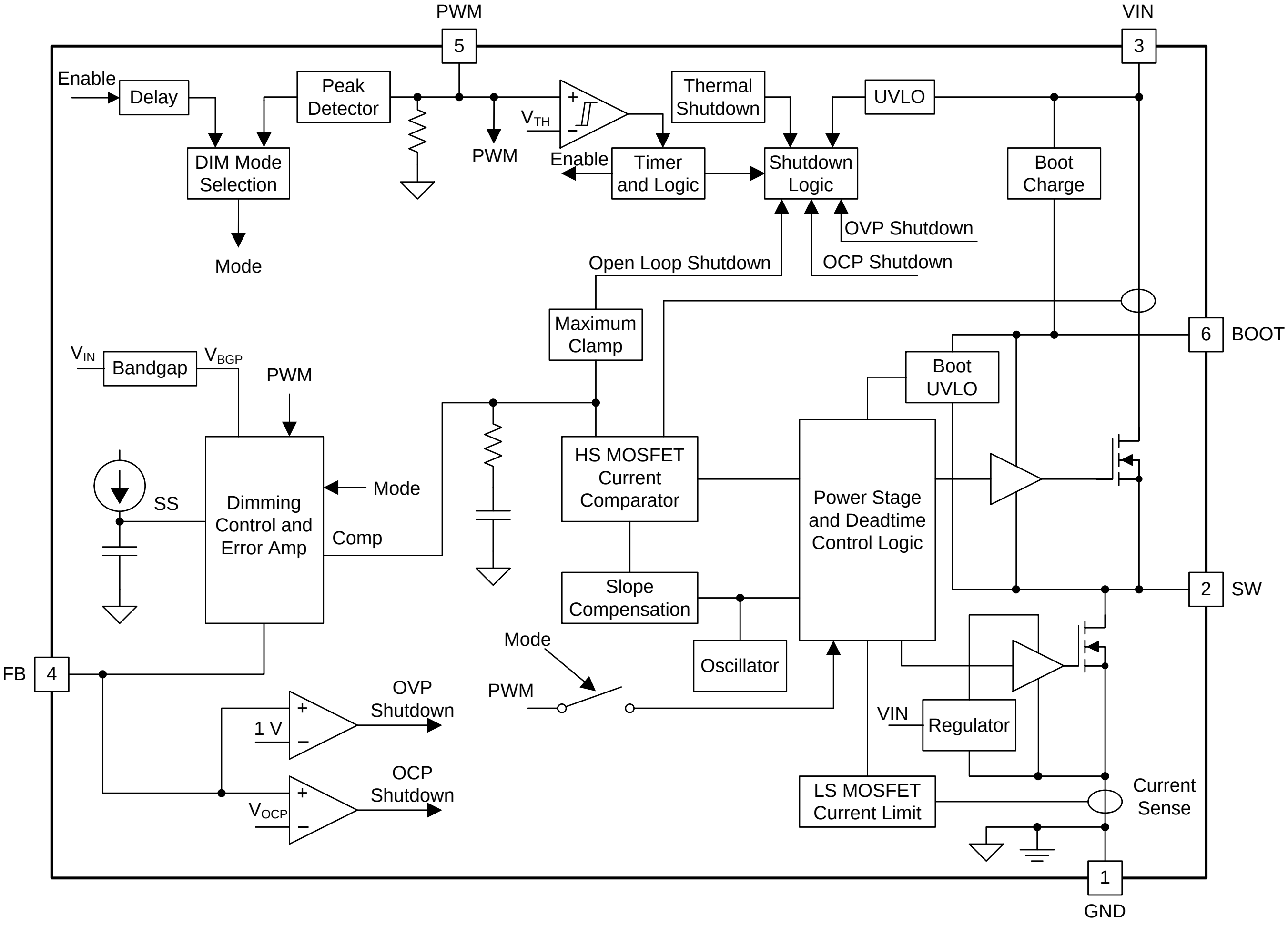
The integrated 150-mΩ high-side MOSFET and 70-mΩ low-side MOSFET allow for the high-efficiency LED driver with continuous output currents up to 1.5 A.

The TPS5420x supports deep dimming in both analog and PWM dimming mode. In analog dimming mode, the internal reference voltage is changed proportional to the duty cycle of PWM signal in 1% to 100% range. In PWM dimming mode, LED will be turn on and off according to PWM duty cycle periodically. For higher efficiency, the internal reference will be halved to 100 mV.

Cycle-by-cycle current limit in high-side MOSFET protects the converter in over-load condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. There is a low-side MOSFET sinking current limit to prevent excessive reverse current.

For safety and protection the TPS5420x includes LED open and short protection, sense resistor open and short protection, and device thermal protection. TPS54200 implements shutdown-and-latch mode protection, while TPS54201 adopts hiccup up mode protection.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The LED current is sensed by resistor in series with LED string. The sensed voltage is fed to FB pin through a RC filter, and then compared to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high-side power switch is turned off and the low-side power switch is turned on. Thus, the error amplifier output voltage will regulate inductor peak current, and in turn, the LED current to a target value. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal voltage reference. The trans-conductance of the error amplifier is 240 μA/V typically. The frequency compensation components are placed internally between the output of the error amplifier and ground.

7.3.3 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.4 Input Under Voltage Lockout

The device implements internal under-voltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold, which is 3.7 V typical. The internal VIN UVLO threshold has a hysteresis of 470 mV.

7.3.5 Voltage Reference

The voltage reference system produces a precise ±2.5% voltage-reference over temperature by scaling the output of a temperature stable bandgap circuit when PWM duty is 100%. In PWM dimming mode, the voltage reference, V_{REF}, is fixed at 100 mV. In analog dimming mode, V_{REF}, is proportional to duty cycle of PWM as shown in Figure 16.

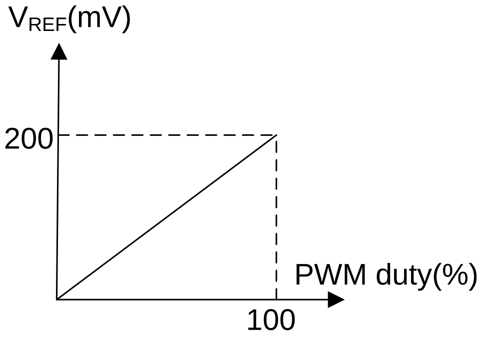


Figure 16. V_{REF} VS PWM Duty in Analog Dimming Mode

Feature Description (continued)

7.3.6 Setting LED Current

Once the voltage reference, V_{REF}, is chosen, one can set LED current by choosing proper sensing resistor according to Equation 1:

$$R_{SENSE} = \frac{V_{REF}}{I_{LED}} \tag{1}$$

7.3.7 Internal Soft Start

The TPS5420x device uses the internal soft-start function. The internal soft-start time is set to 0.6 ms typically.

7.3.8 Bootstrap Voltage (BOOT)

The TPS5420x has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.1 V with a hysteresis of 100 mV. A 6-V bootstrap voltage is maintained between BOOT and SW when V_{IN} > 6 V.

7.3.9 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.9.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off. During overcurrent conditions, such as sensing resistor is shorted, or the feedback filter RC network open circuit that drives FB low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit. This current limit is fixed 3.1 A typical in PWM dimming mode. In analog dimming mode with PWM duty >25%, this limit is also 3.1 A; While if PWM duty <25%, this limit will be halved to 1.5 A typical. Furthermore, if an output over-current condition occurs for more than the shutdown delay time, which is programmed for 512 switching cycles, the device shuts down and latches off to protect LED chip from being over-current damaged.

7.3.9.2 Low-Side MOSFET Over-Current Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle.

7.3.9.3 Low-Side MOSFET Reverse Over-Current Protection

The TPS5420x implements low-side reverse-current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is more than 1.7 A typical. By implementing this additional protection scheme, the converter is able to protect itself from excessive sink current during fault condition.

Feature Description (continued)

7.3.10 Fault Protection

The device is protected from kinds of fault conditions, such as LED open and short, sense resistor open and short, thermal shutdown. The only difference between TPS54200 and TPS54201 is the different protection mode used. TPS54200 implements shutdown-and-latch mode protection, while TPS54201 adopts hiccup up mode protection.

7.3.10.1 LED Open Protection

When LED load is open, FB voltage will be low, internal COMP voltage will be driven high and clamped. This will trigger shutdown delay counter (TPS54200) or hiccup wait counter (TPS54201). For TPS54200, once the shutdown delay time $t_{SHUTDOWN\_DELAY}$, which is programmed for 512 switching cycles, expires, the device shuts down and latches off. Both FETs are kept off. This is a latched shut-down, the device can be reset by recycling V_{IN}. For TPS54201, once the hiccup wait time t_{HIC_WAIT}, which is programmed for 512 switching cycles, expires, the device shuts down and starts hiccup timer t_{HIC_OC}, which is programmed for 16384 switching cycles. During shutdown period, both FETs are kept off. Once the hiccup timer expires, TPS54201 will restart again. If the failure still exist, TPS54201 will repeat above hiccup shutdown and restart process.

7.3.10.2 LED Short Protection

When LED load is shorted, FB voltage will be higher than V_{REF}, and internal COMP voltage will be driven low and clamped, high-side MOSFET will be commanded on for minimum on-time each cycle. In this condition, if the output voltage is too low, the inductor current may not be able to balance in a cycle, causing current runaway. Finally, the inductor current will be clamped by low side MOSFET sourcing current limit which is much higher than target LED current. If the FB voltage is higher than OCP threshold, which is 250 mV typical in analog dimming mode, or 120 mV typical in PWM dimming mode, shutdown delay counter (TPS54200) or hiccup wait counter (TPS54201) will be triggered. For TPS54200, once the shutdown delay time $t_{SHUTDOWN\_DELAY}$, which is programmed for 512 switching cycles, expires, the device shuts down and latches off. Both FETs are kept off. This is a latched shut-down, the device can be reset by recycling V_{IN}. For TPS54201, once the hiccup wait time t_{HIC_WAIT}, which is programmed for 512 switching cycles, expires, the device shuts down and starts hiccup timer t_{HIC_OC}, which is programmed for 16384 switching cycles. During shutdown period, both FETs are kept off. Once the hiccup timer expires, TPS54201 will restart again. If the failure still exist, TPS54201 will repeat above hiccup shutdown and restart process..

7.3.10.3 Sense Resistor Short Protection

When the sense resistor is shorted, FB voltage will be low, internal COMP voltage will be driven high and clamped. This will trigger shutdown delay counter (TPS54200) or hiccup wait counter (TPS54201). For TPS54200, once the shutdown delay time $t_{SHUTDOWN\_DELAY}$, which is programmed for 512 switching cycles, expires, the device shuts down and latches off. Both FETs are kept off. This is a latched shut-down, the device can be reset by recycling V_{IN}. For TPS54201, once the hiccup wait time t_{HIC_WAIT}, which is programmed for 512 switching cycles, expires, the device shuts down and starts hiccup timer t_{HIC_OC}, which is programmed for 16384 switching cycles. During shutdown period, both FETs are kept off. Once the hiccup timer expires, TPS54201 will restart again. If the failure still exist, TPS54201 will repeat above hiccup shutdown and restart process.

7.3.10.4 Sense Resistor Open Protection

When the sense resistor is open before the device power on, the device will charge BOOT capacitor at power on moment, the charging current will flow through inductor, output capacitor and RC filter at FB pin, and charge up the FB pin voltage. Once the device detects FB voltage higher than the 1-V OVP threshold, the device shuts down immediately. For TPS54200, this is a latched shutdown, the device can be reset by recycling V_{IN}. For TPS54201, once the device shuts down, it will starts over voltage hiccup timer t_{HIC_OV}, which is programmed for 32768 switching cycles. During shutdown period, both FETs are kept off. Once the over voltage hiccup timer expires, TPS54201 will restart again. If the failure still exist, TPS54201 will repeat above hiccup shutdown and restart process.

Feature Description (continued)

7.3.10.5 Over Voltage Protection

When the FB pin, for some reason, has a voltage higher than 1 V applied, the device will shut down immediately. Both FETs are kept off. This is called over-voltage protection. For TPS54200, this is a latched shutdown. Recycle V_{IN} can reset the device. For TPS54201, once the device shuts down, it will starts over voltage hiccup timer t_{HIC_OV}, which is programmed for 32768 switching cycles. During shutdown period, both FETs are kept off. Once the over voltage hiccup timer expires, TPS54201 will restart again. If the failure still exist, TPS54201 will repeat above hiccup shutdown and restart process.

7.3.10.6 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. When the junction temperature drops below 150°C typically, the internal thermal-hiccup timer $t_{HIC\_THERMAL}$, which is programmed for 32768 switching cycles, begins to count. The device reinitiates the power-up sequence once the thermal-hiccup timer expires.

7.4 Device Functional Modes

7.4.1 Enable and Disable Device

PWM pin performs not only dimming function, but also enable and disable function. When the VIN voltage is above the UVLO threshold, the TPS5420x can be enabled by driving PWM pin higher than the threshold voltage, 0.56 V typical. To disable the device, the PWM pin should be kept lower than the threshold voltage, 0.55 V typical, for 40 ms or longer. PWM pin has internal pull-down resistor, floating this pin will disable the device.

Suggested power on sequence is applying Vin at first, then followed by PWM signal.

7.4.2 Mode Detection

The magnitude of PWM signal is used to determine which dimming mode the device will enter. The internal peak detector at PWM pin will hold the magnitude of PWM signal. Once the device is enabled, after 300-µs delay, the output of the peak detector will be compared with two voltage thresholds VADIM and VPDIM, which is 1 V and 2.07 V respectively. If the output of peak detector is higher than 2.07 V, analog dimming mode will be chosen and locked. If it's between 1 V and 2.07 V, PWM dimming mode will be chosen and locked. If it is less than 1 V, the device will wait another 300 µs and compare again, and this process will repeat until at least one mode is chosen and locked. See Figure 17 and Table 1 for reference. After the mode is detected and locked, soft start begins, output voltage ramps up and the LED current will be regulated at target value. The dimming mode can not be changed unless V_{IN} or PWM is recycled.

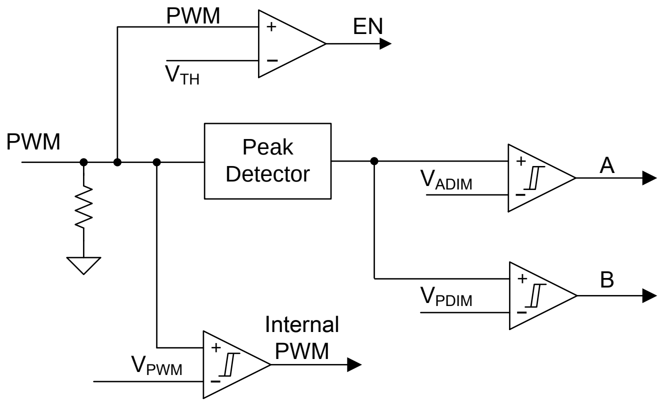


Figure 17. Mode Detection Circuit

Table 1. Mode Detection Condition

A	B	MODE
H	H	Enter analog dimming mode
L	H	Enter PWM dimming mode
L	L	Keep detecting until lock one dimming mode

7.4.3 Analog Dimming Mode Operation

Once Analog dimming mode is chosen, the internal voltage reference for FB pin will be ~200 mV at full scale, and proportional to PWM duty cycle as shown in Figure 16. LED current is continuous in this mode, and the current magnitude can be adjusted by changing PWM duty cycle, see Figure 18. Since the internal voltage reference is filtered from the PWM signal, too low PWM frequency may cause a little big ripple at voltage reference. To minimize this ripple, suggested PWM signal frequency is 10 kHz or higher, such as 50 kHz.

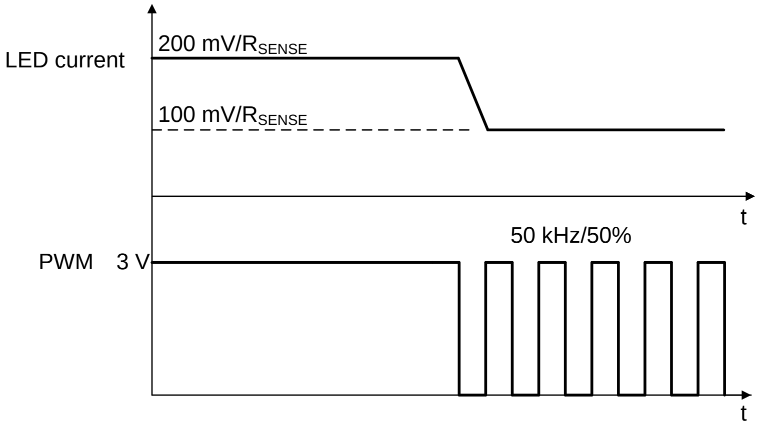


Figure 18. Analog Dimming Operation

A comparator with 400-mV hysteresis is used to generate the internal PWM signal, see Figure 17. This internal PWM duty cycle will decide the voltage reference. To make sure PWM pin signal is correctly identified, the high level of PWM signal should be higher than 1 V, and low level should be lower than 0.6 V. Figure 19 shows the relationship between external PWM and internal PWM signal.

7.4.4 PWM Dimming Mode Operation

Once PWM dimming mode is chosen, the internal voltage reference for FB pin will be fixed at 100mV, LED current will be on/off corresponding to PWM duty cycle, see Figure 19. Due to the limited control loop response, to get a relatively linear dimming performance, suggested PWM signal frequency should be less than 1 kHz.

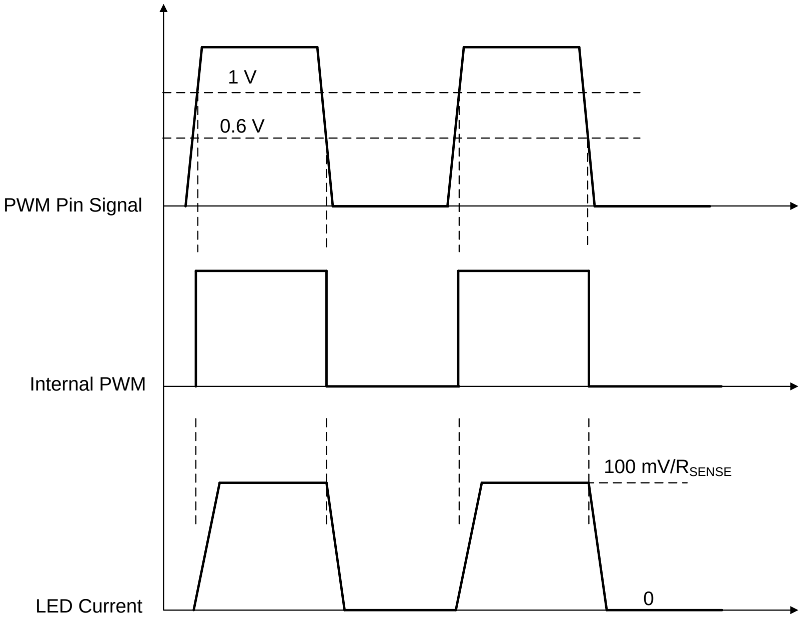


Figure 19. PWM Dimming Operation

In some application where dimming is not needed, one can just connect resistor divider from V_{IN} to PWM pin as Figure 20 shows.

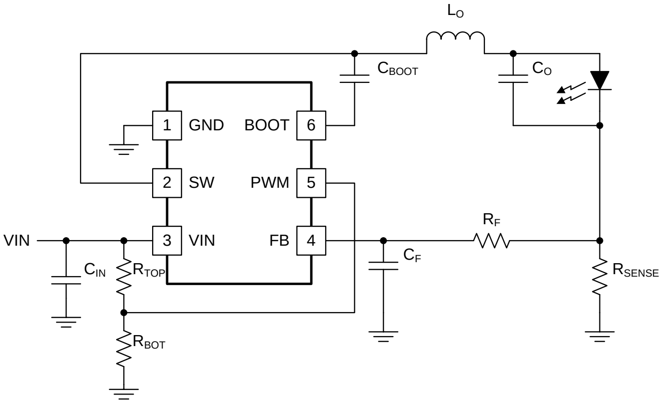


Figure 20. Application Without Dimming

R_{TOP} and R_{BOT} should be sized to make sure PWM pin voltage higher than 1 V when V_{IN} reach its steady voltage. It is best to make sure the PWM pin voltage is less than 2 V, thus one can have 100 mV at the FB pin for better efficiency. 10 kΩ is a good starting point for R_{BOT}, then choose R_{TOP} according to Equation 2:

$$R_{TOP} = \left(\frac{V_{IN}}{V_{PWM}} - 1 \right) \times R_{BOT} \quad (2)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS5420x is typically used as a buck converter to drive one or more LEDs from 4.5-V to 28-V input. The TPS5420x supports both analog dimming mode and PWM dimming mode.

8.2 Typical Application

8.2.1 TPS5420x 12-V Input, 1.5-A, 3-Piece IR LED Driver with Analog Dimming

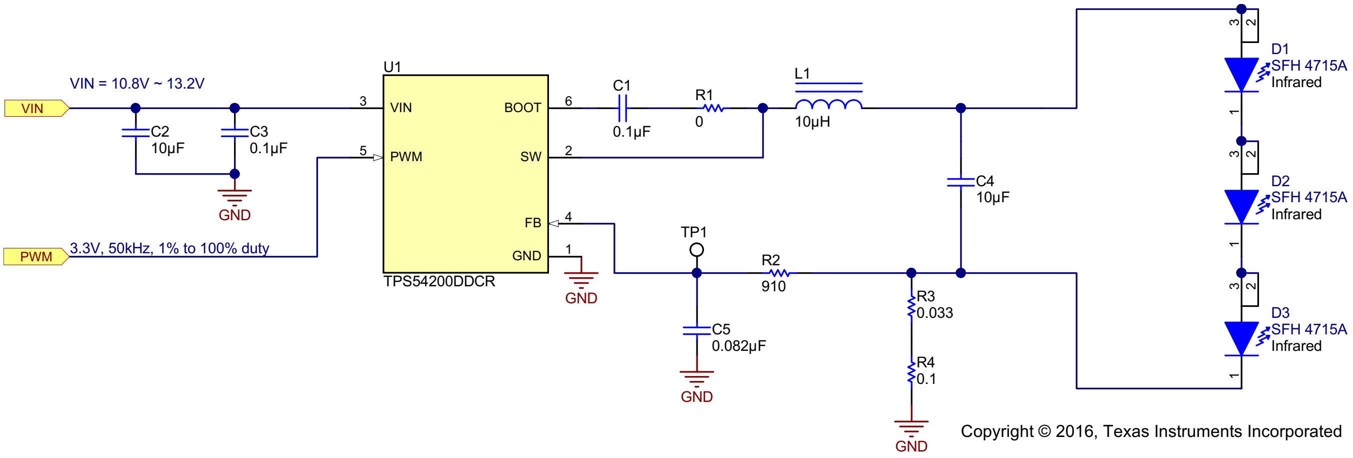


Figure 21. 12-V_{IN}, 1.5-A, 3-piece IR LED, Analog Dimming Reference Design

8.2.1.1 Design Requirements

For this design example, use the parameters in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage range	10.8 V to 13.2 V
LED string forward voltage	5.4-V stack
Output voltage	5.6 V
LED current at 100% PWM duty	1.5 A
LED current ripple	30 mA or less
Input voltage ripple	400 mV or less
PWM dimming range	1% to 100%, 3.3 V/50 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

Use Equation 3 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{LED} \times F_{SW}}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED Current.
- I_{LED} is the maximum LED current.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor. (3)

In general, the value of K_{IND} is suggested between 0.2 and 0.4. For the application that can tolerate higher LED current ripple or use larger output capacitors, one can choose 0.4 for K_{IND}, otherwise, smaller K_{IND} like 0.2 can be chosen to get small enough LED current ripple.

With the chosen inductor value the user can calculate the actual inductor current ripple using Equation 4.

$$I_{L(ripple)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L \times F_{SW}} \quad (4)$$

The inductor RMS current and saturation current ratings must be greater than those seen in the application. This ensures that the inductor does not overheat or saturate. During power-up, transient conditions, or fault conditions, the inductor current can exceed its normal operating current. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the converter current limit. This is not always possible due to application size limitations. The peak inductor current and the RMS current equations are shown in Equation 5 and Equation 6.

$$I_{L(peak)} = I_{LED} + \frac{I_{L(ripple)}}{2} \quad (5)$$

$$I_{L(rms)} = \sqrt{I_{LED}^{2} + \frac{I_{L(ripple)}^{2}}{12}} \quad (6)$$

In this design, choose K_{IND} = 0.3, according to LED manufacturer's data sheet, IR LED has 1.75-V forward voltage at 1.5-A current, V_{OUT} = 1.75 V × 3 + 0.2 V = 5.45 V, the calculated inductance is 11.9 µH. A 10-µH inductor (part number is 744066100 from Wurth) is chosen. With this inductor, the ripple, peak and RMS current of inductor is 0.53 A, 1.77 A and 1.51 A respectively. The chosen inductor has ample margin.

8.2.1.2.2 Input Capacitor Selection

The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10-µF capacitor is enough. An additional 0.1-µF capacitor from VIN to GND is optional to provide additional high-frequency filtering. The input-capacitor voltage rating must be greater than the maximum input voltage and have a ripple-current rating greater than the maximum input-current ripple of the converter. The RMS input-ripple current is calculated in Equation 7, where D is the duty cycle (output voltage divided by input voltage).

$$I_{CIN(rms)} = I_{LED} \times \sqrt{D \times (1 - D)} \quad (7)$$

Use Equation 8 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor. Ceramic capacitance tends to decrease as the applied DC voltage increases. This depreciation must be accounted for when calculate input ripple voltage.

$$V_{IN(ripple)} = \frac{I_{LED} \times D \times (1 - D)}{C_{IN} \times F_{SW}} + I_{LED} \times ESR_{CIN} \quad (8)$$

In this design, a 10-µF, 35-V X7R ceramic capacitor, part number GRM32ER7YA106KA12L, from muRata is chosen. This yields around 70-mV input ripple voltage. The calculated RMS input ripple current is 0.75 A, well below the capacitor's ripple current rating.

8.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency ripple current through the LED string. Various guidelines disclose how much high-frequency ripple current is acceptable in the LED string. Excessive ripple current in the LED string increases the RMS current in the LED string, and therefore the LED temperature also increases.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer’s data sheet.
2. Calculate the required impedance of the output capacitor (ZOUT) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated previously in inductor selection.
3. Calculate the minimum effective output capacitance required.
4. Increase the output capacitance appropriately due to the derating effect of applied dc voltage.

See Equation 9, Equation 10 and Equation 11.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \# \text{ of LEDs} \tag{9}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(ripple)} - I_{LED(ripple)}} \tag{10}$$

$$C_{OUT} = \frac{1}{2\pi \times F_{SW} \times Z_{COUT}} \tag{11}$$

Once the output capacitor is chosen, Equation 12 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \tag{12}$$

OSRAM IR LED SFH4715A is used here. The dynamic resistance of this LED is 0.25 Ω at 1.5-A forward current. In this design, a 10-µF, 35-V X7R ceramic capacitor is chosen, the part number is GRM32ER7YA106KA12L, from muRata. The calculated ripple current of the LED is about 20 mA.

8.2.1.2.4 FB Pin RC Filter Selection

The RC filter RF and CF connected between sense resistor and FB pin is used to generate a pole for loop stability purpose. Moving this pole can adjust loop bandwidth. Suggested frequency of pole is 2 kHz in analog dimming mode, and 4 kHz in PWM dimming mode. Use Equation 13 to choose RF and CF. Due to DC offset current of internal amplifier, suggest RF less than 1 kΩ to minimize the effect on LED current regulation accuracy.

$$C_F = \frac{1}{2\pi \times R_F \times f_{POLE}} \tag{13}$$

Analog dimming mode is implemented in this design. The design choose the pole at around 2 kHz, and 910 Ω as the filter resistor, then the calculated filter capacitance is 87 nF. A 82 nF is chosen for this filter.

8.2.1.2.5 Sense Resistor Selection

The maximum target LED current at 100% PWM duty is 1.5 A, the corresponding V_{REF} is 200 mV. By using Equation 1, calculates the needed sense resistance at 133 mΩ. Pay close attention to the power consumption of the sense resistor in this design at 300 mW, make sure the chosen resistor has enough margin in power rating.

8.2.1.3 Application Curves

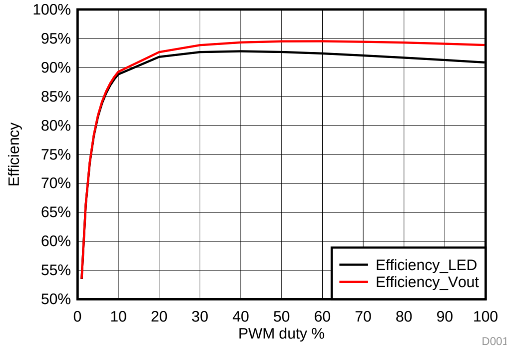
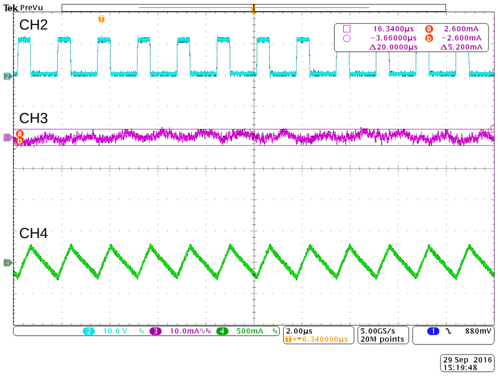
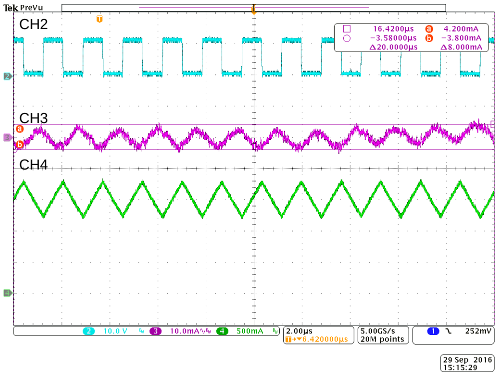


Figure 22. Efficiency



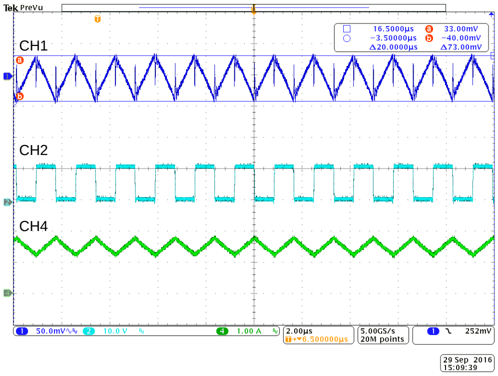
CH2: SW CH3: LED Current CH4: Inductor Current
(AC Coupled)

Figure 23. LED Current Ripple at 1% PWM Duty



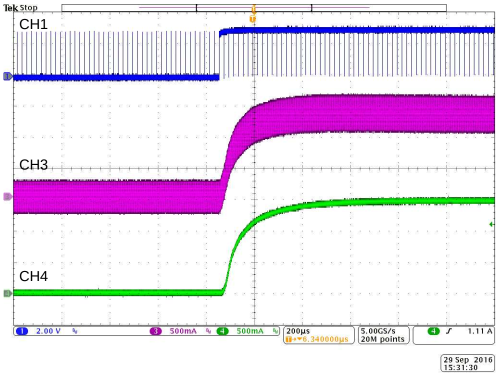
CH2: SW CH3: LED Current CH4: Inductor Current
(AC Coupled)

Figure 24. LED Current Ripple at 100% PWM Duty



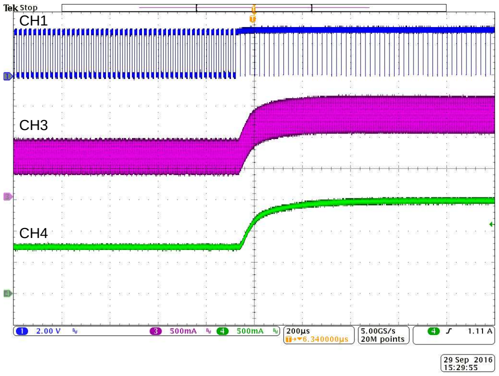
CH1: V_{IN} CH2: SW CH4: Inductor Current
(AC Coupled)

Figure 25. Input Voltage Ripple at 100% PWM Duty



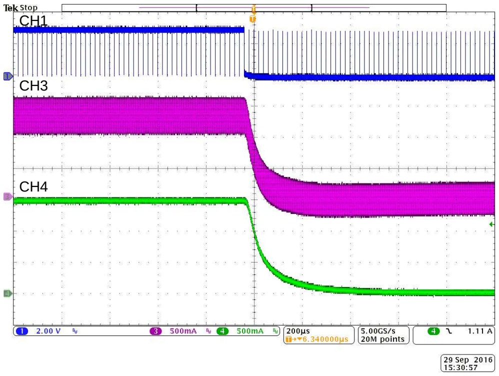
CH1: PWM CH3: Inductor Current CH4: LED Current

Figure 26. LED Current Transient as PWM Duty Change from 1% to 99%



CH1: PWM CH3: Inductor Current CH4: LED Current

Figure 27. LED Current Transient as PWM Duty Change from 50% to 99%



CH1: PWM CH3: Inductor Current CH4: LED Current

Figure 28. LED Current Transient as PWM Duty Change from 99% to 1%

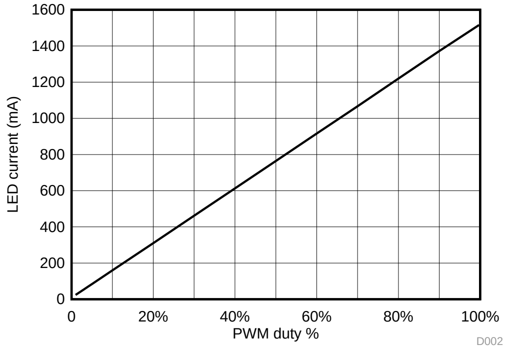
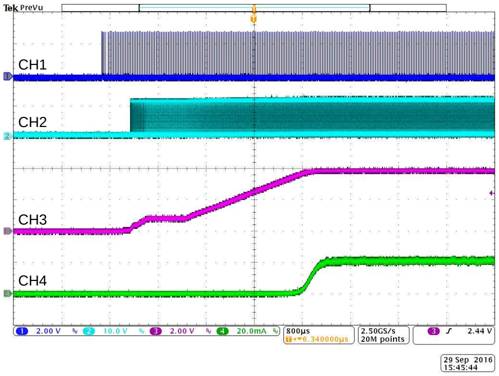
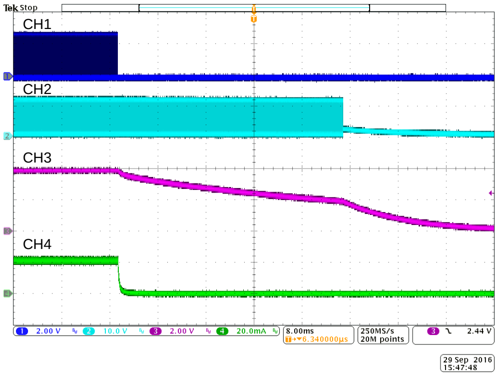


Figure 29. LED Current vs PWM Duty



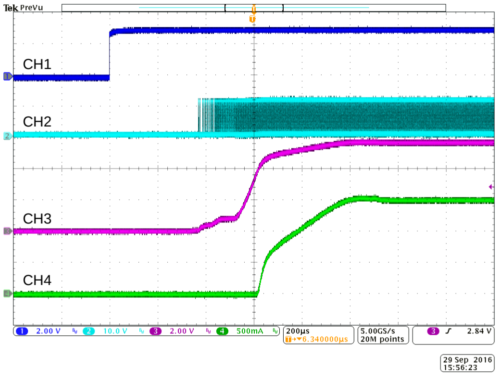
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current;

Figure 30. Start Up at 1% PWM Duty/50 kHz



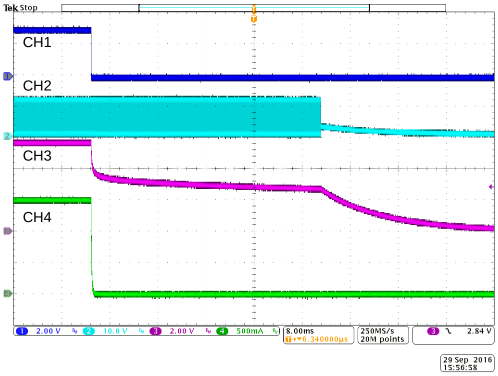
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current;

Figure 31. Shutdown at 1% PWM Duty/50 kHz



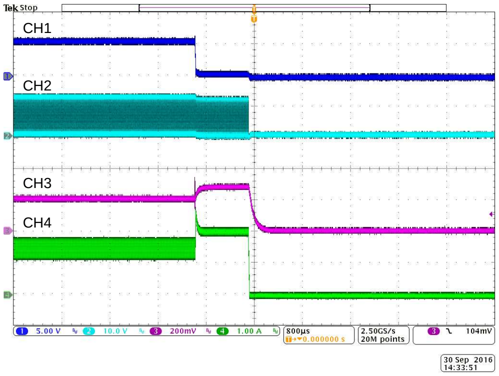
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 32. Start Up at 100% PWM Duty



CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 33. Shutdown at 100% PWM Duty

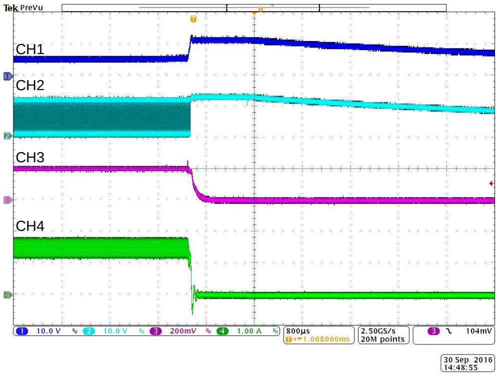


CH1: VOUT CH2: SW CH3: FB CH4: Inductor Current

Figure 34. LED Short Protection (100% duty PWM) of TPS54200

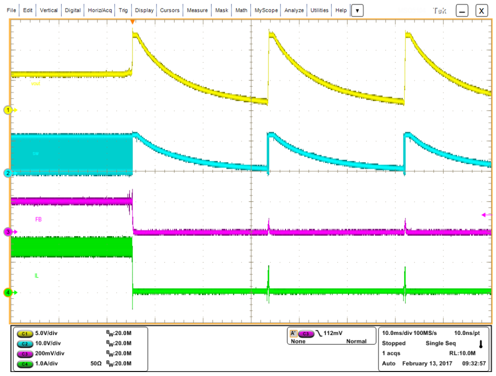
CH1: VOUT CH2: SW CH3: FB CH4: Inductor Current

Figure 35. LED Short Protection (100% duty PWM) of TPS54201



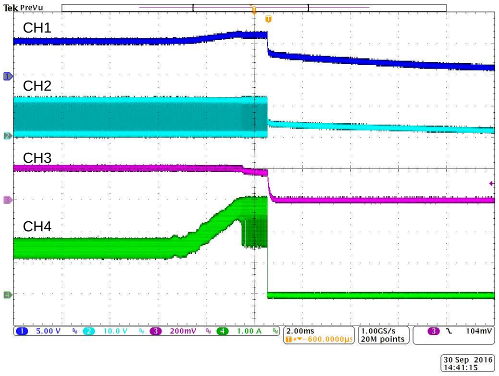
CH1: VOUT CH2: SW CH3: FB CH4: Inductor Current

Figure 36. LED Open Protection(100% duty PWM) of TPS54200



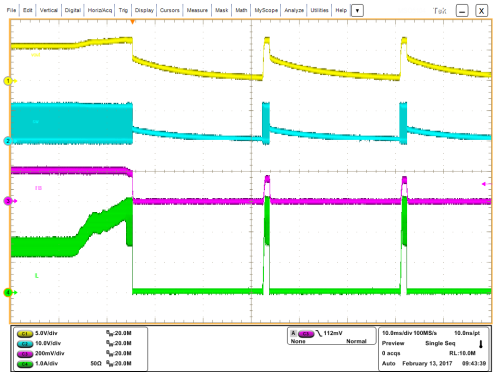
CH1: VOUT CH2: SW CH3: FB CH4: Inductor Current

Figure 37. LED Open Protection (100% duty PWM) of TPS54201



CH1: VOUT CH2: SW CH3: FB CH4:Inductor Current

Figure 38. Sense Resistor Short Protection (100% duty PWM) of TPS54200



CH1: VOUT CH2: SW CH3: FB CH4: Inductor Current

Figure 39. Sense Resistor Short Protection (100% duty PWM) of TPS54201

8.2.2 TPS5420x 24-V Input, 1-A, 4-piece WLED Driver with PWM Dimming

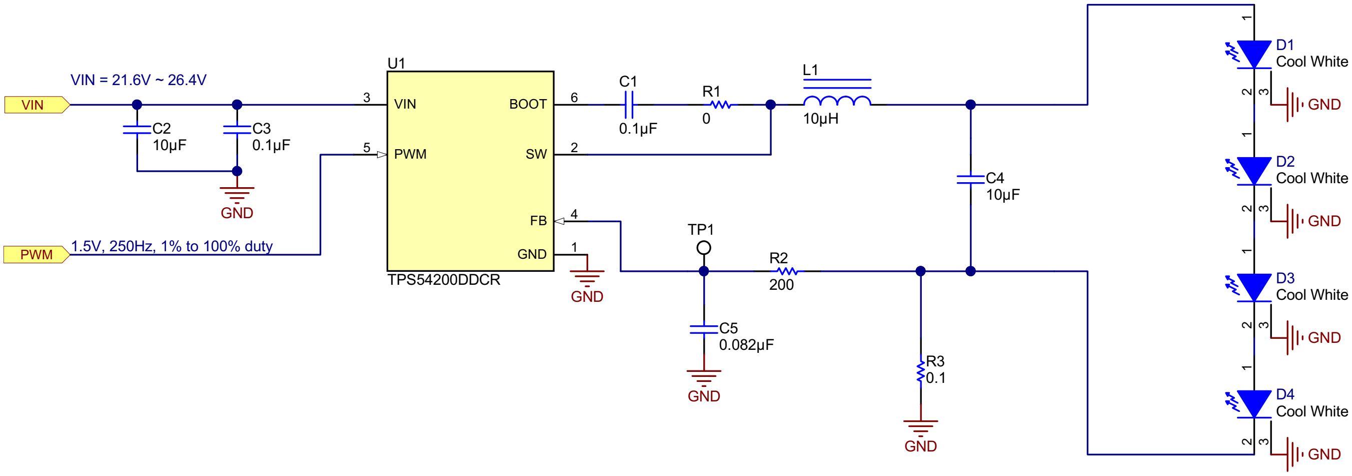


Figure 40. 24-V Input, 1-A, 4-Piece WLED Driver with PWM Dimming Reference Design

8.2.2.1 Design Requirements

For this design example, use the parameters in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage range	21.6 V to 26.4 V
LED string forward voltage	11.6-V stack
Output voltage	11.7 V
LED current at 100% PWM duty	1 A
LED current ripple	30 mA or less
Input voltage ripple	400 mV or less
PWM dimming range	1% to 100%, 1.5 V/250 Hz

8.2.2.2 Detailed Design Procedure

The detail design process in this example is basically the same with that shown in previous design example. Shown below is the design results.

8.2.2.2.1 Inductor Selection

Cree White LED XLampXML is used. According to the LED manufacturer's data sheet, this LED has 2.9-V forward voltage at 1-A current, V_{OUT} = 2.9 V × 4 + 0.1 V = 11.7 V. Choose K_{IND} = 0.3 which gives a 36-µH inductance. With this inductance, the ripple current on the inductor is only 0.3-A peak-to-peak, which is too conservative and increases total system cost and size.

For this application concerns with system cost and size was taken into account, decide the inductance by choosing a larger peak-to-peak inductor ripple current. To choose a proper peak-to-peak inductor ripple, the low-side FET sink current limit should not be violated when converter works in no-load condition, this requires the half of peak-to-peak inductor ripple to be lower than that limit. Another consideration is the increased core loss and copper loss in the inductor with this larger peak-to-peak ripple current which is also acceptable. Once this peak-to-peak inductor ripple current is chosen, Equation 14 can be used to calculate the required inductance.

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times I_{L(ripple)} \times F_{SW}}$$

where

- $I_{L(RIPPLE)}$ is the peak-to-peak inductor ripple current. (14)

Choose 1-A peak-to-peak inductor ripple current, half of the current is 0.5 A, much lower than the minimum low-side sink current limit of 1.25 A. The calculated inductance is 10.9 µH. Choose a 10-µH inductor, the part number is 744066100 from Wurth, the ripple, peak and RMS current of the inductor is 1.09 A, 1.54 A and 1.05 A respectively. The chosen inductor has ample margin in this design.

8.2.2.2.2 Input Capacitor Selection

In this design, a 10-µF, 35-V X7R ceramic capacitor, part number GRM32ER7YA106KA12L, from muRata is chosen. This yields around 70-mV input-ripple voltage. The calculated RMS input ripple current is 0.5 A, well below the capacitor's ripple current rating.

8.2.2.2.3 Output Capacitor Selection

The dynamic resistance of this LED is 0.184 Ω at 1-A forward current. In this design, choose a 10-µF, 35-V X7R ceramic capacitor, part number GRM32ER7YA106KA12L, from muRata, the calculated ripple current of LED is about 40 mA.

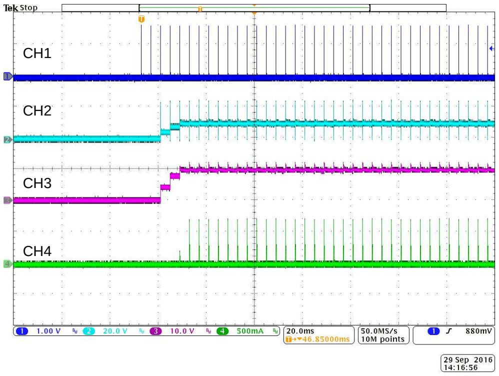
8.2.2.2.4 FB Pin RC Filter Selection

PWM dimming mode is implemented in this design. Choose the pole at around 4 kHz, and choose 475 Ω as the filter resistor, with those values an 82 nF should be chosen for this filter. To get a faster loop response, choose a smaller filter resistor. In this design, 200 Ω was chosen to get a pole at ~10 kHz.

8.2.2.2.5 Sense Resistor Selection

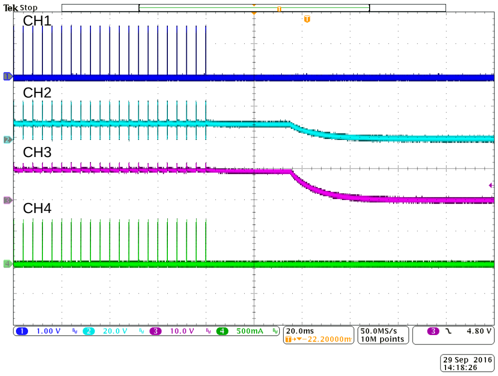
The maximum target LED current at 100% PWM duty is 1 A, the corresponding V_{REF} is 100 mV. By using Equation 1, one can calculate the needed sense resistance is 100 mΩ. Pay close attention to the power consumption of the sense resistor in this design at 100 mW, make sure the chosen resistor has enough margin in the power rating.

8.2.2.3 Application Curves



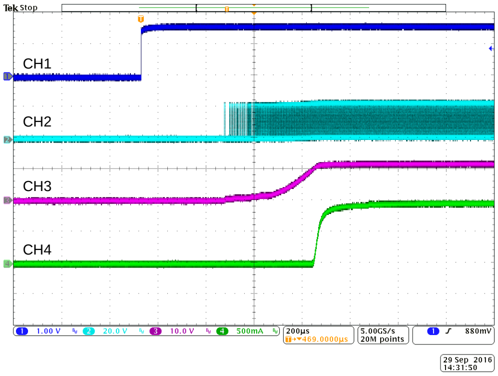
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 41. Start Up at 1% PWM Duty/250 Hz



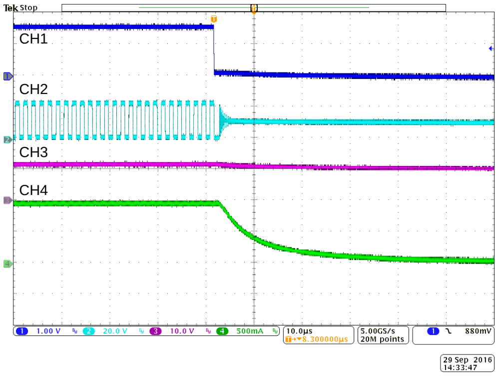
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 42. Shutdown at 1% PWM Duty/250 Hz



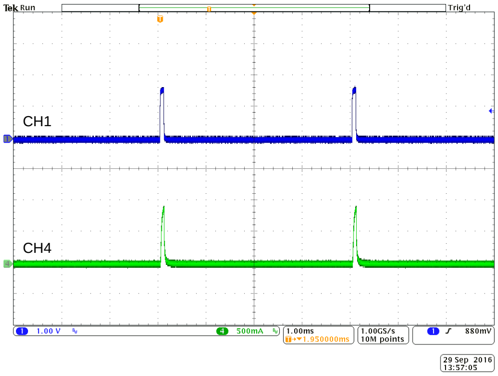
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 43. Start Up at 100% PWM Duty



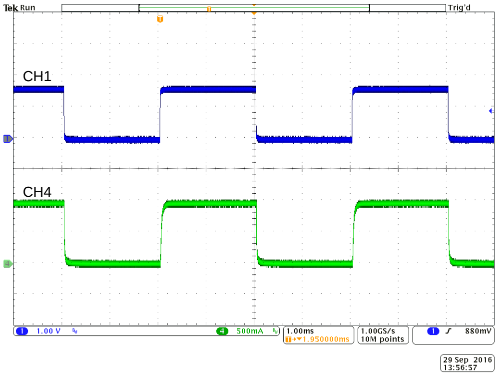
CH1: PWM CH2: SW CH3: VOUT CH4: LED Current

Figure 44. Shutdown at 100% PWM Duty



CH1 PWM CH4: LED Current

Figure 45. PWM Dimming with 2% duty, 250 Hz



CH1: PWM CH4: LED Current

Figure 46. PWM Dimming with 50% duty, 250 Hz

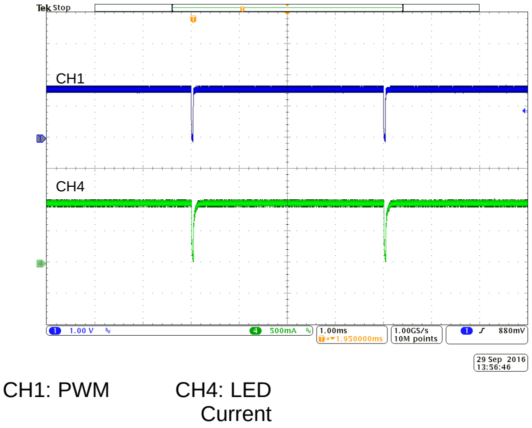


Figure 47. PWM Dimming with 99% Duty, 250 Hz

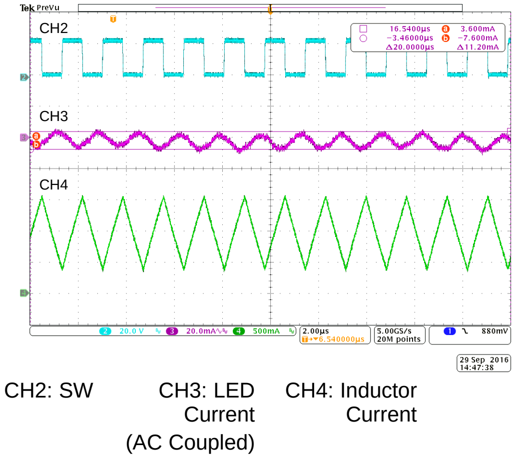


Figure 48. LED Current Ripple at 100% PWM Duty

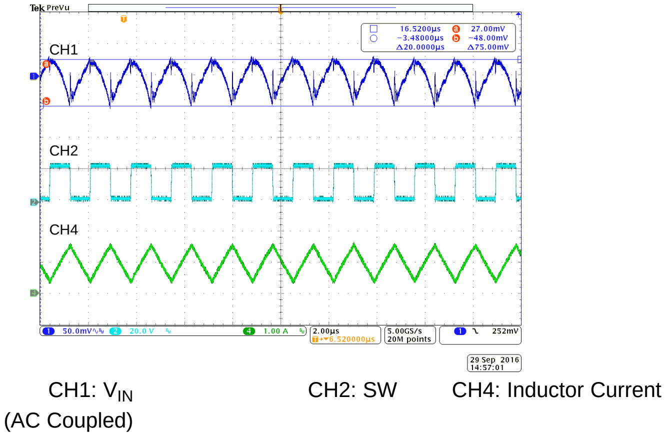


Figure 49. Input Voltage Ripple at 100% PWM Duty

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

The TPS5420x requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

10.1 Layout Guidelines

An example of a proper layout for the TPS5420x is shown in Figure 50.

- Creating a large GND plane for good electrical and thermal performance is important.
- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas advantages provides excellent heat dissipation.
- Thermal vias can be used to connect the topside GND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the VIN pin and the GND pin.
- The SW trace must be kept as short as possible to reduce the possibility of radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The FB trace should be kept as short as possible and placed away from the high-voltage switching trace, and the ground shield.
- In higher current applications, routing the load current of the current-sense resistor to the junction of the input capacitor and GND node may be necessary.

10.2 Layout Example

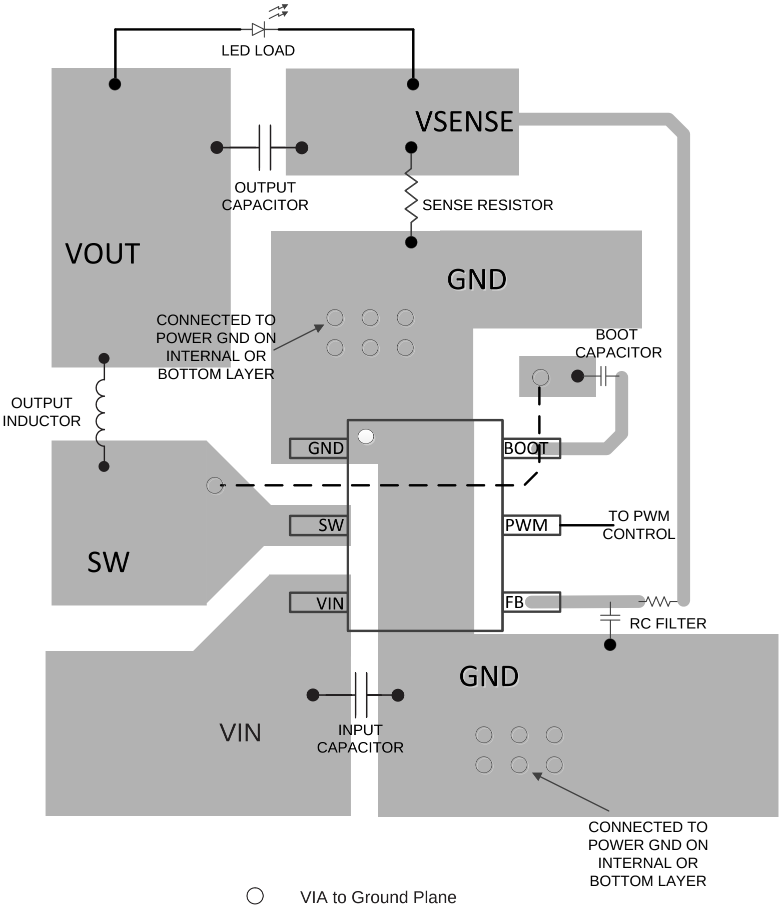


Figure 50. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54200DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4200	Samples
TPS54200DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4200	Samples
TPS54201DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	4201	Samples
TPS54201DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	4201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

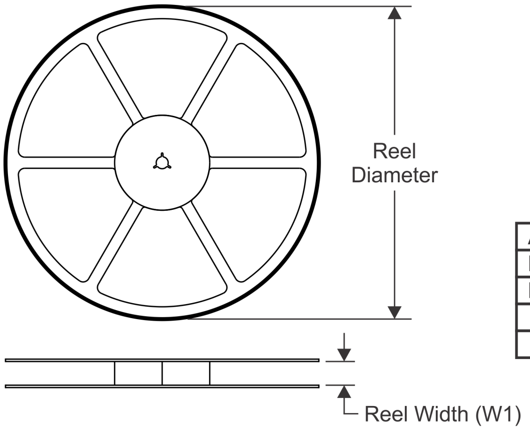
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

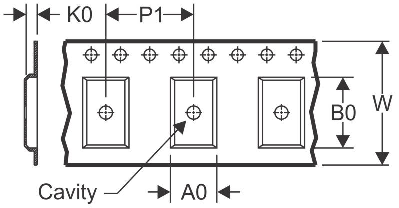
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

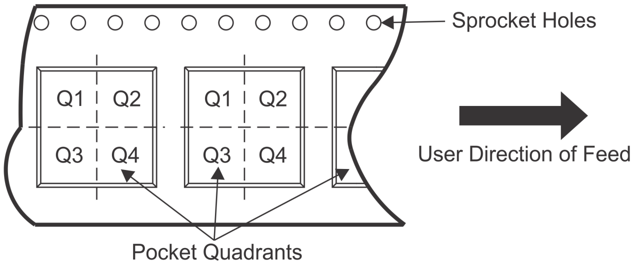


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

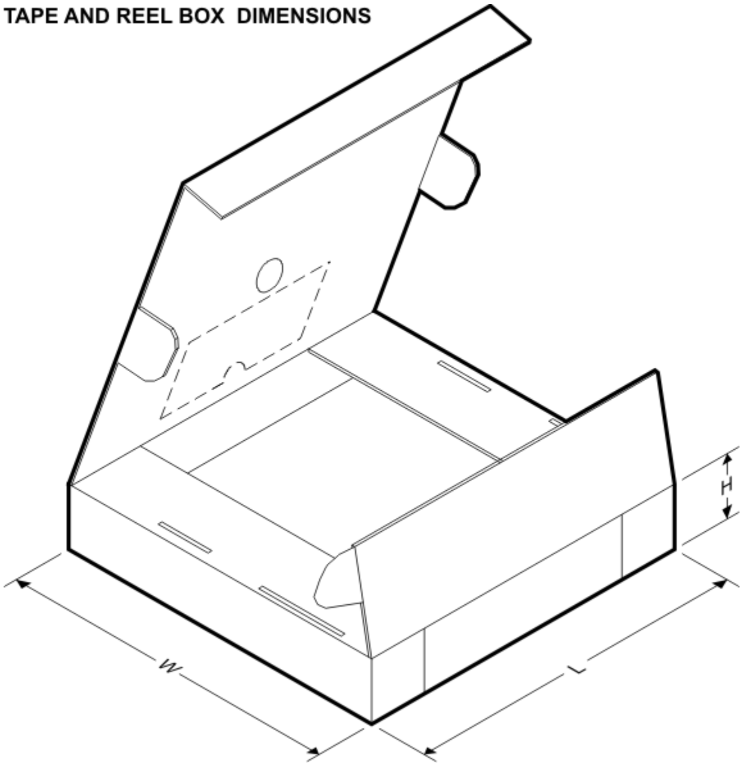
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54200DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54200DDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54201DDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS54201DDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

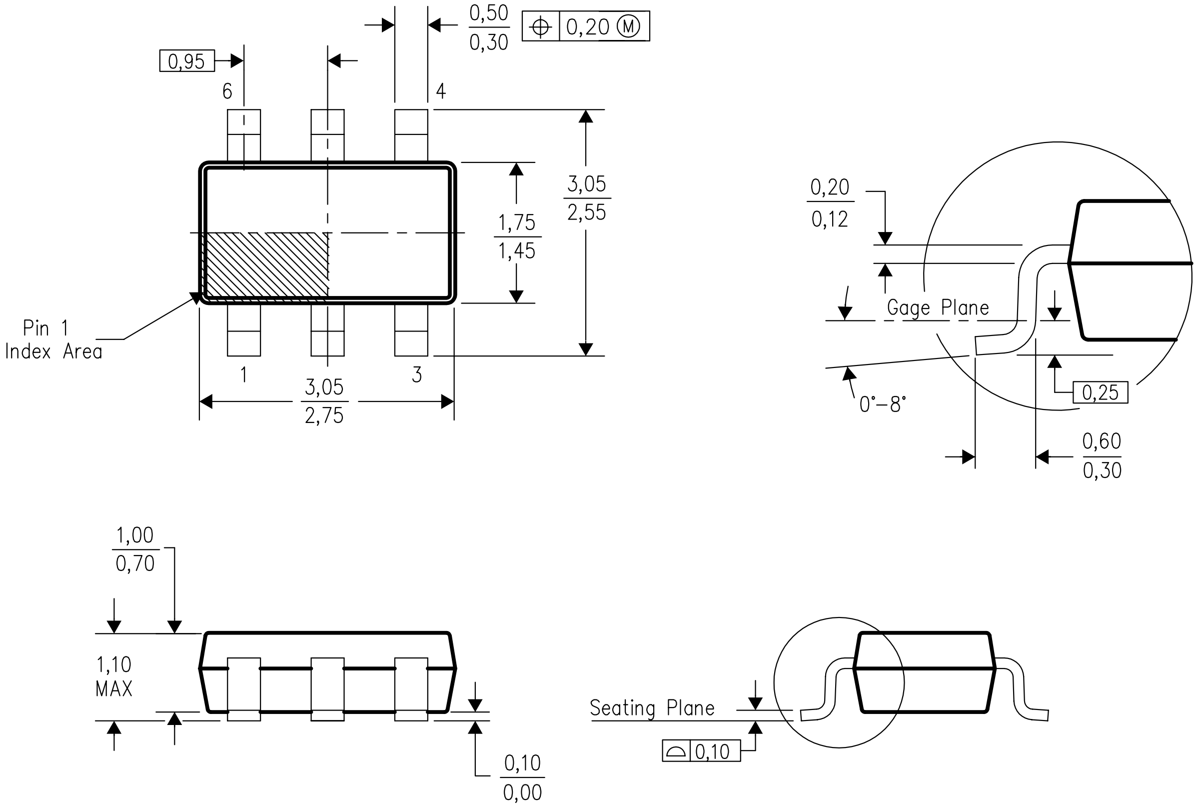
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54200DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS54200DDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0
TPS54201DDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TPS54201DDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–193 variation AA (6 pin).

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