TPS53622 Dual-Channel (1-Phase + 1-Phase) or (2-Phase + 0-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™ for VR13 Server V_{CCIO} + V_{MCP}

1 Device Overview

1.1 Features

- Intel VR13 Serial VID (SVID) Compliant
- Full VR13 Server Feature Set Including Digital Input Power Monitor
- Programmable Loop Compensations
- Configurable with Non-Volatile Memory (NVM) for Low External Component Counts
- Individual Phase Current Calibrations and Reports
- Dynamic Phase Shedding with Programmable Current Threshold for Optimizing Efficiency at Light and Heavy Loads
- Fast Phase-Adding for Undershoot Reduction (USR)
- Backward VR12.0 and VR12.5 Compatible
- 8-Bit DAC with Selectable 5 mV or 10 mV Resolution and Output Ranges from 0.25 V to 1.52 V or 0.5 to 2.8125 V for Dual Channels
- Driverless Configuration for Efficient High-Frequency Switching
- Fully Compatible with TI NextFET™ Power Stage for High-Density Solutions
- Accurate, Adjustable Voltage Positioning
- 16 Individual Frequency Selections
- Patented AutoBalance™ Phase Balancing
- Selectable, 16-level Per-Phase Current Limit
- PMBus™ System Interface for Telemetry of Voltage, Current, Power, Temperature, and Fault Conditions
- Dynamic Output Voltage Transitions with Programmable Slew Rates via SVID or PMBus Interface
- Conversion Voltage Range: 4.5 V to 17 V
- Low Quiescent Current
- 5 mm × 5 mm, 40-Pin, QFN PowerPad™ Package

1.2 Applications

- VR13 CPU V_{CCIO} + V_{MCP} of Server Applications
- ASIC Needs Dual Power Rails
- High-Performance Processor Power

1.3 Description

The TPS53622 is a fully VR13 SVID compliant step-down controller with dual channels, built-in non-volatile memory (NVM), and PMBus™ interface, and is fully compatible with TI NexFET ™power stage. Advanced control features such as D-CAP+™ architecture with undershoot reduction (USR) provide fast transient response, low output capacitance, and good current sharing. The device also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at different loads. Adjustable control of V_{CORE} slew rate and voltage positioning round out the Intel® VR13™ features. In addition, the device supports the PMBus communication interface for reporting the telemetry of voltage, current, power, temperature, and fault conditions to the systems. All programmable parameters can be configured by the PMBus interface and can be stored in NVM as the new default values to minimize the external component count.

The TPS53622 device if offered in a thermally enhanced 40-pin QFN packaged and is rated to operate from –40°C to 125°C.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TPS53622	QFN (40)	5 mm × 5 mm

(1) For more information, see, *Mechanical, Packaging, and Orderable Information*.

2 Device and Documentation Support

2.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

2.3 Trademarks

NextFET, AutoBalance, PowerPad, PMBus, NexFET, D-CAP+, E2E are trademarks of Texas Instruments.
VR13 is a trademark of Intel.
Intel is a registered trademark of Intel.
PMBus is a trademark of SMIF, Inc..

2.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

2.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

3 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53622RSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53622	Samples
TPS53622RSBT	ACTIVE	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TPS 53622	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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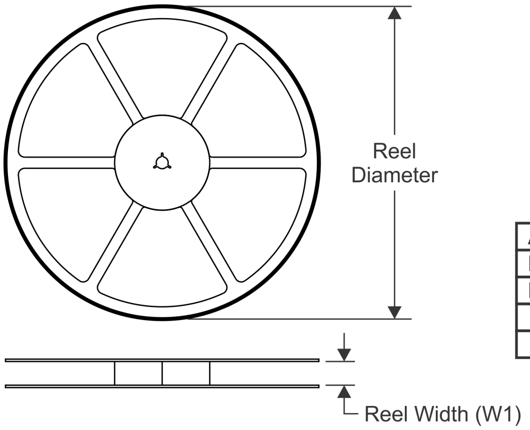
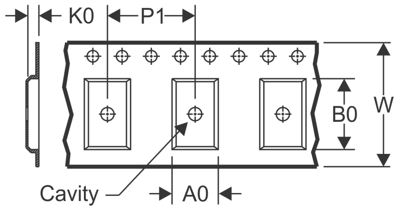
TAPE AND REEL INFORMATION

REEL DIMENSIONS

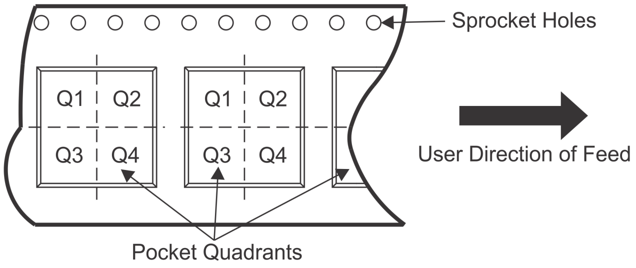


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

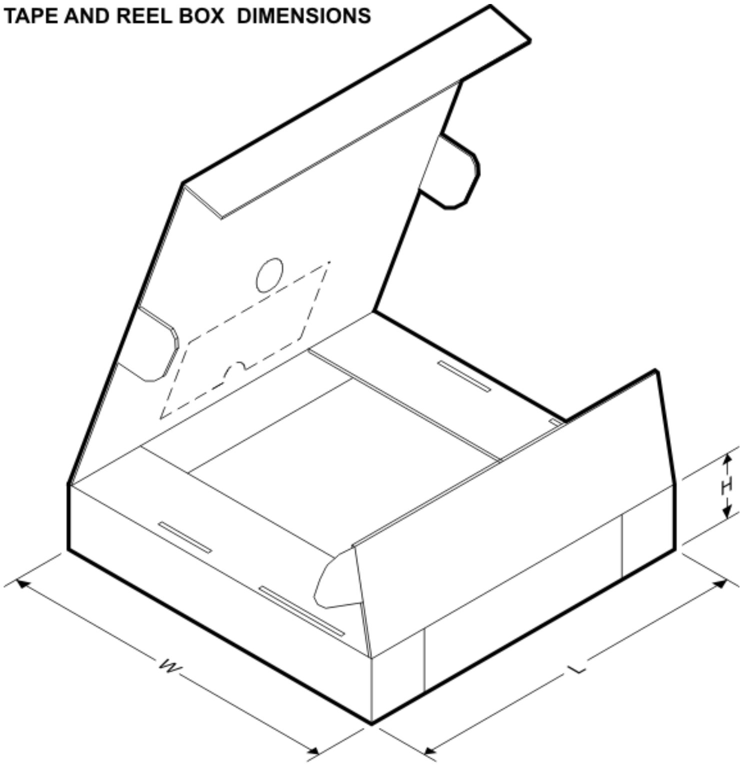
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53622RSBR	WQFN	RSB	40	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS53622RSBT	WQFN	RSB	40	250	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

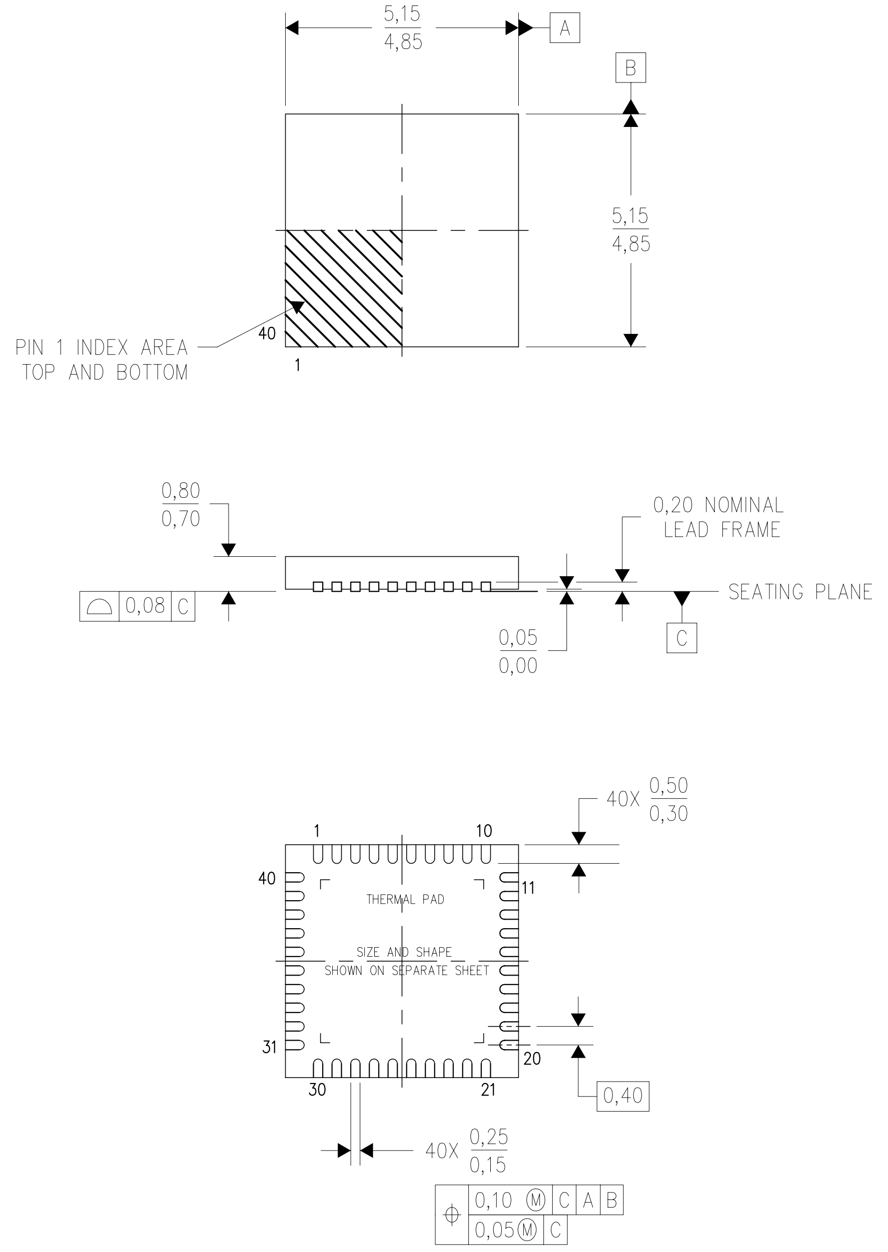
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53622RSBR	WQFN	RSB	40	3000	338.0	355.0	50.0
TPS53622RSBT	WQFN	RSB	40	250	338.0	355.0	50.0

RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

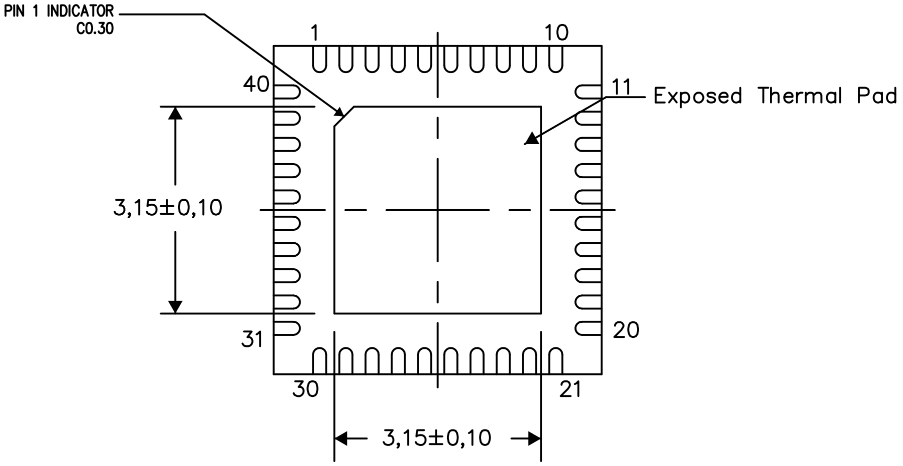
RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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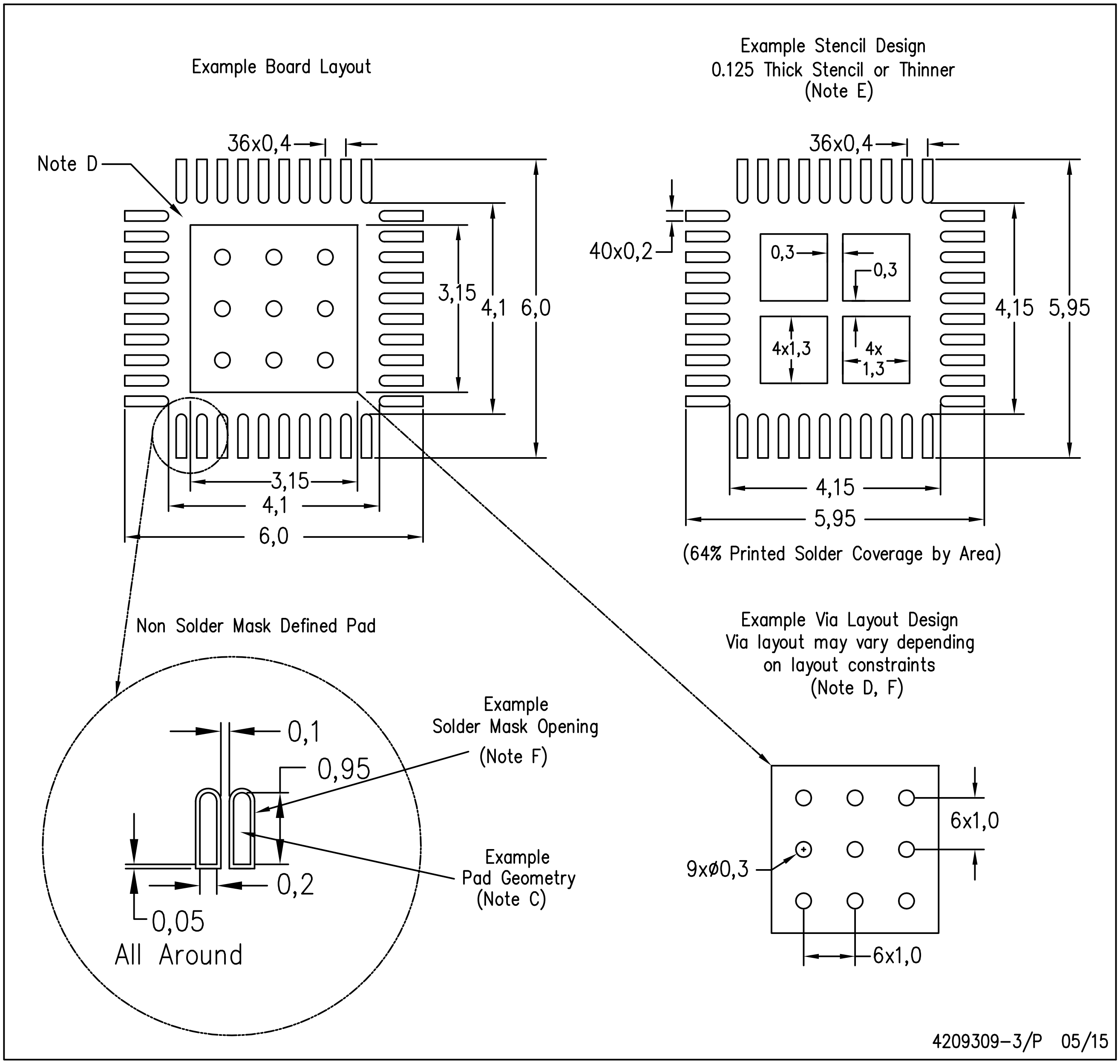
NOTE: All linear dimensions are in millimeters

RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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