6-A Step-Down Regulator with Integrated Switcher

Check for Samples: TPS53313

FEATURES

- **4.5-V to 16-V Conversion Voltage Range**
- **Adjustable Output Voltage Ranging from 0.6 V to 0.7×V_{IN}**
- **Continuous 6-A Output Current**
- **Supports All MLCC Output Capacitors**
- **Selectable SKIP Mode or Forced CCM**
- **Selectable Soft-Start Time (1 ms, 3 ms, or 6 ms)**
- **Selectable 4-5 A, 6-A or 9-A Peak Current Limit**
- **Optimized Efficiency at Light and Heavy Loads**
- **Voltage Mode Control**
- **Programmable Switching Frequency from 250 kHz to 1.5 MHz**
- **Synchronizes to External Clock**
- **$R_{DS(on)}$ Sensing for Zero Crossing Detection and Overcurrent Protection**
- **Soft-Stop Output Discharge During Disable**
- **Overcurrent, Overvoltage and Undervoltage Protection with Hiccup**
- **Over-Temperature Protection**
- **Open-Drain, Power Good Indication**
- **Internal Bootstrap Switch**
- **4 mm × 4 mm, 24-Pin, QFN Package**

LOW VOLTAGE APPLICATIONS

- **POL Applications for 5-V or 12-V Step-Down Rail**

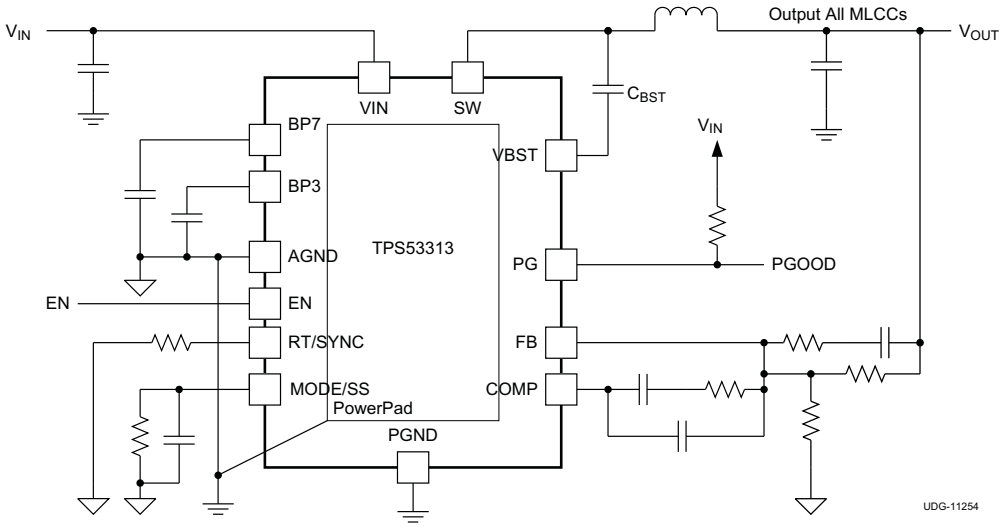
DESCRIPTION

TPS53313 provides a 5-V or 12-V synchronous buck converter that integrates two N-Channel MOSFETs. Due to low $R_{DS(on)}$ and TI proprietary SmoothPWM™ skip mode of operation, it optimizes the efficiency at light-load condition without compromising the output voltage ripple.

The TPS53313 features programmable (from 250 kHz to 1.5MHz) switching frequency with selectable skip mode or forced CCM mode operation. The device provides pre-biased startup, soft-stop, integrated bootstrap switch, power good function, EN/input UVLO protection. It supports input voltages from 4.5 V to 16 V and no extra bias voltage is needed. The output voltage is adjustable from 0.6 V up to 0.7 × V_{IN}.

The TPS53313 is available in a 4 mm × 4 mm, 24-pin, QFN package (Green RoHs compliant and Pb free) and operates between -40°C and 85°C.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SmoothPWM is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
Plastic QFN (RGE)	–40°C to 85°C	TPS53313RGER	24	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53313RGET	24	Mini reel	250	

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Over operating free air-temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Input voltage range	VIN		–0.3	20.0	V
	VBST		–0.3	27.0	
	VBST to SW		–0.3	7.0	
	SW (bidirectional)	DC	–2	20	
		transient < 20 ns	–3	20	
	EN	V_{VIN} ≥ 17	–0.3	17.0	
		V_{VIN} < 17	–0.3	V_{VIN}+0.1	
	FB, MODE/SS		–0.3	3.6	
Output voltage range	COMP, RT/SYNC, BP3		–0.3	3.6	V
	BP7		–0.3	7.0	
	PGD		–0.3	17.0	
Output Current				6	A
Ground Pins	GND		–0.3	0.3	V
Electrostatic Discharge	Human Body Model (HBM)			2000	V
	Charged Device Model (CDM)			500	
Storage temperature, T_{stg}			–55	150	°C
Operating temperature, T_J			–40	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				300	C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding LL terminal.

RECOMMENDED OPERATING CONDITIONS(1)(2)

			VALUE		UNIT
			MIN	MAX	
Input voltage range	VIN (main supply)		4.5	16.0	V
	VBST		–0.1	22.0	
	VBST to SW		–0.1	6.5	
	SW (bidirectional)	dc	–1	18	
		transient < 20 ns	–2	18	
	EN		–0.1	V_{VIN} + 0.1	
	FB, MODE/SS		–0.1	3.5	
Output voltage range	COMP, RT/SYNC, BP3		–0.1	3.5	V
	BP7		–0.1	6.5	
	PGD		–0.1	14	
Ground	GND		–0.1	0.1	
Junction temperature range, T_J			–40	125	°C
Ambient temperature range, T_A			–40	85	°C

(1) Voltage values are with respect to the corresponding LL terminal.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53313	UNITS
		RGE (24) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	44.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	35.0	
θ_{JB}	Junction-to-board thermal resistance	19.0	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	8.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VIN} = 12 V, PGND = GND (Unless otherwise noted (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN}	VIN supply voltage	Nominal input voltage range	4.5		16.0	V
V_{POR}	VIN POR threshold	Ramp up; EN =HIGH	4.00	4.23	4.40	V
$V_{POR(hys)}$	VIN POR hysteresis			200		mV
I_{STBY}	Standby current	EN =LOW. V_{IN} = 12 V		58		µA
R_{BOOT}	Bootstrap on-resistance			10		Ω
REFERENCE						
V_{VREF}	Internal precision reference voltage			0.6		V
TOL_{VREF}	VREF tolerance		–1%		1%	
ERROR AMPLIFIER						
UGBW(1)	Unity gain bandwidth		14			MHz
A_{OL}(1)	Open loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin		50		nA
$I_{EA(max)}$	Output sinking and sourcing current			5		mA
SR(1)	Slew rate			5		V/µs
ENABLE						
R_{ENPD}(1)	Enable pull-down resistor			800		kΩ
V_{ENH}	EN logic high	V_{VIN} = 4.5 V	1.8			V
V_{ENHYS}	EN hysteresis	V_{VIN} = 4.5 V			0.6	V
I_{EN}	EN pin current	V_{EN} = 0 V			1	µA
		V_{EN} = 3.3V		3.3	5.0	
		V_{EN} = 14 V		17.8	27.5	
SOFT-START						
t_{SS_1}	Delay after EN asserts	EN = High		0.65		ms
t_{SS_2}	Soft start ramp_up time	0 V ≤ V_{SS} ≤ 0.6 V, 39-kΩ or no resistor to MODE/SS pin		1		ms
		0 V ≤ V_{SS} ≤ 0.6 V, 20-kΩ or 160-kΩ resistor to MODE/SS pin		3		
		0 V ≤ V_{SS} ≤ 0.6 V, 10-kΩ or 82-kΩ resistor to MODE/SS pin		6		
$t_{PGDENDLY}$	PGD startup delay time	V_{SS} = 0.6 V to PGD (SSOK) going high, t_{SS} = 1 ms		0.2		ms
RAMP						
	Ramp amplitude	4.5 V ≤ V_{VIN} ≤ 14.4 V		V_{VIN}/9		V
		14.4 V ≤ V_{VIN} ≤ 16 V		1.6		
PWM						
$t_{MIN(off)}$	Minimum OFF-time	f_{SW} = 1 MHz		150		ns
$t_{MIN(on)}$	Minimum ON-time	No load			90	ns
D_{MAX}	Maximum duty cycle	f_{SW} = 1 MHz		80%		
SWITCHING FREQUENCY						
f_{SW}	Switching frequency tolerance	f_{SW} = 1 MHz, R_T = 45.3 kΩ	–10%		10%	
SOFT DISCHARGE						
R_{SFTDIS}	Soft-discharge transistor resistance	EN = Low, V_{IN} = 4.5 V, V_{OUT} = 0.6 V		120		Ω

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

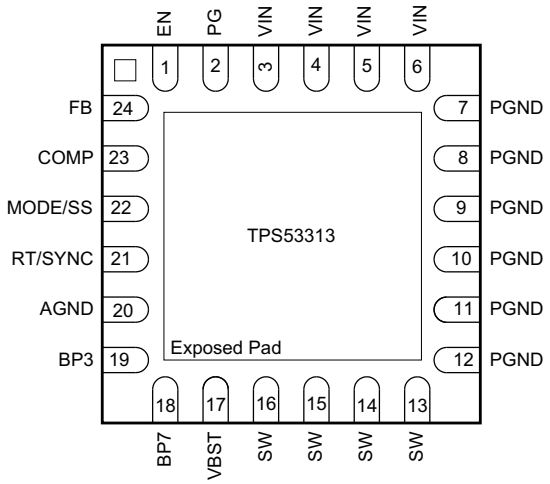
over operating free-air temperature range, V_{VIN} = 12 V, PGND = GND (Unless otherwise noted (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OVERCURRENT AND ZERO CROSSING						
I_{OCPL}	Overcurrent limit on high-side FET (peak)	When I_{OUT} exceeds this threshold for 4 consecutive cycles, 2.2-nF capacitor to MODE/SS pin		4.5		A
		When I_{OUT} exceeds this threshold for 4 consecutive cycles, no capacitor to MODE/SS pin		6		A
		When I_{OUT} exceeds this threshold for 4 consecutive cycles, 10-nF capacitor to MODE/SS pin		9		
I_{OCPH}	One time overcurrent shut-off on the low-side FET (peak)	Immediately shut down when sensed current reach this value, 2.2-nF capacitor to MODE/SS pin		4.5		A
		Immediately shut down when sensed current reach this value, no capacitor to MODE/SS pin		6		A
		Immediately shut down when sensed current reach this value, 10-nF capacitor to MODE/SS pin		9		
V_{ZXOFF}	Zero crossing comparator internal offset	SW – PGND, SKIP mode		–3		mV
POWER GOOD						
V_{PGDL}	Power good low threshold	Measured at the FB pin w/r/t VREF	80%	83%	86%	
V_{PGDH}	Power good high threshold	Measured at the FB pin w/r/t VREF	114%	117%	120%	
$V_{PG(hys)}$	Power good hysteresis			2		
$V_{IN(min\_pg)}$	Minimum Vin voltage for valid PG at startup.	Measured at V_{IN} with 1-mA (or 2-mA) sink current on PG pin at startup			1	V
$V_{PG(pd)}$	Power good pull-down voltage	Pull down voltage with 4-mA sink current		0.2	0.4	V
$I_{PG(leak)}$	Power good leakage current	Hi-Z leakage current, apply 3.3-V in off state		12.0	16.2	µA
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
T_{OVPDLY}	Overvoltage protection delay time	Time from FB out of +17% of VREF to OVP fault		2		µs
T_{UVPDLY}	Undervoltage protection delay time	Time from FB out of -17% of VREF to UVP fault		10		µs
THERMAL SHUTDOWN						
THSD(2)	Thermal shutdown	Shut-down controller, attempt soft-stop	130	140	150	°C
$THSD_{HYST}$(2)	Thermal shutdown hysteresis	Controller re-starts after temperature drops		40		°C

(2) Ensured by design. Not production tested.

DEVICE INFORMATION

RGE (QFN) PACKAGE
24 PINS
(BOTTOM VIEW)

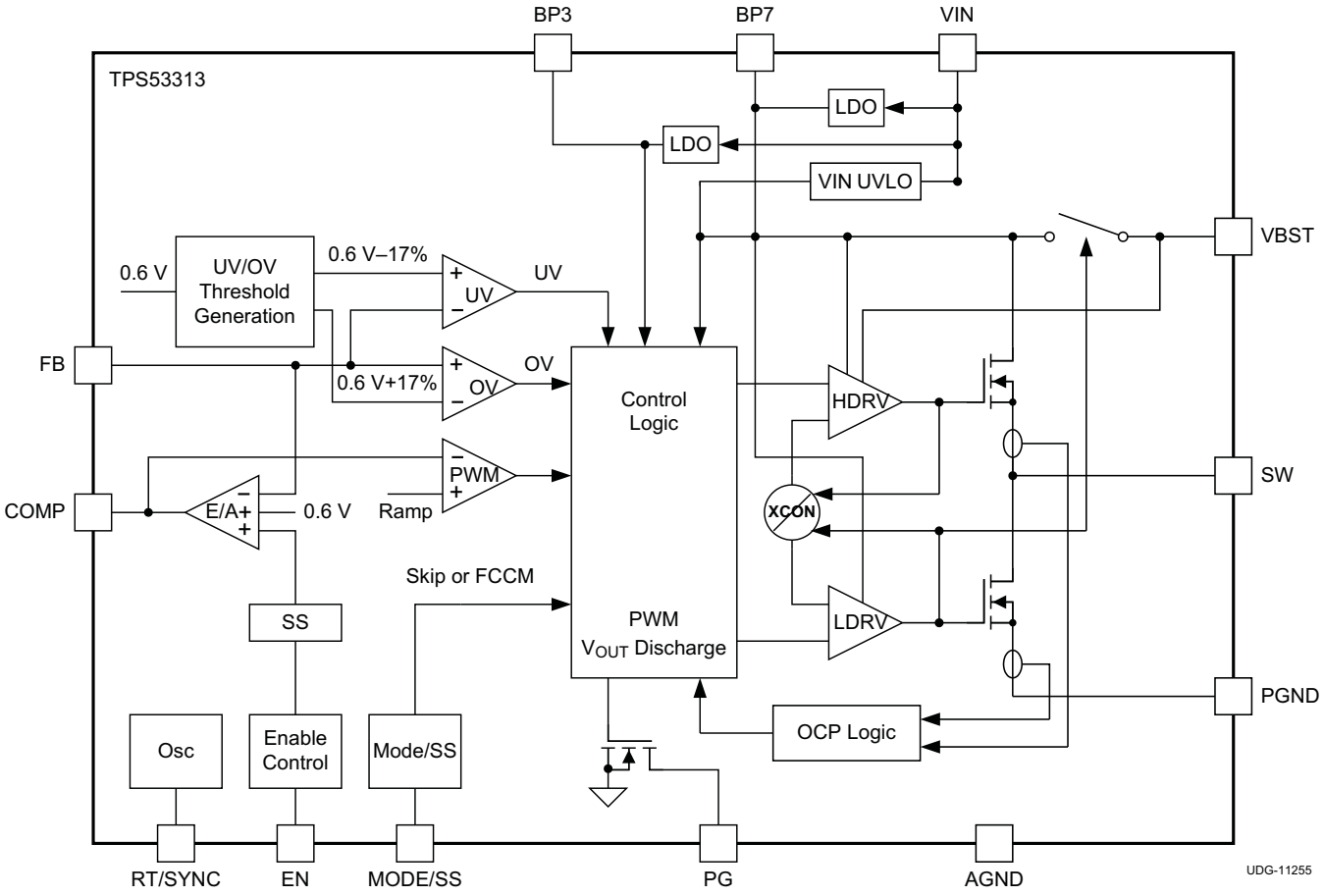


PIN DESCRIPTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	20	G	Device analog ground terminal
BP3	19	P	Input bias supply for analog functions
BP7	18	P	Bias for internal circuitry and driver
COMP	23	O	Error amplifier compensation terminal. Type III compensation method is generally recommended for stability.
EN	1	I	Enable pin.
FB	24	I	Voltage feedback pin. Use for OVP, UVP and power good determination
PG	2	O	Power good output flag. Open drain output. Pull up to an external rail via a resistor
PGND	7	P	Device power ground terminal
	8		
	9		
	10		
	11		
	12		
MODE/SS	22	I	Mode configuration pin. Connect with a resistor to GND sets different modes and soft-start time, parallel a capacitor (or no capacitor) with the resistor changes the current limit threshold. See Table 1 and Table 2 for resistor and capacitor settings. (shorting MODE/SS pin to supply inhibits the device. Shorting MODE/SS pin to AGND is equivalent to 10-kΩ resistor setting—*not recommended*)
RT/SYNC	21	I/O	Synchronized to external clock. Program the switching frequency by connecting with a resistor to GND.
SW	13	O	Output inductor connection to integrated power devices
	14		
	15		
	16		
VBST	4	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal
VIN	3	P	Gate driver supply and power conversion voltage.
	4		
	5		
	6		

(1) I – Input; B – Bidirectional; O – Output; G – Ground; P – Supply (or Ground)

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

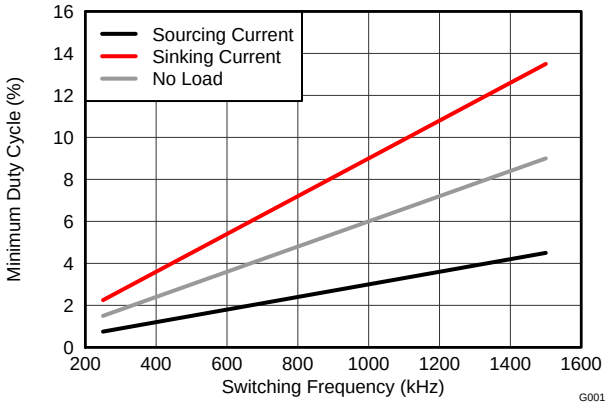


Figure 1. Ensured Minimum Duty Ratio

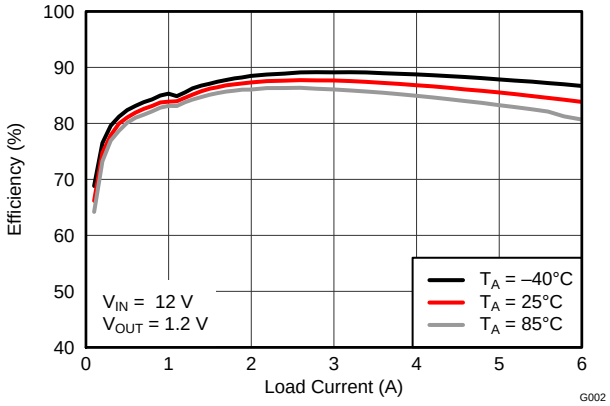


Figure 2. Efficiency, V_{IN} = 12 V

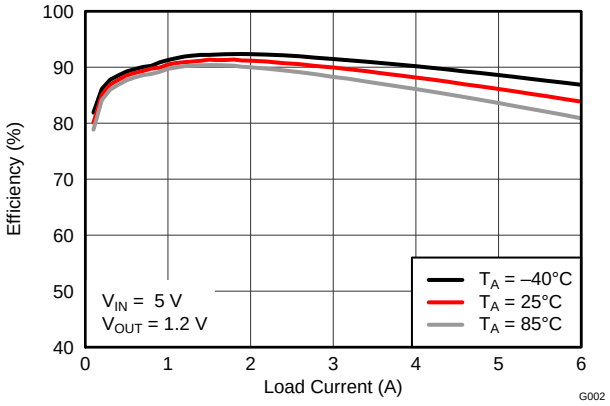


Figure 3. Efficiency, V_{IN} = 5 V

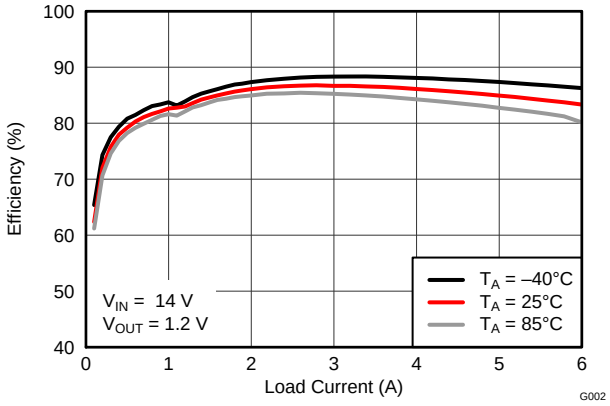


Figure 4. Efficiency, V_{IN} = 14 V

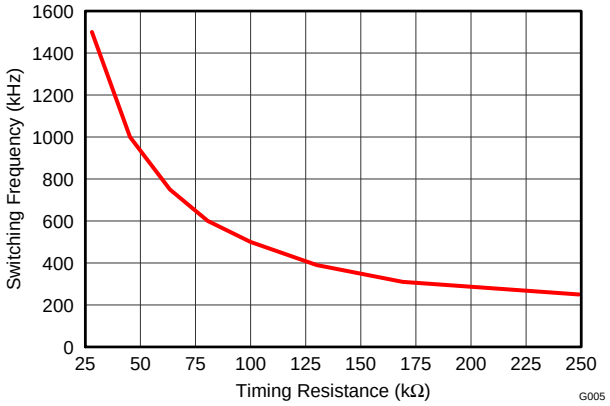


Figure 5. Switching Frequency vs. Timing Resistance (R_T)

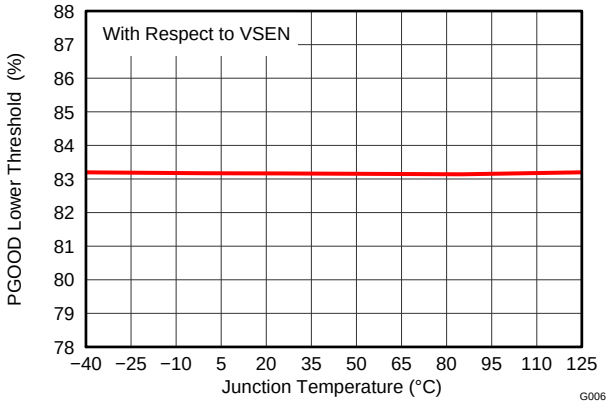


Figure 6. PGOOD Lower Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

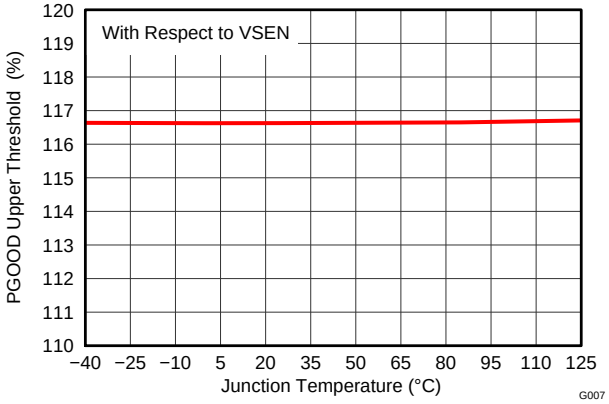


Figure 7. PGOOD Upper Threshold vs. Junction Temperature

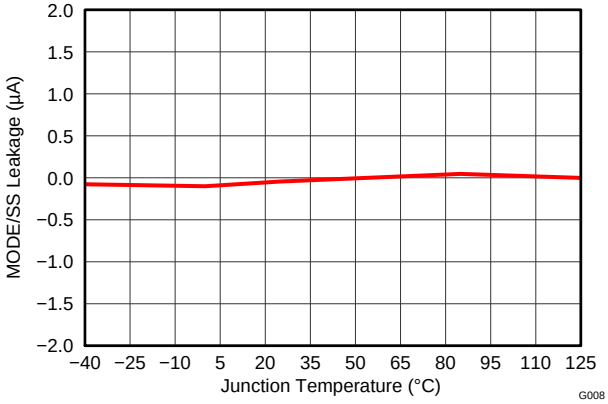


Figure 8. MODE/SS Leakage Current vs. Junction Temperature

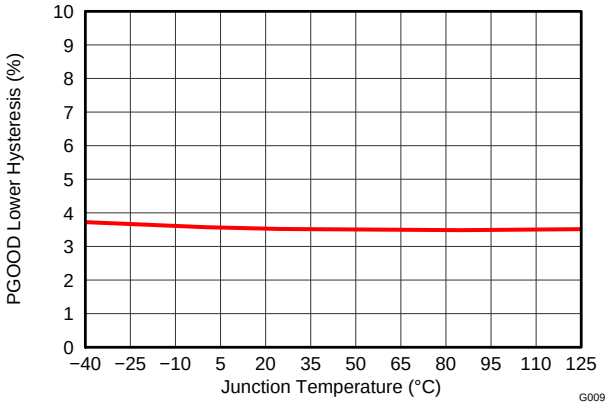


Figure 9. PGOOD Lower Hysteresis vs. Junction Temperature

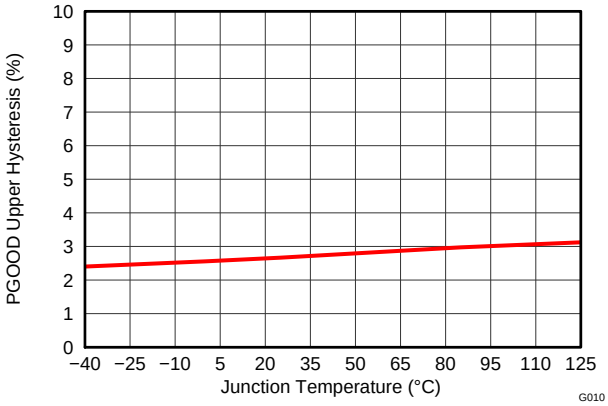


Figure 10. PGOOD Upper Hysteresis vs. Junction Temperature

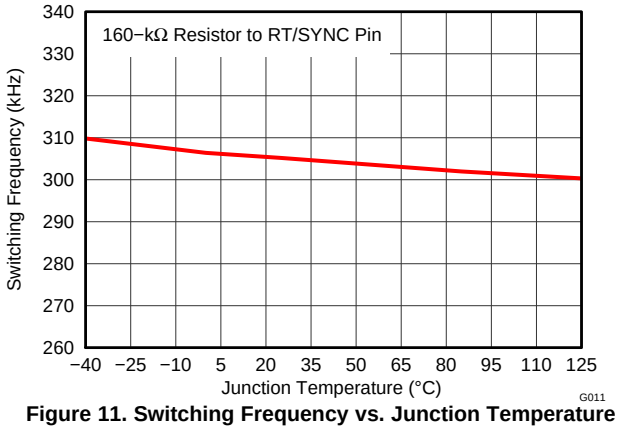


Figure 11. Switching Frequency vs. Junction Temperature

DETAILED DESCRIPTIONS

OVERVIEW

The TPS53313 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 6 A of load current. The TPS53316 provides output voltage from 0.6 V up to 0.7 × V_{IN} from 4.5V to 16 V wide input voltage range. The output voltage accuracy is better than ±1% over load, line, and temperature.

This device can operate in either forced continuous conduction mode (FCCM) or skip mode with selectable soft-start time to fit various application needs. Skip mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

OPERATION MODE

The TPS53313 has 6 operation modes determined by the MODE/SS pin connection as listed in Table 1. The current limit thresholds and associated capacitance selections are shown in Table 2 .

Table 1. Operation Mode Selection

MODE/SS PIN CONNECTION	OPERATION MODE	t_{SS} SOFT-START TIME (ms)
10 kΩ to GND	FCCM	6
20 kΩ to GND	FCCM	3
39 kΩ to GND	FCCM	1
82 kΩ to GND	Skip Mode	6
160 kΩ to GND	Skip Mode	3
Floating	Skip Mode	1

Table 2. Capacitor Selection

MODE/SS PIN SETTING (nF)	CURRENT LIMIT THRESHOLD (A)
No Capacitor	6
2.2	4.5
10	9

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In this mode, the switching frequency remains constant over the entire load range which is suitable for applications that need tight control of switching frequency.

In skip mode, the high-side FET is on during the on-time and low-side FET is on during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET. The on-pulse in skip mode is designed to be 25% higher than CCM to provide hysteresis to avoid chattering between CCM and skip mode.

Also, the overcurrent protection threshold can be set to 4.5 A, 6 A or 9 A by changing the capacitor that is in parallel with MODE/SS pin. Specifically, a 6-A current limit threshold is set without an external capacitor, the 4.5 A current limit threshold is set with a 2.2-nF capacitor, and the 9-A current limit threshold is set when a 10-nF capacitor is in parallel with MODE/SS pin.

LIGHT LOAD OPERATION

In skip mode, when the load current is less than half of inductor ripple current, the inductor current reaches zero by the end of OFF-Time. The light load control scheme then turns off the low-side MOSFET when inductor current reaches zero. Since there is no negative inductor current, the energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation. The controller then reduces the switching frequency to maintain the output voltage regulation. The switching loss is reduced and thus efficiency is improved.

In skip mode, when the load current decreases, the switching frequency also decreases continuously in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. It is also required that the difference between V_{VBST} and V_{SW} to be higher than 3.3 V to ensure the supply for high-side gate driver.

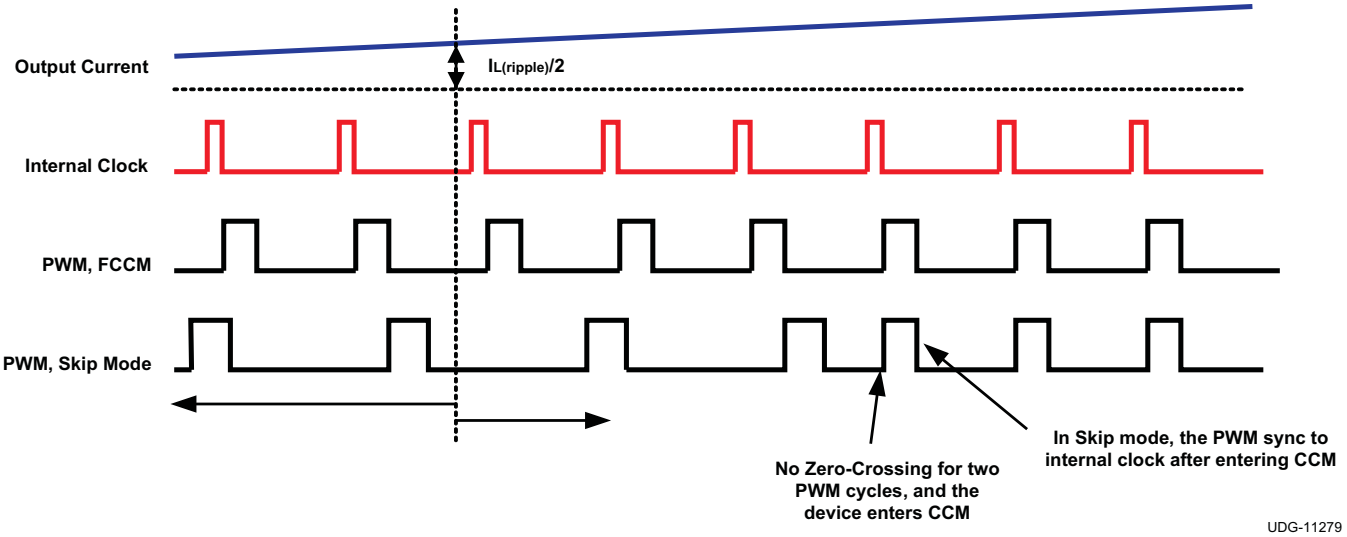


Figure 12. TPS53313 Operation Modes in Light and Heavy Load Conditions

FORCED CONTINUOUS CONDUCTION MODE

When choosing FCCM, the TPS53313 is operating in continuous conduction mode in both light and heavy load condition. In this mode, the switching frequency remains constant over the entire load range which is suitable for applications need tight control of switching frequency at a cost of lower efficiency at light load.

SOFT-START OPERATION

The soft-start operation reduces the inrush current during the start-up time. A slow rising reference is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, a fixed 600-mV reference voltage is used for the error amplifier. The soft-start time has selectable values of 1 ms, 3 ms and 6 ms.

POWER GOOD

The TPS53313 monitors the output voltage through the FB pin. If the FB voltage is within 117% and 83% of the reference voltage, the power good signal remains high. If the FB voltage is outside of this range, the PG pin pin is pulled low by the internal open drain output.

During start up, the power good signal has a 200-µs delay after the FB voltage falls into the power good range limit when the soft-start time is set to 1 ms. There is also 10-µs delay during shut down.

UVLO FUNCTION

The TPS53313 provides UVLO protection for input voltage, VIN. If the input voltage is lower than UVLO threshold voltage minus the hysteresis, the device shut off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 4.23 V. Hysteresis of 200 mV for input voltage is provided to prevent glitch.

OVERCURRENT (OC) PROTECTION

The TPS53313 provides peak current protection and continuously monitors the current flowing through high-side and low-side MOSFETs. If the current through the high-side FET exceeds the current limit threshold, the high-side FET turns off and the low-side FET turns on. An overcurrent (OC) counter starts to increment every switching cycle to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches 4. The OC counter resets if the detected current is less than 6 A (with 6-A OC setting) after an OC event.

Another set of overcurrent circuitry monitors the current through low-side FET. If the current through the low-side FET exceeds 6 A (with 6-A OC setting), the overcurrent protection is engaged and turns off both high-side and low-side FETs immediately.

Therefore, the device is fully protected against overcurrent during both on-time and off-time. Also, the OC threshold is selectable and can be set to 4.5 A, 6 A or 9 A by connecting different capacitor in parallel with MODE/SS pin. After OC events, the device stops switching and enters hiccup mode. A re-start is attempted after a hiccup waiting time. If the fault condition is not cleared, hiccup mode operation may continue indefinitely

OVERVOLTAGE AND UNDERVOLTAGE PROTECTION

The TPS53313 monitors the voltage divided feedback voltage to detect the overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, overvoltage protection is triggered, the high-side MOSFET turns off and the low-side MOSFET turns on. Then the output voltage drops and the FB voltage reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device goes into tri-state logic.

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection counter starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 µs, the device turns off both the high-side and low-side MOSFETs and then goes into tri-state logic.

After the undervoltage events, the device stops switching and enters hiccup mode. A restart is attempted after a hiccup waiting time. If the fault condition is not cleared, hiccup mode operation may continue indefinitely.

OVERTEMPERATURE PROTECTION

The TPS53313 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device is cooled to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

OUTPUT DISCHARGE

When the EN pin is low, the TPS53313 discharges the output capacitors through an internal MOSFET switch between SW and GND while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge switch on resistance is 120 Ω. This function is disabled when V_{VIN} is less than 1 V.

SWITCHING FREQUENCY SETTING AND SYNCHRONIZATION

The clock frequency is programmed by the value of the resistor connected from the RT/SYNC pin to GND. The switching frequency is programmable between 250 kHz and 1.5 MHz.

Also, TPS53313 is able to synchronize to external clock. The synchronization is fulfilled by connecting the RT/SYNC pin to external clock source. If no external pulse is received from RT/SYNC pin, the device continues to operate the internal clock.

APPLICATION INFORMATION

DESIGN EXAMPLE

The following example illustrates the design process and component selection for a single-output synchronous buck converter using the TPS53313. The design example schematic of a is shown in Figure 13. The specification of the converter is listed in Table 3.

Table 3. Design Example Converter Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12.0	13.2	V
V_{OUT}	Output voltage			1.2		V
V_{RIPPLE}	Output ripple	I_{OUT} = 6 A		1% of V_{OUT}		V
I_{OUT}	Output current				6	A
f_{SW}	Switching frequency			600		kHz

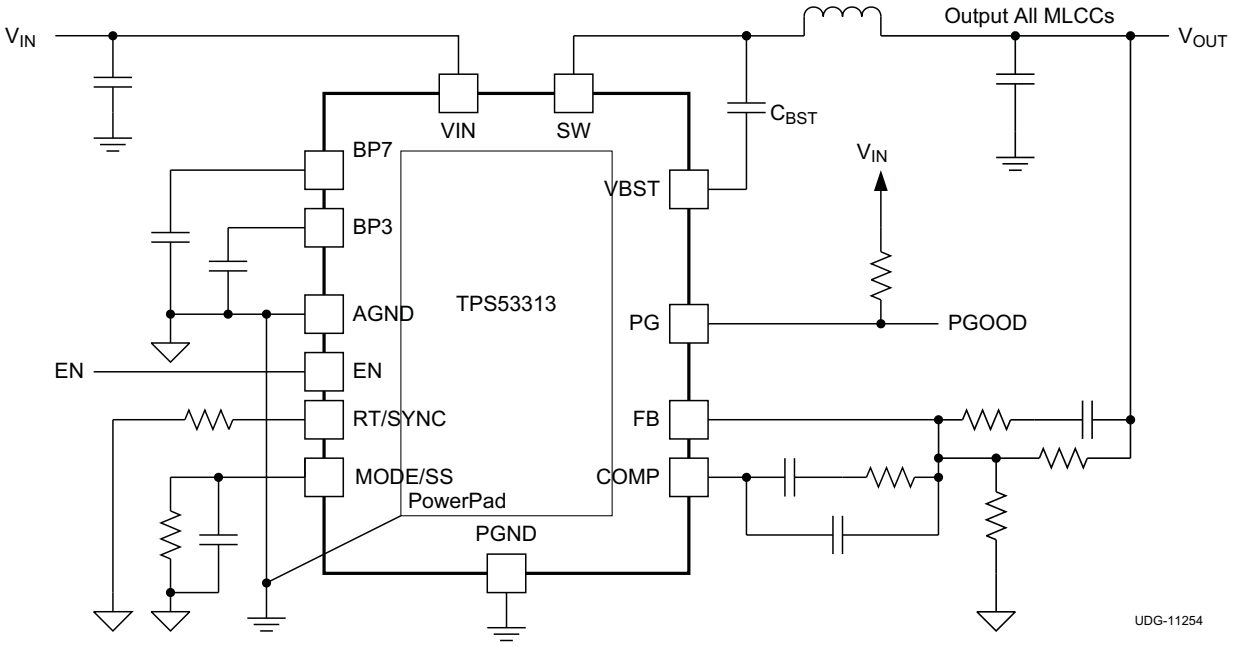


Figure 13. Typical 12-V input Application Circuit Diagram

Output Inductor Selection

The inductance value should be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

The inductor also requires a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

Output Capacitor Selection

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (2)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (3)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (4)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (5)$$

When ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL should be the equivalent of the all output capacitors in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 6.

$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times f_{SW} \times C_{OUT} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient and can be expressed as shown in Equation 7. (6)

$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (7)$$

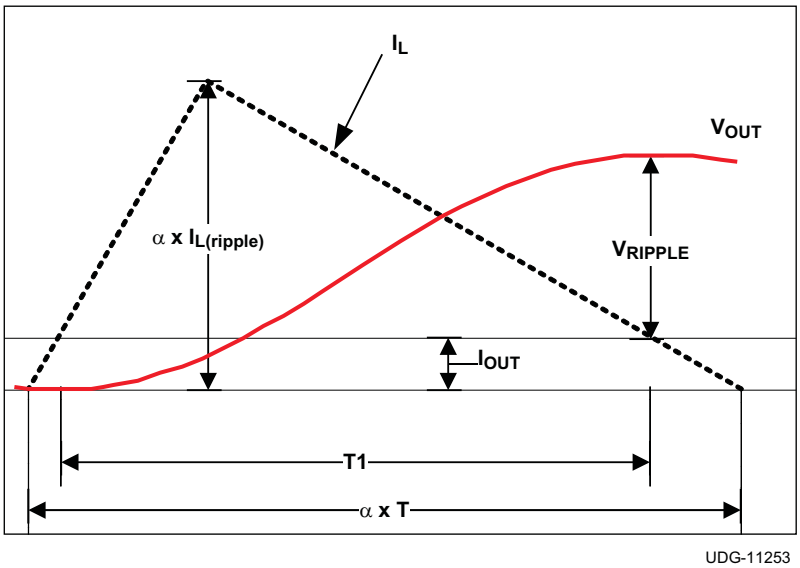


Figure 14. DCM Output Voltage Ripple

Input Capacitor Selection

The selection of input capacitor should be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as shown in Equation 8.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as shown in Equation 9. (8)

$$D = \frac{V_{OUT}}{V_{IN}} \quad (9)$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors should be placed close to the device. The ceramic capacitor is recommended due to its low ESR and low ESL. The input voltage ripple can be calculated as below when the total input capacitance is determined by Equation 10.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \tag{10}$$

Output Voltage Setting Resistors Selection

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Equation 11. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended value for R1 is from 1k to 5k. Determine R2 using .

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \tag{11}$$

Compensation Design

The TPS53313 employs voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \tag{12}$$

The output LC filter introduces a double pole which can be calculated as shown in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \tag{13}$$

The ESR zero of can be calculated as shown in Equation 14.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \tag{14}$$

Figure 15 and Figure 16 shows the configuration of Type III compensation and typical pole and zero locations. Equation 15 through Equation 17 describe the compensator transfer function and poles and zeros of the Type III network.

$$G_{EA} = \frac{(1 + s \times C1 \times (R1 + R3))(1 + s \times R4 \times C2)}{(s \times R1 \times (C2 + C3)) \times (1 + s \times C1 \times R3) \times \left(1 + s \times R4 \frac{C2 \times C3}{C2 + C3}\right)} \tag{15}$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R4 \times C2} \tag{16}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} \cong \frac{1}{2 \times \pi \times R1 \times C1} \tag{17}$$

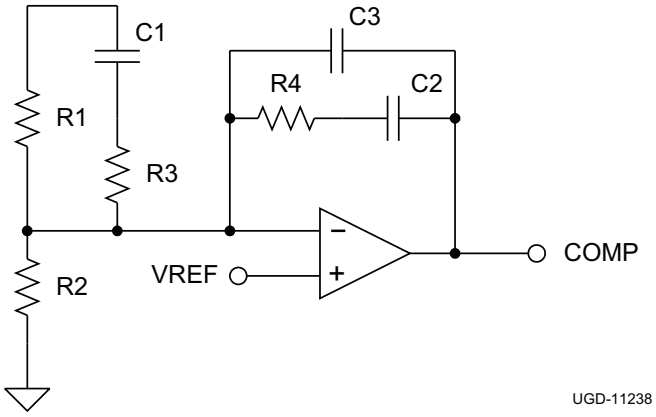


Figure 15. Type III Compensation Network Schematic

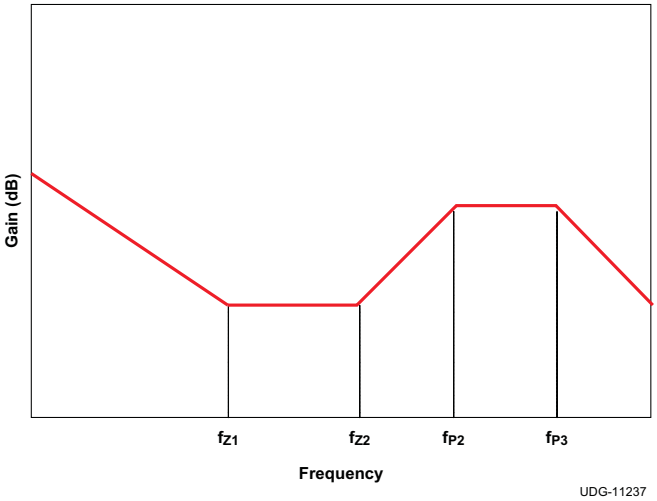


Figure 16. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C1} \quad (19)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R4 \times \left(\frac{C2 \times C3}{C2 + C3} \right)} \cong \frac{1}{2 \times \pi \times R4 \times C3} \quad (20)$$

The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

For DCM operation, a capacitor with a value between 100 pF and 220 pF is recommended for C3 when the output capacitance is between 22 µF and 220 µF.

LAYOUT CONSIDERATIONS

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use 4 vias to connect the thermal pad to power ground.
- Place VIN, BP7 and BP3 decoupling capacitors as close to the device as possible.
- Use wide traces for VIN, PGND and SW. These nodes carry high-current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, VBST).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS53313RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS53313RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

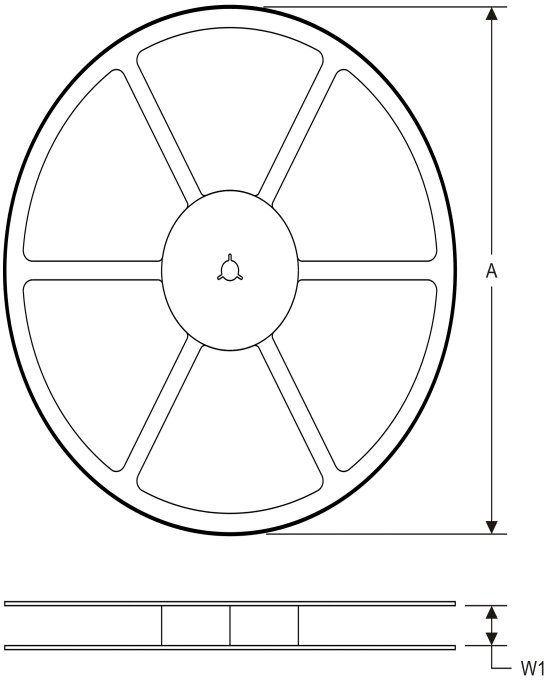
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

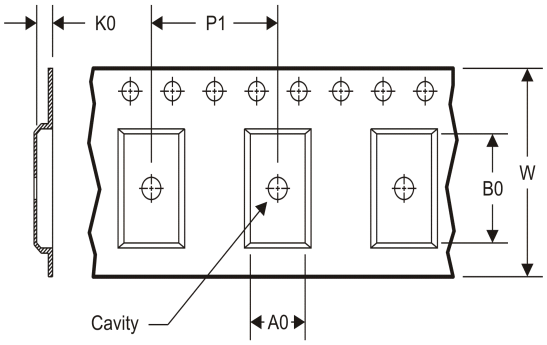
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



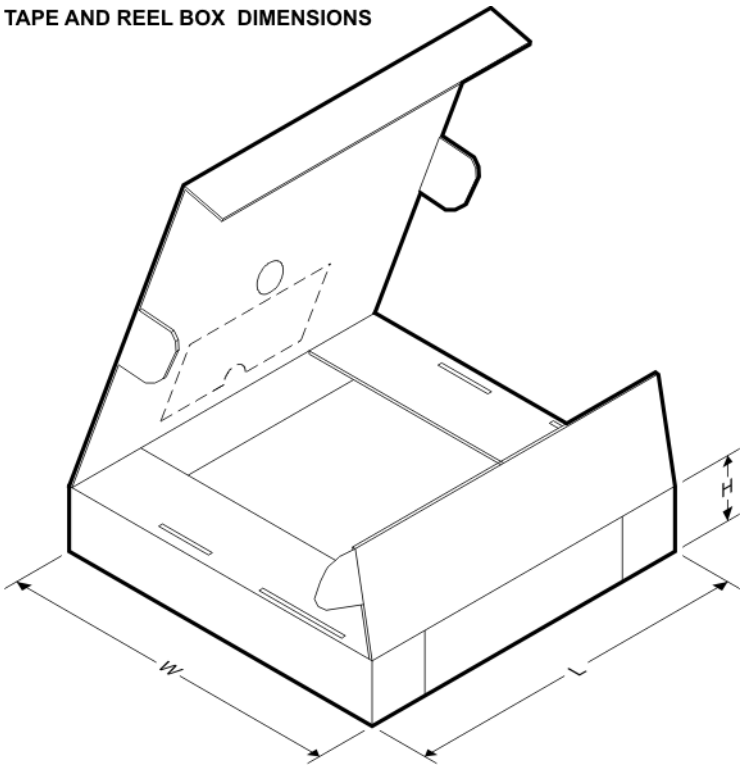
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53313RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53313RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

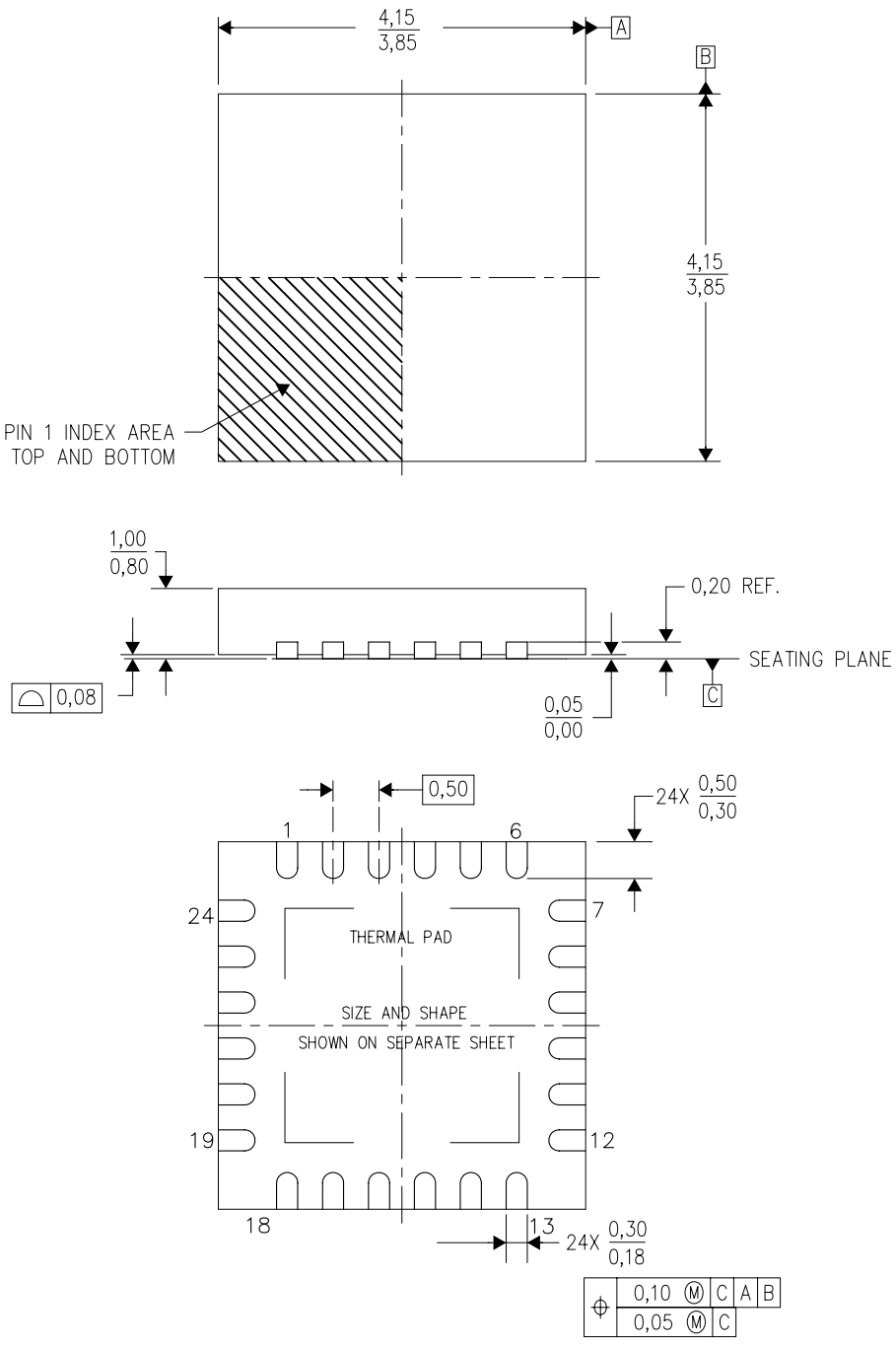
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53313RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS53313RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

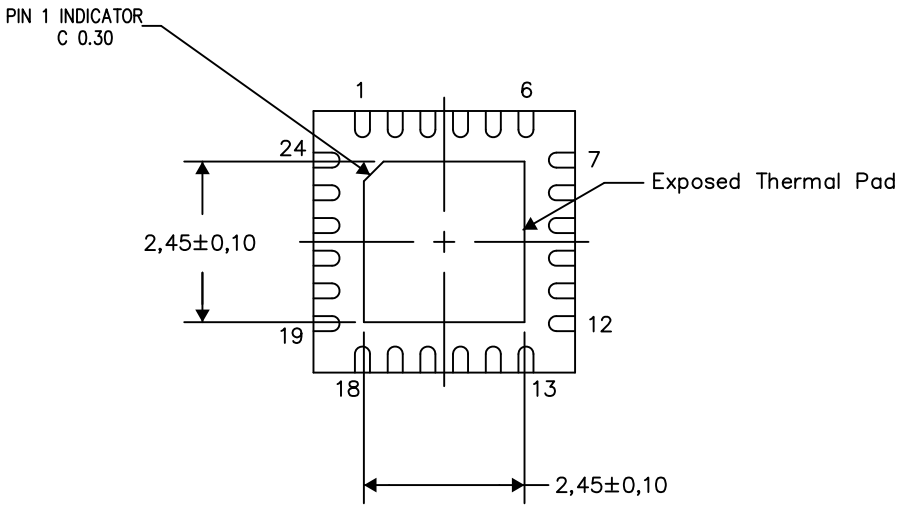
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



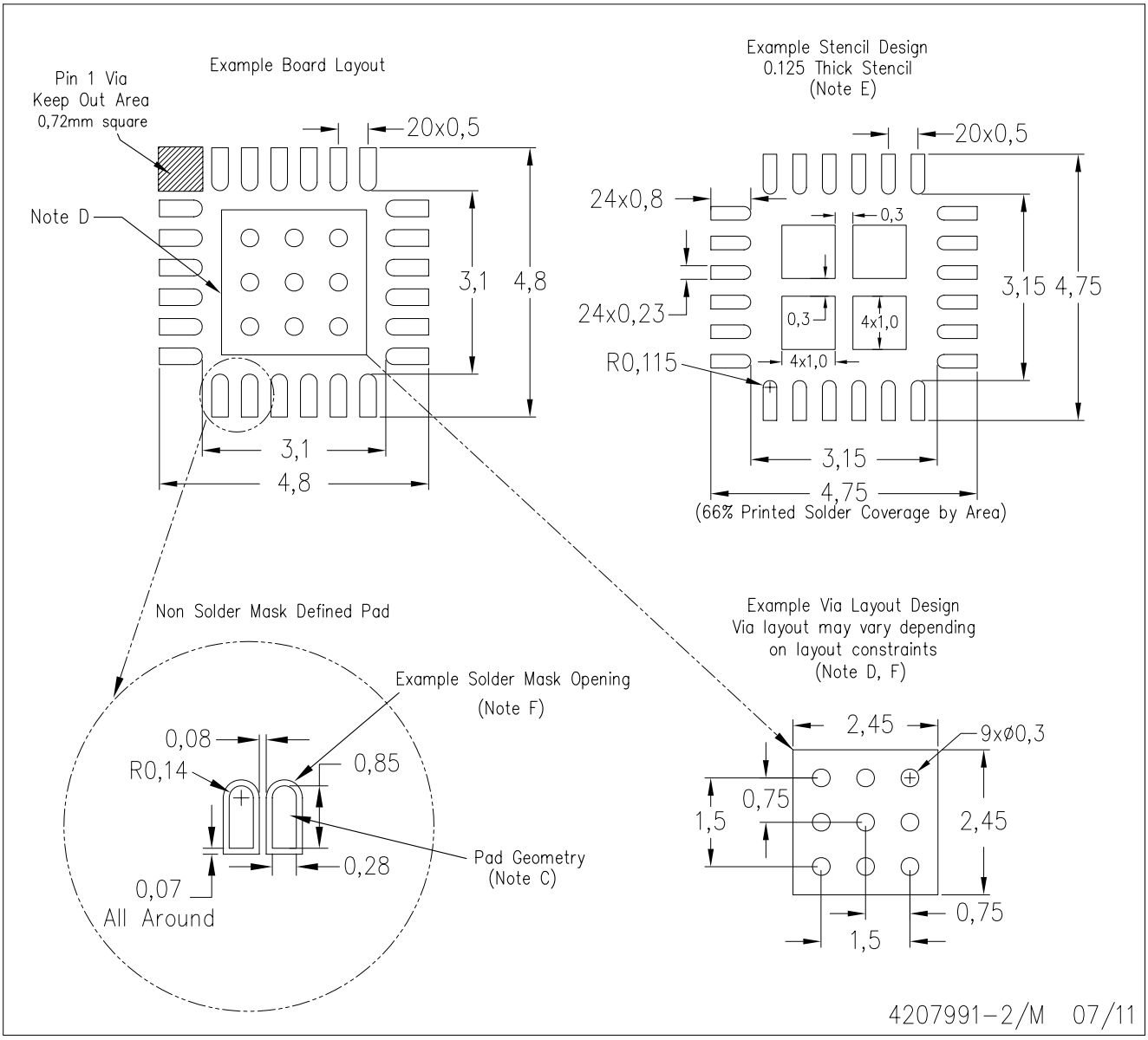
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AA 04/12

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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