3.3-V/5-V Input, D-CAP+™ Mode Synchronous Step-Down Integrated FETs Converter With 2-Bit VID

Check for Samples: TPS51462

FEATURES

- **Integrated FETs Converter w/TI Proprietary D-CAP+™ Mode Architecture**
- **Minimum External Parts Count**
- **Support all MLCC Output Capacitor and SP/POSCAP**
- **Auto Skip Mode**
- **Selectable 700-kHz and 1-MHz Frequency**
- **Small 4 mm × 4 mm, 24-Pin, QFN Package**

APPLICATIONS

- **Low-Voltage Applications Stepping Down from 5-V or 3.3-V Rail**
- **Notebook/Desktop Computers**

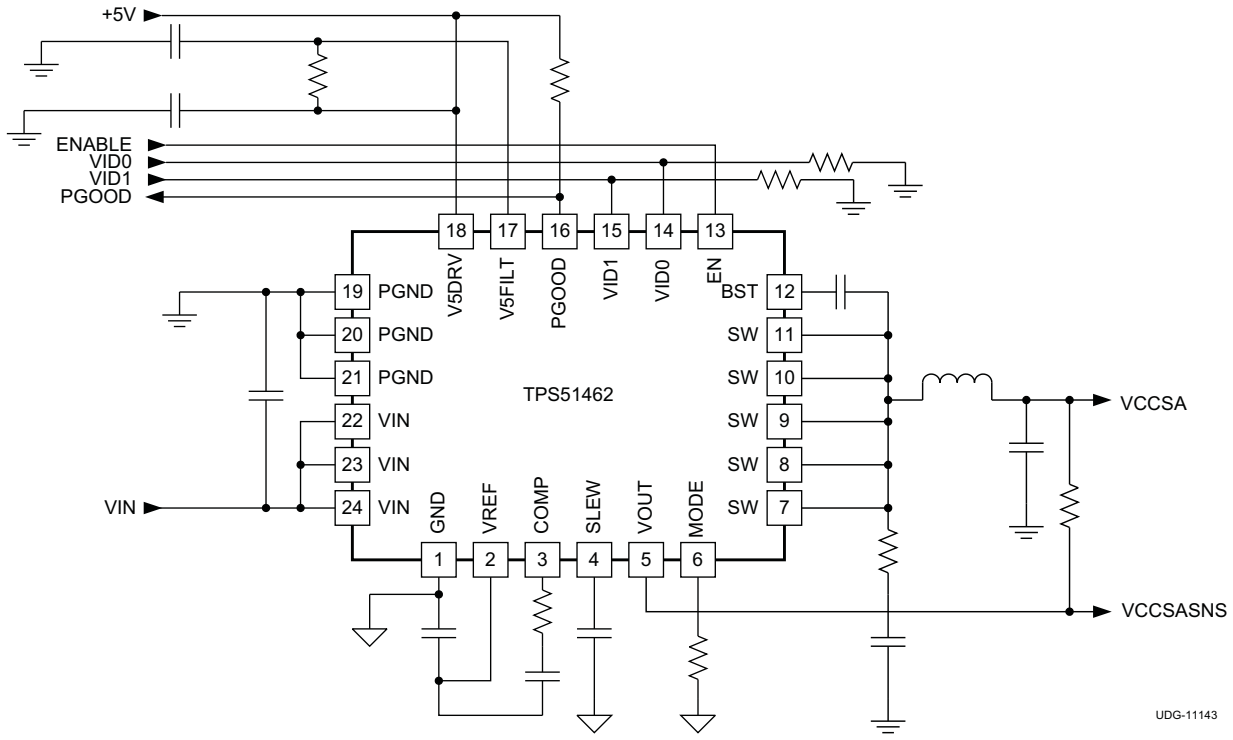
DESCRIPTION

The TPS51462 is a fully integrated synchronous buck regulator employing D-CAP+™. It is used for up to 5-V step-down where system size is at its premium, performance and optimized BOM are must-haves.

This device fully supports Intel system agent applications with integrated 2-bit VID function.

The TPS51462 also features two switching frequency settings (700 kHz and 1 MHz), skip mode, pre-bias startup, programmable external capacitor soft-start time/voltage transition time, output discharge, internal VBST Switch, 2-V reference (±1%), power good and enable.

The TPS51462 is available in a 4 mm × 4 mm, 24-pin, QFN package (Green RoHs compliant and Pb free) and is specified from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP+ is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERING NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
-40°C to 85°C	Plastic QFN (RGE)	TPS51462RGER	24	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS51462RGET	24	Mini reel	250	

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51462 RGE (24) PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	38.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.7	
θ_{JB}	Junction-to-board thermal resistance	16	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	16.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Input voltage range	VIN, EN, MODE	–0.3	7.0	V
	V5DRV, V5FILT, VBST (with respect to SW)	–0.3	7.0	
	VBST	–0.3	12.5	
	VID0, VID1	–0.3	3.6	
	VOUT	–1.0	3.6	
Output voltage range	SW	–2.0	7.0	V
	SW (transient 20 ns and E=5 µJ)	–3.5		
	COMP, SLEW, VREF	–0.3	3.6	
	PGND	–0.3	0.3	
	PGOOD	–0.3	7.0	
Electrostatic Discharge	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	
Storage temperature	T_{stg}	–55	150	°C
Junction temperature	T_J	–40	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		VALUE			UNIT
		MIN	TYP	MAX	
Input voltage range	VIN, EN, MODE	–0.1		6.5	V
	V5DRV, V5FILT, VBST(with respect to SW)	–0.1		5.5	
	VBST	–0.1		11.75	
	VID0, VID1	–0.1		3.5	
	VOUT	–0.8		2.0	
Output voltage range	SW	–0.8		6.5	V
	COMP, SLEW, VREF	–0.1		3.5	
	PGOOD	–0.1		6.5	
	PGND	–0.1		0.1	
Ambient temperature range, T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V_{VIN} = 5.0 V, V_{V5DRV} = V_{V5FILT} = 5 V, MODE = OPEN, PGND = GND (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS AND 5 V UVLO						
I_{VINSD}	VIN shutdown current	EN = 'LO'		0.02	5	µA
V_{5VIN}	5VIN supply voltage	V5DRV and V5FILT voltage range	4.5	5.0	5.5	V
I_{5VIN}	5VIN supply current	EN ='HI', V5DRV + V5FILT supply current		1.6	3.0	mA
I_{5VINSD}	5VIN shutdown current	EN = 'LO', V5DRV + V5FILT shutdown current		10	50	µA
V_{V5UVLO}	V5FILT UVLO	Ramp up; EN = 'HI'	4.2	4.3	4.5	V
$V_{V5UVHYS}$	V5FILT UVLO hysteresis	Falling hysteresis		440		mV
$V_{VREFUVLO}$	REF UVLO(1)	Rising edge of VREF, EN = 'HI'		1.8		V
$V_{VREFUVHYS}$	REF UVLO hysteresis(1)			100		mV
$V_{POR5VFILT}$	Reset	OVP latch is reset by V5FILT falling below the reset threshold	1.5	2.3	3.1	V
VOLTAGE FEEDBACK LOOP: VREF, VOUT, AND VOLTAGE GM AMPLIFIER						
V_{OUTTOL}	VOUT accuracy	V_{VOUT} = 0.8V, No droop	–1.5%	0%	1.5%	
V_{VREF}	VREF	I_{VREF} = 0 µA, T_A = 25°C		2		V
G_M	Transconductance			1		mS
V_{DM}	Differential mode input voltage		0		80	mV
$I_{COMPSRC}$	COMP pin maximum sourcing current	V_{COMP} = 2 V		–80		µA
V_{OFFSET}	Input offset voltage	T_A = 25°C	–5	0	5	mV
R_{DSCH}	Output voltage discharge resistance			42		Ω
f_{-3dbVL}	–3dB Frequency(1)			6		MHz
CURRENT SENSE: CURRENT SENSE AMPLIFIER, OVER CURRENT AND ZERO CROSSING						
A_{CSINT}	Internal current sense gain	Gain from the current of the low-side FET to PWM comparator when PWM = "OFF"	43	50	57	mV/A
I_{OCL}	Positive overcurrent limit (valley)			6.6		A
$I_{OCL(neg)}$	Negative overcurrent limit (valley)			–6		A
V_{ZXOFF}	Zero crossing comp internal offset			0		mV
DRIVERS: BOOT STRAP SWITCH						
$R_{DSONBST}$	Internal BST switch on-resistance	I_{VBST} = 10 mA, T_A = 25°C		5	10	Ω
I_{BSTLK}	Internal BST switch leakage current	V_{VBST} = 14 V, V_{SW} = 7 V, T_A = 25°C			1	µA

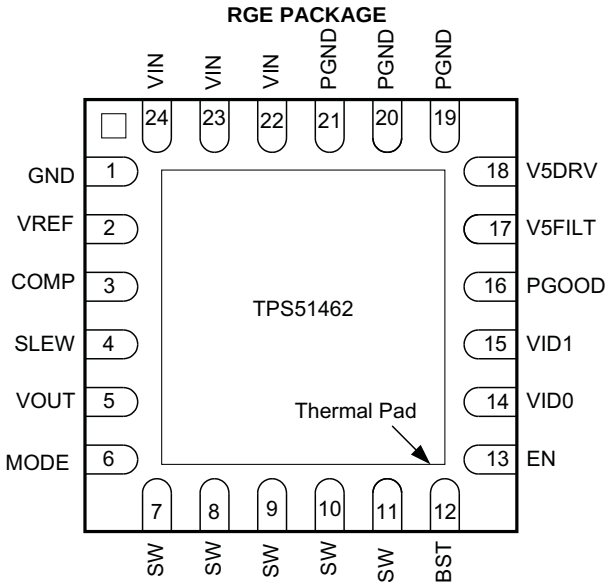
(1) Ensured by design, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V_{VIN} = 5.0 V, V_{V5DRV} = V_{V5FILT} = 5 V, MODE = OPEN, PGND = GND (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: OVP, UVP, PGOOD, and THERMAL SHUTDOWN						
V_{PGDLL}	PGOOD deassert to lower (PGOOD → Low)	Measured at the VOUT pin w/r/t V_{SLEW}	82%	84%	86%	
$V_{PGHYSHL}$	PGOOD high hysteresis			8%		
V_{PGDLH}	PGOOD de-assert to higher (PGOOD → Low)	Measured at the VOUT pin w/r/t V_{SLEW}	114%	116%	118%	
$V_{PGHYSHH}$	PGOOD high hysteresis			-8%		
$V_{INMINPG}$	Minimum VIN voltage for valid PGOOD	Measured at the VIN pin with a 2-mA sink current on PGOOD pin	0.9	1.3	1.5	V
V_{OVP}	OVP threshold	Measured at the VOUT pin w/r/t V_{SLEW}	118%	120%	122%	
V_{UVP}	UVP threshold	Measured at the VOUT pin w/r/t V_{SLEW}, device latches OFF, begins soft-stop	66%	68%	70%	
TH_{SD}	Thermal shutdown(2)	Latch off controller, attempt soft-stop.		125		°C
$TH_{SD(hys)}$	Thermal Shutdown hysteresis(2)	Controller re-starts after temperature has dropped		10		°C
TIMERS: ON-TIME, MINIMUM OFF TIME, SS, AND I/O TIMINGS						
$t_{ONESHOTC}$	PWM one-shot(2)	V_{VIN} = 5 V, V_{VOUT} = 0.8 V, f_{SW} = 667 kHz, fixed VID mode		240		ns
		V_{VIN} = 5 V, V_{VOUT} = 0.8 V, f_{SW} = 1 MHz, fixed VID mode		160		ns
$t_{MIN(off)}$	Minimum OFF time(2)	V_{VIN} = 5 V, V_{VOUT} = 0.8 V, f_{SW} = 1 MHz, DRVL on, SW = PGND, V_{VOUT} < V_{SLEW}		357		ns
t_{PGDDLY}	PGOOD startup delay time (2)(excl. SLEW ramp up time)	Delay starts from VOUT = VID code 00 and excludes SLEW ramp up time		3		ms
$t_{PGDPDLYH}$	PGOOD high propagation delay time(2)	50 mV over drive, rising edge	0.8	1	1.2	ms
$t_{PGDPDLYL}$	PGOOD low propagation delay time(2)	50 mV over drive, falling edge		10		µs
t_{OVPDLY}	OVP delay time(2)	Time from the VOUT pin out of +20% of V_{SLEW} to OVP fault		0.2		µs
$t_{UVDLYEN}$	Undervoltage fault enable delay (excl. SLEW ramp up time)(2)	Time from (VOUT = VID code 00) going high to undervoltage fault is ready		3		ms
t_{UVPDLY}	UVP delay time(2)	Time from the VOUT pin out of –30% of V_{SLEW} to UVP fault		8.5		µs
I_{SLEW}	Soft-start and voltage transition	C_{SS} = 10 nF assuming voltage slew rate of 1 mV/µs	9	10	11	µA
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGDPD}	PGOOD pull down voltage	PGOOD low impedance, I_{SINK} = 4 mA, V_{VIN} = V_{V5FILT} = 4.5 V			0.3	V
I_{PGDLKG}	PGOOD leakage current	PGOOD high impedance, forced to 5.5 V	–1	0	1	µA
V_{ENH}	EN logic high	EN, VCCP logic	0.8			V
V_{ENL}	EN logic low	EN, VCCP logic			0.3	V
I_{EN}	EN input current				1	µA
V_{VIDH}	VID logic high	VID0, VID1	0.8			V
V_{VIDL}	VID logic low	VID0, VID1			0.3	V
V_{MODETH}	MODE threshold voltage(3)	MODE 3	0.37	0.42	0.47	V
		MODE 4	0.55	0.60	0.65	
		MODE 7	1.75	1.80	1.85	
I_{MODE}	MODE current			15		µA
R_{PD}	VID pull-down resistance			10		kΩ

(2) Ensured by design, not production tested.
(3) See Table 3 for descriptions of MODE parameters.



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
19	PGND	I	Power ground. Source terminal of the rectifying low-side power FET.
20			
21			
22	VIN	I	Power supply input pin. Drain terminal of the switching high-side power FET.
23			
24			
1	GND	–	Signal ground.
2	VREF	O	2.0-V reference output. Connect a 0.22-µF ceramic capacitor to GND.
3	COMP	O	Connect series R-C to the VREF pin for loop compensation.
4	SLEW	I/O	Program the startup and voltage transition time using an external capacitor via 10-µA current source.
5	VOUT	I	Output voltage monitor input pin.
6	MODE	I	Allows selection of switching frequencies and output voltage. (See Table 3)
7	SW	I/O	Switching node output. Connect to the external inductor.
8			
9			
10			
11			
12	BST	I	Power supply for internal high-side gate driver. Connect a 0.1-µF bootstrap capacitor between this pin and the SW pin.
13	EN	I	Enable of the SMPS.
14	VID0	I	2-bit VID input.
15	VID1		
16	PGOOD	O	Power good output. Connect pull-up resistor.
17	V5FILT	I	5-V power supply for analog circuits.
18	V5DRV	I	5-V power supply for the gate driver.
Thermal Pad		–	Connect directly to system GND plane with multiple vias.

BLOCK DIAGRAM

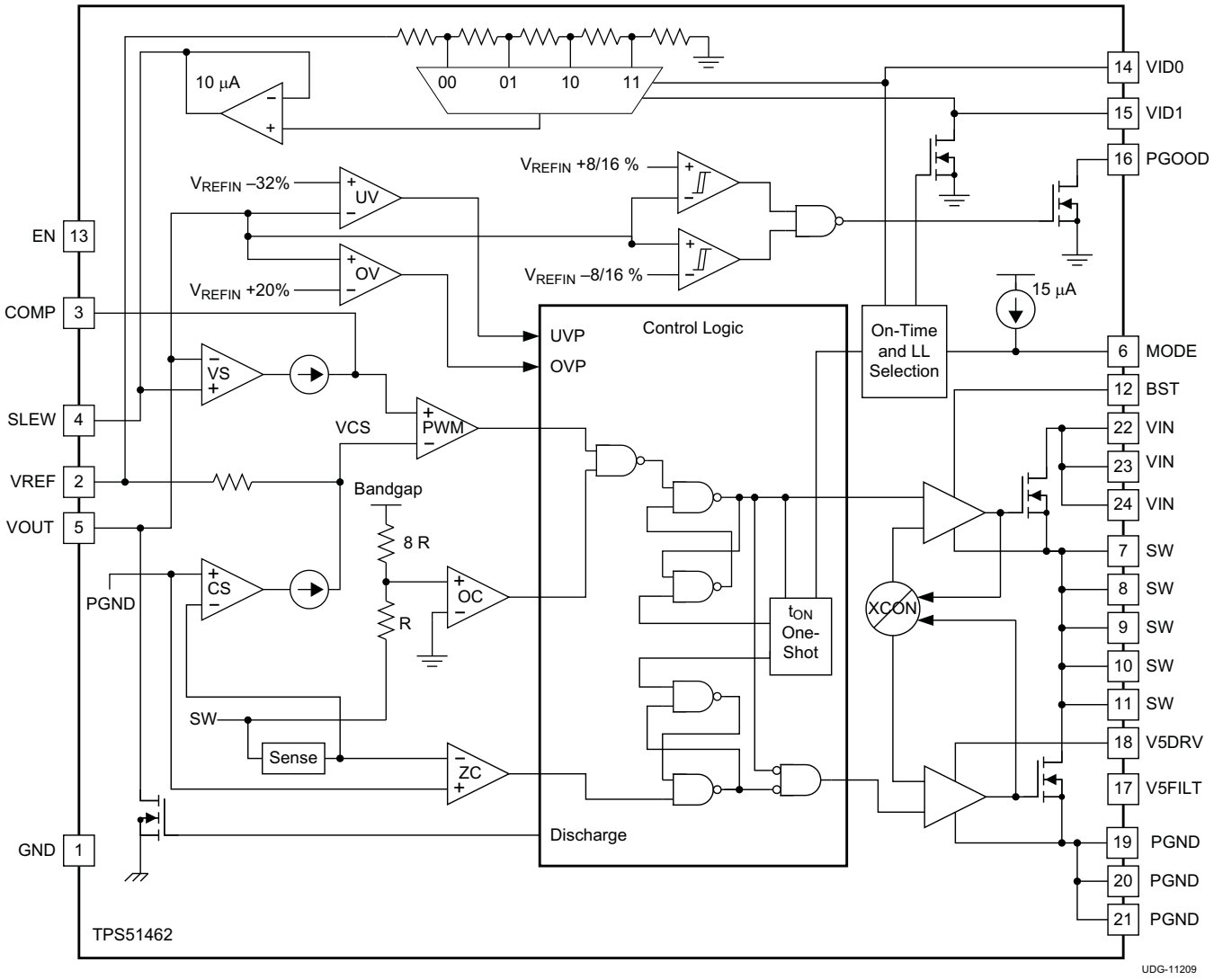


Table 1. Intel SA VID

VID 0	VID 1	VCCSA
0	0	0.9 V
0	1	0.80 V (1)MODE = Open
0	1	0.85 V (1)MODE = 33 kΩ
1	0	0.725 V
1	1	0.675 V

(1) 0.8 V for 2012/2013 SV processors and 0.85 V for 2012 LV/ULV processors.

TPS51462 APPLICATION DIAGRAM

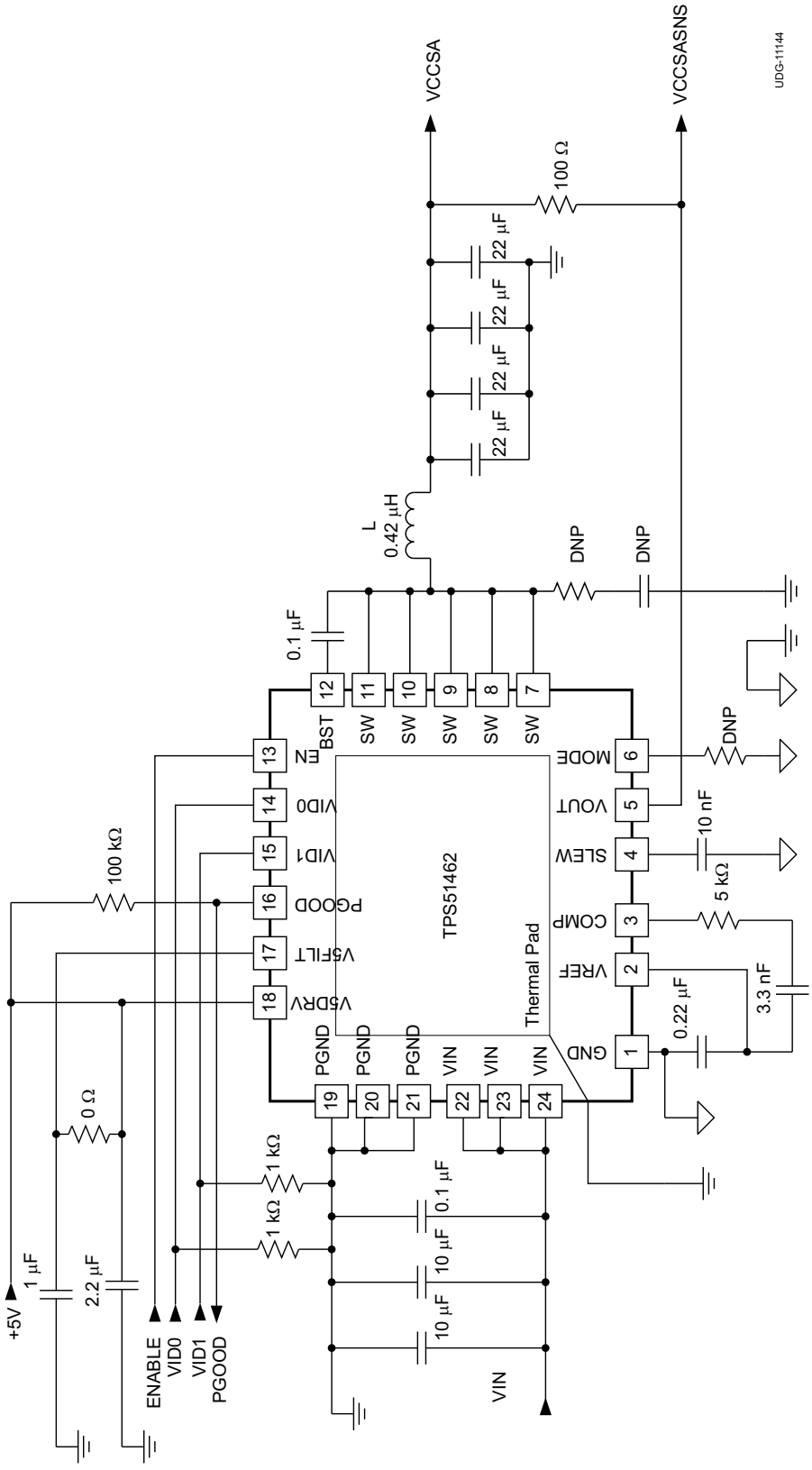


Figure 1. Application Schematic Using Non-Droop Configuration

Application Circuit List of Materials

Recommended part numbers for key external components for the circuit in Figure 1 are listed in Table 2.

Table 2. Key External Component Recommendations (Figure 1)

FUNCTION	MANUFACTURER	PART NUMBER
Output Inductor	Nec-Tokin	MPCG0740LR42C
Ceramic Output Capacitors	Panasonic	ECJ2FB0J226M
	Murata	GRM21BR60J226ME39L

APPLICATION INFORMATION

Functional Overview

The TPS51462 is a D-CAP+™ mode adaptive on-time converter. The output voltage is set using a 2-bit DAC that outputs a reference voltage in accordance with the code defined in Table 1. *VID-on-the-fly* transitions are supported with the slew rate controlled by a single capacitor on the SLEW pin. The converter automatically runs in discontinuous conduction mode (DCM) to optimize light-load efficiency. Two switching frequency selections are provided, (700 kHz and 1 MHz) to enable optimization of the power chain for the cost, size and efficiency requirements of the design.

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS51462, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the reference voltage and the feedback voltage.

PWM Operation

Referring to Figure 2, in steady state, continuous conduction mode, the converter operates in the following way.

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback (V_{CS}) is higher than the error amplifier output (V_{COMP}). V_{CS} falls until it hits V_{COMP}, which contains a component of the output ripple voltage. V_{CS} is not directly accessible by measuring signals on pins of TPS51462. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

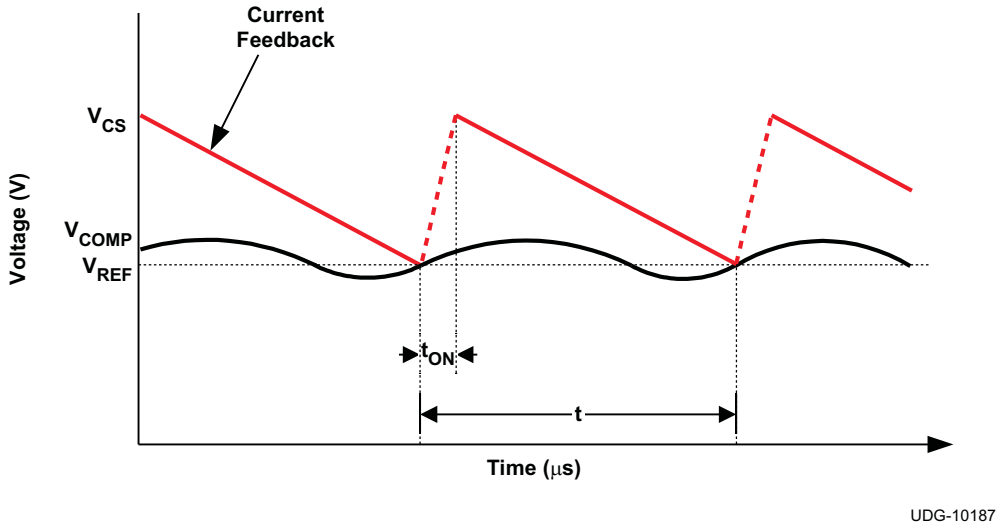


Figure 2. D-CAP+™ Mode Basic Waveforms

The current feedback is an amplified and filtered version of the voltage between PGND and SW during low-side FET on-time. The TPS51462 also provides a single-ended differential voltage (V_{OUT}) feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

PWM Frequency and Adaptive on Time Control

In general, the on-time (at the SW node) can be estimated by Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

where

- f_{SW} is the frequency selected by the connection of the MODE pin

The on-time pulse is sent to the top FET. The inductor current and the current feedback rises to peak value. Each ON pulse is latched to prevent double pulsing. Switching frequency settings are shown in Table 3.

Non-Droop Configuration

The TPS51462 offers a non-droop solution only. The benefit of a non-droop approach is that load regulation is flat, therefore, in a system where tight DC tolerance is desired, the non-droop approach is recommended. For the Intel system agent application, non-droop is recommended as the standard configuration.

The non-droop approach can be implemented by connecting a resistor and a capacitor between the COMP and the VREF pins. The purpose of the type II compensation is to obtain high DC feedback gain while minimizing the phase delay at unity gain cross over frequency of the converter.

The value of the resistor (R_C) can be calculated using the desired unity gain bandwidth of the converter, and the value of the capacitor (C_C) can be calculated by knowing where the zero location is desired. An application tool that calculates these values is available from your local TI Field Application Engineer.

Figure 3 shows the basic implementation of the non-droop mode using the TPS51462.

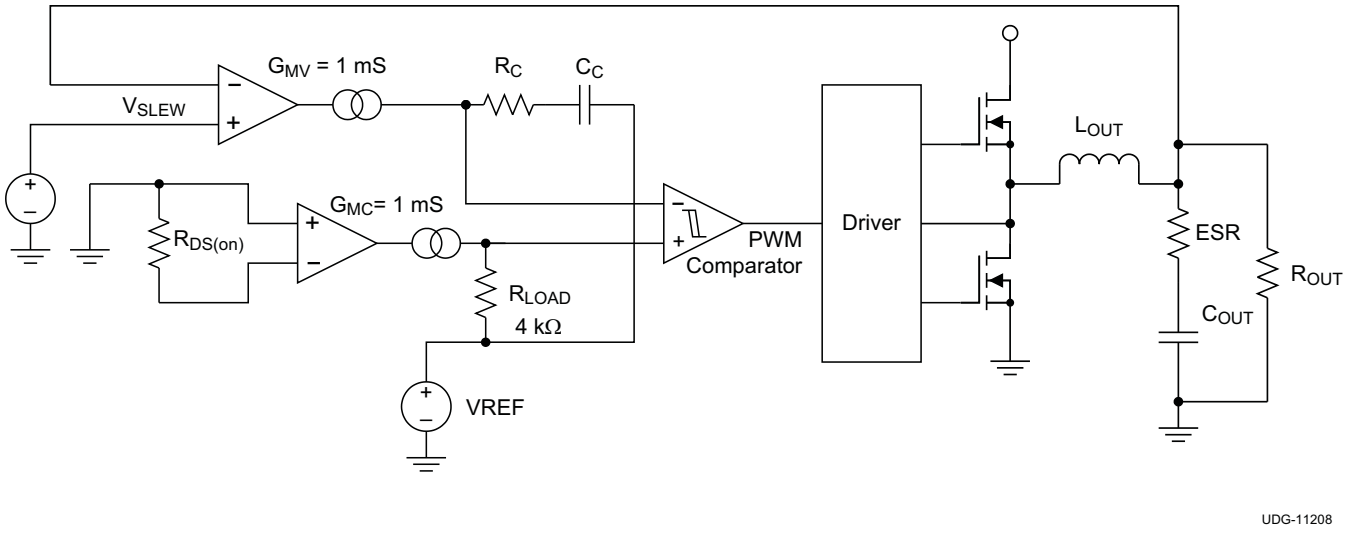


Figure 3. Non-Droop Mode Basic Implementation

Figure 4 shows the load regulation of the system agent rail using non-droop configuration.

Figure 5 shows the transient response of TPS51462 using non-droop configuration where C_{OUT} = 4 × 22 µF. The applied step load is from 0 A to 2 A.

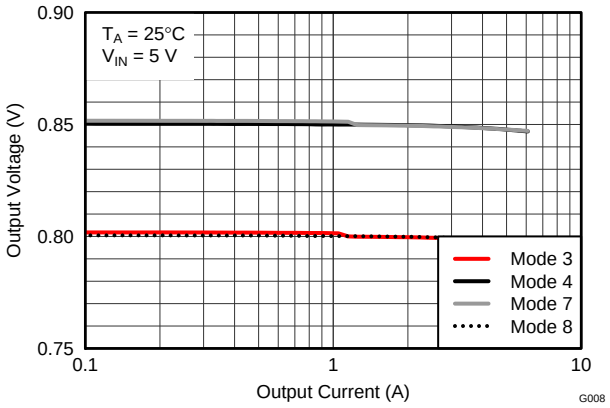


Figure 4. 0.8 V/0.85 V Load Regulation (V_{IN} = 5 V) Non-Droop Configuration

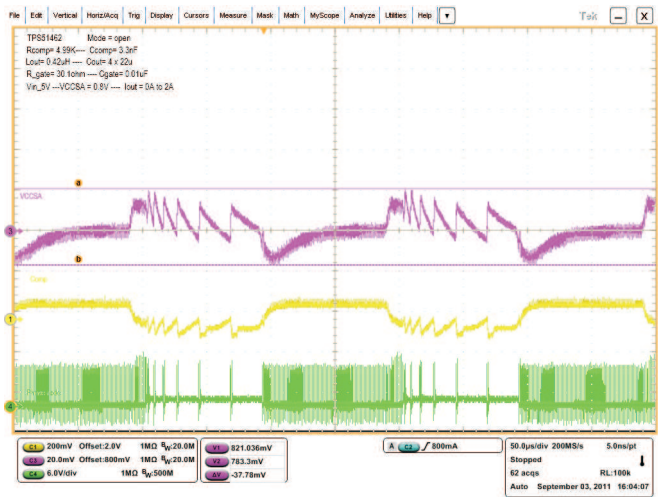


Figure 5. Non-Droop Configuration Transient Response

Table 3. Mode Parameter Table

MODE	MODE CONNECTION	SWITCHING FREQUENCY (f_{SW})	VID1 = 1 VID0 = 0 (V)
3	22 kΩ	700 kHz	0.80
4	33 kΩ	1 MHz	0.85
7	100 kΩ	700 kHz	0.85
8	Open	1 MHz	0.80

Light Load Power Saving Features

The TPS51462 has an automatic pulse-skipping mode to provide excellent efficiency over a wide load range. The converter senses inductor current and prevents negative flow by shutting off the low-side gate driver. This saves power by eliminating re-circulation of the inductor current. Further, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

Voltage Slewing

The TPS51462 ramps the SLEW voltage up and down to perform the output voltage transitioning. The timing is independent of switching frequency, as well as output resistive and capacitive loading. It is set by a capacitor from SLEW pin to GND, called C_{SLEW}, together with an internal current source of 10 µA. The slew rate is used to set the startup and voltage transition rate.

$$C_{SLEW} = \frac{I_{SLEW}}{SR}$$

$$t_{SS} = \frac{C_{SLEW} \times 0.9\,V}{I_{SLEW}} \quad (2)$$

where

- I_{SLEW} = 10 µA (nom)
- SR is the target output voltage slew rate, per Intel specification between 0.5 mV/µs and 10 mV/µs (3)

For the current reference design, an SR of 1 mV/µs is targeted. The C_{SLEW} is calculated to be 10 nF. The slower slew rate is desired to minimize large inductor current perturbation during startup and voltage transitioning thus reducing the possibility of acoustic noise.

After the power up, when VID1 is transitioning from 0 to 1, TPS51462 follows the SLEW voltage entering the forced PWM mode to actively discharge the output voltage from 0.9 V to 0.8 V. The actual output voltage slew rate is approximately the same as the set slew rate while the bandwidth of the converter supports it and there is no overcurrent triggered by additional charging current flowing into the output capacitors. After SLEW transition is completed, PWM mode is maintained for 64 µs (16 clock cycles when the frequency is 1 MHz) to ensure voltage regulation.

Protection Features

The TPS51462 offers many features to protect the converter power chain as well as the system electronics.

5-V Undervoltage Protection (UVLO)

The TPS51462 continuously monitors the voltage on the V5FILT pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3 V and has a nominal of 440 mV of hysteresis. If the 5-V UVLO limit is reached, the converter transitions the phase node into a 3-state function. And the converter remains in the off state until the device is reset by cycling 5 V until the 5-V POR is reached (2.3-V nominal). The power input does not have an UVLO function

Power Good Signals

The TPS51462 has one open-drain *power good* (PGOOD) pin. During startup, there is a 3 ms power good delay starting from the output voltage reaching the regulation point (excluding soft-start ramp-up time). And there is also a 1 ms power good high propagation delay. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an undervoltage condition on V5FILT is detected. The PGOOD signal is blanked during VID voltage transitions to prevent false triggering during voltage slewing.

Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS51462 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately 120% × V_{SLEW}. In this case, the converter de-asserts the PGOOD signals and performs the overvoltage protection function. The converter remains in this state until the device is reset by cycling 5 V until the 5-V POR threshold (2.3 V nominal) is reached.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the Overcurrent Protection and Overcurrent Limit sections. If the output voltage drops below 70% of V_{SLEW}, after an 8-µs delay, the device latches OFF. Undervoltage protection can be reset only by EN or a 5-V POR.

Overcurrent Protection

Both positive and negative overcurrent protection are provided in the TPS51462:

- Overcurrent Limit (OCL)
- Negative OCL (level same as positive OCL)

Overcurrent Limit

If the sensed current value is above the OCL setting, the converter delays the next ON pulse until the current drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. The TPS51462 uses a valley current limiting scheme where the DC OCL trip point is the OCL limit plus half of the inductor ripple current. The minimum valley OCL is 6 A over process and temperature.

During the overcurrent protection event, the output voltage likely droops until the UVP limit is reached. Then, the converter de-asserts the PGOOD pin, and then latches OFF after an 8-µs delay. The converter remains in this state until the device is reset by EN or a 5VFILT POR.

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} \quad (4)$$

Negative OCL

The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a *valley* mode, the absolute value of the negative OCL set point is typically -6.5 A.

Thermal Protection

Thermal Shutdown

The TPS51462 has an internal temperature sensor. When the temperature reaches a nominal 125°C, the device shuts down until the temperature cools by approximately 10°C. Then the converter restarts.

Startup and VID Transition Timing Diagrams

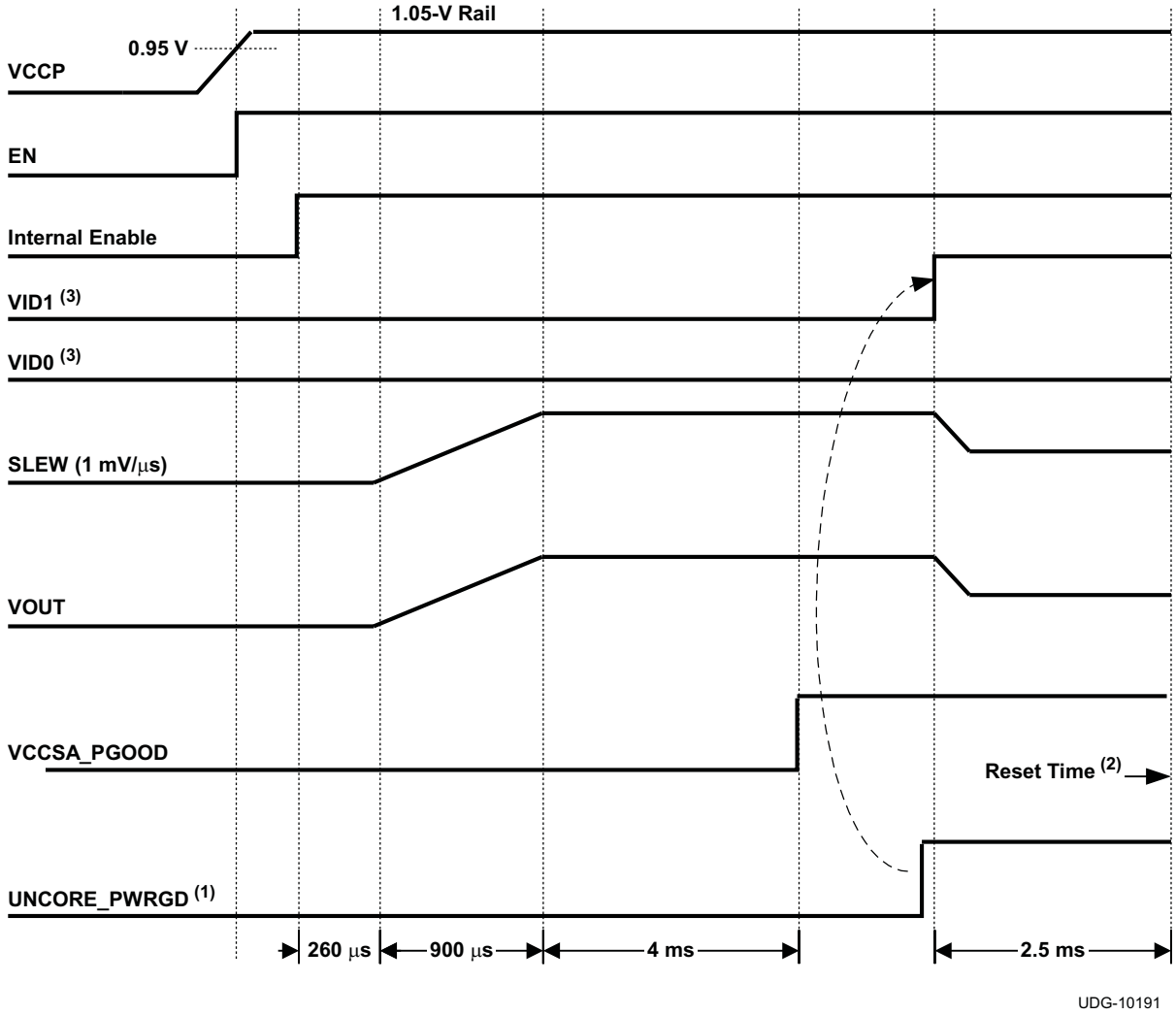


Figure 6. Fixed VID/Fixed Step Startup and VID Toggle Timing Diagram for 2011 Intel Platform

For Figure 6:

(1) Includes VCCA, VCCAXG, and VDDQ power rails.

(2) Processor reset: VID transition must be completed by this time.

(3) 1-kΩ pull-down resistor required.

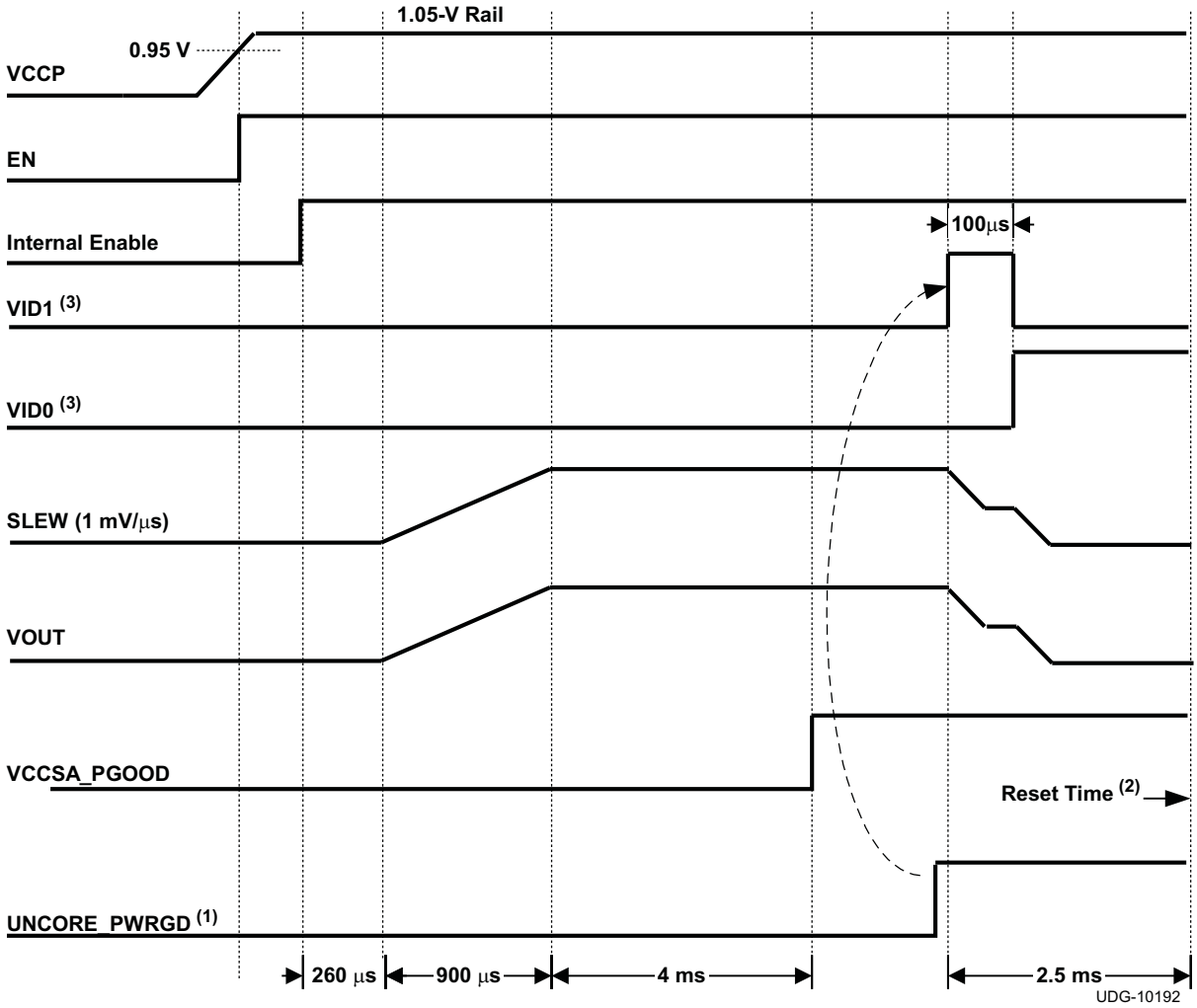


Figure 7. Fixed VID/Fixed Step Startup and VID Toggle Timing Diagram for 2012 Intel Platform

For Figure 7:

(1) Includes VCCA, VCCAXG, and VDDQ power rails.

(2) Processor reset: VID transition must be completed by this time.

(3) 1-kΩ pull-down resistor required.

TYPICAL CHARACTERISTICS

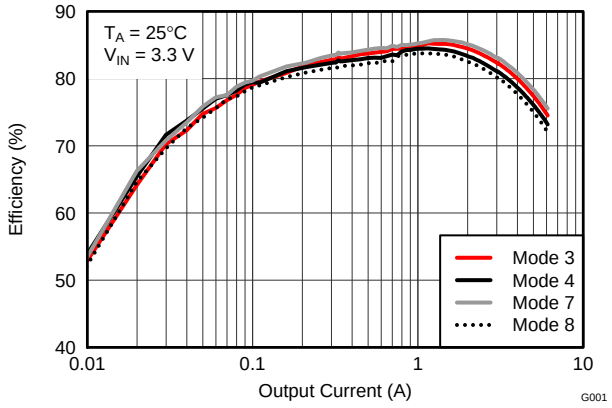


Figure 8. Efficiency vs. Output Current

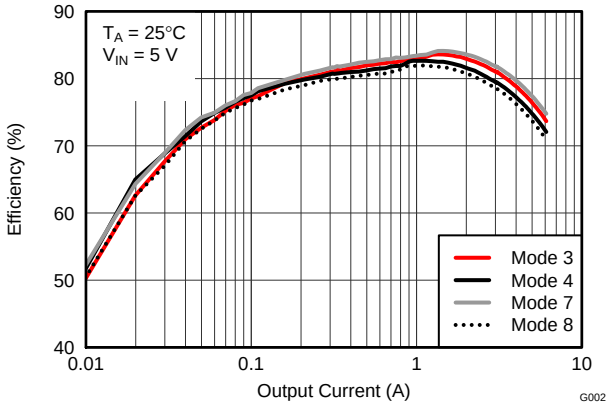


Figure 9. Efficiency vs. Output Current

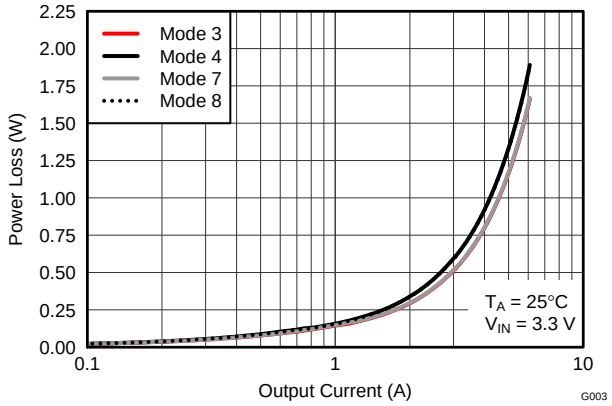


Figure 10. Power Loss vs. Output Current

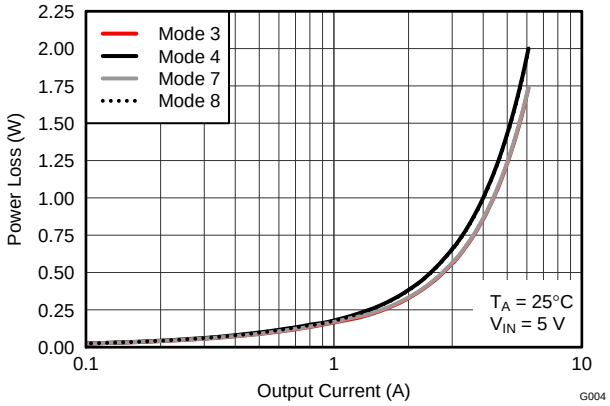


Figure 11. Power Loss vs. Output Current

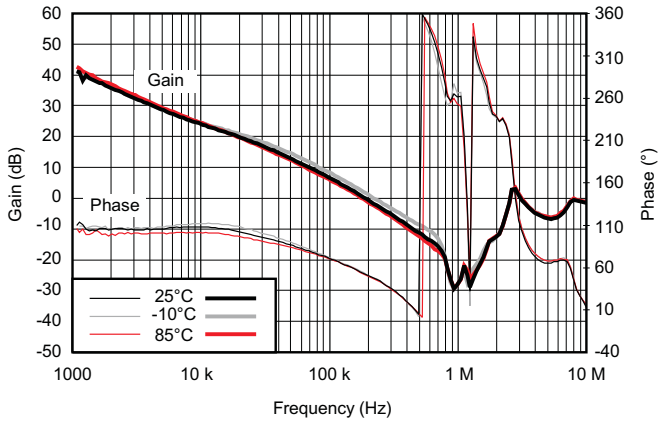


Figure 12. Bode Plot, Non-Droop Mode

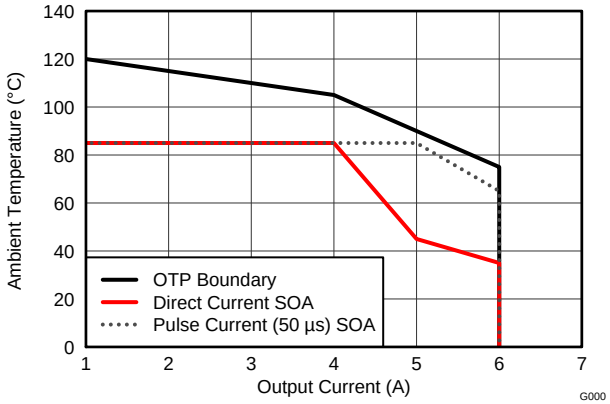


Figure 13. Safe Operating Area

TYPICAL CHARACTERISTICS (continued)

Figure 14. Mode=8, I_{OUT} = 0 A, VID Transitioning

Figure 15. Mode=8, I_{OUT} = 3 A, VID Transitioning

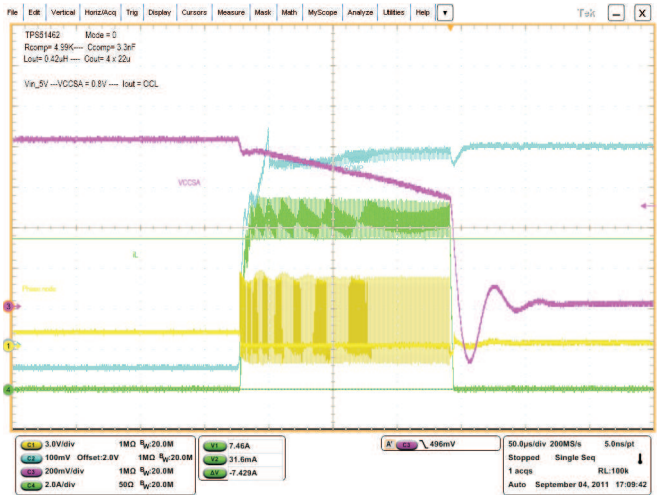


Figure 16. Mode = 8, OCL

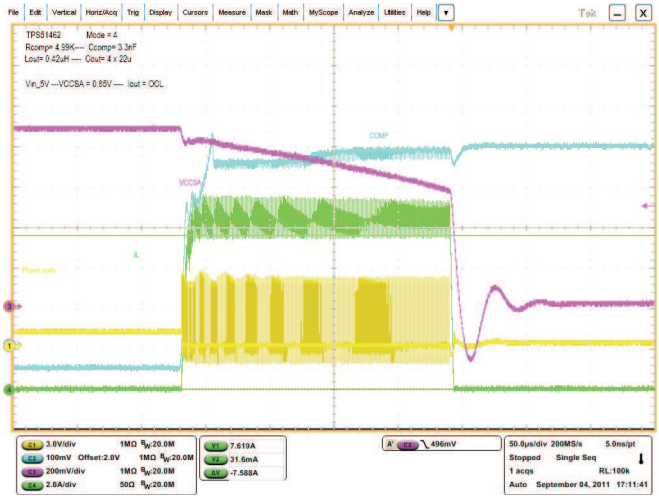


Figure 17. Mode=4, OCL

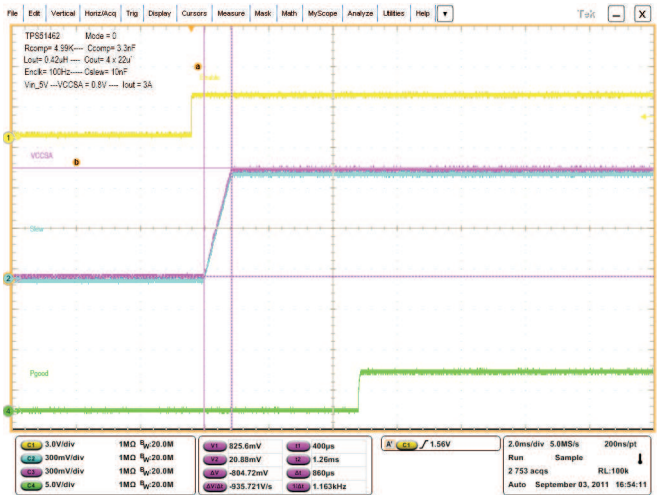


Figure 18. Mode= 8, I_{OUT} = 3 A, Soft-Start

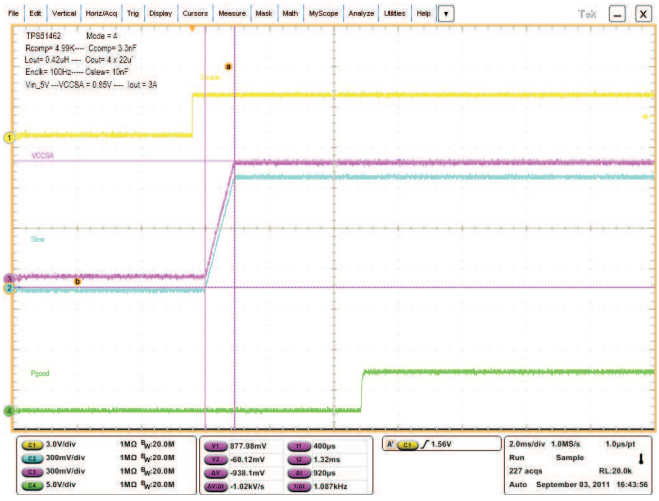


Figure 19. Mode= 4, I_{OUT} = 3 A, Soft-Start

DESIGN PROCEDURE

The simplified design procedure is done for a non-droop application using the TPS51462 converter.

Step One

Determine the specifications.

The System Agent Rail requirements provide the following key parameters:

1. V_{00} = 0.90 V
2. V_{10} = 0.80 V
3. $I_{CC(max)}$ = 6 A
4. $I_{DYN(max)}$ = 2 A
5. $I_{CC(tdc)}$ = 3 A

Step Two

Determine system parameters.

The input voltage range and operating frequency are of primary interest. For example:

1. V_{IN} = 5 V
2. f_{SW} = 1 MHz

Step Three

Determine inductor value and choose inductor.

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this case, use 25%:

$$I_{P-P} = 6\,A \times 0.25 = 1.5\,A \tag{5}$$

At f_{SW} = 1 MHz, with a 5-V input and a 0.80-V output:

$$L = \frac{V \times dT}{I_{P-P}} = \frac{(V_{IN} - V_{10}) \times \left(\frac{V_{10}}{(f_{SW} \times V_{IN})}\right)}{I_{P-P}} = \frac{(5 - 0.8) \times \left(\frac{0.8}{(1 \times 5)}\right)}{1.5\,A} = 0.45\,\mu H \tag{6}$$

For this application, a 0.42-µH, 1.55-mΩ inductor from NEC-TOKIN with part number MPCG0740LR42C is chosen.

Step Four

Set the output voltage.

The output voltage is determined by the VID settings. The actual voltage set point for each VID setting is listed in Table 1. No external resistor dividers are needed for this design.

Step Five

Calculate C_{SLEW}.

VID pin transition and soft-start time is determined by C_{SLEW} and 10 µA of internal current source.

$$C_{SLEW} = \frac{I_{SLEW}}{SR_{DAC}} = \frac{10\,\mu A}{1\,mV/\mu s} = 10\,nF \tag{7}$$

The slower slew rate is desired to minimize large inductor current perturbation during startup and voltage transition, thus reducing the possibility of acoustic noise.

Given the C_{SLEW}, use Equation 8 to calculate the soft start time.

$$t_{SS} = \frac{C_{SLEW} \times 0.9\,V}{I_{SLEW}} = \frac{10\,nF \times 0.9\,V}{10\,\mu A} = 900\ \mu s \tag{8}$$

Step Six

Calculate OCL.

The DC OCL level of TPS51462 design is determined by Equation 9,

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} = 6\,A + \frac{1}{2} \times 1.5\,A = 6.75\,A \tag{9}$$

The minimum valley OCL is 6 A over process and temperature, and I_{P-P} = 1.5 A, the minimum DC OCL is calculated to be 6.75A.

Step Seven

Determine the output capacitance.

To determine COUT based on transient and stability requirement, first calculate the the minimum output capacitance for a given transient.

Equation 11 and Equation 10 can be used to estimate the amount of capacitance needed for a given dynamic load step/release. Please note that there are other factors that may impact the amount of output capacitance for a specific design, such as ripple and stability. Equation 11 and Equation 10 are used only to estimate the transient requirement, the result should be used in conjunction with other factors of the design to determine the necessary output capacitance for the application.

$$C_{OUT(min\_under)} = \frac{L \times \Delta I_{LOAD(max)}^{2} \times \left(\frac{V_{VOUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)} \right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{VOUT}}{V_{IN(min)}} \right) \times t_{SW} - t_{MIN(off)} \right) \times V_{VOUT}} \tag{10}$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)} \right)^{2}}{2 \times \Delta V_{LOAD(release)} \times V_{VOUT}} \tag{11}$$

Equation 10 and Equation 11 calculate the minimum C_{OUT} for meeting the transient requirement, which is 72.9 µF assuming the following:

- ±3% voltage allowance for load step and release
- MLCC capacitance derating of 60% due to DC and AC bias effect

In this reference design, 4, 22-µF capacitors are used in order to provide this amount of capacitance.

Step Eight

Determine the stability based on the output capacitance C_{OUT}.

In order to achieve stable operation. The 0-dB frequency, f_0 should be kept less than 1/5 of the switching frequency (1 MHz). (See Figure 3)

$$f_0 = \frac{1}{2\pi} \times \frac{G_M}{C_{OUT}} \times \frac{R_C}{R_S} = 150\,kHz$$

where

- $R_S = R_{DS(on)} \times G_{MC} \times R_{LOAD}$ (12)

$$R_C = \frac{f_0 \times R_S \times 2\pi \times C_{OUT}}{G_M} = \frac{150\,kHz \times 53m\Omega \times 2\pi \times 88\,\mu F}{1mS} \approx 5k\Omega \quad (13)$$

Using 4, 22-µF capacitors, the compensation resistance, R_C can be calculated to be approximately 5 kΩ.

The purpose of the comparator capacitor (C_C) is to reduce the DC component to obtain high DC feedback gain. However, as it causes phase delay, another zero to cancel this effect at f_0 is needed. This zero can be determined by values of C_C and the compensation resistor, R_C.

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} = \frac{f_0}{10} \quad (14)$$

And since R_C has previously been derived, the value of C_C is calculated to be 2.2 nF. In order to further boost phase margin, a value of 3.3-nF is chosen for this reference design.

Step Nine

Select decoupling and peripheral components.

For TPS51462 peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5DRV decoupling ≥ 2.2 µF, ≥ 10 V
- V5FILT decoupling ≥ 1 µF, ≥10 V
- VREF decoupling 0.22 µF to 1 µF, ≥ 4 V
- Bootstrap capacitors ≥ 0.1 µF, ≥ 10 V
- Pull-up resistors on PGOOD, 100 kΩ

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

- Connect PGND pins (or at least one of the pins) to the thermal PAD underneath the device. Also connect GND pin to the thermal PAD underneath the device. Use four vias to connect the thermal pad to internal ground planes.
- Place VIN, V5DRV, V5FILT and 2VREF decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, VOUT, PGND and SW pins. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (SLEW, COMP) away from noisy signals (SW, VBST).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
FX006	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51462	Samples
TPS51462RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51462	Samples
TPS51462RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51462	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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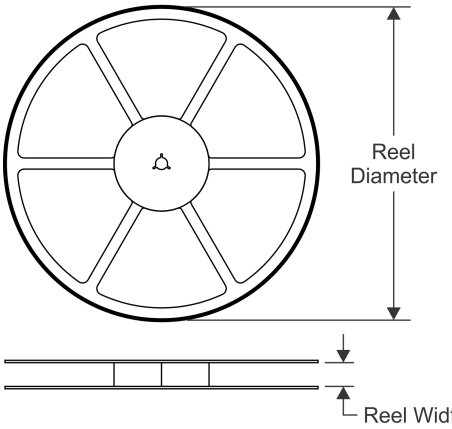
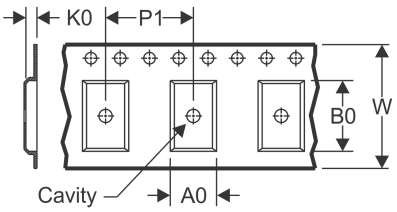
TAPE AND REEL INFORMATION

REEL DIMENSIONS

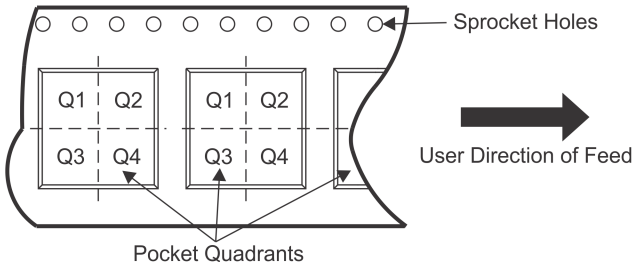


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

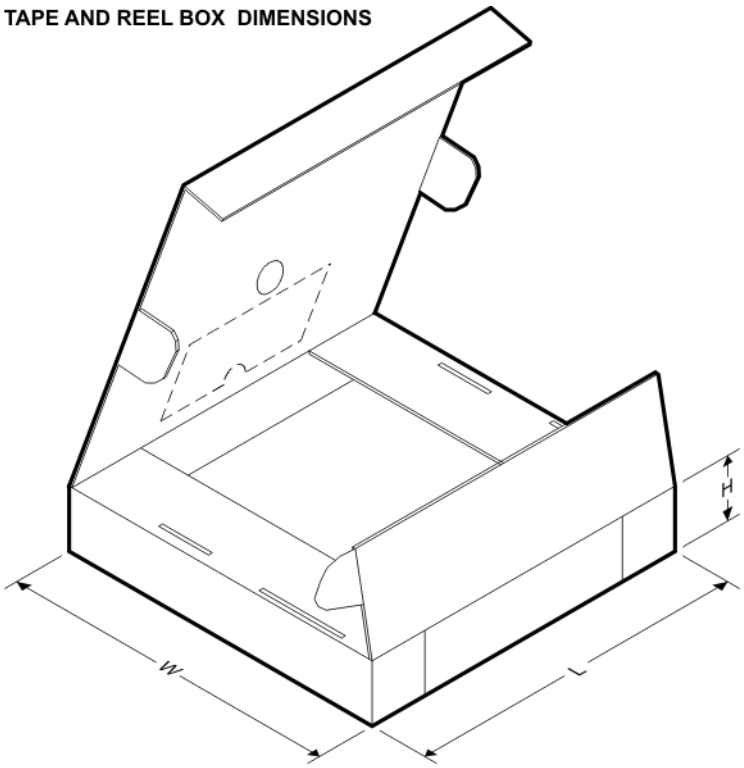
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51462RGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS51462RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51462RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51462RGET	VQFN	RGE	24	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2

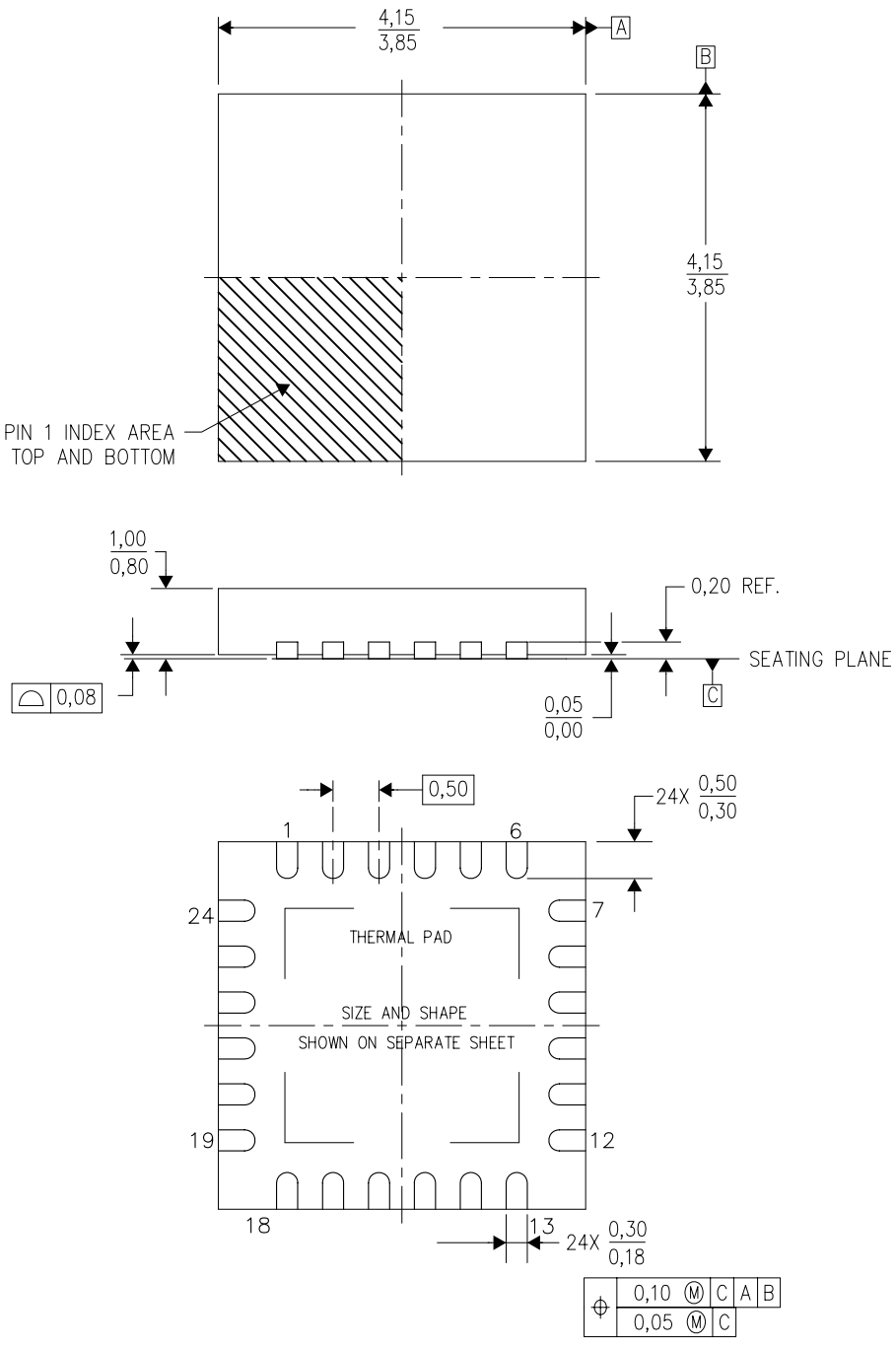
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51462RGER	VQFN	RGE	24	3000	338.0	355.0	50.0
TPS51462RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS51462RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS51462RGET	VQFN	RGE	24	250	338.0	355.0	50.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

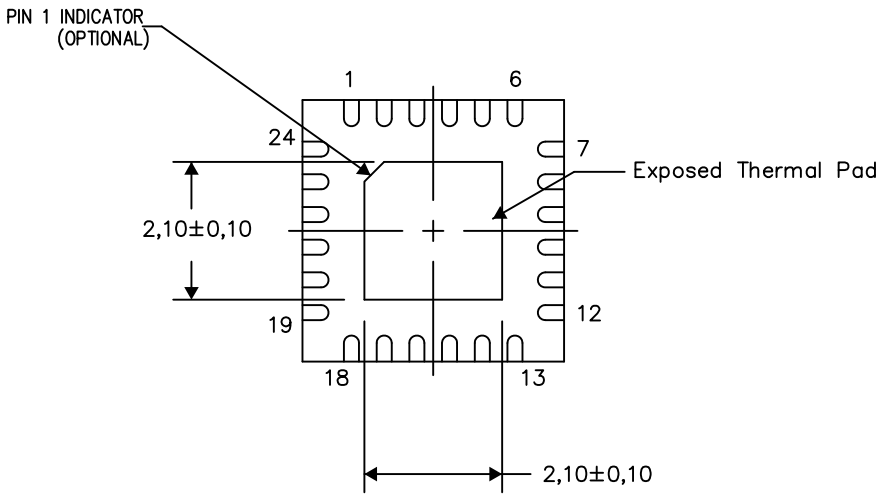
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



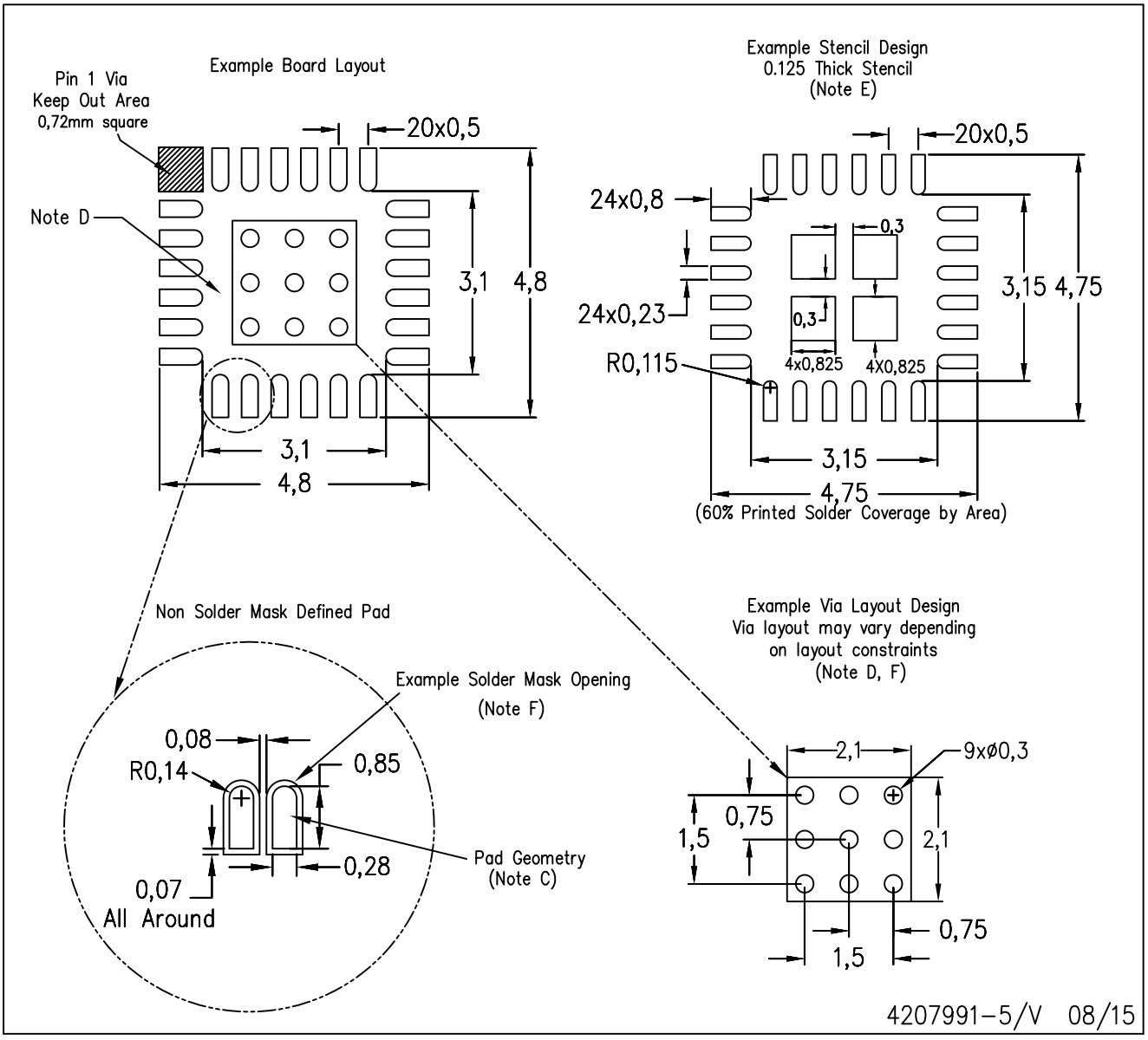
Bottom View

Exposed Thermal Pad Dimensions

4206344–7/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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