10-A STEP-DOWN SYNCHRONOUS SWITCHER WITH INTEGRATED MOSFETs

Check for Samples: TPS51315

FEATURES

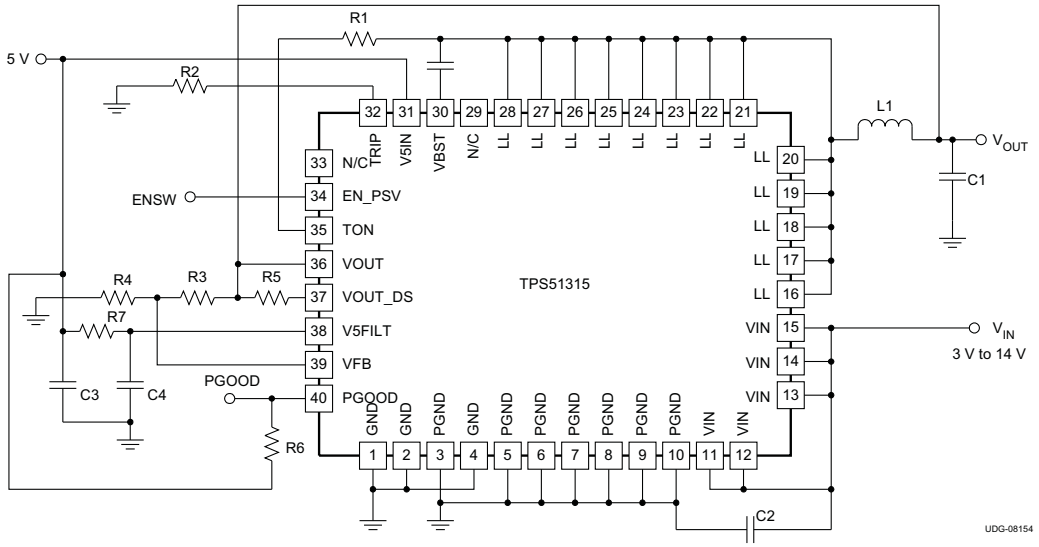
- **Input Voltage Range: 3 V to 14 V**
- **Output Voltage Range: 0.75 V to 5.5 V**
- **Integrated Power MOSFETs with 10-A Continuous Current Output**
- **< 5-µA Shutdown Current**
- **D-CAP™ Mode with Fast Transient Response**
- **Programmable Switching Frequency with External Resistor From 100 kHz to 1 MHz**
- **Selectable Auto-Skip or PWM-Only Operation**
- **< 1% Initial Reference Accuracy**
- **Internal Soft-Start Control**
- **Integrated Boost Diode**
- **Power Good Signal**
- **Adjustable Overcurrent Limit via External Resistor**
- **OVP/UVP/UVLO Protection**
- **Integrated Selectable Output Discharge**
- **Prebias Output Voltage Start-Up with Disabled Output Discharge**
- **Thermal Shutdown**
- **40-Pin QFN Package with Exposed Thermal Pad**
- **Supports All Ceramic Output Capacitors**

APPLICATIONS

- **Portable Device Application**
- **Notebook Computers**
- **Server and Desktop**

DESCRIPTION

The TPS51315 is a D-CAP™ Mode, 10-A, synchronous step-down converter with integrated MOSFETs. The combination of D-CAP™ mode and on-board MOSFETs provides fast transient response performance with ease of use, less external component count and small footprint. Externally adjustable switching frequency allows optimal design between component size and efficiency tradeoff. Ceramic output capacitors can be employed by adding a few extra components. The TPS51315 is available in the thermally-efficient 40-pin, 5 mm x 7 mm, QFN package and is specified from -40°C to 85°C ambient.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN(2)
-40°C to 125°C	Plastic QFN (RGF)	TPS51315RGFT	40	Tape and Reel	250	Green (RoHS and no Pb/Br)
		TPS51315RGFR			3000	

(1) For most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the web site at www.ti.com.

(2) These devices meet the following planned eco-friendly classification:
Green (RoHS and No Sb/Br): Texas Instruments defines *Green* to mean Pb-free (RoHS compatible) and free of bromine (Br)- and antimony (Sb)-based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information. These devices have a Cu NiPdAu lead/ball finish.

ABSOLUTE MAXIMUM RATINGS(1)

		TPS51315	UNIT
Input voltage range	VIN	–0.3 to 20	V
	VBST	–0.3 to 26	
	VBST (with respect to LL)	–0.3 to 6	
	EN_PSV, TRIP, V5IN, V5FILT	–0.3 to 6	
	VOUT, VOUT_DS	–0.3 to 6	
	TON	–0.3 to 6	
Output voltage range	LL	–1 to 20	V
	PGOOD	–0.3 to 6	
	PGND	–0.3 to 0.3	
Source/Sink current	TON	1	mA
	VBST	50	
Operating free-air temperature, T_A		–40 to 85	°C
Storage temperature range, T_{stg}		–55 to 150	
Junction temperature range, T_J		–40 to 125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Input voltage range	VIN	3		14	V
	VBST (with respect to LL)	4.5		5.5	
	EN_PSV, V5IN, V5FILT, VOUT, VOUT_DS	–0.1		5.5	
Output voltage range	LL	–0.8		15	V
	PGOOD	–0.1		5.5	
Junction temperature range, T_J		–40		125	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
40-Pin Plastic QFN (RGF)	2.85 W	25 mW/°C	1.35 W

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)		2000		V
Charged Device Model (CDM)		500		

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5IN}	V5IN supply current	V5IN current, T_A = 25°C, No Load, EN_PSV = 5V, V_{VFB} = 0.75 V, V_{LL} = 0.5 V		0	1	µA
I_{V5FILT}	V5FILT supply current	V5FILT current, T_A = 25°C, No Load, V_{EN_PSV} = 5 V, V_{VFB} = 0.75 V, LL = 0.5 V		400		µA
$I_{V5INSDN}$	V5IN shutdown current	V5IN current, T_A = 25°C, No Load, V_{EN_PSV} = 0 V		0	1	µA
$I_{V5FILTSDN}$	V5FILT shutdown current	V5FILT current, T_A = 25°C, No Load, V_{EN_PSV} = 0 V	1.5	4.5	7.5	µA
VOUT AND VREF VOLTAGES						
V_{OUT}	Output voltage	Adjustable output range	0.75		5.5	V
V_{VFB}	VFB regulation voltage	V_{FB} voltage		751		mV
V_{VFB_TOL}	VFB regulation voltage tolerance	T_A = 25°C, bandgap initial accuracy	–0.9%		0.9%	
		0°C ≤ T_A ≤ 85°C	–1.3%		1.3%	
		–40°C ≤ T_A ≤ 85°C	–1.6%		1.6%	
I_{VFB}	VFB input current	V_{VFB} = 0.75 V, T_A = 25°C		–0.025		µA
R_{Dischg}	VOUT_DS discharge resistance	V_{EN_PSV} = 0 V, VOUT_DS = 0.75 V		20		Ω
HOUSEKEEPING CLOCK, ON-TIME TIMER, and INTERNAL SOFT START						
T_{ONN}	Nominal on-time	V_{IN} = 10 V, V_{OUT} = 2.5 V, $R_{T(on)}$ = 250 kΩ		1115		ns
T_{ONF}	Fast switch on-time	V_{IN} = 10 V, V_{OUT} = 2.5 V, $R_{T(on)}$ = 100 kΩ		865		ns
T_{ONS}	Slow switch on-time	V_{IN} = 10 V, V_{OUT} = 2.5 V, $R_{T(on)}$ = 400 kΩ		1515		ns
T_{ON}	Minimum on-time	V_{IN} = 10 V, V_{OUT} = 0.75 V, $R_{T(on)}$ = 100 kΩ(1)		170	200	ns
$T_{OFF(min)}$	Minimum off-time	T_A = 25°C, V_{VFB} = 0.75 V, V_{LL} = –0.1V, V_{TRIP} = OPEN		385		ns
T_{SS}	Internal soft-start time	T_A = 25°C, V_{EN_PSV} > 3 V		1.06		ms
f_{CLK}	Clock frequency	Soft-start, UVP, OVP, PGOOD(2)	240	250	260	kHz
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{V5IN-VBST}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakagecurrent	V_{VBST} = 26 V, LL = 20 V, T_A = 25°C		0.1	1	µA
PROTECTIONS: OVERCURRENT LIMIT (OCL), UNDERCURRENT LIMIT (UCL)						
$V_{OCL(off)}$	Overcurrent limit comparator offset	($V_{TRIP-GND}$– $V_{PGND-LL}$) voltage $V_{TRIP-GND}$ = 60 mV	–10	0	10	mV
$V_{UCL(off)}$	Undercurrent limit comparator offset	($V_{TRIP-GND}$– $V_{LL-PGND}$) voltage $V_{TRIP-GND}$ = 60 mV, EN_PSV=FLOAT	–9.5	0.5	10.5	mV
$V_{ZC(off)}$	Zero crossing comparator offset	$V_{PGND-LL}$ voltage, V_{EN_PSV} = 3.3V	–9.5	0.5	10.5	mV
V_{RTRIP}	Current limit threshold setting range	$V_{TRIP-GND}$ voltage(2) , T_A = 25°C	30			mV
I_{TRIP}	TRIP source current	V_{TRIP} < 0.3 V, T_A = 25°C	9	10	11	µA
TC_{ITRIP}	Trip source current temperature coefficient	T_A = 25°C(2)		4500		ppm/°C

(1) Design constraint. Ensure actual on-time is greater than the maxiumum value (design $R_{T(on)}$ so that the minimum tolerance is 100 kΩ).
(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range (unless otherwise noted)

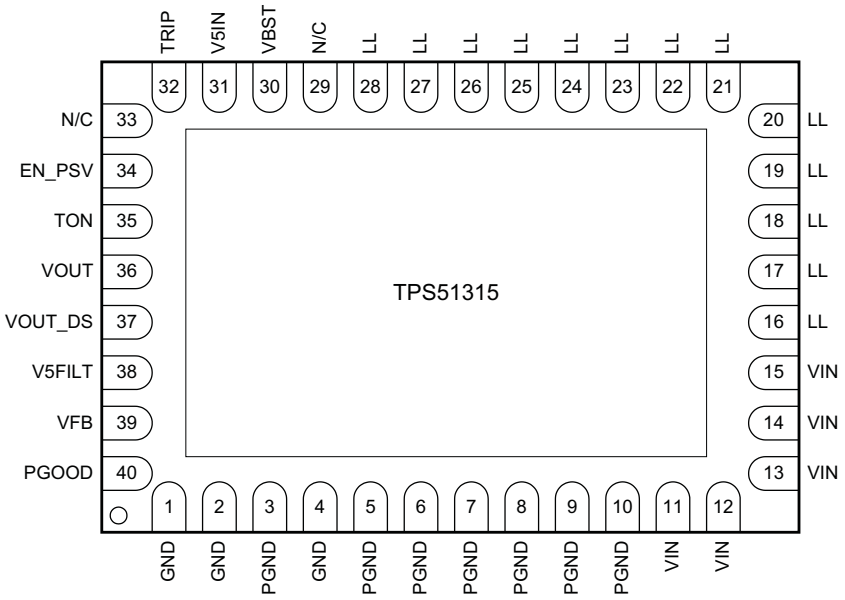
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	Powergood threshold	PG in from lower (PGOOD goes high), T_A = 25°C	92.5%	95%	97.5%	
		PG Low hysteresis (PGOOD goes low)	–4.5%	–5.5%	–6.5%	
		PG in from higher (PGOOD goes high), T_A = 25°C	102.5%	105%	107.5%	
		PG High hysteresis (PGOOD goes low)	4.5%	5.5%	6.5%	
$I_{PG(max)}$	Powergood sink current	V_{PGOOD} = 0.5 V	2.5	7.5		mA
T_{PGDEL}	PGOOD delay	Delay for PGOOD in		64		µs
UVLO / LOGIC THRESHOLD						
V_{UVLO}	V5FILT UVLO threshold	Wake up (UVLO out)	3.4	3.7	3.9	V
		Hysteresis	200	300	400	mV
V_{EN_PSV}	EN_PSV connection	SKIP mode enabled		3.3V		
		PWM-Only mode enabled		FLOAT		
V_{EN_PSV}	EN_PSV logic input voltage	EN_PSV low	0.7	1	1.3	V
		Hysteresis	130	160	220	mV
		EN_PSV float	1.70	1.95	2.25	V
		EN_PSV high	2.2	2.5	2.9	V
		Hysteresis	100	170	250	mV
PROTECTION: OVERVOLTAGE (OVP) AND UNDERVOLTAGE (UVP)						
V_{OVP}	VFB OVP trip threshold	OVP detect	110%	115%	120%	
		Hysteresis		5%		
V_{UVP}	VFB UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		
T_{UVPDEL}	VFB UVP delay			32		µs
T_{UVPEN}	Output UVP enable delay			2		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal SDN threshold	Shutdown temperature(3)	145	160	175	°C
		Hysteresis(3)	10	12	14	°C
INTEGRATED MOSFET						
$R_{DS(on)upper}$	Upper MOSFET $R_{DS(on)}$	See (3)		19		mΩ
$R_{DS(on)lower}$	Lower MOSFET $R_{DS(on)}$	See (3)		7		mΩ

(3) Ensured by design. Not production tested.

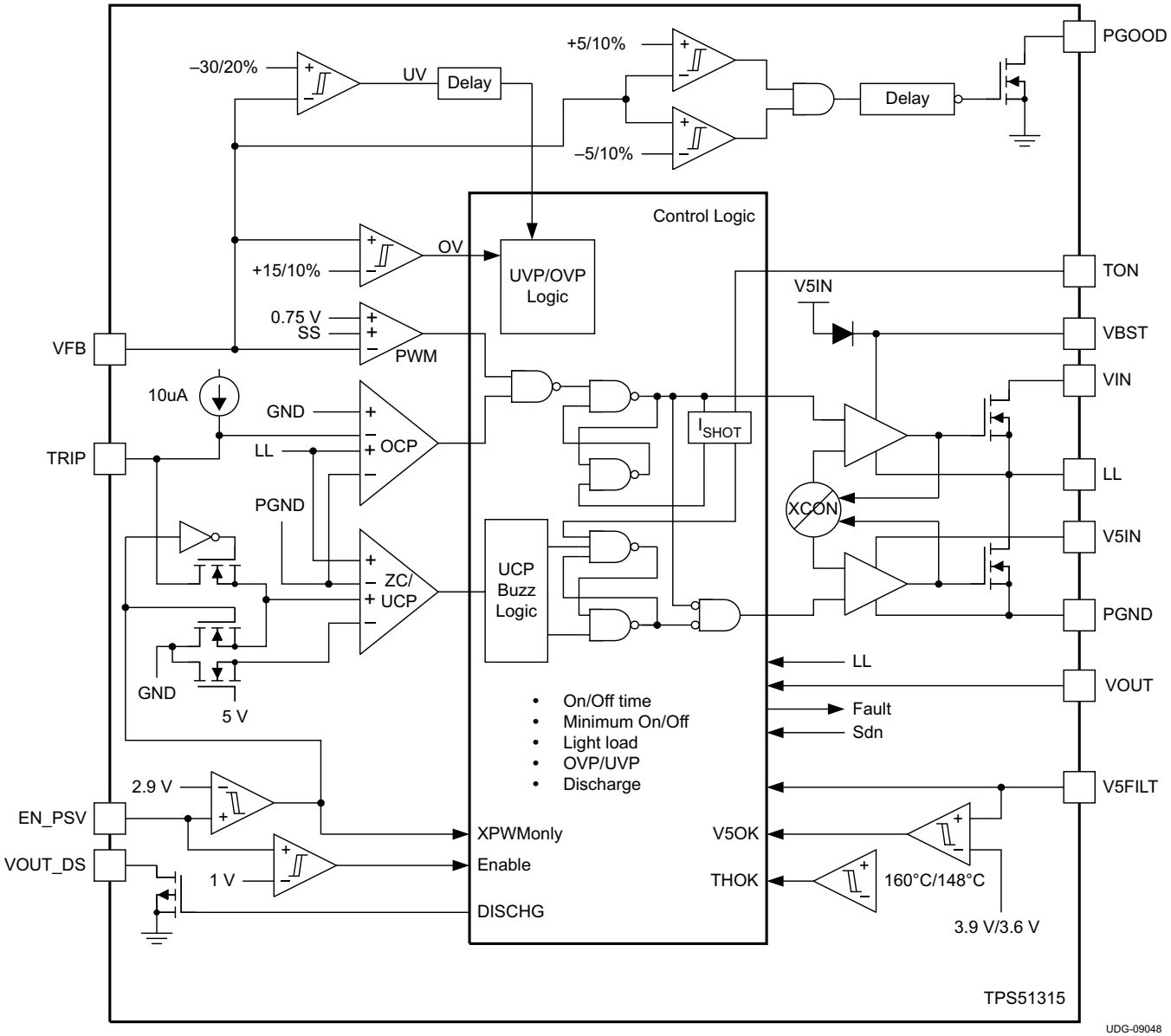
PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN_PSV	34	I	Enable/power-save pin. Connect to ground to disable switched-mode power supply (SMPS). Connect to 3.3 V or 5 V to turn on SMPS and enable skip mode. Float to turn on SMPS but disable skip mode (forced continuous conduction mode).
GND	1	I	Signal ground pin.
	2		
	4		
LL	16	I/O	Source node of the high-side power FET and drain node of the low-side power FET. Connect this pin to output inductor.
	17		
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26		
	27		
	28		
NC	29	—	No connection inside. Leave open.
	33		
PGND	3	I/O	Power GND. Source node of the low-side power FET.
	5		
	6		
	7		
	8		
	9		
	10		
PGOOD	40	O	Power-good window comparator: open drain output. Pull up to 5-V rail with a pull-up resistor. Current capability is 7.5 mA.
TON	35	I	On-time / frequency adjustment pin. Connect to LL with proper resistor to program switching frequency.
TRIP	32	I	Overcurrent trip point set input. Connect resistor from this pin to signal ground to set threshold for both overcurrent and negative overcurrent limit.
V5FILT	38	I	5-V power supply input for all control circuitry except gate drivers. Apply an R-C filter to reject high-frequency switching noise.
V5IN	31	I	5-V Power supply input for FET gate drivers. Internally connected to VBST by a PN diode. Connect a cpacitor with a value of 1 µF or greater between this pin and PGND to support instantaneous current for gate drivers.
VBST	30	I	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL-node. An internal PN diode is connected between V5IN to this pin. Add an external schottky diode if forward drop is critical to ensure efficient operation.
VFB	39	I	SMPS voltage feedback input. Connect the resistor divider here for adjustable output.
VIN	11	I	Input power source. Drain node of the high-side power FET.
	12		
	13		
	14		
	15		
VOUT	36	I	Connect to SMPS output. This terminal serves as the output voltage monitor for on-time adjustment.
VOUT_DS	37	O	Prebias start-up and selectable output discharge. It is also the input for the output discharge switch.

40-PIN RGY (QFN) PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Dual PWM Operations

The primary control loop of the switched-mode power supply (SMPS) functions as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ mode. D-CAP™ mode uses an internal compensation circuit and is suitable for a low external component count configuration with an appropriate amount of equivalent series resistance (ESR) at the output capacitor(s). The output voltage is monitored at a feedback point voltage.

At the beginning of each cycle, the upper synchronous MOSFET is turned on, or enters the ON state. This MOSFET is turned off, or enters the OFF state, after an internal one-shot timer expires. This one shot is determined by the input voltage (V_{VIN}) and the output volage (V_{OUT}) to maintain a relatively constant frequency over the input voltage range. This is called *adaptive on-time control* (see *PWM Frequency and Adaptive On-Time Control* section). The MOSFET is turned on again when feedback indicates an insufficient output voltage and the inductor current falls below the overcurrent limit. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous lower (rectifying) MOSFET is turned on at each OFF state in order to minimize the conduction losses.

The TPS51315 supports both PWM-Only and Auto-Skip operating modes. When the EN_PSV pin is grounded, the switcher is disabled. When the EN_PSV pin is connected to a 3.3-V supply or a 5-V supply, Auto-Skip mode is enabled. The rectifying MOSFET is turned off when the inductor current is zero. This feature enables a seamless transition to the reduced-frequency operation at light load conditions so that high efficiency is maintained over a broad range of load currents. When the EN_PSV pin is floated, it is internally pulled up to 1.9 V, and PWM-Only mode is enabled. In this mode, the rectifying MOSFET is not turned off when the inductor current reaches zero, and so the switching frequency does not change at light load; however the efficiency is lower in PWM-Only mode than it is in Auto-Skip mode.

The dc output voltage can be set by the external resistor divider as shown in Equation 1.

$$V_{OUT} = \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \times 0.75\,V \tag{1}$$

Light Load Conditions

When Auto-Skip mode is enabled, the TPS51315 automatically reduces the switching frequency under light load conditions to maintain high efficiency.

As the output current decreases from a heavy load condition, the inductor current is also reduced and eventually its *valley* falls to zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when zero inductor current is detected. As the load current continues to decrease, the converter runs in discontinuous conduction mode, taking longer to discharge the output capacitor toward the reference voltage. The on-time maintains the same as when under a heavy load condition. Alternatively, when the output current increase from light load to heavy load, switching frequency increases to the preset value as the inductor current reaches the continuous conduction threshold. The transition load point to the light load operation $I_{OUT(LL)}$ (that is, the threshold between continuous and discontinuous conduction mode) can be calculated using Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{2}$$

where

- f is the PWM switching frequency

Switching frequency versus output current under light load conditions is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from $I_{OUT(LL)}$ as calculated in Equation 2. For example, it is approximately 60 kHz at $I_{OUT(LL)}$/5 when the PWM frequency is 300 kHz.

PWM Frequency and Adaptive On Time Control

TPS51315 employs an adaptive on-time control scheme and does not include a dedicated oscillator on the device. However, the device runs with pseudo-constant frequency by feed-forwarding the input voltage and output voltage to the on-time, one-shot timer. The on-time control is inversely proportional to the input voltage and proportional to the output voltage, so that the duty ratio is maintained as V_{OUT}/V_{IN} with the same cycle time, as shown in Equation 3.

$$T_{ON} = 19 \times 10^{-12} \times R_{T(on)} \left(\frac{(2/3)V_{OUT} + 100\,mV}{V_{IN}} \right) + 50\,ns \quad (3)$$

where

- $R_{T(on)x}$ is the external resistor connected from T_{ON} to LL

For the TPS51315, the input voltage is monitored at the LL pin during the ON state. An advantage of switching-node monitoring is that any loss in the high-side n-channel FET becomes part of the on-time calculation, thereby making the frequency more stable with load.

Another consideration regarding frequency is jitter. Jitter may have many causes, but the constant on-time D-CAP mode scheme has some amount of inherent jitter. Because the output voltage ripple height is in the range of approximately 20 mV, on the order of a milli-volt of noise on the feedback signal can affect the frequency between approximately 3% and 10%. This is normal operation and risks only a small amount of influence to the power supply performance.

Soft-Start

The TPS51315 includes an independent, internal, 1.06-ms, voltage servo soft-start function with overcurrent limit. When the EN_PSV pin goes high, an internal digita-to-analog converter (DAC) begins ramping up the reference voltage to the error amplifier. Smooth control of the output voltage is maintained during start-up.

Powergood

The TPS51315 includes a powergood output function. The powergood function is activated after the soft-start function has completed. If the output voltage comes within ±5% of the target value, internal comparators detect a powergood state and the powergood signal becomes high after a 64-µs internal delay. If the output voltage rises above or falls below 10% of the target value, the powergood signal goes low immediately.

Output Discharge Control

The TPS51315 discharges output when EN_PSV is low or when the channel is in either a UVP or OVP fault condition. The TPS51315 discharges output using an internal 20-Ω MOSFET that is connected to VOUT_DS and PGND. The current capability of the MOSFET is limited to discharge slowly. An external resistor can be connected between VOUT_DS and VOUT to program discharge slow rate. In case the discharge function is not wanted, leave VOUT_DS open.

Overcurrent Limit

The TPS51315 has cycle-by-cycle overcurrent limit function. The inductor current is monitored during the OFF state using the low-side FET $R_{DS(on)}$ which is 7 mΩ (typ). The controller maintains the OFF state and does not release next ON cycle until the detected current comes down to the overcurrent trip level set by the TRIP resister. Because of this scheme, R_{TRIP} establishes the valley level of the inductor current. Note that the load current at the overcurrent threshold, I_{OCL}, is higher than this value calculated in Equation 4.

$$V_{TRIP} = \left(I_{OCL} - \left(\frac{I_{RIPPLE}}{2} \right) \right) \times 7\,m\Omega \tag{4}$$

R_{TRIP} value can be calculated by Equation 5, but cannot exceed 12.1-kΩ to protect the internal FETs from overloading.

$$R_{TRIP} = \frac{V_{TRIP}}{10\,\mu A} \tag{5}$$

Undercurrent Limit

The TPS51315 also supports a cycle-by-cycle undercurrent limit in PWM-Only mode. The undercurrent limit is the negative value of the overcurrent limit. If the output voltage continues to rise, the lower MOSFET is always on: thus, the inductor current reduces and reverses direction after it reaches zero (in PWM-Only mode). When there is too much negative current through the inductor, the lower MOSFET is turned off and the current flows to the VIN pin through the body diode of the upper MOSFET. Because there is less current with which to discharge the output capacitor, output voltage tends to rise, eventually reaching the overvoltage protection threshold and shutting down the TPS51315. In order to prevent triggering a false OVP shut down, the lower MOSFET is turned on 400-ns after it is turned off. If the device reaches an undercurrent threshold again before the output voltage is discharged to the target level, the lower MOSFET is turned off and the process repeats. This logic is called *UCL Buzz*. It ensures maximum allowable discharge capability when the output voltage continues to rise. Alternatively, if the output voltage is discharged to the target level before the UCL threshold is reached, the lower MOSFET is turned off, the upper MOSFET is then turned on, and the device resumes normal operation.

Overvoltage Protection

The TPS51315 monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage becomes greater than 115% of the target value, the upper MOSFET is turned off and the lower MOSFET is turned on immediately. The output is also discharged by the internal 20-Ω transistor if it is connected to VOUT_DS.

The, TPS51315 monitors the output voltage directly. If it becomes greater than 5.75 V, TPS51315 turns off the upper MOSFET driver. In no case should the device operate at more than 6 V, as damage would occur.

Undervoltage Protection

When the feedback voltage becomes lower than 70% of the target value, the undervoltage comparator output goes high and an internal UVP delay counter begins to increment. After 32 µs, TPS51315 latches off both the upper and lower MOSFETs and discharges the output with the internal 20-Ω transistor if it is connected to VOUT_DS. This function is enabled after 2ms from when EN_PSV is brought high, i.e., UVP is disabled during the start up.

UVLO Protection

The TPS51315 has V5FILT undervoltage lockout (UVLO) protection. When the V5FILT voltage is lower than UVLO threshold voltage, TPS51315 is shut off. This protection is not latched.

Thermal Shutdown

The TPS51315 includes a die-temperature monitor function. If the temperature exceeds the threshold value (typically 160°C), TPS51315 shutd off. This protection is not latched. The device recovers once the temperature has cooled to 148°C.

TYPICAL CHARACTERISTICS

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

PWM SUPPLY CURRENT vs JUNCTION TEMPERATURE

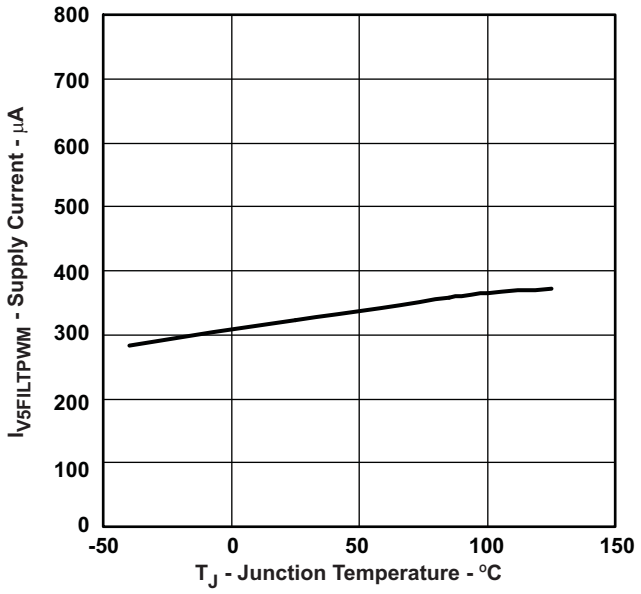


Figure 1.

V5FILT SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

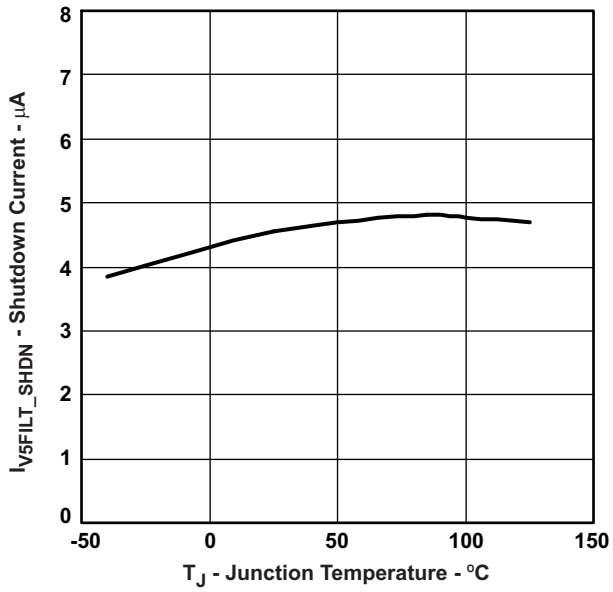


Figure 2.

TRIP CURRENT vs JUNCTION TEMPERATURE

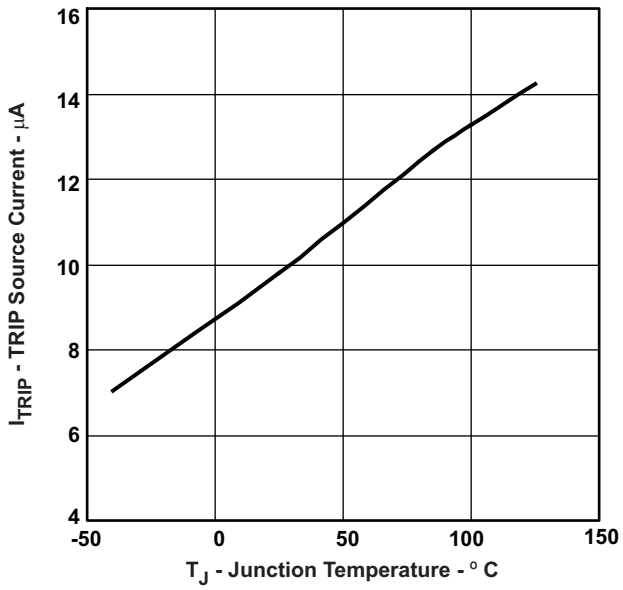


Figure 3.

OVP/UVP THRESHOLD vs JUNCTION TEMPERATURE

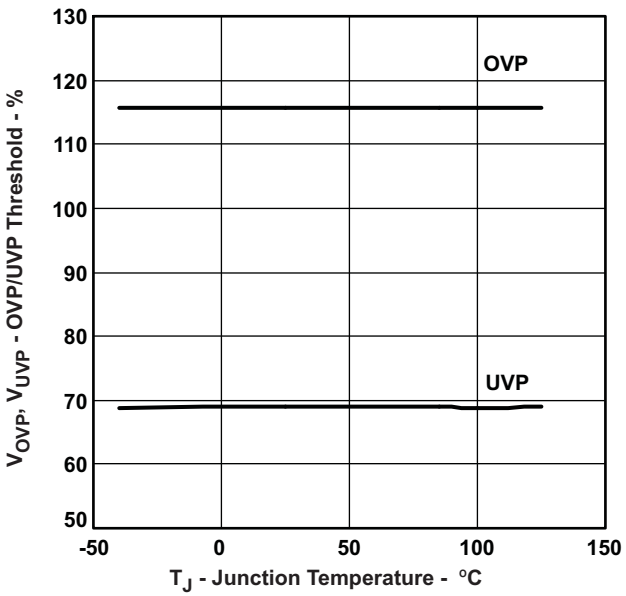


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

SWITCHING FREQUENCY vs OUTPUT CURRENT

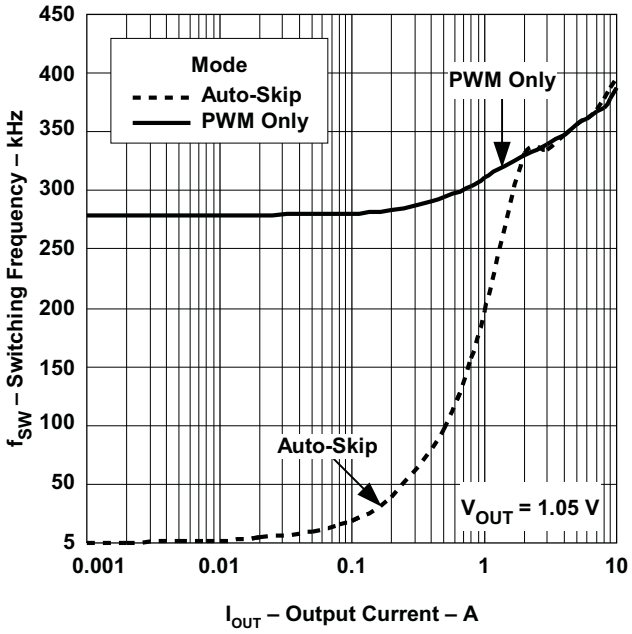


Figure 5.

SWITCHING FREQUENCY vs OUTPUT CURRENT

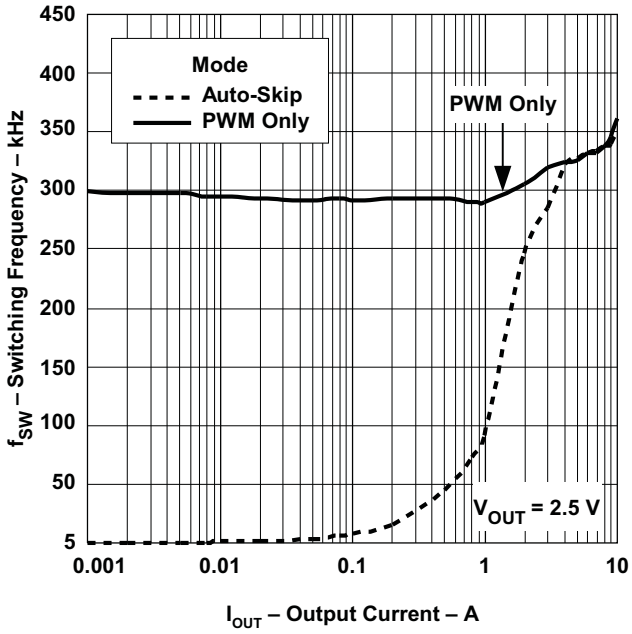


Figure 6.

OUTPUT VOLTAGE vs OUTPUT CURRENT

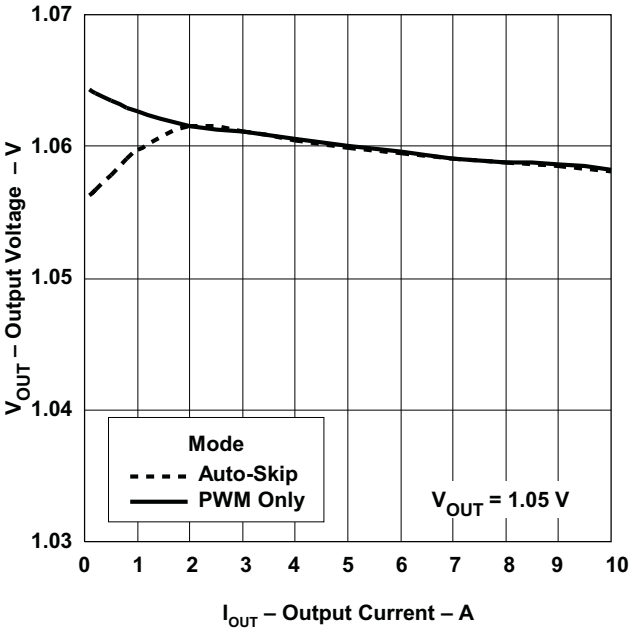


Figure 7.

OUTPUT VOLTAGE vs OUTPUT CURRENT

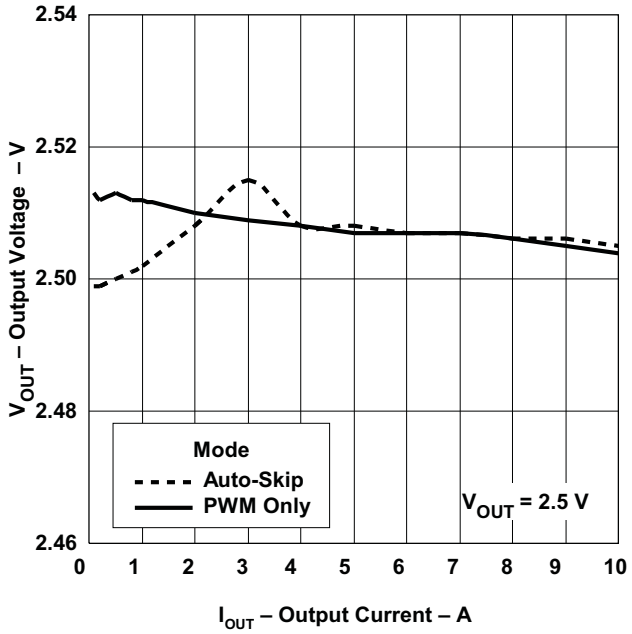


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

OUTPUT VOLTAGE vs INPUT VOLTAGE

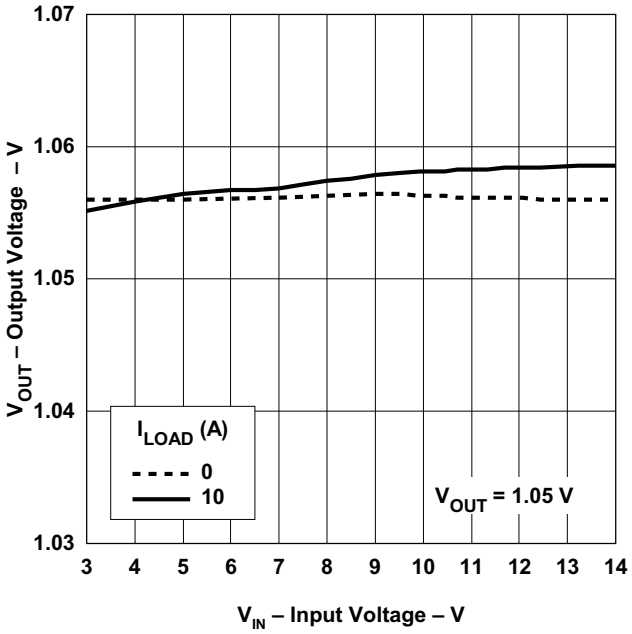


Figure 9.

OUTPUT VOLTAGE vs INPUT VOLTAGE

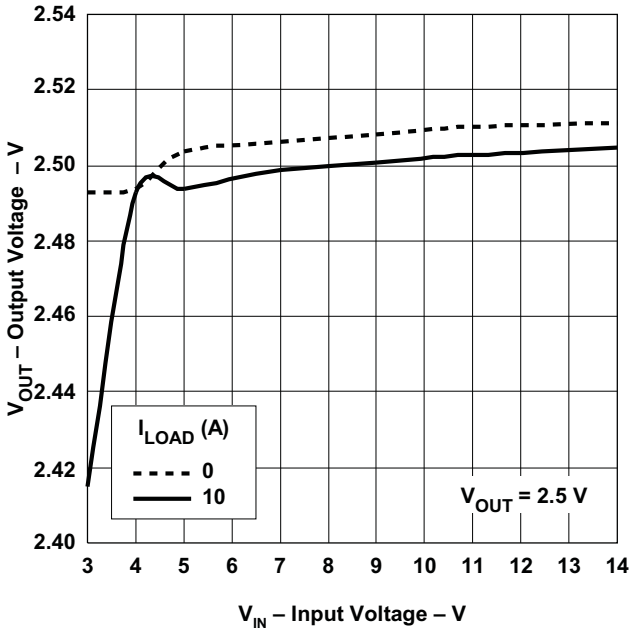


Figure 10.

SWITCHING FREQUENCY vs INPUT VOLTAGE

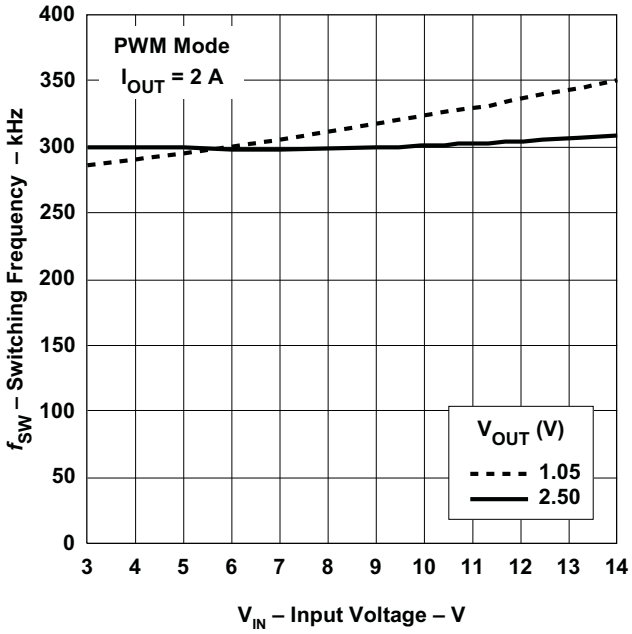


Figure 11.

MEASURED SWITCHING FREQUENCY vs ON-TIME RESISTANCE

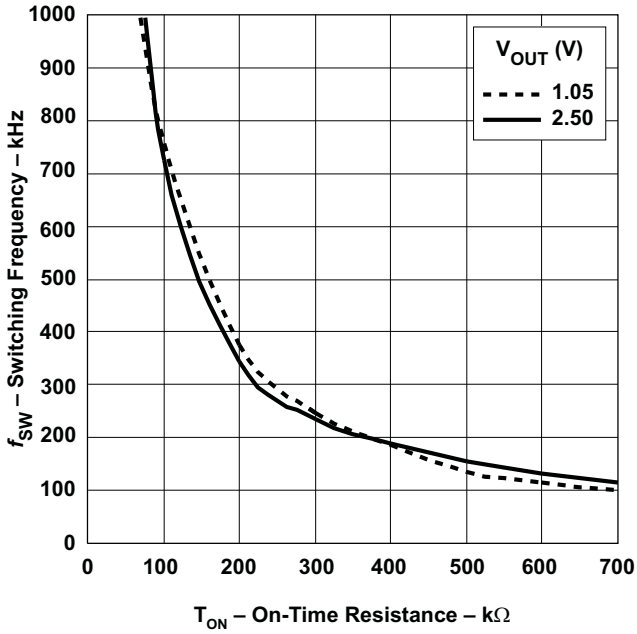


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

EFFICIENCY
vs
OUTPUT CURRENT

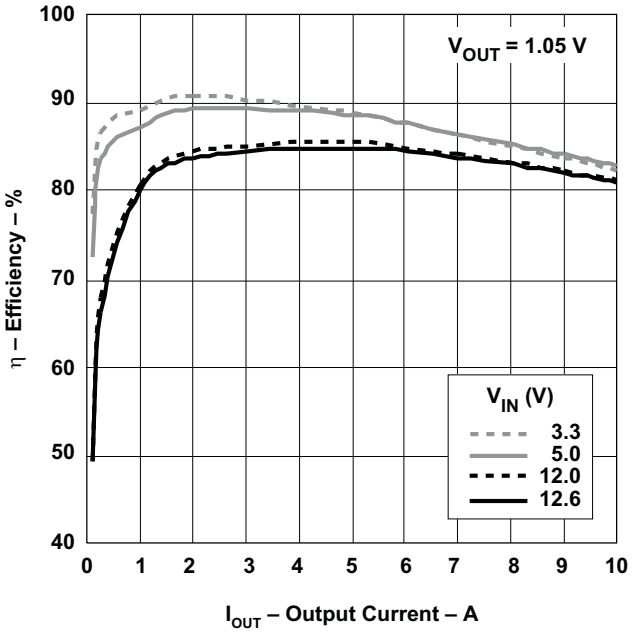


Figure 13.

EFFICIENCY
vs
OUTPUT CURRENT

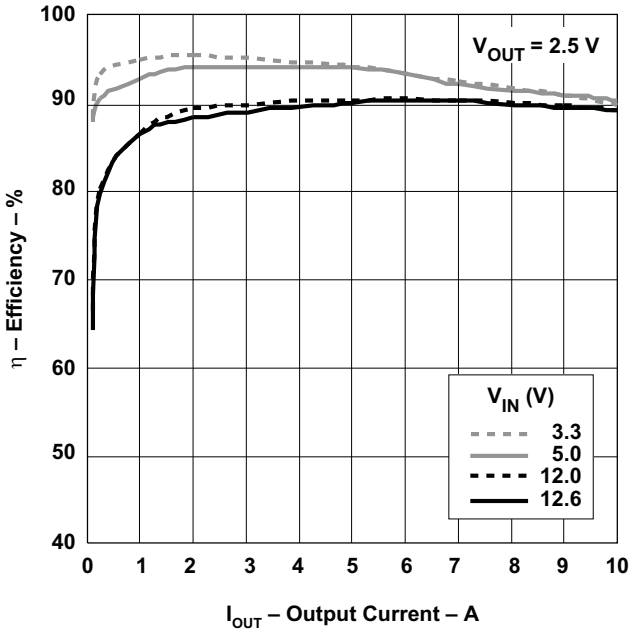


Figure 14.

EFFICIENCY
vs
OUTPUT CURRENT

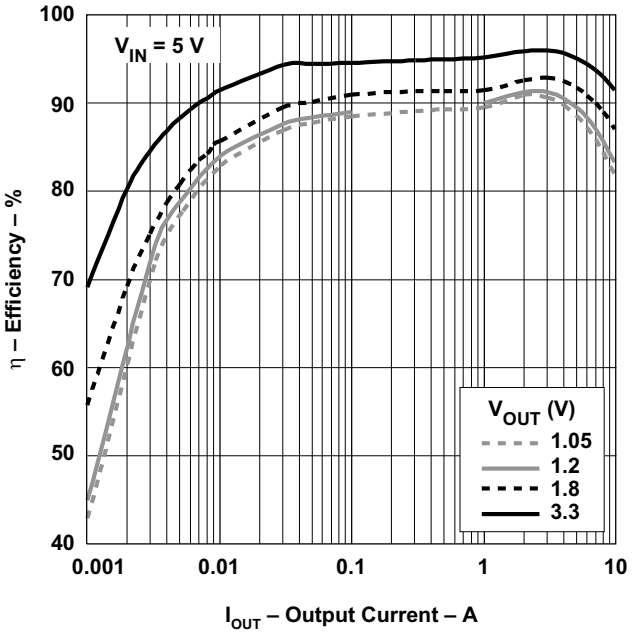


Figure 15.

EFFICIENCY
vs
OUTPUT CURRENT

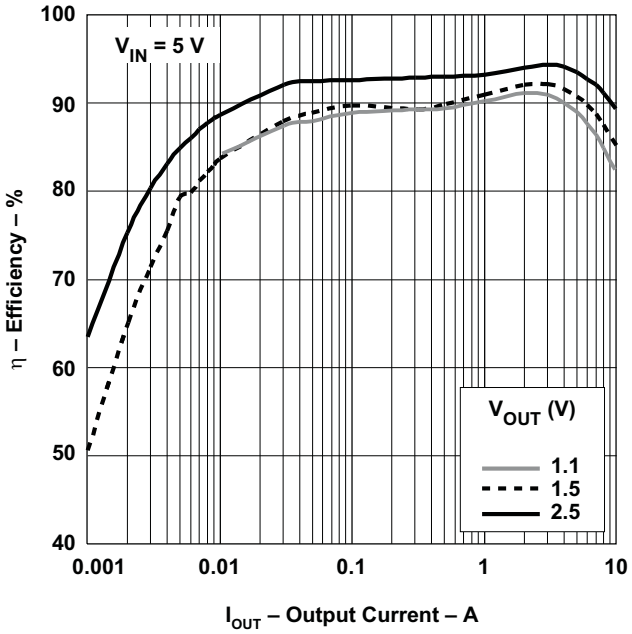


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

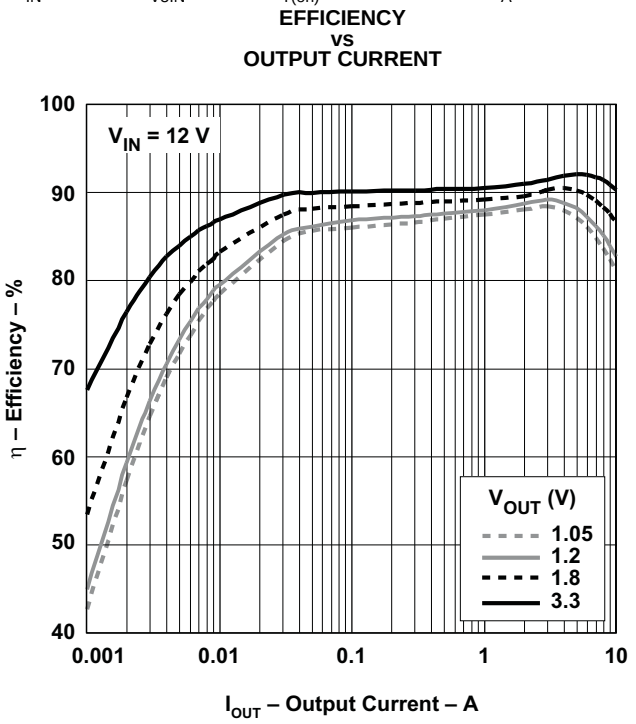


Figure 17.

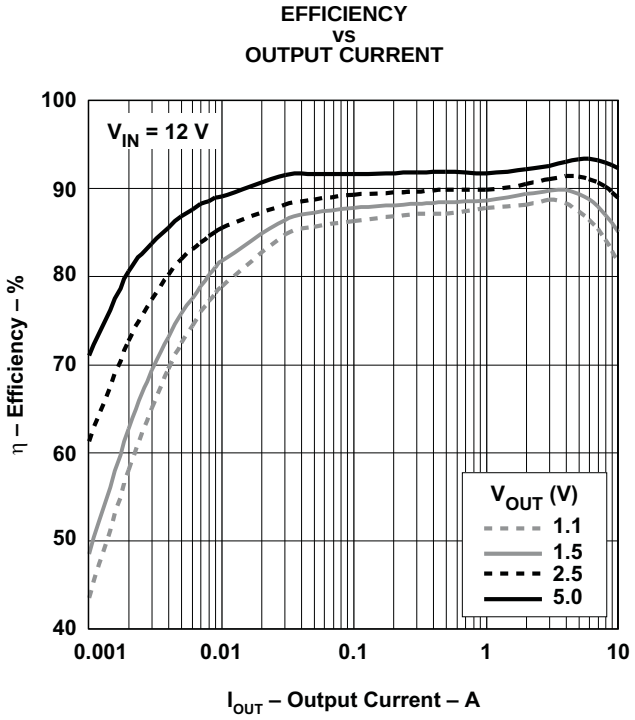


Figure 18.

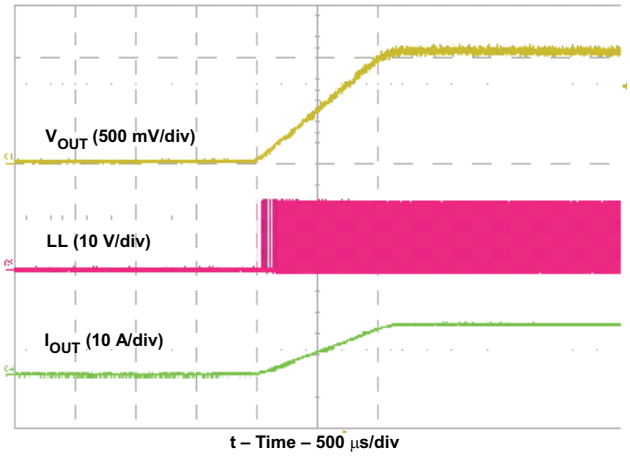


Figure 19. 1.05-V Start-Up Waveforms (Heavy Load)

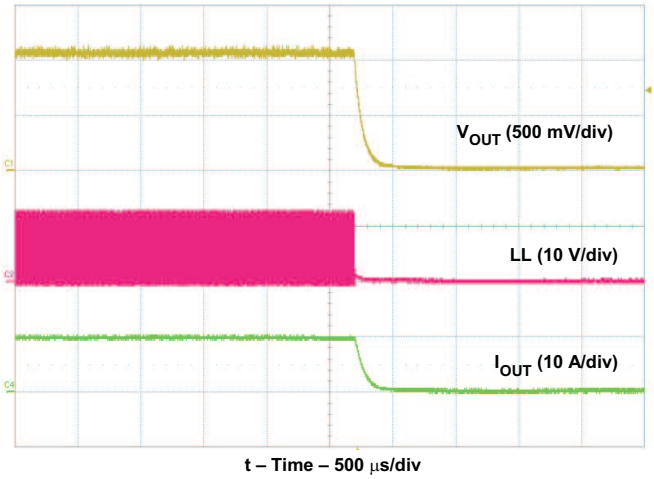


Figure 20. 1.05-V Shut-Down Waveforms (Heavy Load)

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = 12 V, V_{V5IN} = 5 V, $R_{T(on)}$ = 237 kΩ, and T_A = 25°C, unless otherwise noted.

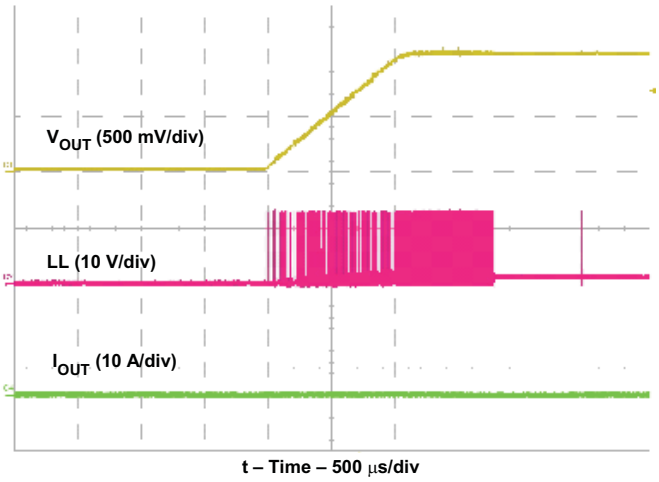


Figure 21. 1.05-V Start-Up Waveforms (Light Load)

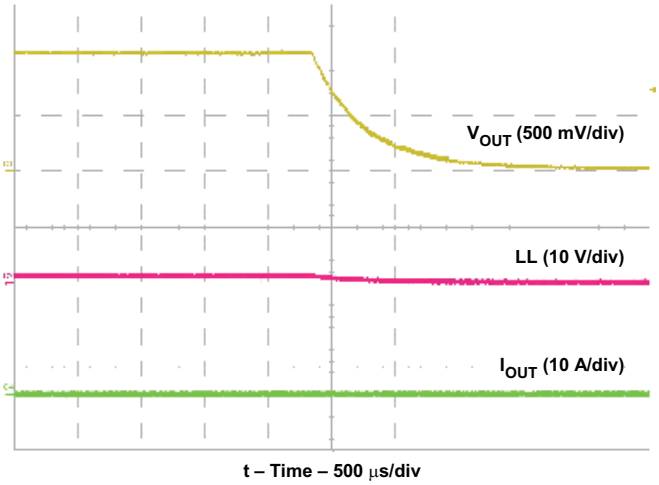


Figure 22. 1.05-V Shut-Down Waveforms (Light Load)

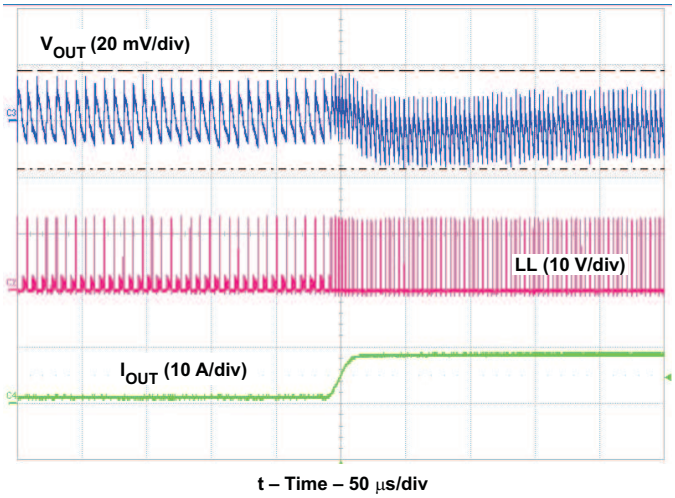


Figure 23. 1.05-V Load Step-Up Waveforms

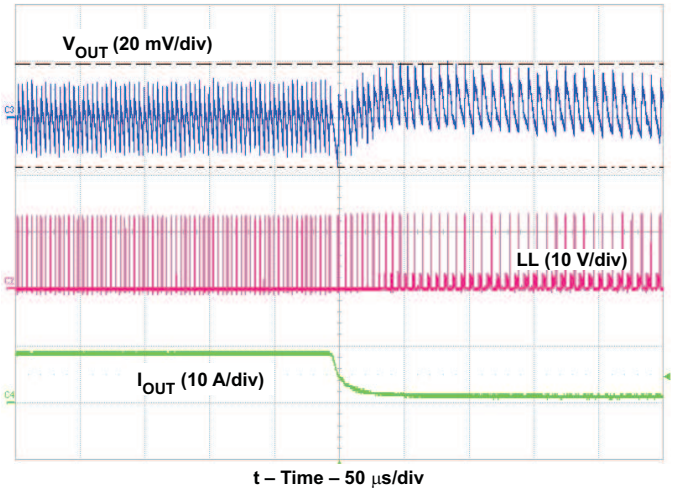


Figure 24. 1.05-V Load Step-Down Waveforms

APPLICATION INFORMATION

Loop Compensation and External Parts Selection

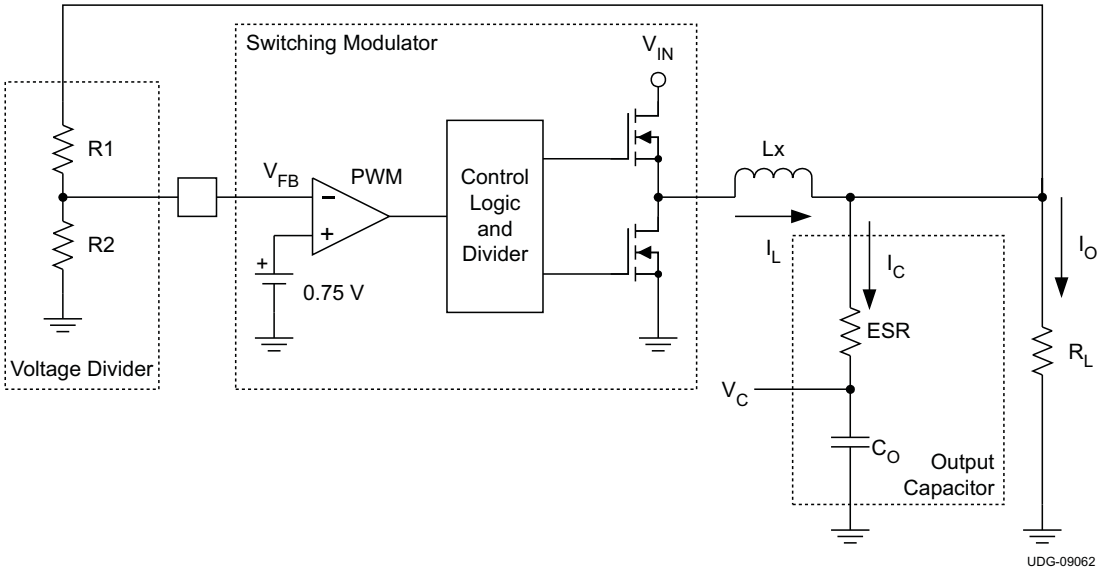


Figure 25. Simplified Modulator Block Diagram

The feedback voltage (V_{VFB}) is compared to the internal reference voltage after the divider resistors. The PWM comparator determines when to turn on the upper MOSFET. The gain and speed of the comparator is high enough to maintain the voltage level relatively constant at the beginning of each on cycle, or at the end of each off cycle . The dc output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increases.

For loop stability, the 0 dB frequency, f_0, defined in Equation 6 must be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \tag{6}$$

Because f_0 is determined solely by the output capacitor characteristics, the loop stability of the D-CAP™ Mode is determined by capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have and output capacitance on the order of several hundred micro-farads and and ESR of approximately 10 mΩ. These values make f_0 on the order of 100 kHz or less and create a stable loop. However, ceramic capacitors have an f_0 of more than 700 kHz, which is not suitable for this operating mode, although the D-CAP™ Mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time. These advantages are realized because there is no error amplifier in the loop, so a sufficient feedback signal is required from an external circuit to reduce the jitter level. The required signal level is approximately 15 mV at the comparing point. This generates output ripple at the output node that can be calculated in Equation 7. The output capacitor ESR should meet this requirement.

$$V_{RIPPLE} = \left(V_{OUT} / 0.75 \right) \times 15 \text{ mV} \tag{7}$$

For applications with all ceramic output capacitors, a few external components need to be added to ensure the loop stability. Please refer to Figure 29. Since ceramics capacitors have low ESR, feedback ripple in phase with inductor current is recommended. R-C network across the output inductor can mimic inductor current when RC ≈ L / DCR, the ripple current can be coupled to the feedback through a 1-µF capacitor.

External Component Selection

External component selection is a simple process in D-CAP™ Mode.

1. Determine the value of R1 and R2.

   The recommended R2 value is 10 kΩ to 100 kΩ. Calculate R1 by using Equation 8.

$$R1 = \frac{V_{OUT} - 0.75}{0.75} \times R2 \tag{8}$$

2. Choose $R_{T(on)}$

   The switching frequency is usually determined by overall view of the dc-dc converter designer in consideration of size, efficiency or cost, and mostly dictated by external component constraints such as the size of inductor and/or the output capacitor. If an extremely low or high duty factor is expected, the minimum on-time or off-time must also be considered to satisfy the required duty factor. Once the switching frequency is decided, $R_{T(on)}$ can be determined by Equation 9 and Equation 10.

$$T_{ON(max)} = \frac{1}{f} \times \frac{V_{OUT}}{V_{IN(min)}} \tag{9}$$

$$R_{T(on)} = \frac{3}{2} \times \frac{\left(T_{ON(max)} - 50\,ns\right)}{19 \times 10^{-12}} \times \frac{V_{IN(min)}}{\left(V_{OUT} + 150\,mV\right)} \left(\Omega\right) \tag{10}$$

3. Choose the inductor.

   To begin, choose an inductance value where the ripple current is approximately 1/4 to 1/2 of the maximum output current.

$$L_{IND} = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{11}$$

   For applications that require a fast transient response with a minimum of V_{OUT} overshoot, consider a smaller inductance value than calculated in Equation 11. The cost of a small inductance value is higher steady-state ripple, larger line regulation, and higher switching loss.

   The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above the peak inductor current before saturation. The peak inductor current can be estimated by Equation 12.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{12}$$

4. Choose output capacitor(s).

   Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine an ESR to meet the required ripple voltage. A quick approximation is shown in Equation 13.

$$ESR = \frac{V_{OUT} \times 0.015}{I_{RIPPLE} \times 0.75} \approx \frac{V_{OUT}}{I_{OUT(max)}} \times 60\ (m\Omega) \tag{13}$$

5. Choose an R_{TRIP} value.

   Select an appropriate R_{TRIP} value with the considerations shown in Equation 14. Maximum R_{TRIP} should be less than 12.1 kΩ.

$$R_{TRIP} = \frac{I_{OUT(max)} \times 7\,m\Omega}{I_{TRIP(min)}} \quad (14)$$

6. V5FILT input capacitor.

   In order to reject high-frequency noise possibly contained on +5-V supply and V5IN voltages, apply 1-µF of ceramic capacitor closely at the V5FILT pin with a 10-Ω resistor to create a low-pass filter between +5-V supply and the pin.

7. Applying the VBST capacitor and VBST diode.

   Apply 0.1-µF MLCC between VBST and the LL node as the flying capacitor for internal high-side FET driver. The TPS51315 has its own on-board boost diode between V5IN and VBST. This diode is a P-N junction diode and strong enough for most typical applications. However, if efficiency has priority over cost, the designer may add a Schottky diode externally to improve the gate drive voltage of the high-side FET. A Schottky diode has a higher leakage current, especially at high temperatures, than a P-N junction diode. A low-leakage diode should be selected in order to maintain VBST voltage during low-frequency operation in Auto-Skip mode.

Layout Considerations

Certain concepts must be considered before starting printed curcuit board (PCB) layout work using the TPS51315.

- Connect the R-C low-pass filter from the 5-V supply to the V5FILT pin. A filter resistance of 10 Ω and a filter capacitance of 1 µF is recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inches) if possible.
- Connect the overcurrent setting resistors from TRIP to GND close to the device if possible. The trace from TRIP to the resistor and from the resistor to GND should avoid coupling to a high-voltage switching node.
- The discharge path (V_{OUT_DS}) should have a dedicated trace to the output capacitor(s); separate from the output voltage sensing trace, and use a 1,5 mm (60 mils) or wider trace with no loops. Make sure the feedback current setting resistor (the resistor between VFB to GND) is tied close to the device GND. The trace from this resistor to the VFB pin should be short and narrow. Place the trace on the component side and avoid vias between this resistor and the device.
- All sensitive analog traces and components such as VOUT, VFB, GND, EN_PSV, PGOOD, TRIP, V5FILT, and TON should be placed away from high-voltage switching nodes such as LL or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback traces from power traces and components.
- Gather the ground terminals of the V_{IN} capacitor(s), V_{OUT} capacitor(s), and the PGND as close as possible. GND (signal ground) and PGND (power ground) should be connected strongly together near the device. The PCB trace defined as LL node, which connects to the source of the upper MOSFET, the drain of the lower MOSFET, and the high-voltage side of the inductor, should be as short and wide as possible.

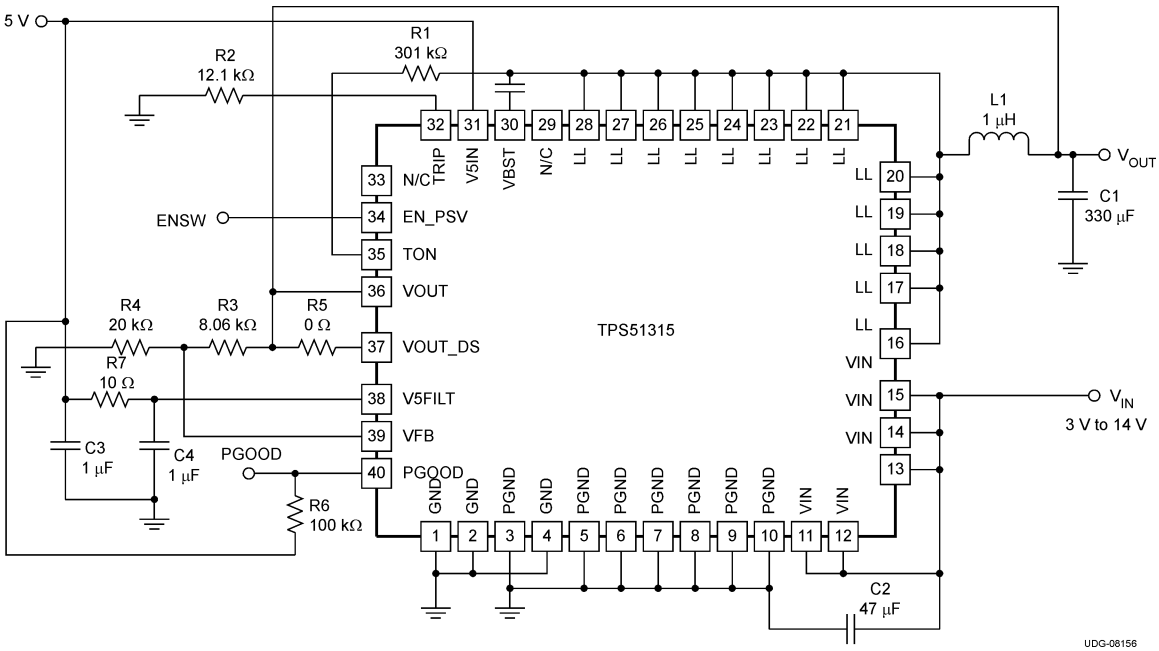


Figure 26. Typical 1.05-V/10-A Application

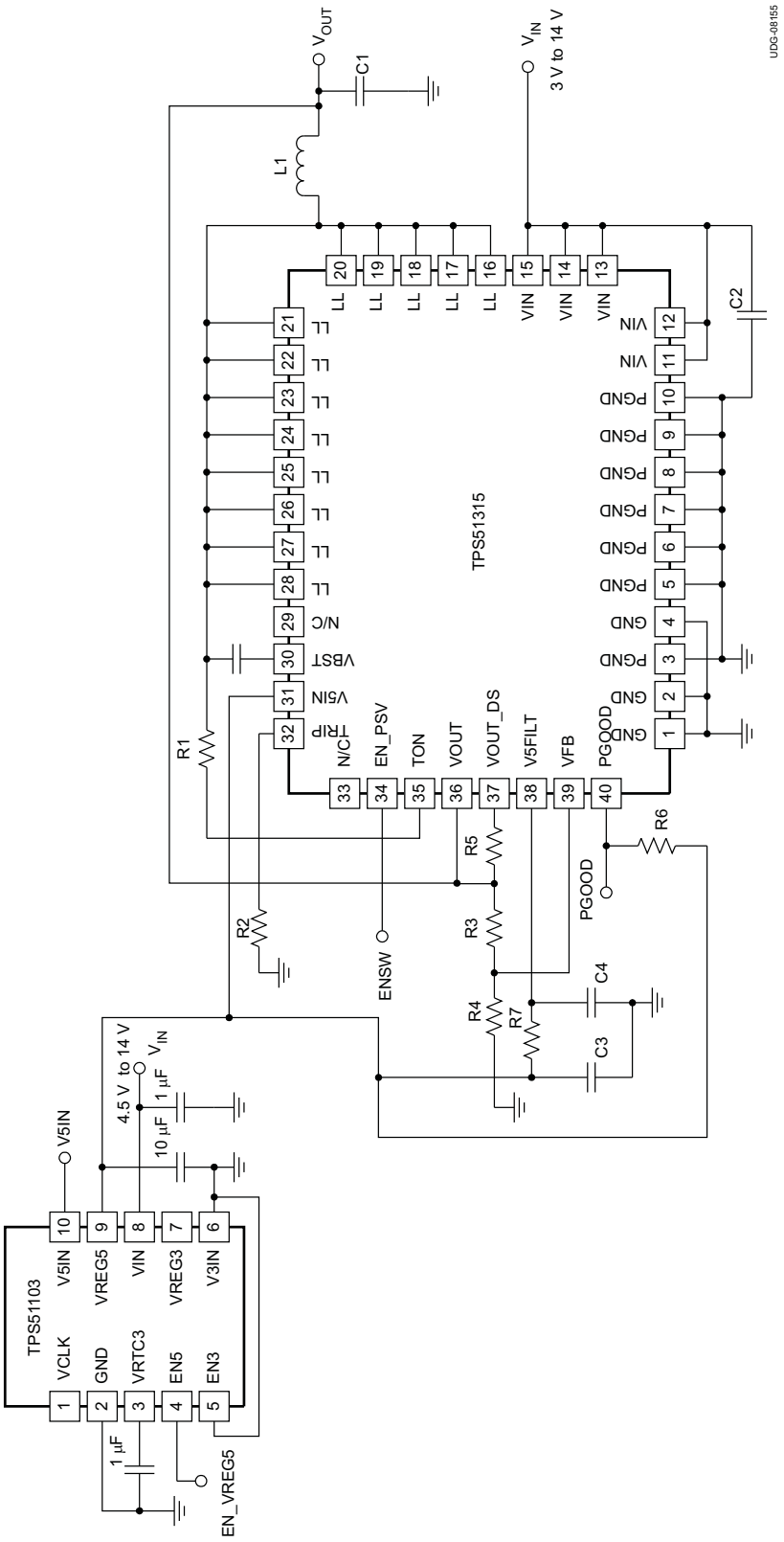


Figure 27. 1.05-V/10-A Applications with TPS51103

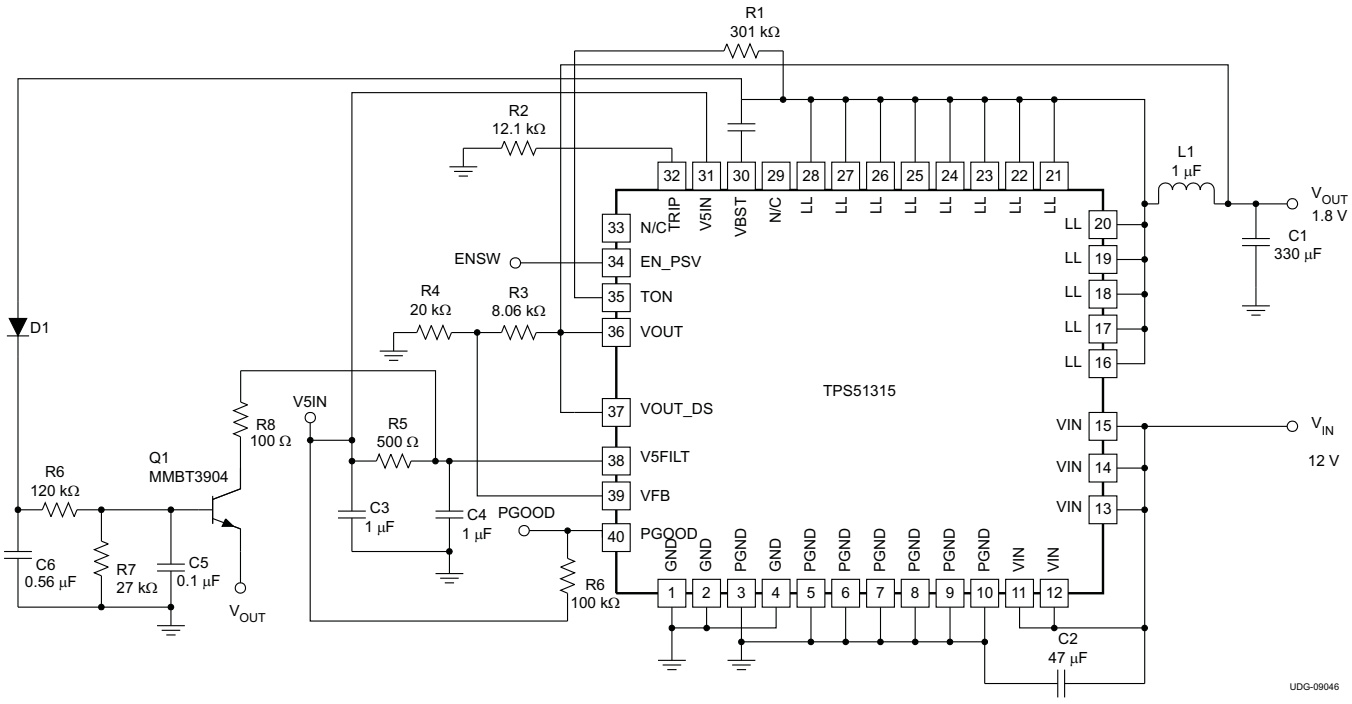


Figure 28. Typical 1.05-V/10-A Application with Hiccup Operation Mode

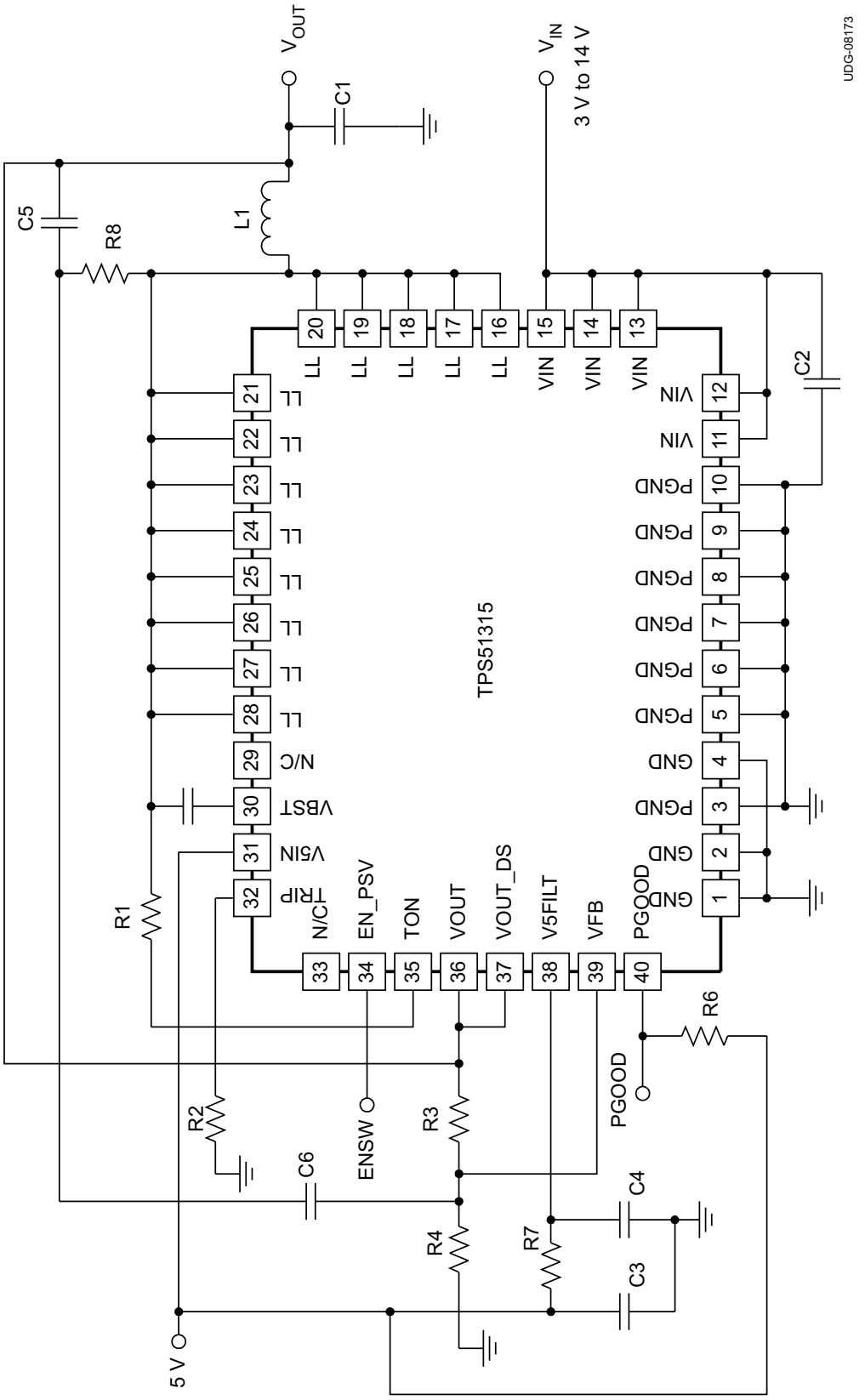


Figure 29. Typical Applications with All Ceramic Output

REVISION HISTORY

Changes from Original (MAY 2009) to Revision A	Page
• Changed pinout to reflect correct placement of Pin 1 registration mark	7

Changes from Revision A (MAY 2011) to Revision B	Page
• Changed ESD HBM rating from "1.5 kV" to "2.0 kV" (typographical error)	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51315RGFR	NRND	VQFN	RGF	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 51315	
TPS51315RGFT	NRND	VQFN	RGF	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 51315	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

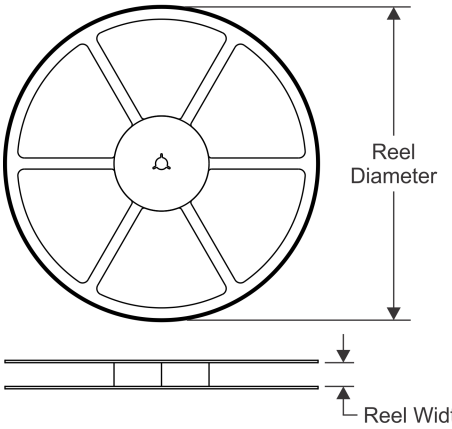
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

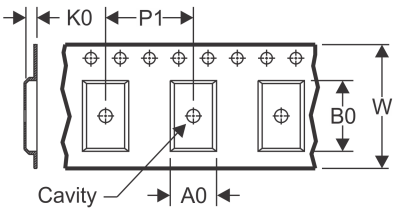
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

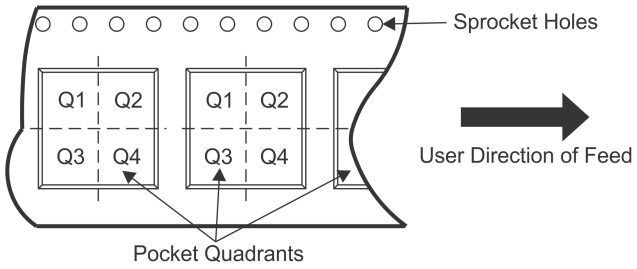


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

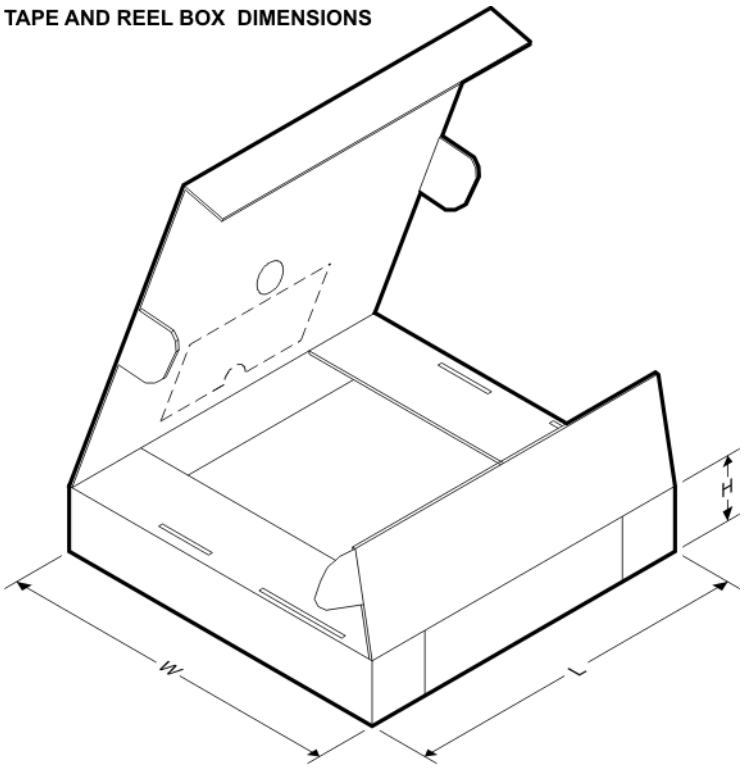
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51315RGFR	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TPS51315RGFT	VQFN	RGF	40	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TPS51315RGFT	VQFN	RGF	40	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

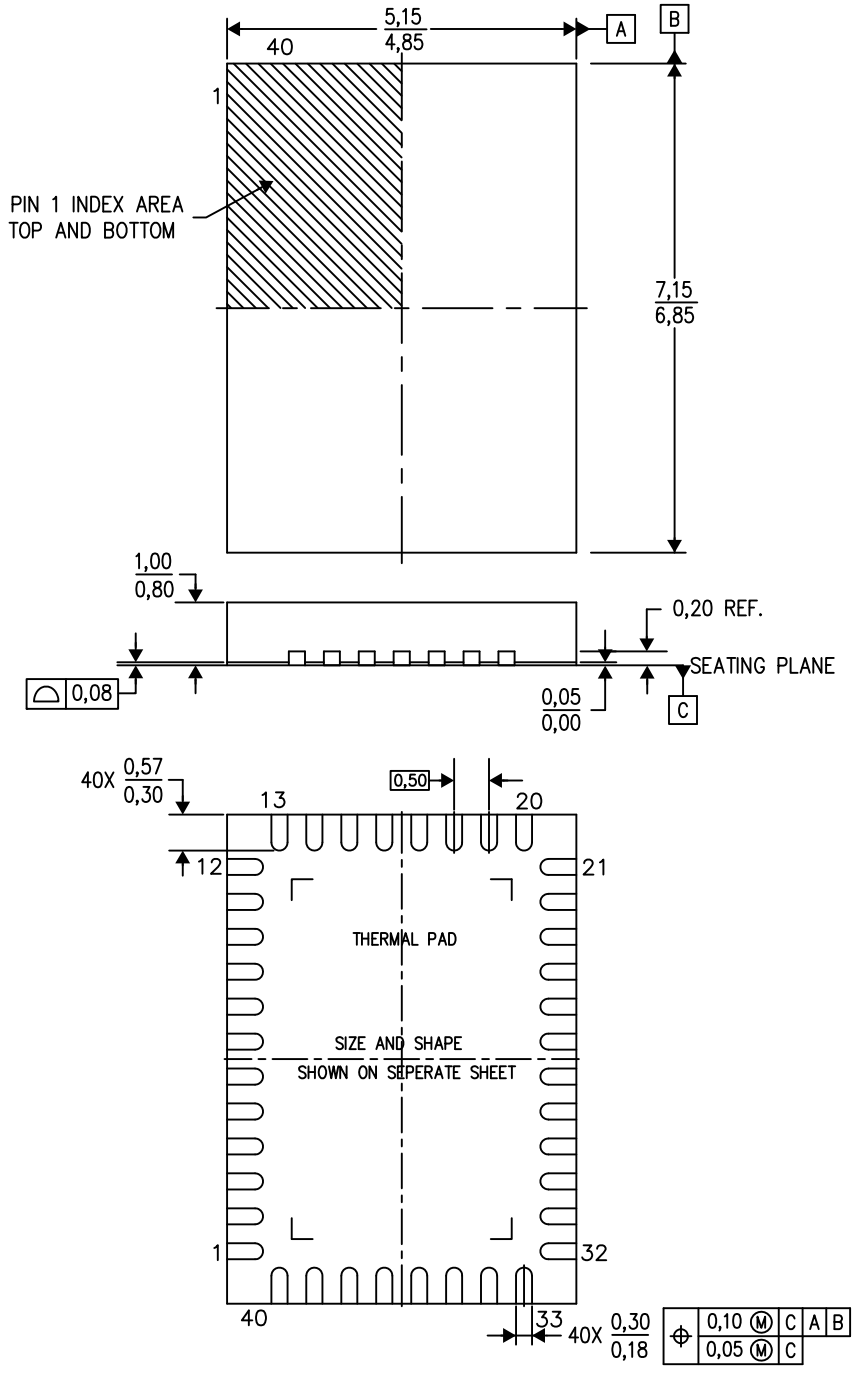
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51315RGFR	VQFN	RGF	40	3000	367.0	367.0	38.0
TPS51315RGFT	VQFN	RGF	40	250	210.0	185.0	35.0
TPS51315RGFT	VQFN	RGF	40	250	210.0	185.0	35.0

RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding lands and the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

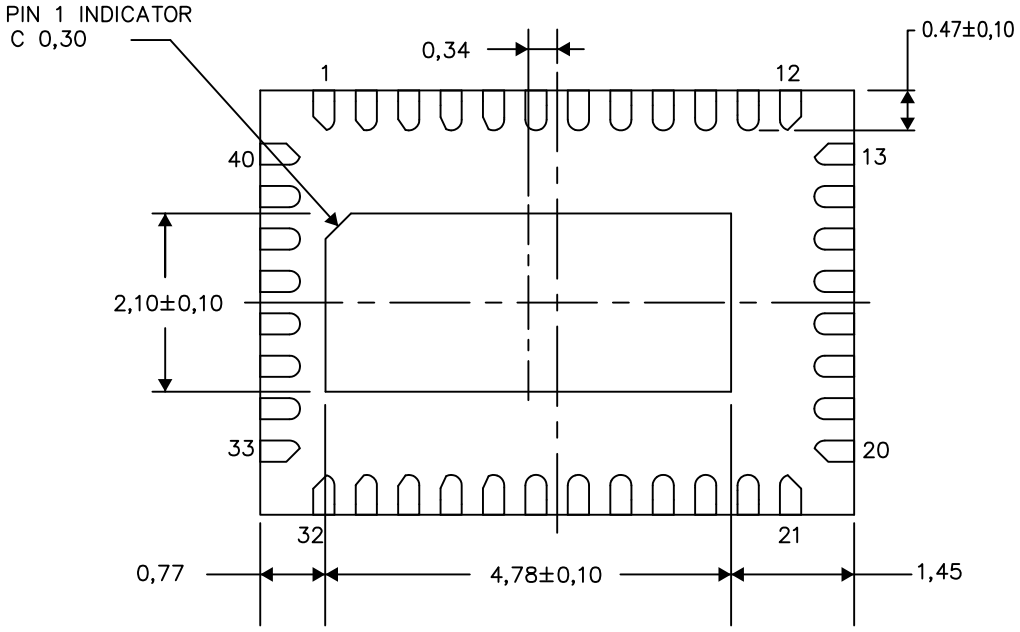
RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



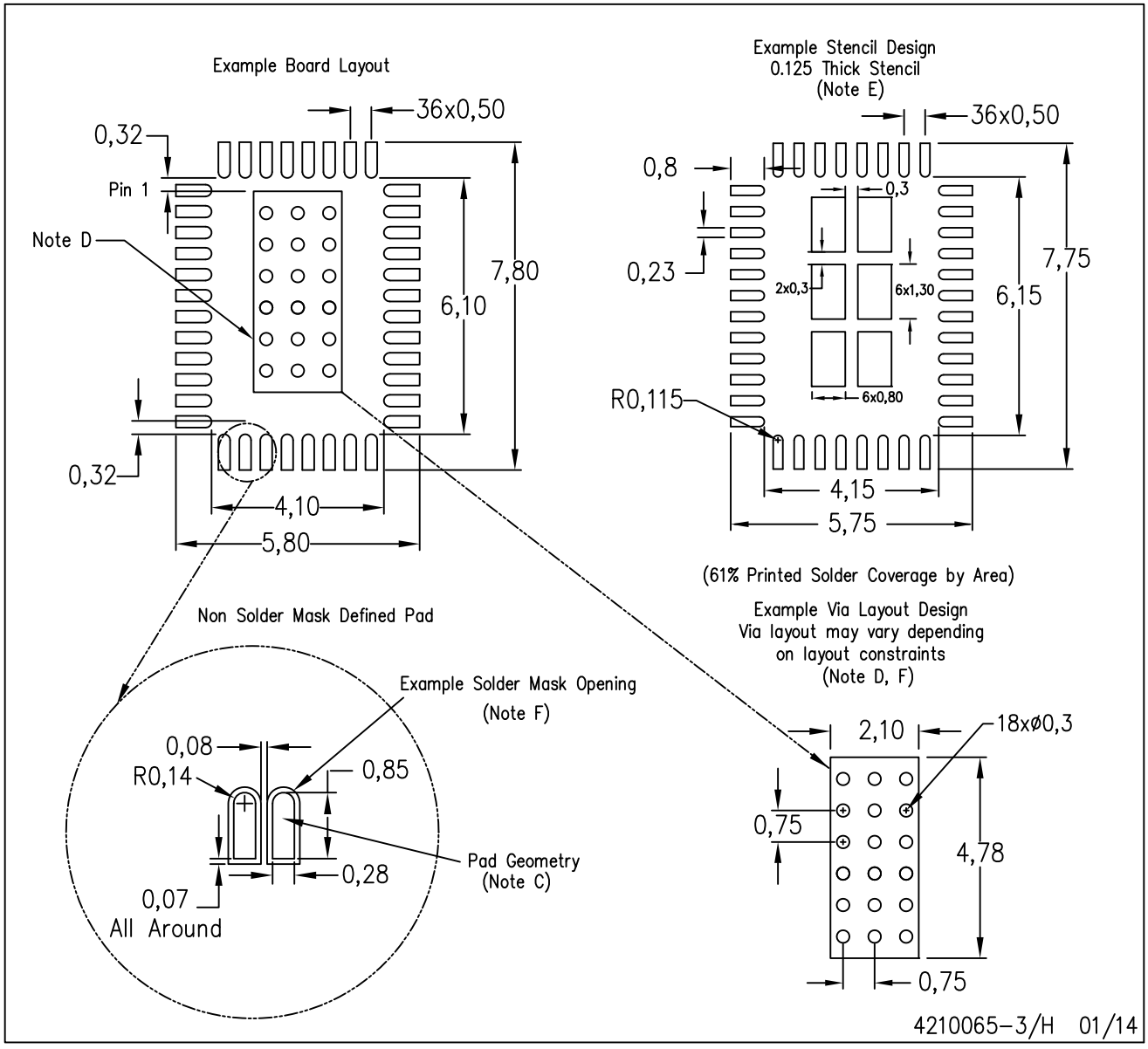
Bottom View

Exposed Thermal Pad Dimensions

4206345–7/N 01/14

NOTE: A. All linear dimensions are in millimeters

RGF (R–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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