# TPS22970 3.6-V, 4-A, 5.3-mΩ On-Resistance Load Switch

## 1 Features

- Input Voltage Range ($V_{IN}$): 0.65 V to 3.6 V
- On-Resistance
  - $R_{ON}$ = 5.3 mΩ (Typical) at $V_{IN}$ ≥ 1.8 V
  - $R_{ON}$ = 5.8 mΩ (Typical) at $V_{IN}$ = 1.05 V
  - $R_{ON}$ = 7.5 mΩ (Typical) at $V_{IN}$ = 0.65 V
- Maximum Continuous Switch Current ($I_{MAX}$): 4 A
- ON State ($I_Q$): 35 µA (Typical) at $V_{IN}$ = 3.6 V
- OFF State ($I_{SD}$): 1 µA (Typical) at $V_{IN}$ = 3.6 V
- Controlled Slew Rate to Avoid Inrush Current
- Low Threshold Enable (ON) Supports Use of Logic as Low as 0.9 V ($V_{IH}$) of Logic
- Thermal Shutdown ($T_{SD}$): $T_J$ > 125°C
- Quick Output Discharge (QOD): 150-Ω (Typical)

## 2 Applications

- Notebook, Tablet
- Industrial PC
- Smartphones
- Telecom
- Storage

## 3 Description

The TPS22970 is a small, space-saving load switch with controlled turn on to reduce inrush current. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.65 V to 3.6 V and pulsed switch currents up to 4 A. An integrated charge pump biases the NMOS switch in order to achieve a minimum switch ON resistance ($r_{ON}$). The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22970 is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range.

The TPS22970 also offers an integrated 150-Ω onchip load resistor for quick output discharge when the switch is turned off, which insures that the output is not left floating.

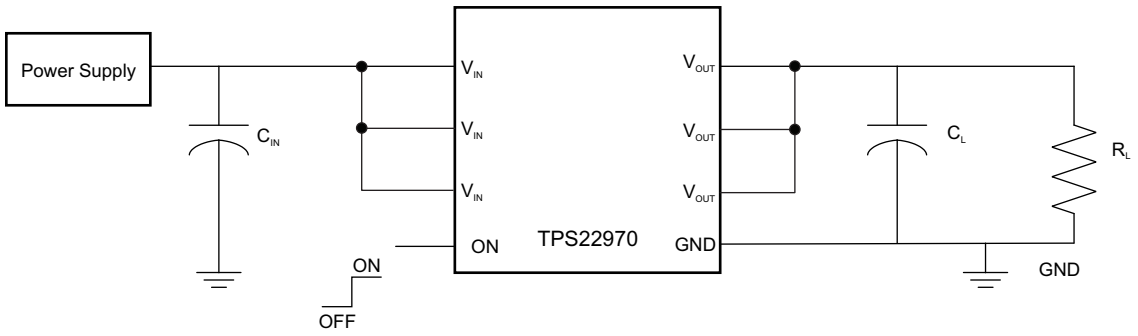
The TPS22970 has an internally controlled rise time in order to reduce inrush current. The TPS22970 is available in an ultra-small, space saving 8-pin WCSP package and is characterized for operation over the free-air temperature range of –40°C to +105°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS22970YZPT | DSBGA (8) | 1.90 mm × 0.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application**



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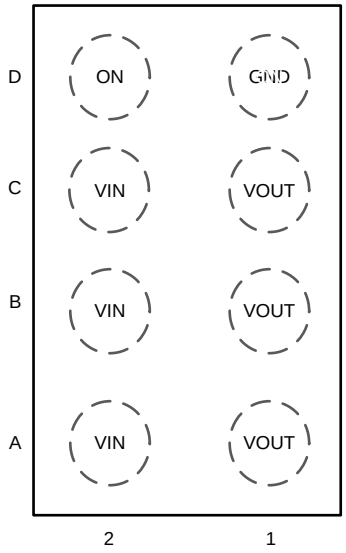
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

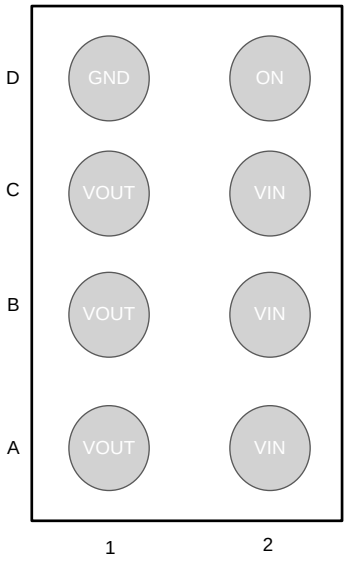
| DATE | REVISION | NOTES |
|---|---|---|
| May 2017 | * | Initial release. |

# 5 Pin Configuration and Functions

**YZP Package**
**8-Pin DSBGA**
**Laser Marking View**




**YZP Package**
**8-Pin DSBGA**
**Bump View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | D1 | GND | Ground |
| ON | D2 | I | Switch control input. Do not leave floating |
| $V_{IN}$ | A2 | I | Switch input, bypass this input with a ceramic capacitor to ground |
| | B2 | | |
| | C2 | | |
| $V_{OUT}$ | A1 | O | Switch output |
| | B1 | | |
| | C1 | | |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | –0.3 | 4 | V |
| $V_{OUT}$ | Output voltage | –0.3 | 4 | V |
| $V_{ON}$ | ON voltage | –0.3 | 4 | V |
| $V_{PG}$ | PG voltage | –0.3 | 4 | V |
| $I_{MAX}$ | Maximum continuous switch current | | 4 | A |
| $I_{PLS}$ | Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle | | 6 | A |
| $T_J$ | Maximum junction temperature | Internally Limited | | |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 0.65 | 3.6 | V |
| $V_{OUT}$ | Output voltage | | $V_{IN}$ | V |
| $V_{IH}$ | High-level input voltage, ON | 0.9 | 3.6 | V |
| $V_{IL}$ | Low-level input voltage, ON | 0 | 0.45 | V |
| $T_J$ | Operating temperature | –40 | 125 | °C |
| $C_T$ | $C_T$ pin capacitor voltage rating | 7 | | V |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS22970 YZP (DSBGA) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 130 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 50 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 6.5 Electrical Characteristics

Unless otherwise noted, $V_{IN}$ = 0.65 V to 3.6 V

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | $V_{OUT}$ = Open, Switch enabled | $V_{IN}$ = 3.6 V | –40°C to +85°C | | 35 | 75 | µA |
| | | | | –40°C to +105°C | | | 90 | |
| | | | $V_{IN}$ = 2.5 V | –40°C to +85°C | | 32 | 70 | |
| | | | | –40°C to +105°C | | | 84 | |
| | | | $V_{IN}$ = 1.8 V | –40°C to +85°C | | 30 | 68 | |
| | | | | –40°C to +105°C | | | 82 | |
| | | | $V_{IN}$ = 1.2 V | –40°C to +85°C | | 25 | 60 | |
| | | | | –40°C to +105°C | | | 72 | |
| | | | $V_{IN}$ = 1.05 V | –40°C to +85°C | | 20 | 55 | |
| | | | | –40°C to +105°C | | | 66 | |
| | | | $V_{IN}$ = 0.65 V | –40°C to +85°C | | 18 | 55 | |
| | | | | –40°C to +105°C | | | 66 | |
| $I_{SD}$ | Shutdown current | $V_{OUT}$ = GND, Switch disabled | $V_{IN}$ = 3.6 V | –40°C to +85°C | | 1 | 9 | µA |
| | | | | –40°C to +105°C | | | 16 | |
| | | | $V_{IN}$ = 2.5 V | –40°C to +85°C | | 1 | 8 | |
| | | | | –40°C to +105°C | | | 12 | |
| | | | $V_{IN}$ = 1.8 V | –40°C to +85°C | | 1 | 8 | |
| | | | | –40°C to +105°C | | | 12 | |
| | | | $V_{IN}$ = 1.2 V | –40°C to +85°C | | 1 | 6 | |
| | | | | –40°C to +105°C | | | 9 | |
| | | | $V_{IN}$ = 1.05 V | –40°C to +85°C | | 1 | 6 | |
| | | | | –40°C to +105°C | | | 9 | |
| | | | $V_{IN}$ = 0.65 V | –40°C to +85°C | | 1 | 6 | |
| | | | | –40°C to +105°C | | | 9 | |
| $R_{ON}$ | ON-resistance | $I_{OUT}$ = –200 mA | $V_{IN}$ = 3.6 V | 25°C | | 5.3 | 8.5 | mΩ |
| | | | | –40°C to +85°C | | | 9.5 | |
| | | | | –40°C to +105°C | | | 11.5 | |
| | | | $V_{IN}$ = 2.5 V | 25°C | | 5.3 | 8.5 | |
| | | | | –40°C to +85°C | | | 9.5 | |
| | | | | –40°C to +105°C | | | 11.5 | |
| | | | $V_{IN}$ = 1.8 V | 25°C | | 5.3 | 8.5 | |
| | | | | –40°C to +85°C | | | 9.5 | |
| | | | | –40°C to +105°C | | | 11.5 | |
| | | | $V_{IN}$ = 1.2 V | 25°C | | 5.5 | 9.1 | |
| | | | | –40°C to +85°C | | | 10.1 | |
| | | | | –40°C to +105°C | | | 12.1 | |
| | | | $V_{IN}$ = 1.05 V | 25°C | | 5.8 | 9.4 | |
| | | | | –40°C to +85°C | | | 10.4 | |
| | | | | –40°C to +105°C | | | 12.4 | |
| | | | $V_{IN}$ = 0.65 V | 25°C | | 7.5 | 11.5 | |
| | | | | –40°C to +85°C | | | 12.5 | |
| | | | | –40°C to +105°C | | | 14.5 | |
| $R_{PD}$ | Output pull down resistance(1) | $I_{OUT}$ = 3 mA, Switch disabled | $V_{IN}$ = 3.6 V | –40°C to +105°C | | 150 | | Ω |
| | | | $V_{IN}$ = 0.65 V | –40°C to +105°C | | 710 | | Ω |
| $I_{ON}$ | ON input leakage current | $V_{ON}$ = 0 V to 3.6 V | | –40°C to +105°C | | | 0.1 | µA |

(1) See the *Quick Output Discharge (QOD)* section.

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## Electrical Characteristics (continued)

Unless otherwise noted, $V_{IN}$ = 0.65 V to 3.6 V

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $T_{SD}$ | Thermal shutdown | Junction temperature rising | | | 170 | | °C |
| $T_{SD, HYS}$ | Thermal shutdown hysteresis | Junction temperature falling | | | 26 | | °C |

## 6.6 Switching Characteristics

| PARAMETER | | TEST CONDITION | TYP | UNIT |
|---|---|---|---|---|
| **$V_{IN}$ = 3.6 V, $V_{ON}$ = 3.6 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | |
| $t_{ON}$ | Turnon time | | 1535 | µs |
| $t_{OFF}$ | Turnoff time | | 3.3 | |
| $t_R$ | VOUT Rise time | | 985 | |
| $t_F$ | VOUT Fall time | $C_L$ = 0.1 µF, $R_L$ = 10Ω | 1.8 | |
| $t_D$ | ON delay time | | 550 | |
| **$V_{IN}$ = 1.8 V, $V_{ON}$ = 3.6 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | |
| $t_{ON}$ | Turnon time | | 1175 | µs |
| $t_{OFF}$ | Turnoff time | | 4.9 | |
| $t_R$ | VOUT Rise Time | | 645 | |
| $t_F$ | VOUT Fall time | $C_L$ = 0.1 µF, $R_L$ = 10Ω | 2.2 | |
| $t_D$ | ON delay time | | 530 | |
| **$V_{IN}$ = 0.65 V, $V_{ON}$ = 3.6 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | |
| $t_{ON}$ | Turnon time | | 820 | µs |
| $t_{OFF}$ | Turnoff time | | 61 | |
| $t_R$ | VOUT Rise time | | 325 | |
| $t_F$ | VOUT Fall time | $C_L$ = 0.1 µF, $R_L$ = 10Ω | 6.3 | |
| $t_D$ | ON delay time | | 495 | |

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# 7 Parameter Measurement Information

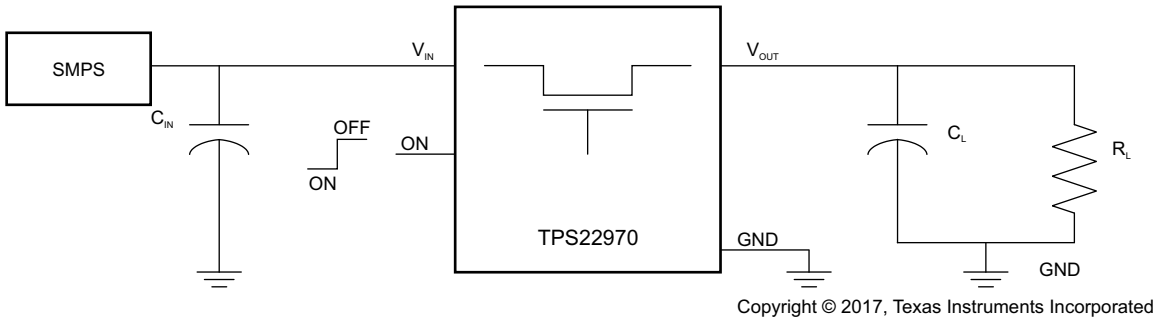



**Figure 1. TPS22970 Test Circuit**

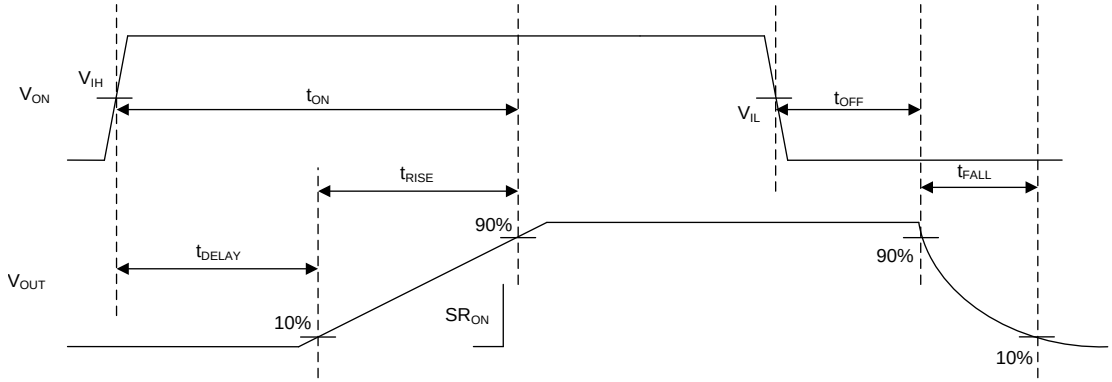


**Figure 2. $T_{ON}$ and $T_{OFF}$ Waveforms**

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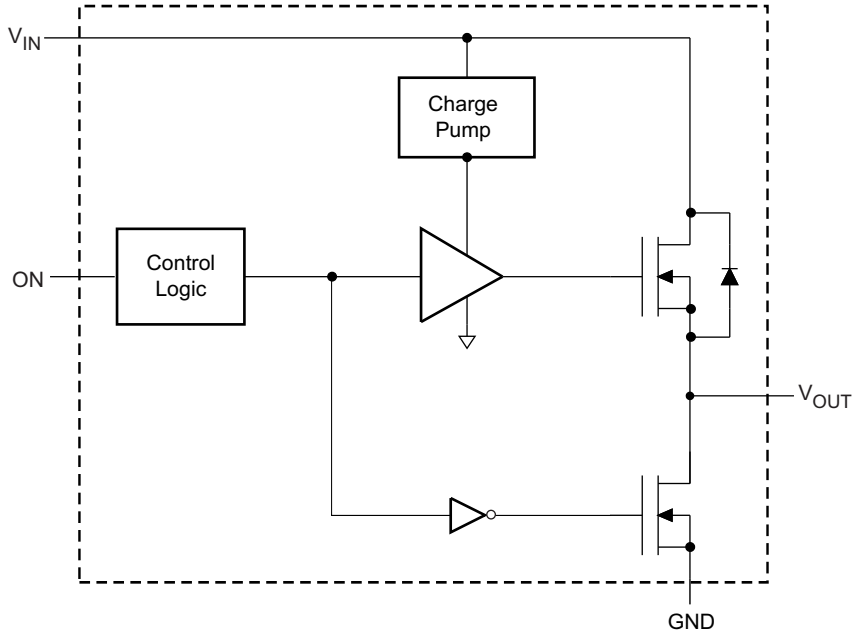
# 8 Detailed Description

## 8.1 Overview

The TPS22970 is a single channel, 4-A load switch in a small, space-saving WCSP-8 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current. This device is also designed to have very low leakage current during off state, which prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 On and Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs. This pin does not have an internal bias and must not be left floating for proper functionality.

### 8.3.2 Quick Output Discharge (QOD)

The TPS22970 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 150 Ω and prevents the output from floating while the switch is disabled.

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## 8.4 Device Functional Modes

Table 1 lists the functional modes for the TPS22970.

**Table 1. Function Table**

| TPS22970 | | |
|---|---|---|
| **ON-Pin** | **$V_{IN}$ to $V_{OUT}$** | **$V_{OUT}$ to GND** |
| Below $V_{IL}$ | OFF | ON |
| Above $V_{IH}$ | ON | OFF |

ADVANCE INFORMATION

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Input Capacitor ($C_{IN}$)

It is recommended to use a capacitor between VIN and GND close to the device pins. This helps limit the voltage droop on the input supply caused by transient inrush currents when the switch is turned on into a discharged capacitor at the load. A 1-µF ceramic capacitor, $C_{IN}$, is usually sufficient. Higher values of $C_{IN}$ can be used to further reduce the voltage droop.

### 9.1.2 Output Capacitor ($C_L$)

A $C_{IN}$ greater than $C_L$ is highly recommended due to the integrated body diode in the NMOS switch. A $C_L$ greater than $C_{IN}$ can cause $V_{OUT}$ to exceed VIN when the system supply is removed. This could result in current flow through the body diode from $V_{OUT}$ to $V_{IN}$.

### 9.1.3 Thermal Consideration

It is recommended to limit the junction temperature ($T_J$) to below 125°C. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 1 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (1)$$

where

- $P_{D(max)}$ is maximum allowable power dissipation
- $T_{J(max)}$ is maximum allowable junction temperature
- $T_A$ is ambient temperature of the device
- $\Theta_{JA}$ is junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout

## 9.2 Typical Application

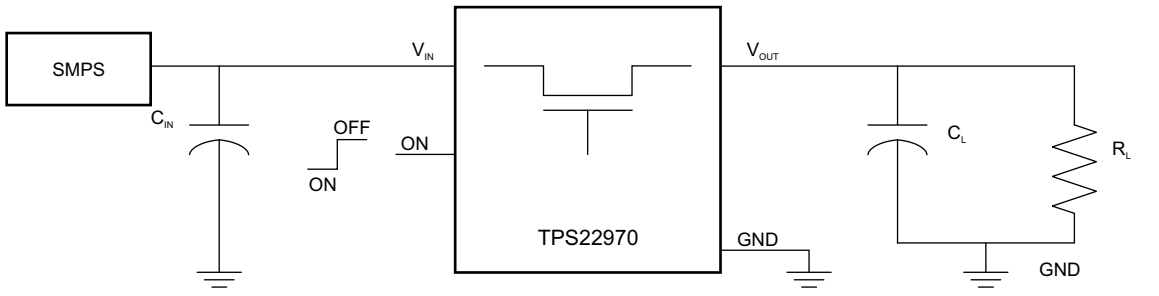




**Figure 3. Typical Application Circuit**

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## Typical Application (continued)

### 9.2.1 Design Requirements

For this design example, below, use the input parameters shown in Table 2.

**Table 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $V_{IN}$ | 1.05 V |
| $I_{LOAD}$ | 2 A |
| Maximum voltage drop | 5% |

### 9.2.2 Detailed Design Procedure

At 1.05-V input voltage, with a maximum voltage drop tolerance of 5%, the TPS22970 has a typical $R_{ON}$ of 5.8 mΩ. The rail is supplying 2 A of current; the voltage drop for a rail is calculated based on Equation 2.

$$V_{DROP} = R_{ON} \times I_{LOAD} \quad (2)$$

$$V_{DROP} = 11.6 \text{ mV} \quad (3)$$

The maximum voltage drop is 5% which is 52.5 mV. The voltage drop caused by the load current across the on resistance is 11.6 mV.

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## 10 Power Supply Recommendations

The device is designed to operate from a VIN range of 0.65 V to 3.6 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

## 11 Layout

### 11.1 Layout Guidelines

All traces must be as short as possible for best performance. Using wide traces for $V_{IN}$, $V_{OUT}$, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

### 11.2 Layout Example

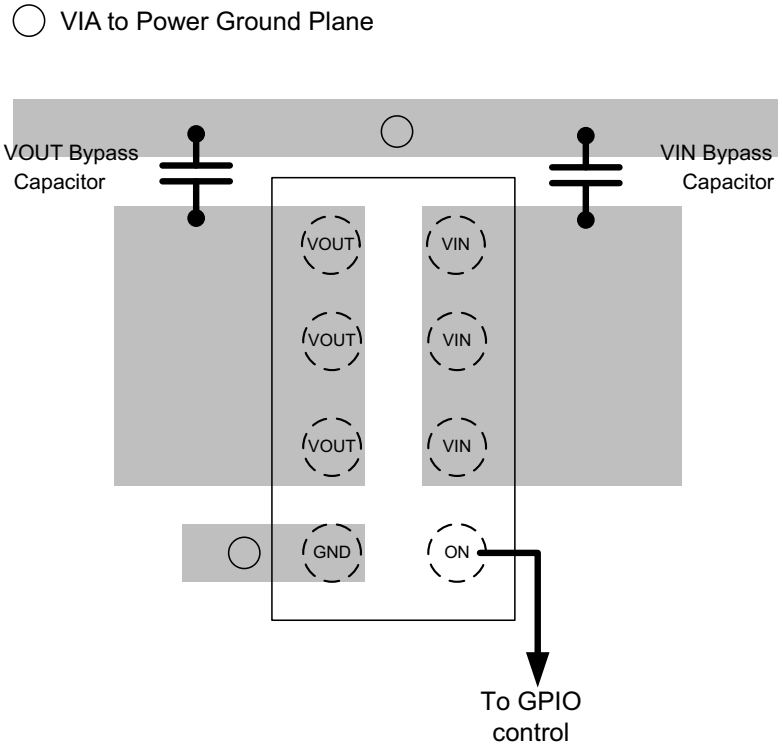



**Figure 4. TPS22970 Package Layout**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*TPS22970 Load Switch Evaluation Module*

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTPS22970YZPT | ACTIVE | DSBGA | YZP | 8 | 250 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TPS22970YZPR | PREVIEW | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | 1CNI | |
| TPS22970YZPT | PREVIEW | DSBGA | YZP | 8 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | 1CMI | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

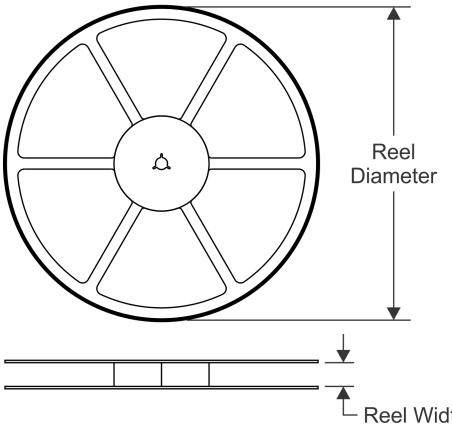
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

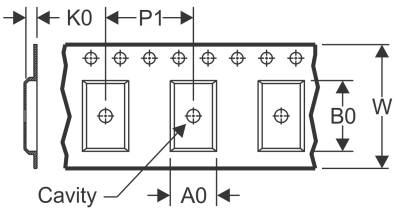
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

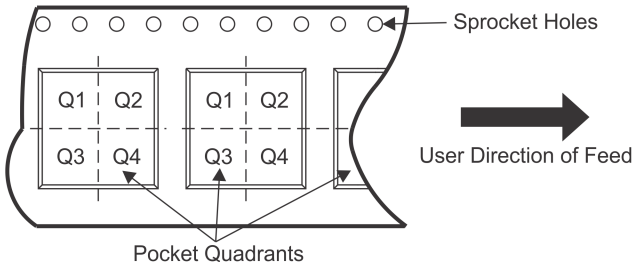



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

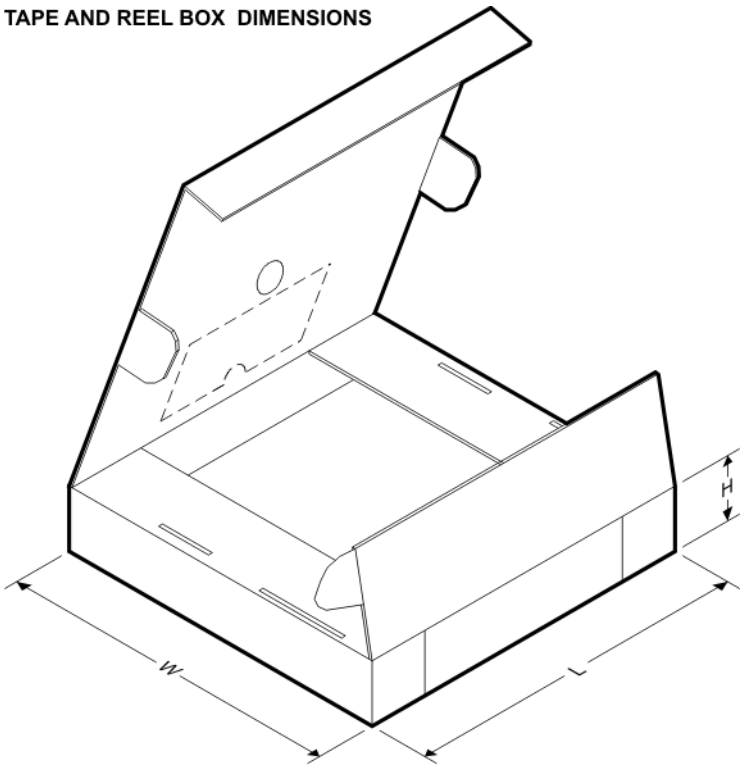
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

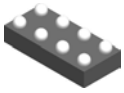
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22970YZPR | DSBGA | YZP | 8 | 3000 | 180.0 | 8.4 | 1.02 | 2.02 | 0.63 | 2.0 | 8.0 | Q1 |
| TPS22970YZPT | DSBGA | YZP | 8 | 250 | 180.0 | 8.4 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS22970YZPR | DSBGA | YZP | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS22970YZPT | DSBGA | YZP | 8 | 250 | 182.0 | 182.0 | 20.0 |

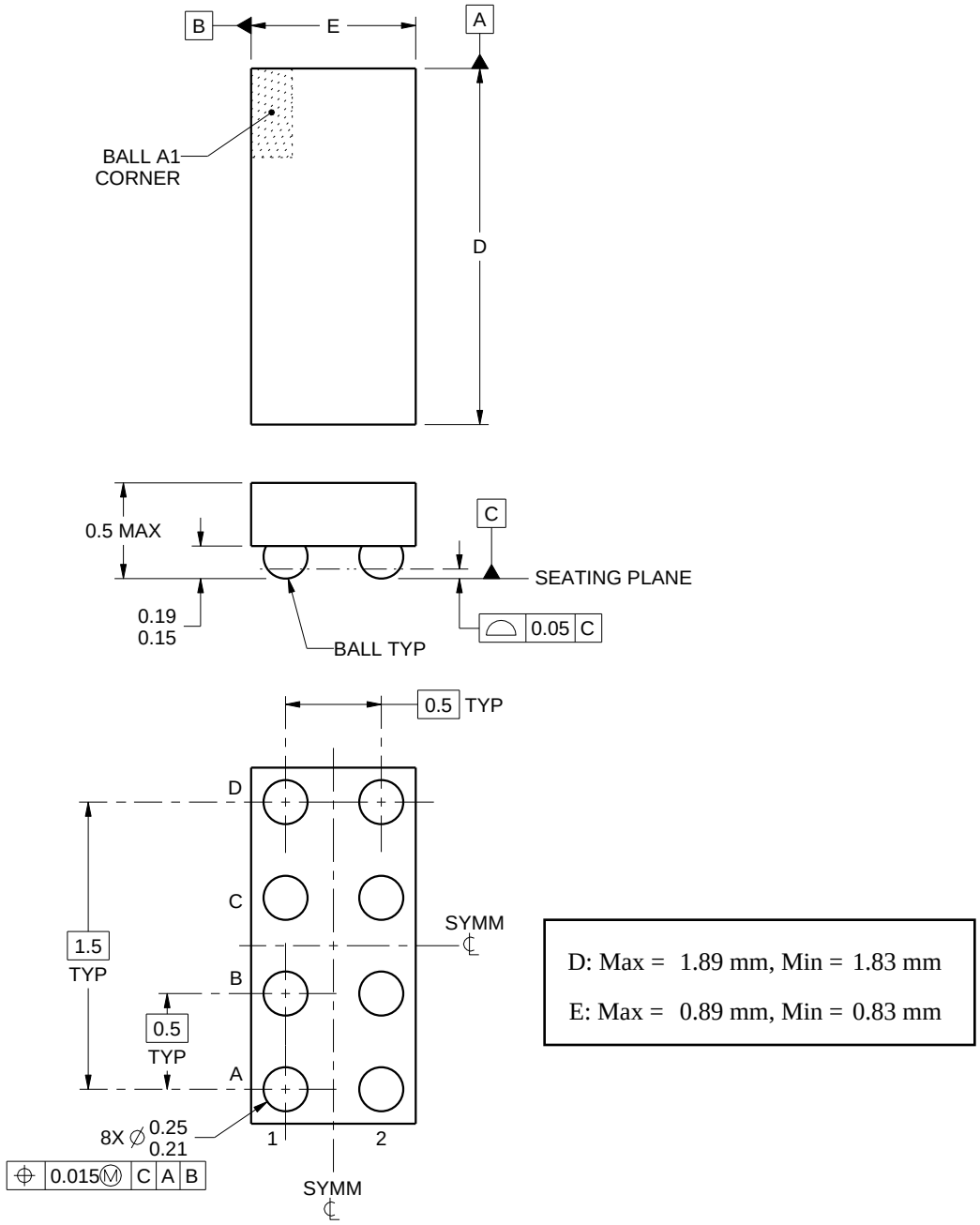


# PACKAGE OUTLINE

## YZP0008

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

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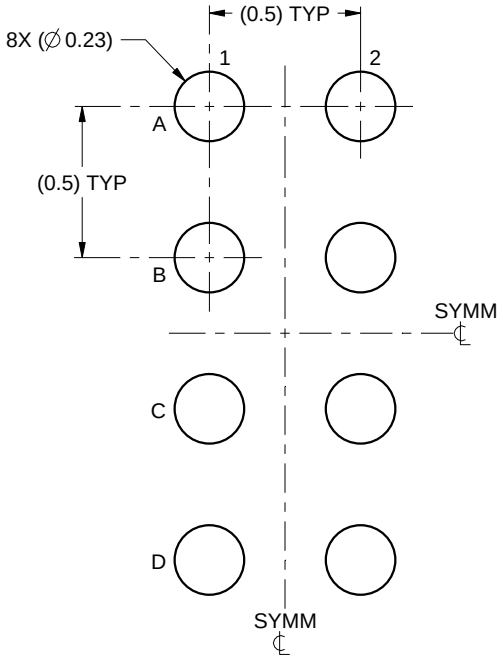
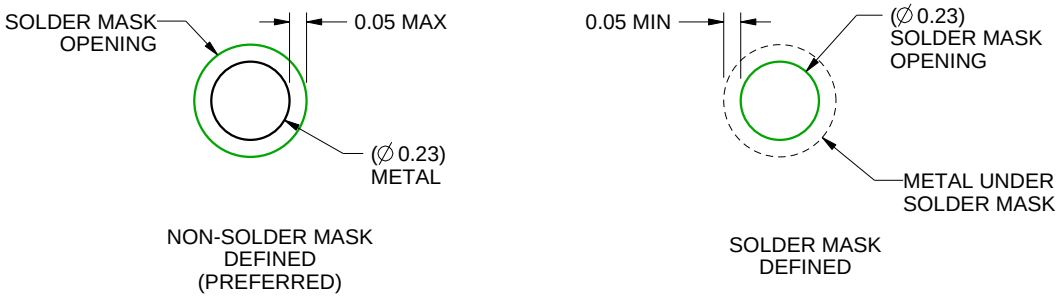
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X




SOLDER MASK DETAILS
NOT TO SCALE

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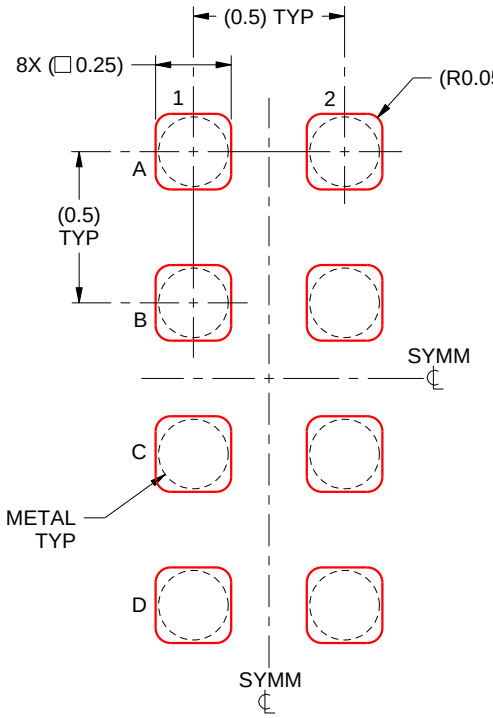
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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