CURRENT-LIMITED LOAD SWITCH WITH LOW NOISE REGULATION CAPABILITY

Check for Samples: TPS22949, TPS22949A

FEATURES

- **Integrated Current Limiter**
  - **Input Voltage Range: 1.62 V to 4.5 V**
  - **Low ON-Resistance**
    - **r_{ON} = 300-mΩ at V_{IN} = 4.5 V**
    - **r_{ON} = 350-mΩ at V_{IN} = 3.3 V**
    - **r_{ON} = 400-mΩ at V_{IN} = 2.5 V**
    - **r_{ON} = 600-mΩ at V_{IN} = 1.8 V**
  - **Integrated 100-mA Minimum Current Limit**
  - **Undervoltage Lockout**
  - **Fast-Current Limit Response Time**
  - **Integrated Fault Blanking and Auto Restart**
- **Stable Without Current Limiter Output Capacitor (TPS22949A Only)**
- **Integrated Low-Noise RF LDO**
  - **Input Voltage Range: 1.62 V to 4.5 V**
  - **Low Noise: 50 µVrms (10 Hz to 100 kHz)**
  - **80-dB V_{IN} PSRR (10 Hz to 10 kHz)**
  - **Fast Start-Up Time: 130 µs**
  - **Low Dropout 100 mV at I_{load} =100 mA**
  - **Integrated Output Discharge**
  - **Stable With 2.2-µF Output Capacitor**
- **1.8-V Compatible Control Input Threshold**
- **ESD Performance Tested Per JESD 22**
  - **3500-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Tiny 8-Terminal YZP Package (1.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height) and SON-8 (DRG) 3.0 mm × 3.0 mm**

APPLICATIONS

- **Fingerprint Module Protection**
- **Portable Consumer Electronics**
- **Smart Phone**
- **Notebooks**
- **Control Access Systems**

DESCRIPTION

The TPS22949 and TPS22949A are devices that provides protection to systems and loads in high-current conditions. The device contains a 500-mΩ current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 4.5 V as well as a low-dropout (LDO) regulator with a fixed output voltage of 1.8 V.

The switch is controlled by an on/off input (EN1), which is capable of interfacing directly with low-voltage control signals. When the switch current reaches the maximum limit, the TPS22949/TPS22949A operates in a constant-current mode to prohibit excessive currents from causing damage. If the constant current condition still persists after 12 ms, these devices shut off the switch and pull the fault signal pin (OC) low. The TPS22949/TPS22949A has an auto-restart feature that turns the switch on again after 70 ms if the EN1 pin is still active.

The output of the current limiter is internally connected to a RF low-dropout (LDO) regulator that offers good ac performance with very low ground current, good power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response. The output of the regulator is stable with ceramic capacitors. This LDO uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations.

The TPS22949A integrates additional internal circuitry that increases the current limit of the switch during the power-up sequence. This feature allows the TPS22949A to operate without a storage capacitor at the input of the LDO.

The TPS22949 and TPS22949A are available in a space-saving 8-terminal WCSP (YZP) or in a 8-pin SON package (DRG). Both are characterized for operation over the free-air temperature range of –40°C to 85°C.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 85°C	SON – DRG	Tape and reel	TPS22949ADRGR	ZUG
	WCSP – YZP	Tape and reel	TPS22949YZPR	_ _ _4Y_
			TPS22949AYZPR	_ _ _4Z_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

YZP PACKAGE

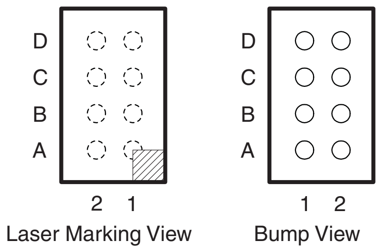
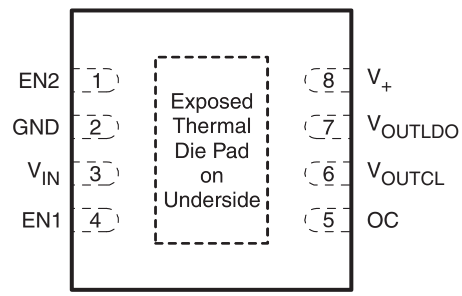


Table 1. YZP PACKAGE TERMINAL ASSIGNMENTS

D	EN1	OC
C	V_{IN}	V_{OUTCL}
B	GND	V_{OUTLDO}
A	EN2	V_+
	2	**1**

DRG PACKAGE
(TOP VIEW)



The exposed center pad, if used, must be connected as a secondary GND or left electrically open.

TERMINAL FUNCTIONS

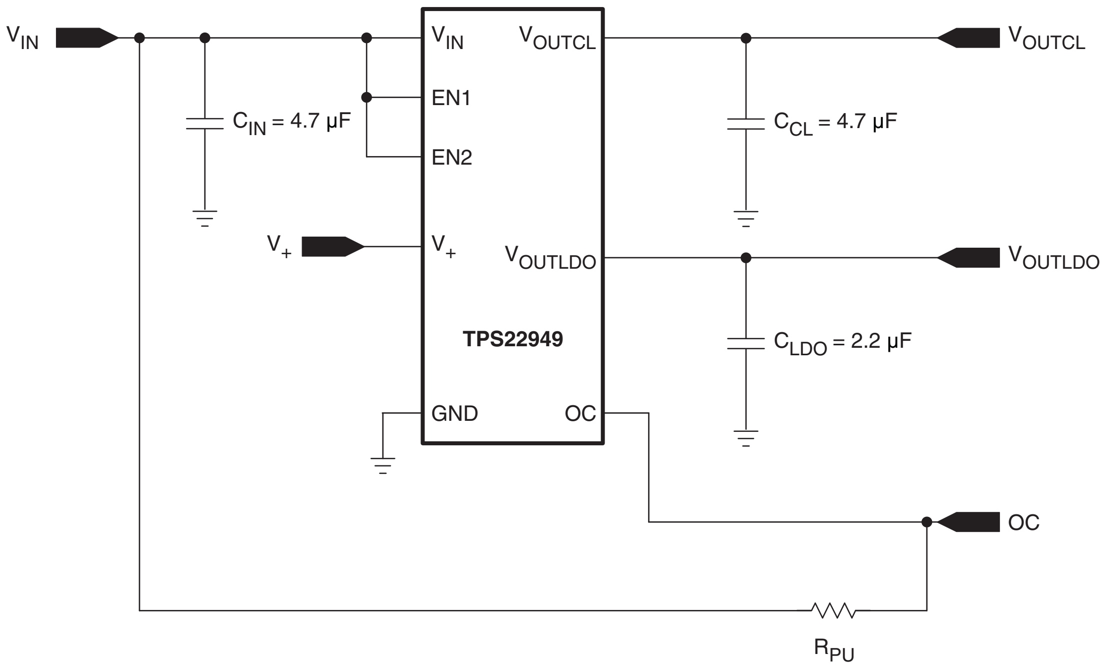
TERMINAL			DESCRIPTION
NO.		NAME	
YZP	DRG		
A1	8	V_+	Supply voltage
A2	1	EN2	LDO control input. Active high. Do not leave floating.
B1	7	V_{OUTLDO}	LDO output. Output of the RF LDO fixed to 1.8 V[1].
B2	2	GND	Ground
C1	6	V_{OUTCL}	Switch output. Output of the power switch
C2	3	V_{IN}	Supply input. Input to the power switch; bypass this input with a ceramic capacitor to ground.
D1	5	OC	Over current output flag. Active low, open-drain output that indicates an over-current, supply undervoltage, or over-temperature state.
D2	4	EN1	Power switch control input. Active high. Do not leave floating.

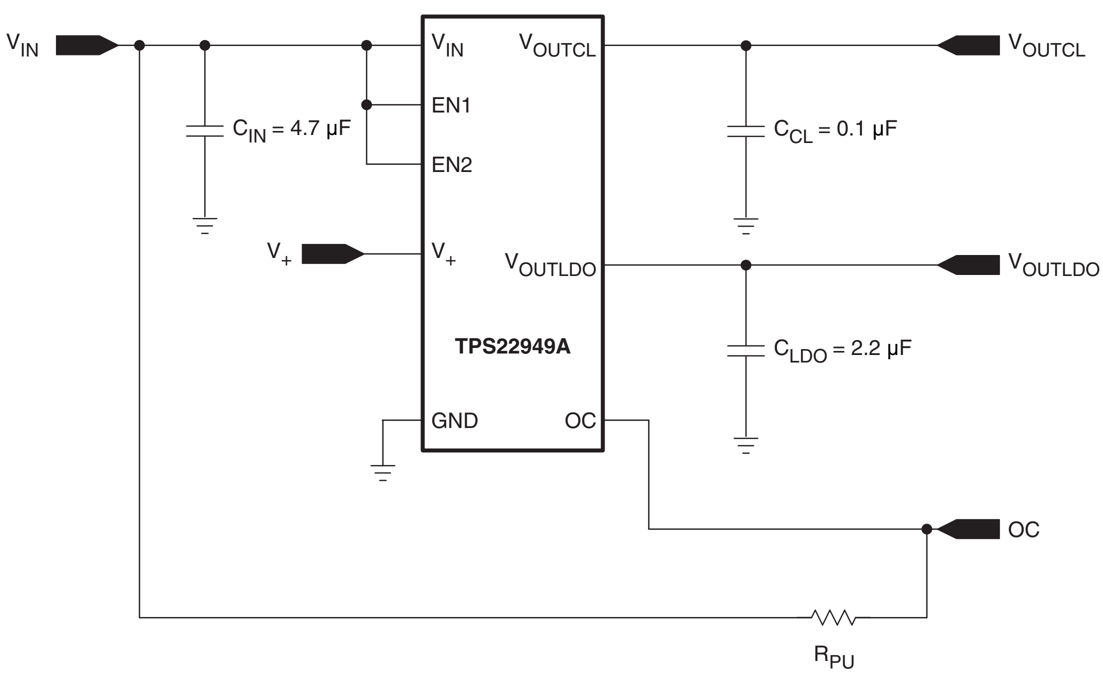
(1) Output voltages from 0.9 V to 3.6 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

FUNCTION TABLE

STATE OF THE DEVICE	EN1	EN2
Current limiter and LDO disabled	0	X
Current limiter enabled/LDO disabled	1	0
Current limiter and LDO enabled	1	1

TYPICAL APPLICATIONS





BLOCK DIAGRAMS

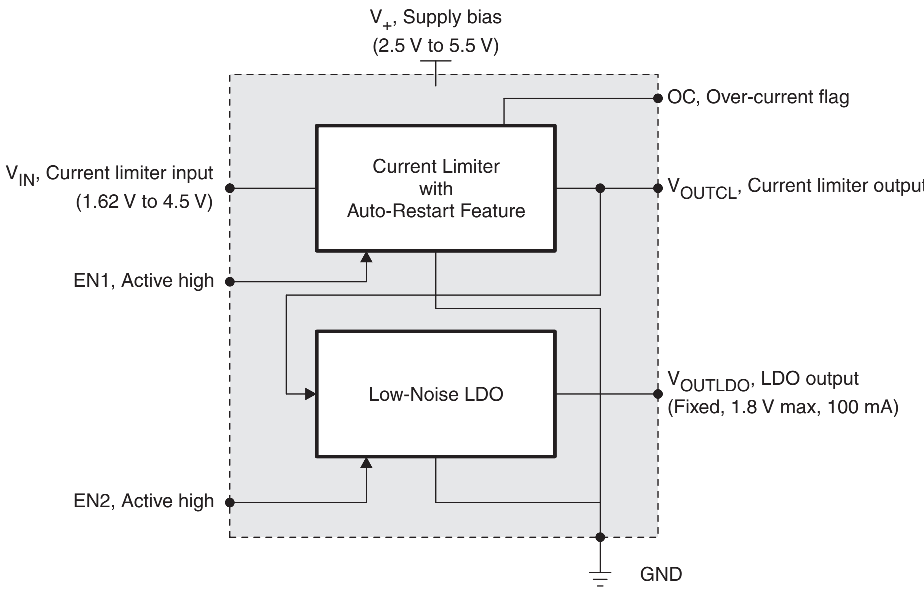


Figure 1. Simplified Block Diagram

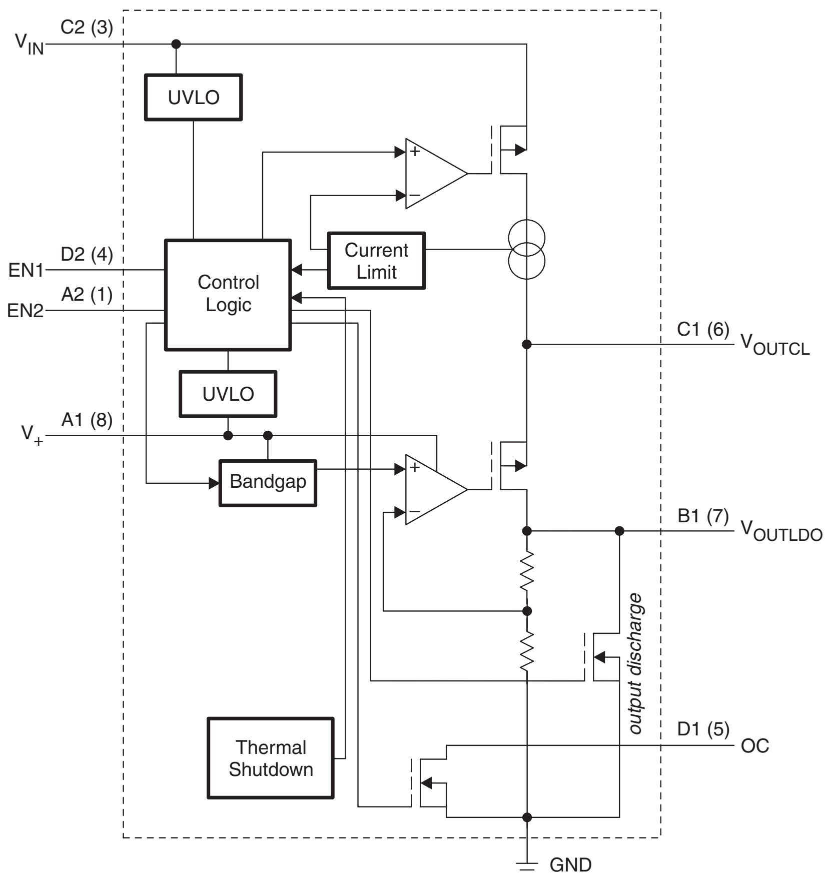


Figure 2. Detailed Block Diagram

ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
V_I	Input voltage	V_{IN}, EN1, EN2, V_+	–0.3	6	V
V_{OUTCL}	Current limiter output voltage			V_{IN} + 0.3	V
T_J	Operating junction temperature range		–40	105	°C
T_{stg}	Storage temperature range		–65	150	°C
	Electrostatic discharge protection (ESD)	Human-Body Model		3.5	kV
		Charged-Device Model		1	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	PACKAGE	RθJC	RθJA	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K (JESD 51-7)	YZP	13.79°C/W	101.92°C/W	98.1 mW/°C	784 mW	343 mW	196 mW
High-K (JESD 51-5)	DRG	56.6°C/W	52.44°C/W	19 mW/°C	1525 mW	667 mW	381 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage(1)	1.62	4.5	V
V_{OUTCL}	Current limiter output voltage		V_{IN}	V
V_+	Supply voltage	2.6	5.5	V
C_{IN}	Input capacitor	1		µF
T_A	Ambient free-air temperature	–40	85	°C
Control Inputs (EN1, EN2)				
V_{IH}	High-level input voltage	1.4	5.5	V
V_{IL}	Low-level input voltage		0.4	V

(1) See the Application Information section

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{GND}	Ground pin current	EN1 and EN2 = V_+ $V_+ = V_{OUT}$ + 1.4 V or 2.5, whichever > 5.5 V, $V_{OUTCL} \geq V_{OUTLDO}$ + 0.5 V I_{OUT2} = 0 mA			85	110	µA
I_{GNDCL}	Ground pin current (current limiter only)	EN1 = V_+ and EN2 = 0			40	75	µA
$I_{GND(OFF)}$	OFF-state ground pin current	EN1 and EN2 = GND, V_{OUTCL} = Open, V_{OUTLDO} = Open	$V_{IN} = V_+$ = 3.3 V			2	µA
			V_{IN} = 3.6 V, V_+ = 5.5 V			6	µA
I_{EN2}	Enable pin 2 current, enabled	VEN2 = V_+ =5.5 V, V_{IN} = 4.5 V				1	µA
I_{EN1}	Enable pin 1 current, enabled	VEN1 = V_+ = 5.5 V, V_{IN} = 4.5 V				1	µA
Thermal shutdown	Shutdown threshold (T_A)	TPS22949			122		°C
		TPS22949A			135		°C
	Return from shutdown	TPS22949			112		°C
		TPS22949A			120		°C
	Hysteresis	TPS22949			10		°C
		TPS22949A			10		°C

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.

CURRENT LIMITER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_+ = 3.3 V, EN1 = V_+, EN2 = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	YZP PACKAGE			DRG PACKAGE			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
r_{ON}	ON-state resistance	I_{OUT} = 20 mA	V_{IN} = 4.5 V	25°C		0.3	0.4		0.4	0.5	Ω
				Full			0.5			0.6	
			V_{IN} = 3.3 V	25°C		0.35	0.6		0.45	0.7	
				Full			0.7			0.8	
			V_{IN} = 2.5 V	25°C		0.4	0.7		0.5	0.8	
				Full			0.8			0.9	
			V_{IN} = 1.8 V	25°C		0.6	0.9		0.7	1	
				Full			1.0			1.1	
			V_{IN} = 1.62 V	25°C		0.7	1.0		0.8	1.1	
				Full			1.1			1.2	
I_{LIM}	Current limit	V_{OUT} = 3 V	V_{IN} = 3.3 V	Full	100	150	200	100	150	200	mA
$I_{LIM\ (INRUSH)}$	Power-ON inrush current limit (TPS22949A only)	V_{OUT} = 3 V	V_{IN} = 3.3 V	Full		750			750		
UVLO-CL	Undervoltage shutdown	V_{IN} increasing			1.39	1.49	1.59	1.39	1.49	1.59	V
	Undervoltage shutdown hysteresis					30			30		mV
	OC output logic low voltage	I_{SINK} = 10 mA	V_{IN} = 4.5 V	Full		0.1	0.3		0.1	0.3	V
			V_{IN} = 1.8 V			0.2	0.4		0.2	0.4	

CURRENT LIMITER SWITCHING CHARACTERISTICS

V_{IN} = 3.3 V, T_A = 25°C, R_L = 500 Ω, C_L = 0.1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 500 Ω, C_{CL} = 0.1 µF		95		µs
t_{OFF}	Turn-OFF time	R_L = 500 Ω, C_{CL} = 0.1 µF		2		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_{CL} = 0.1 µF		25		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_{CL} = 0.1 µF		10		µs
t_{BLANK}	Overcurrent blanking time		6	12	18	ms
t_{RSTRT}	Auto-restart time		40	80	120	ms
t_{INRUSH}	Power-ON inrush current limit time (TPS22949A only)	R_L = 500 Ω, C_{CL} = 0.1 µF		150		µs
	Short-circuit response time	V_{IN} = V_{EN1} = 3.3 V, moderate over-current condition		11		µs
		V_{IN} = V_{EN1} = 3.3 V, hard short		5		

LOW-NOISE LDO REGULATOR ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUTLDO}	Output voltage(1)			1.76	1.8	1.84	V
$\Delta V_{OUTLDO}/\Delta V_{IN}$	V_{IN} line regulation	$V_{IN} = V_{OUTLDO}$ + 0.5 V to 4.5 V, I_{OUT} = 1 mA			±0.1		%/V
	V_{IN} line transient	ΔV_{IN} = 400 mV, $t_r = t_f$ = 1 µs			±2		mV
$\Delta V_{OUTLDO}/\Delta V_+$	V_+ line regulation	$V_{IN} = V_{OUTLDO}$ + 1.4 V or 2.5 V, whichever is > 5.5 V, I_{OUT} = 1 mA			±0.1		%/V
	V_+ line transient	ΔV_{IN} = 600 mV, $t_r = t_f$ = 1 µs			±5		mV
$\Delta V_{OUTLDO}/\Delta I_{OUT2}$	Load regulation	I_{OUT2} = 0 to 100 mA (no load to full load)			±0.01		%/V
	Load transient	I_{OUT2} = 0 to 100 mA, $t_r = t_f$ = 1 µs			±35		mV
V_{DO}	Dropout voltage ($V_{DO} = V_{IN} - V_{OUTLDO}$)	$V_{IN} = V_{OUTLDO(NOM)}$ – 0.1 V, $V_+ - V_{OUTLDO(NOM)}$ = 1.4 V, I_{OUT} = 100 mA			110	200	mV
V_{IN} PSRR	Power-supply rejection ratio	$V_{OUTCL} - V_{OUTLDO} \geq 0.5$ V, $V_+ = V_{OUTLDO}$ + 1.4 V, I_{OUT} = 100 mA,	f = 10 Hz		75		dB
			f = 100 Hz		75		
			f = 1 kHz		80		
			f = 10 kHz		80		
			f = 100 kHz		85		
			f = 1 MHz		85		
V_+ PSRR	Power-supply rejection ratio	$V_{OUTCL} - V_{OUTLDO} \geq 0.5$ V, $V_+ = V_{OUTLDO}$ + 1.4 V, I_{OUT} = 100 mA,	f = 10 Hz		80		dB
			f = 100 Hz		80		
			f = 1 kHz		75		
			f = 10 kHz		65		
			f = 100 kHz		55		
			f = 1 MHz		35		
V_N	Output noise voltage	$V_+ \geq 2.5$ V, $V_{OUTLDO} = V_{OUTCL}$ + 0.5 V	BW = 10 Hz to 100 kHz		50		µVrms
t_{STR}	Startup time	V_{OUT} = 95%, $V_{OUT(NOM)}$, I_{OUT} = 100 mA, C_{OUT} = 2.2 µF			130	250	µs
UVLO-V_+	Undervoltage lockout	V_+ rising		2.3	2.45	2.55	V
	Hysteresis	V_+ falling			150		mV

(1) LDO output voltage is fixed at 1.8 V. However, output voltages from 0.9 V to 3.6 V in 50 mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

TYPICAL CHARACTERISTICS

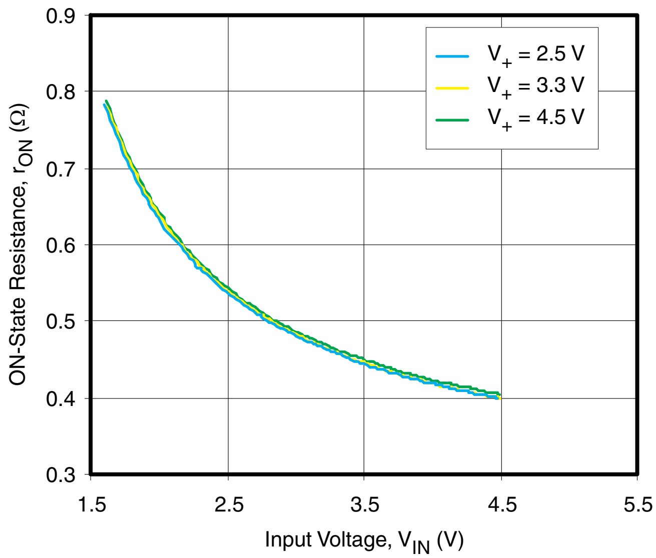


Figure 3. ON-State Resistance vs Input Voltage, T_A = 25°C

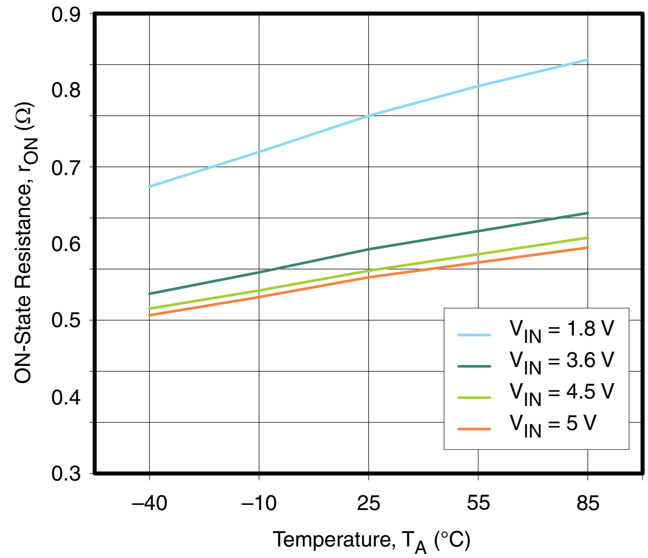


Figure 4. ON-State Resistance vs Temperature, V_+ = 5.5 V

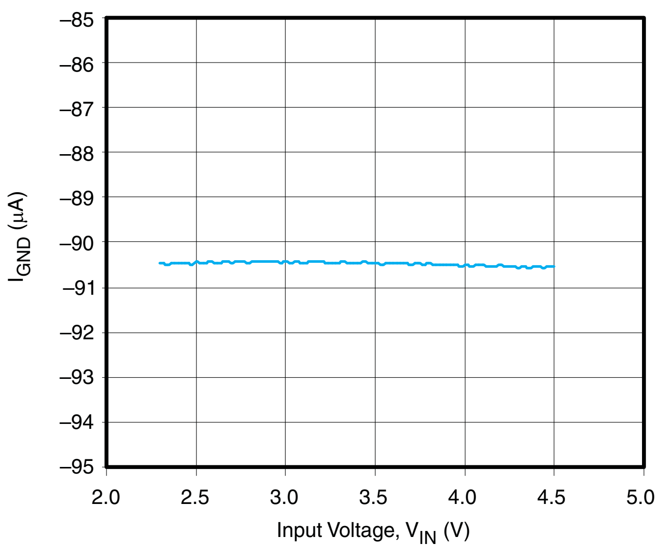


Figure 5. Ground Pin Current vs Input Voltage V_+ = 5.5 V

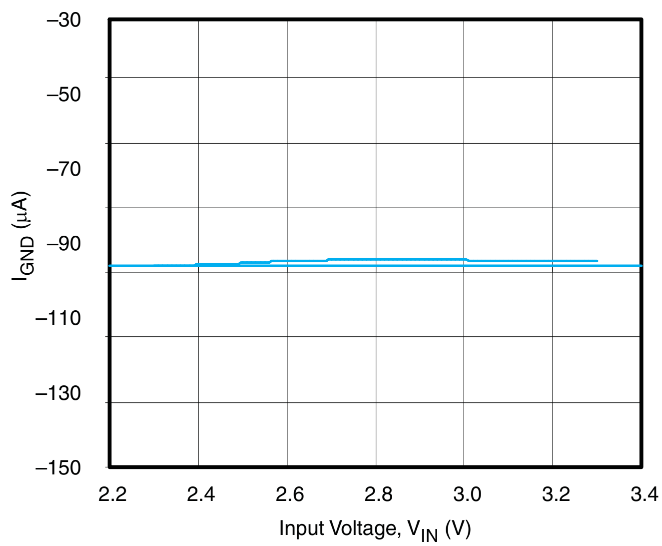


Figure 6. Ground Pin Current vs Input Voltage, V_+ = 3.3 V

TYPICAL CHARACTERISTICS (continued)

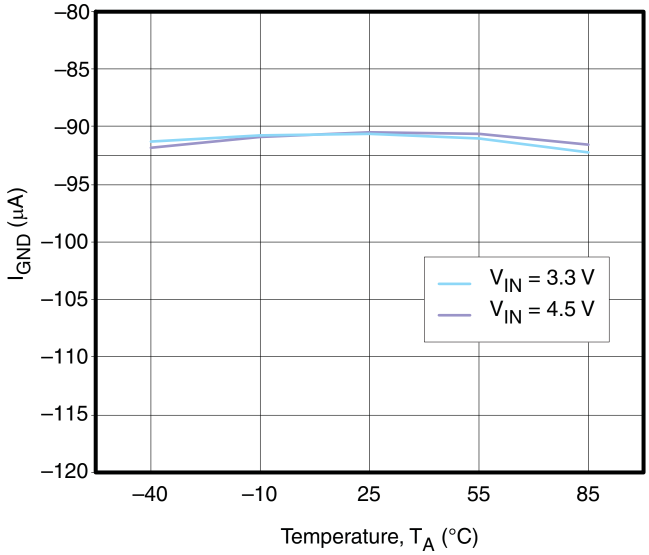


Figure 7. Ground Pin Current vs Temperature, V_+ = 5.5 V

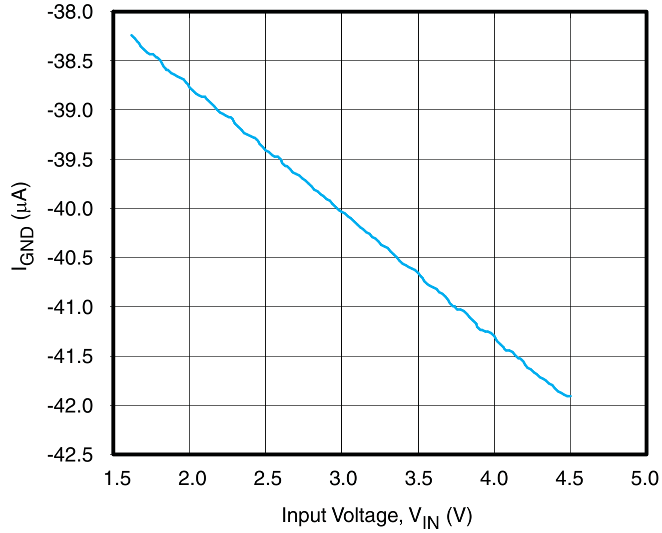


Figure 8. Ground Pin Current vs Input Voltage (Current Limiter Only), V_+ = 5.5 V

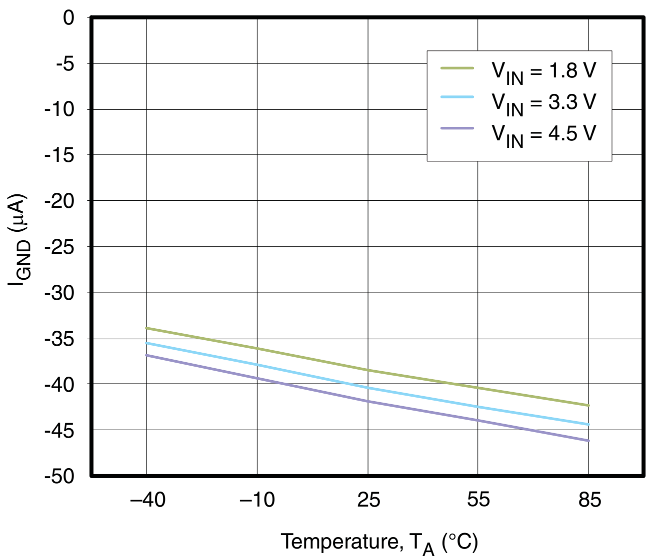


Figure 9. Ground Pin Current vs Temperature (Current Limiter Only), V_+ = 5.5 V

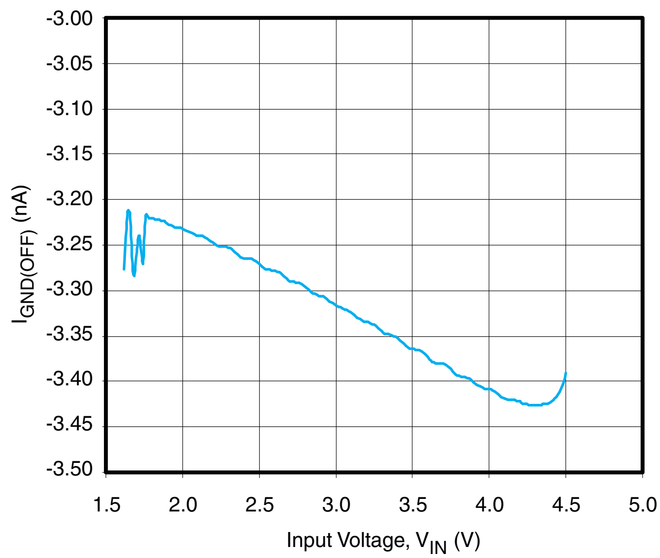


Figure 10. OFF-State Ground Current vs Input Voltage, V_+ = 5.5 V

TYPICAL CHARACTERISTICS (continued)

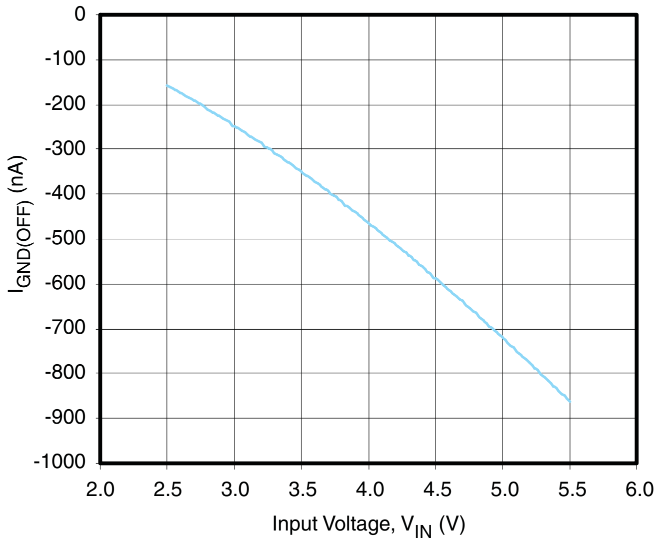


Figure 11. OFF-State Ground Current vs Input Voltage, $V_{IN} = V_+$

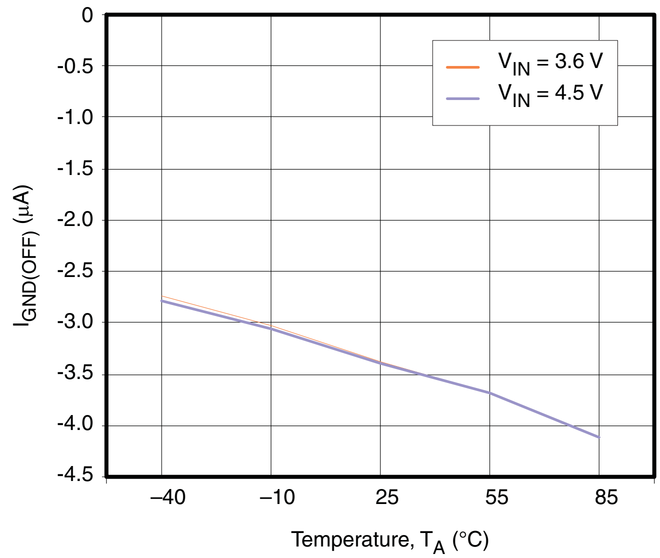


Figure 12. OFF-State Ground Current vs Temperature

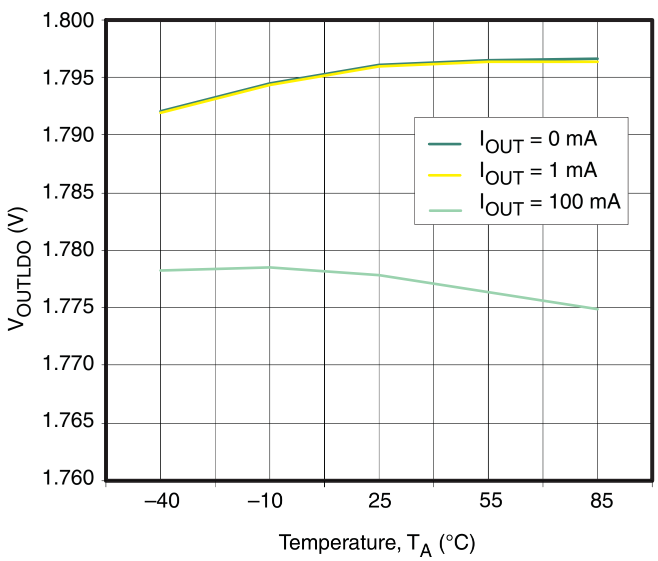


Figure 13. Output Voltage vs Temperature

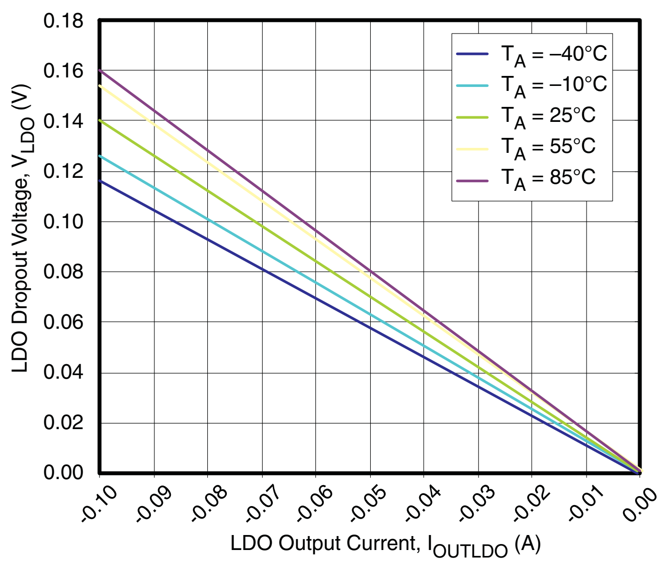


Figure 14. LDO Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

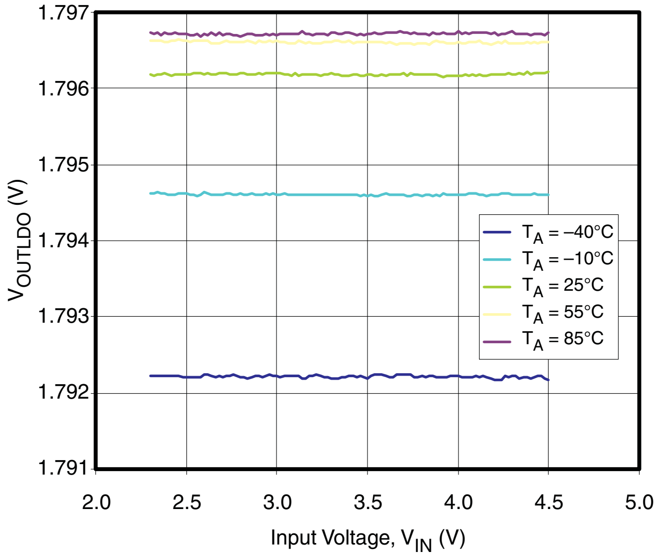


Figure 15. Input Voltage, V_{IN}, Line Regulation, I_{OUT} = 0 mA

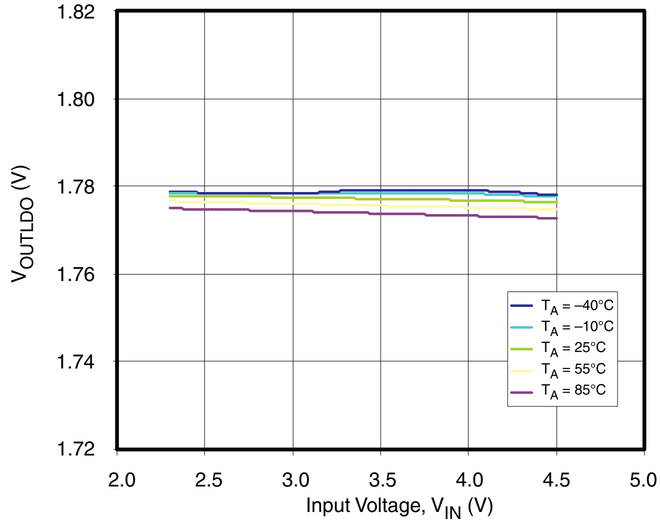


Figure 16. Input Voltage, V_{IN}, Line Regulation, I_{OUT} = 100 mA

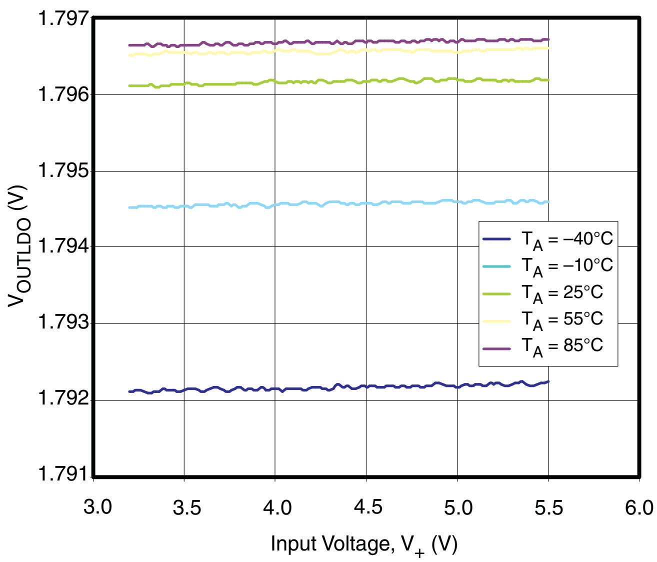


Figure 17. Input Voltage, V_+, Line Regulation, I_{OUT} = 0 mA

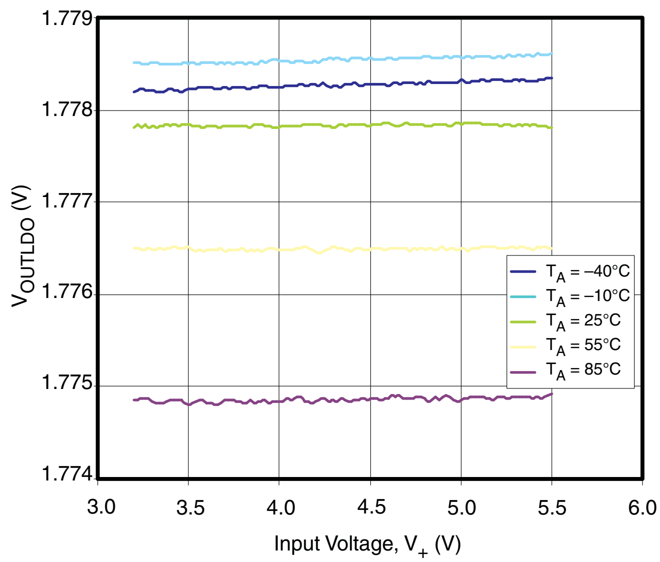


Figure 18. Input Voltage, V_+, Line Regulation, I_{OUT} = 100 mA

TYPICAL CHARACTERISTICS (continued)

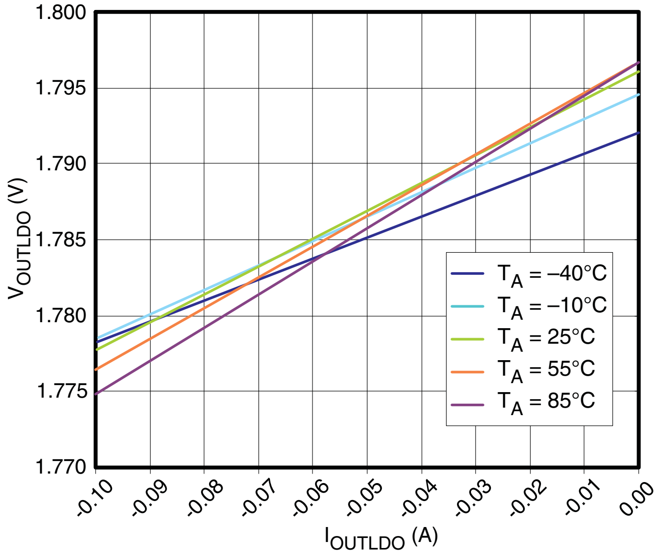


Figure 19. Load Regulation, I_{OUT} = 100 mA

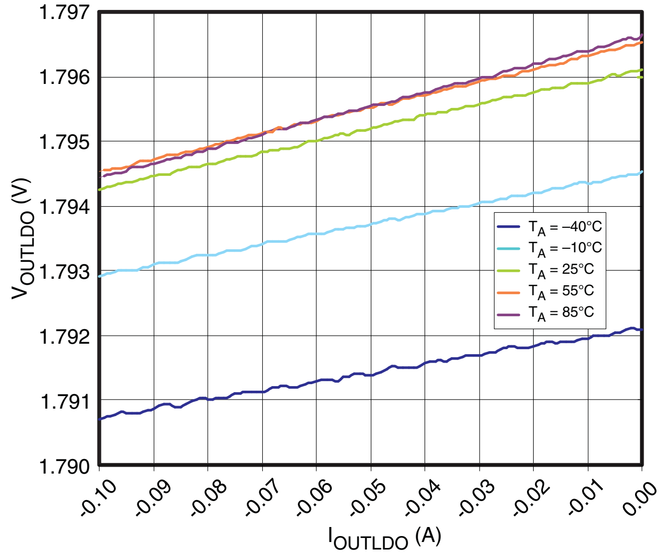


Figure 20. Load Regulation Under Light Loads, I_{OUT} = 10 mA

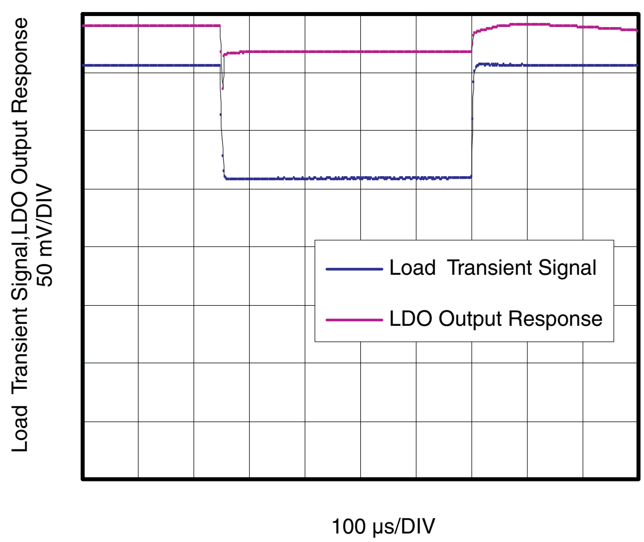


Figure 21. Load Transient

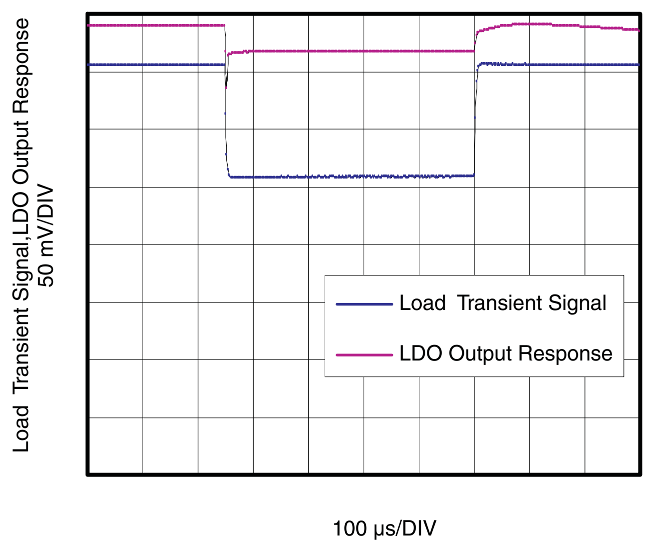


Figure 22. V_{IN} Load Transient

TYPICAL CHARACTERISTICS (continued)

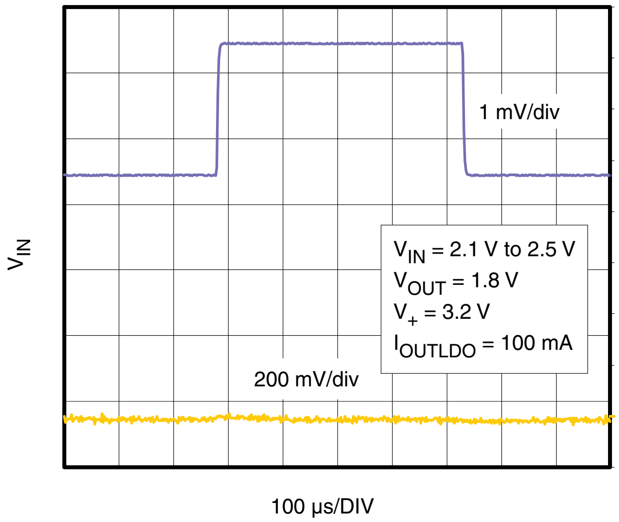


Figure 23. V_+ Load Transient

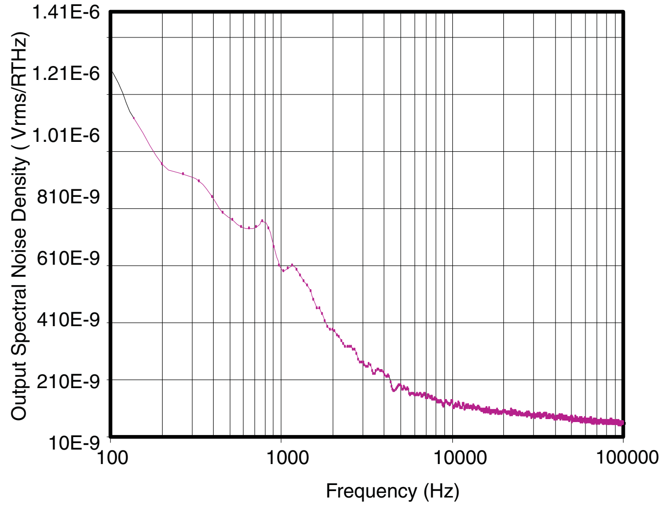


Figure 24. Output Spectral Noise Density vs Frequency

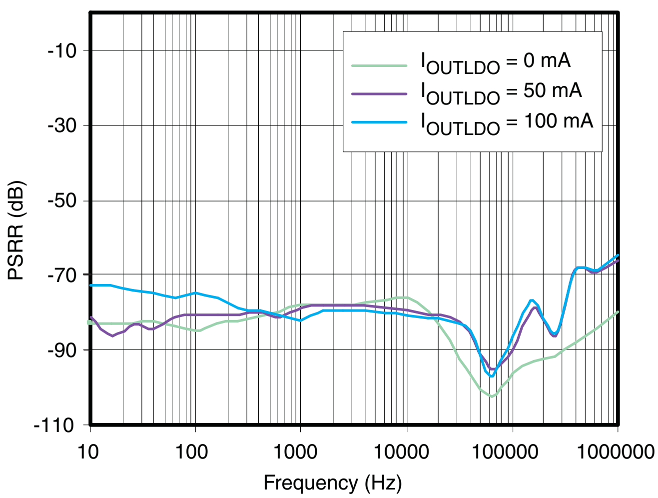


Figure 25. PSRR vs Frequency

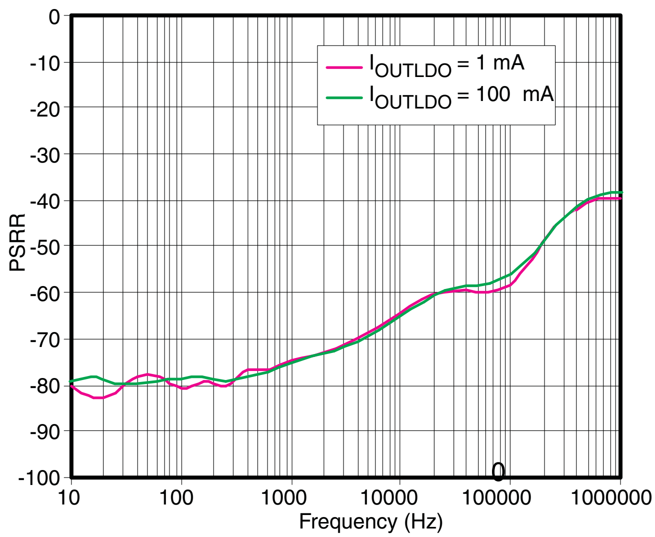


Figure 26. V_+ PSRR vs Frequency

TYPICAL CHARACTERISTICS (continued)

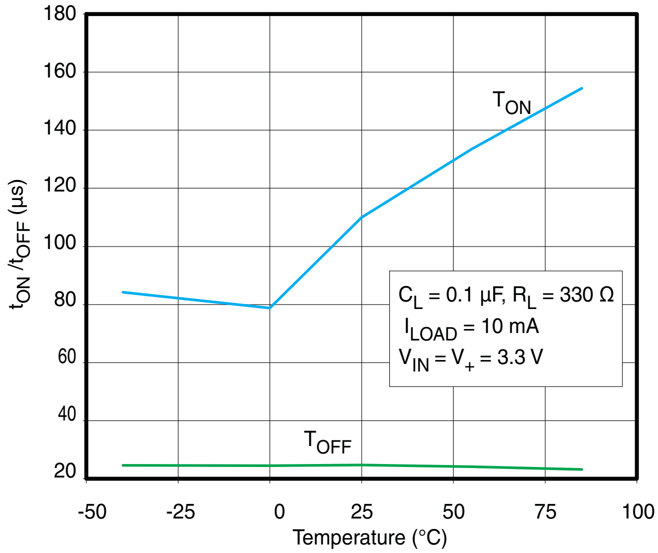


Figure 27. t_{ON}/t_{OFF} vs Temperature

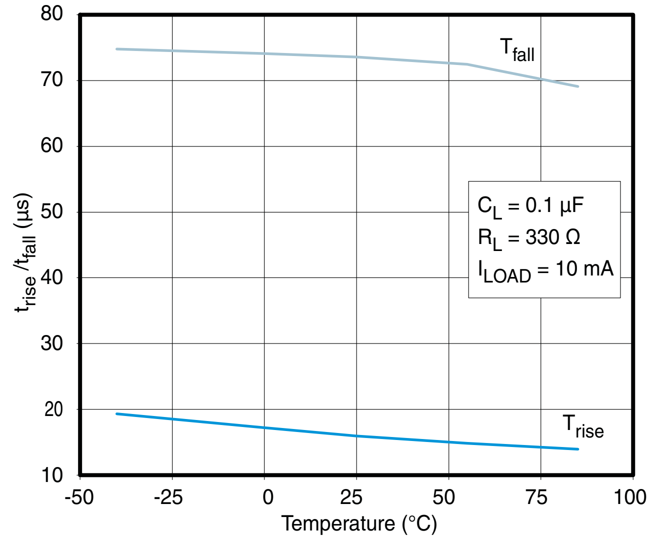


Figure 28. t_{rise}/t_{fall} vs Temperature

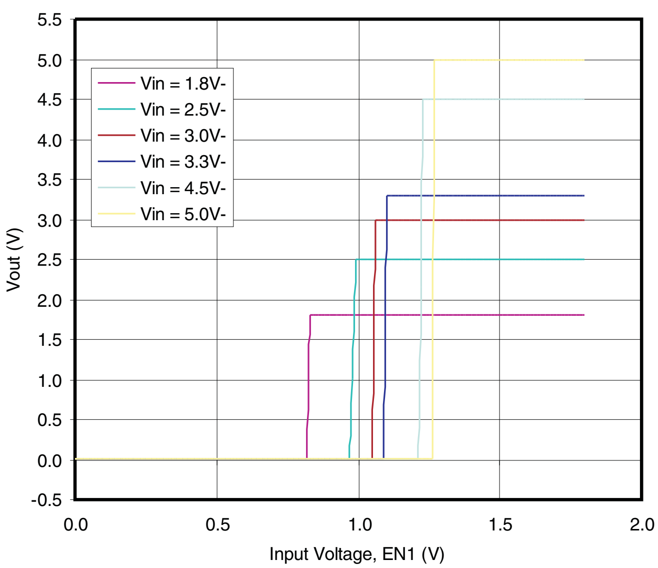


Figure 29. EN1 (Current Limiter) Input Thresholds, V_+ = 5.5 V

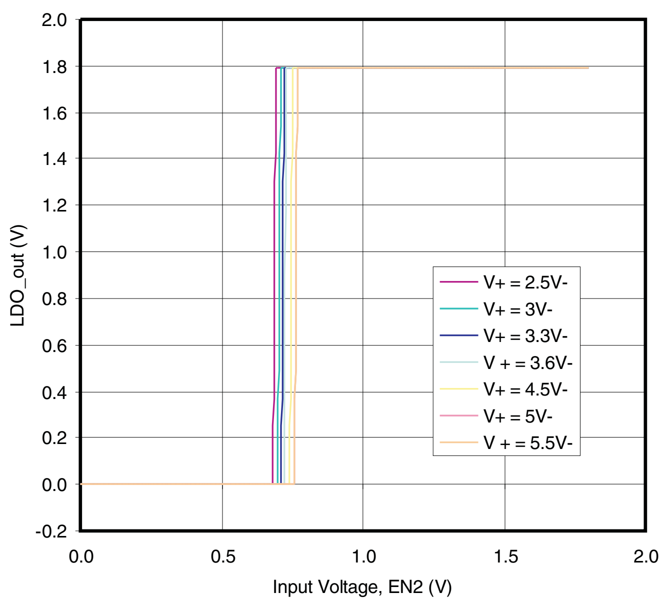


Figure 30. EN2 (LDO) Input Thresholds, V_{IN} = 3.3 V

A. V_{DRV} signal forces the device to go into over-current mode

B. V_{DRV} signal forces the device to go into over-current mode

TYPICAL CHARACTERISTICS (continued)

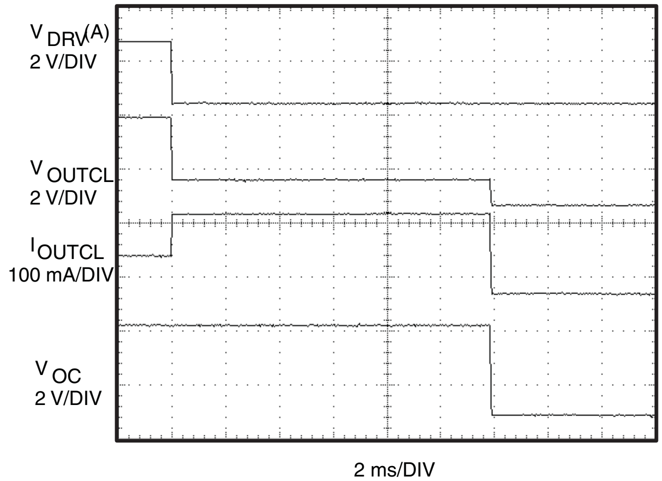


Figure 31. t_{BLANK} Response

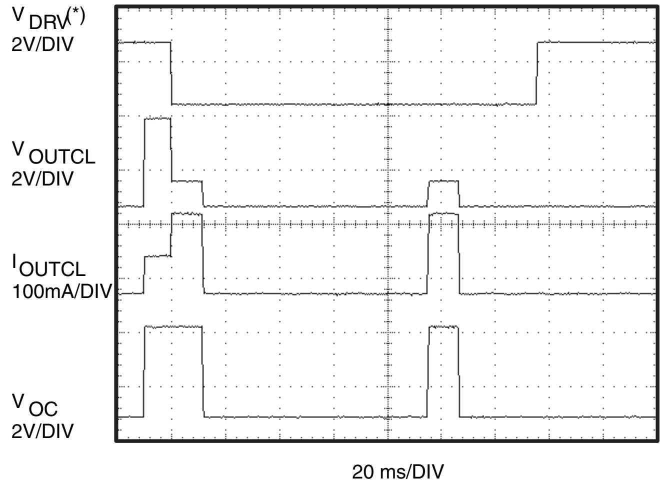


Figure 32. $t_{RESTART}$ Response

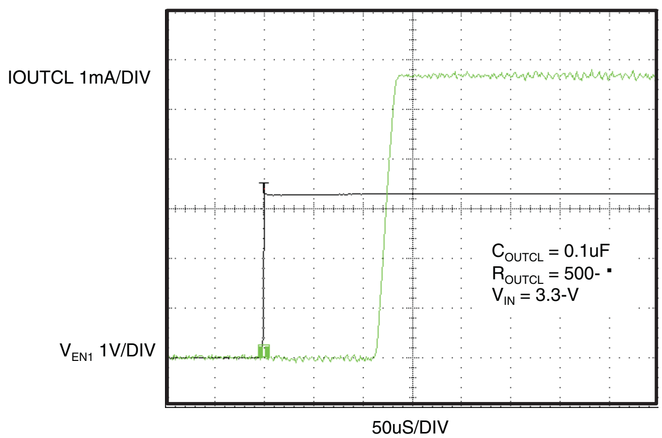


Figure 33. Current Limiter t_{ON} Response

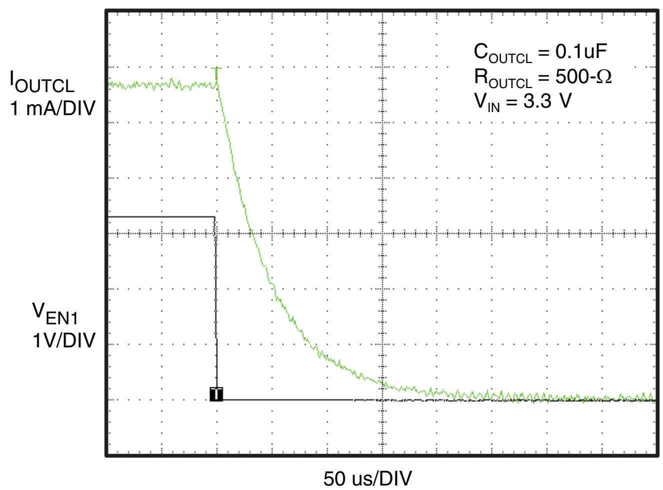


Figure 34. Current Limiter t_{OFF} Response

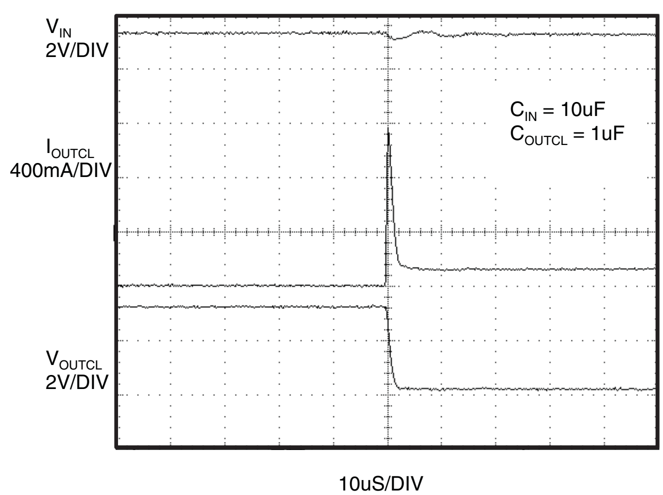


Figure 35. Short-Circuit Response Time (V_{OUTCL} Shorted to GND)

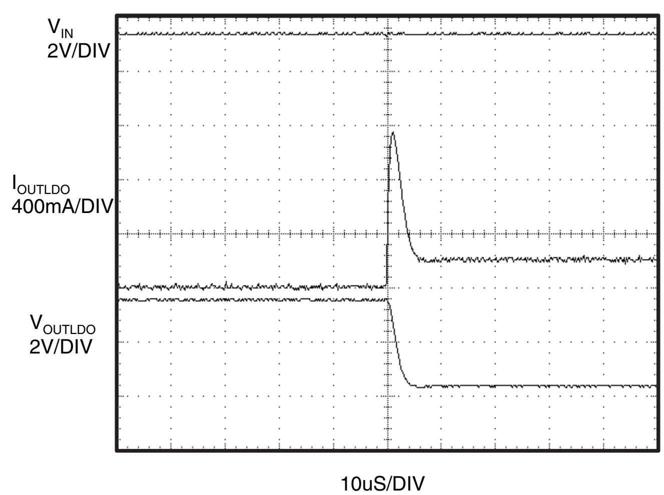


Figure 36. Short-Circuit Response Time (V_{OUTLDO} Shorted to GND)

TYPICAL CHARACTERISTICS (continued)

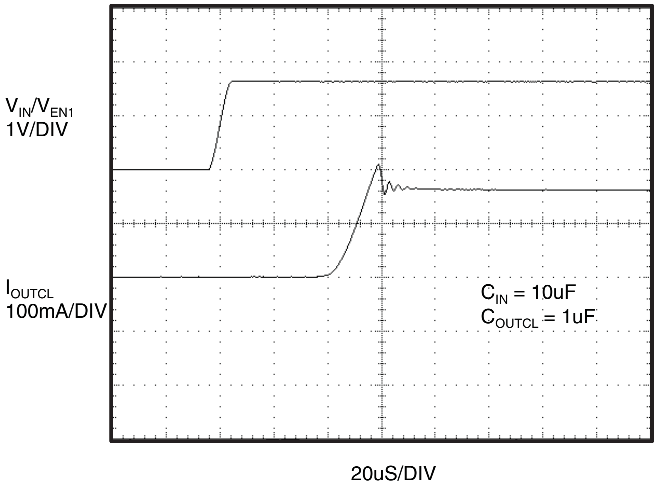


Figure 37. Short-Circuit Response Time (Switch Power-Up to Hard Short) (TPS22949)

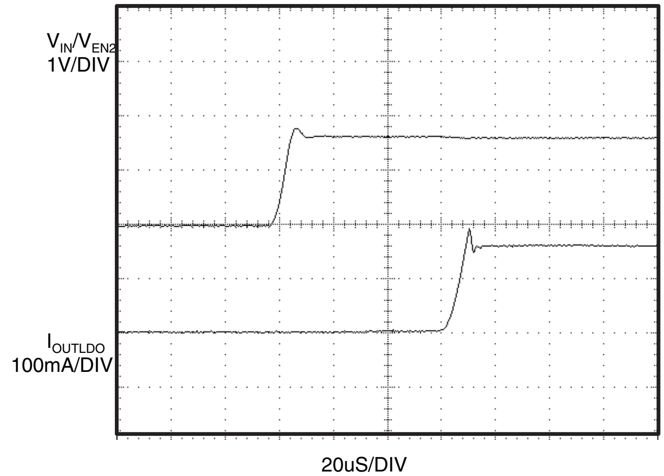


Figure 38. Short-Circuit Response Time (LDO Power-Up to Hard Short) (TPS22949)

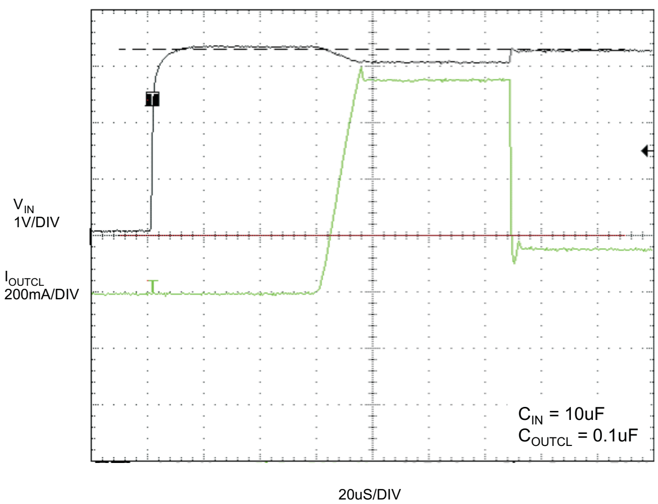


Figure 39. Short-Circuit Response Time (Switch Power-Up to Hard Short) (TPS22949A)

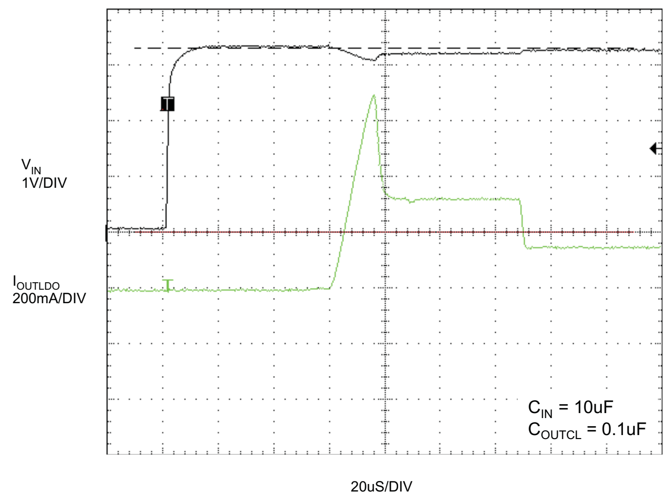


Figure 40. Short-Circuit Response Time (LDO Power-Up to Hard Short) (TPS22949A)

TYPICAL CHARACTERISTICS (continued)

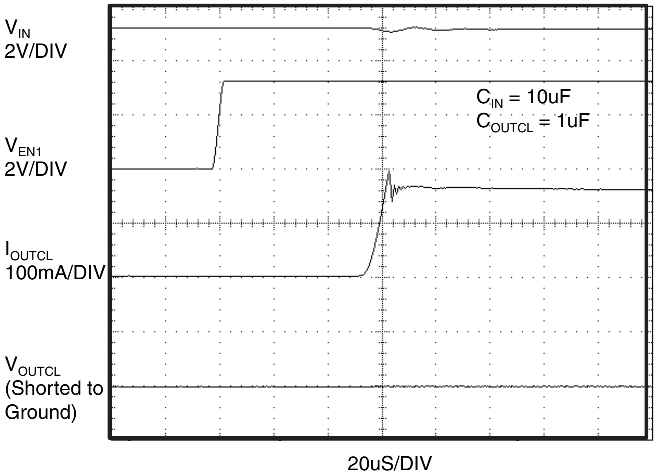


Figure 41. Current Limit Response Time (Current Limiter)

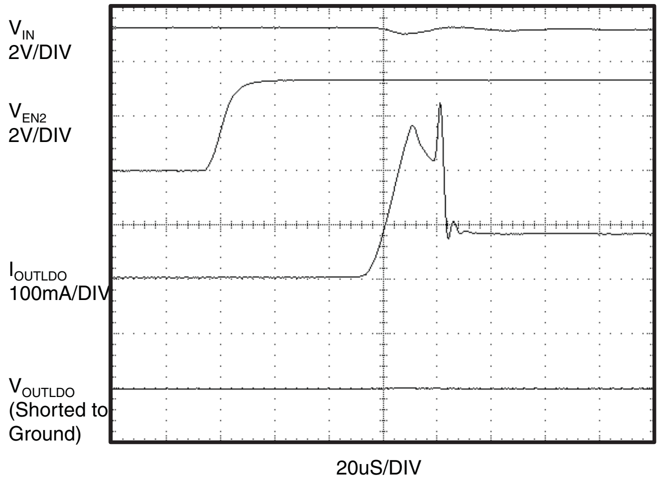


Figure 42. Current Limit Response Time (LDO)

APPLICATION INFORMATION

Undervoltage Lockout (UVLO)

The undervoltage lockout turns off the switch if the input voltage drops below the undervoltage lockout threshold. With the ON pin active, the input voltage rising above the undervoltage lockout threshold causes a controlled turn-on of the switch, which limits current over-shoots. The TPS22949/TPS22949A also has a UVLO on the V_+ bias voltage and keep the output of the LDO shut off until the internal circuitry is operating properly.

Fault Reporting

When an overcurrent, input undervoltage, or overtemperature condition is detected, OC is set active low to signal the fault mode. OC is an open-drain MOSFET and requires a pullup resistor between V_{IN} and OC. During shutdown, the pulldown on OC is disabled, reducing current draw from the supply.

Current Limiting

When the switch current reaches the maximum limit, the TPS22949/TPS22949A operates in a constant-current mode to prohibit excessive currents from causing damage. TPS22949/TPS22949A has a minimum current limit of 100 mA.

Input Voltage

The input voltage (V_{IN}) of the current limiter is set from 1.62 V to 4.5 V, however if both the current limiter and the LDO are enabled, the user must be careful to keep the input voltage (V_{IN}) greater than 1.8 V + (voltage drop through the switch) + (voltage drop through the LDO); otherwise, the LDO does not have a high enough internal input signal to operate properly.

A current limiter input voltage ramp time less than the blanking time (~10 ms typical) is recommended. If the ramp time extends beyond the blanking period, then the current limiter goes into recycle, and the system may not start or operate properly.

Input/Output Capacitors

Although an input capacitor is not required for stability of on the input pin (V_{IN}), it is good analog design practice to connect a 0.1-μF to 1-μF low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher value capacitor may be necessary if large, fast rise time load transients are anticipated, or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability. The V_+ bias pin does not require an input capacitor because it does not source high currents. However, if source impedance is not sufficiently low, a small 0.1-μF bypass capacitor is recommended.

A 0.1-μF capacitor C_{CL}, should be placed between V_{OUTCL} and GND. This capacitor prevents parasitic board inductances from forcing V_{OUTCL} below GND when the switch turns off. For the TPS22949, the total output capacitance must be kept below a maximum value, $C_{CL(max)}$, to prevent the part from registering an over-current condition and turning off the switch. The maximum output capacitance can be determined from the following formula:

$$C_{CL} = I_{LIM(MAX)} \times t_{BLANK(MIN)} \div V_{IN}$$

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_{CL} is highly recommended. A C_{CL} greater than C_{IN} can cause V_{OUTCL} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUTCL} to V_{IN}.

On TPS22949, a storage capacitor (C_{CL}) at the output of the current limiter is recommended to provide enough current to the LDO during the start-up sequence. The storage capacitor is needed to reduce the amount of inrush current supplied through the current-limited load switch to the LDO during the power-up sequence (see Figure 44). If the C_{CL} capacitor is too small, the inrush current needed to start the LDO and charge C_{LDO} could be interpreted by the current limiter as an over-current and, therefore, trigger the current-limiting feature of the switch. The switch would then try to limit the current to the 100-mA limit, and the user would see an undesired drop on the supply line (see Figure 45).

On TPS22949A, the storage capacitor (C_{CL}) is not required. TPS22949A integrates an additional internal circuitry that increases the current limit of the switch to approximately 750 mA (i.e $I_{LIM(INRUSH)}$) for about 250 µs (i.e t_{INRUSH}), initiated when the internal circuitry of the LDO is operating properly (i.e., when the UVLO of the LDO bias (V_+) is disabled (V_+ > 2.6 V). Because the current limit is increased during the power-up sequence, a potential inrush current through the LDO is not interpreted by the current limiter as an over-current. The current needed by the LDO is then be supplied by the input capacitor (C_{IN}) of the current limiter (see Figure 45).

The TPS22949 LDO (V_{OUTLDO}) is designed to be stable with standard ceramic capacitors with values of 2.2 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 250 mΩ. Figure 43, Figure 44, and Figure 45 illustrate the behavior of the TPS22949 and TPS22949A with a 100-mA sinking load and different capacitor values for a typical application where both enables are tied to the same input voltage (see Figure 43).

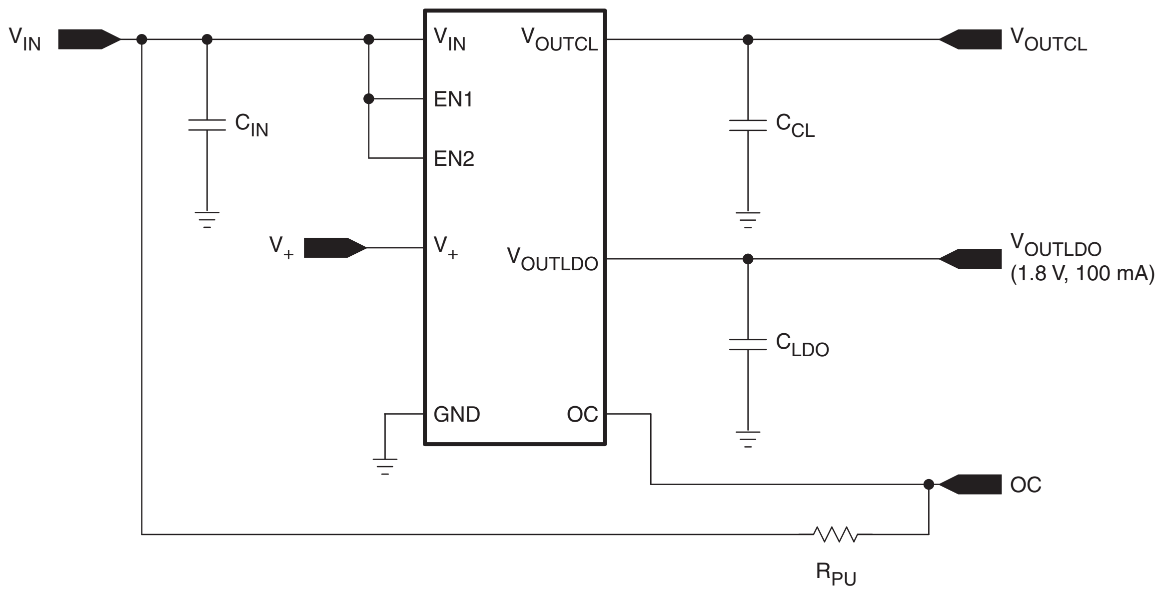


Figure 43. TPS22949/TPS22949A Typical Application With Both Enable Pins Tied to the Input Voltage

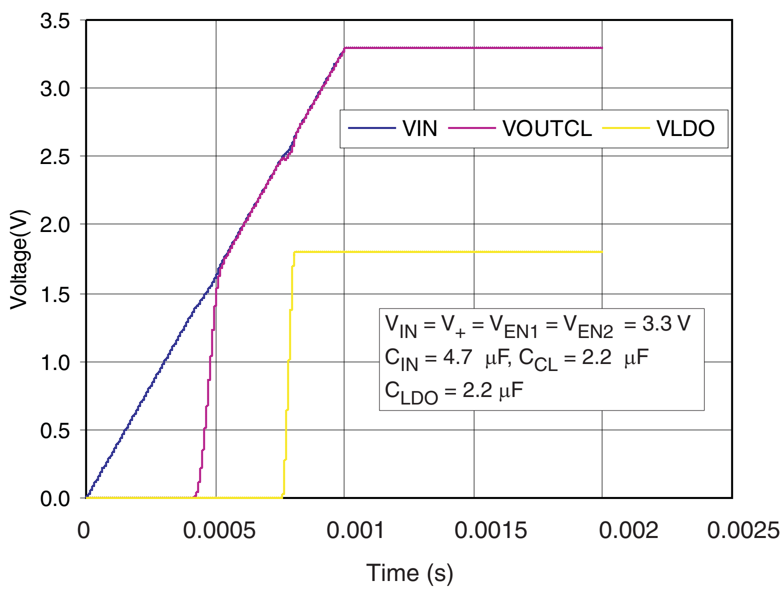


Figure 44. TPS22949 Power-Up Sequence

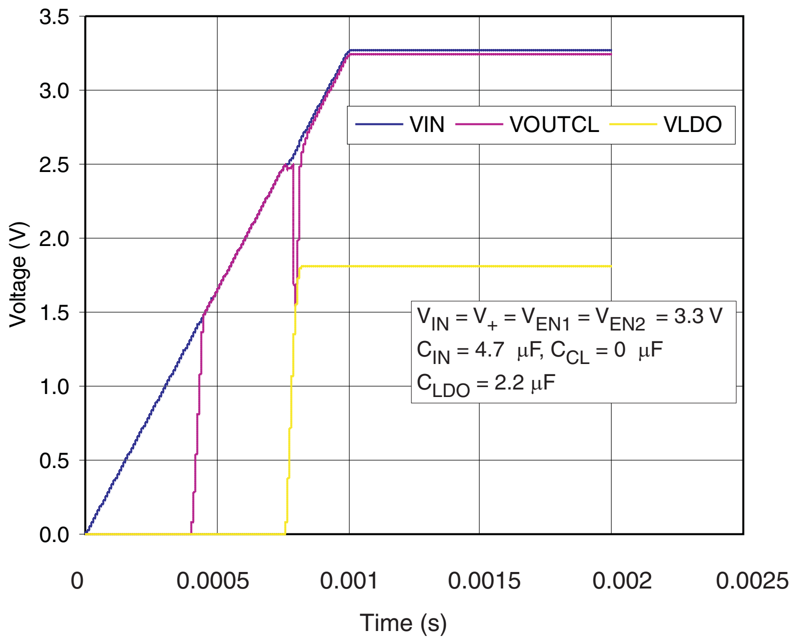


Figure 45. TPS22949 Power-Up Sequence

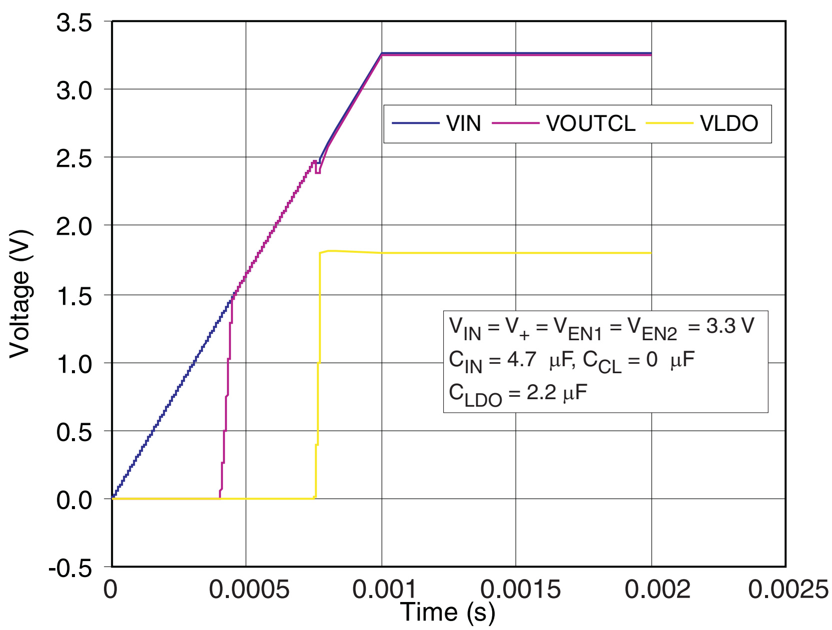


Figure 46. TPS22949A Power-Up Sequence

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS22949ADRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS22949AYZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS22949YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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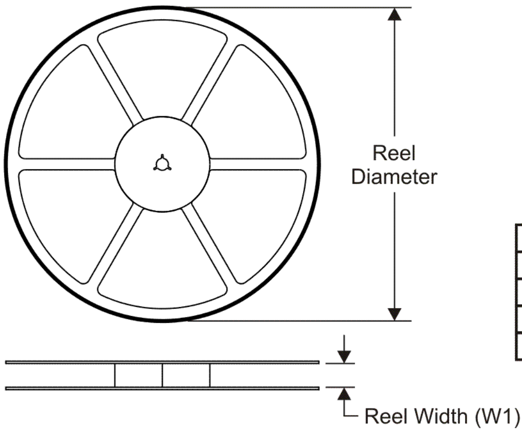
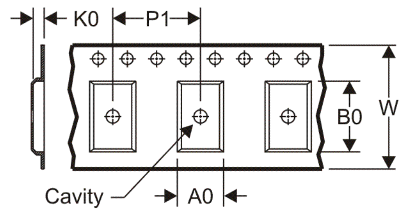
TAPE AND REEL INFORMATION

REEL DIMENSIONS

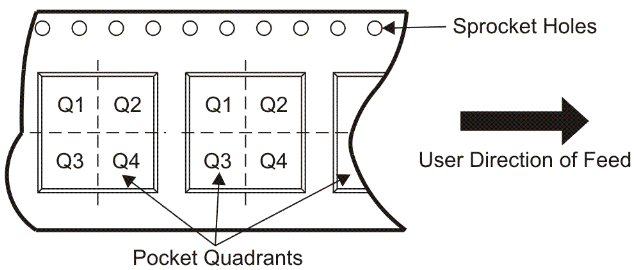


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

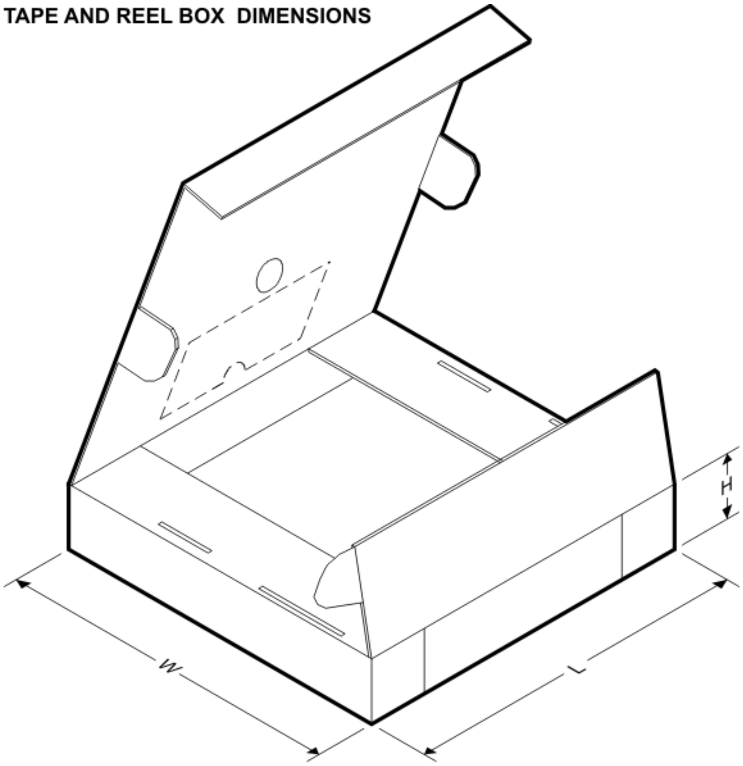
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22949ADRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

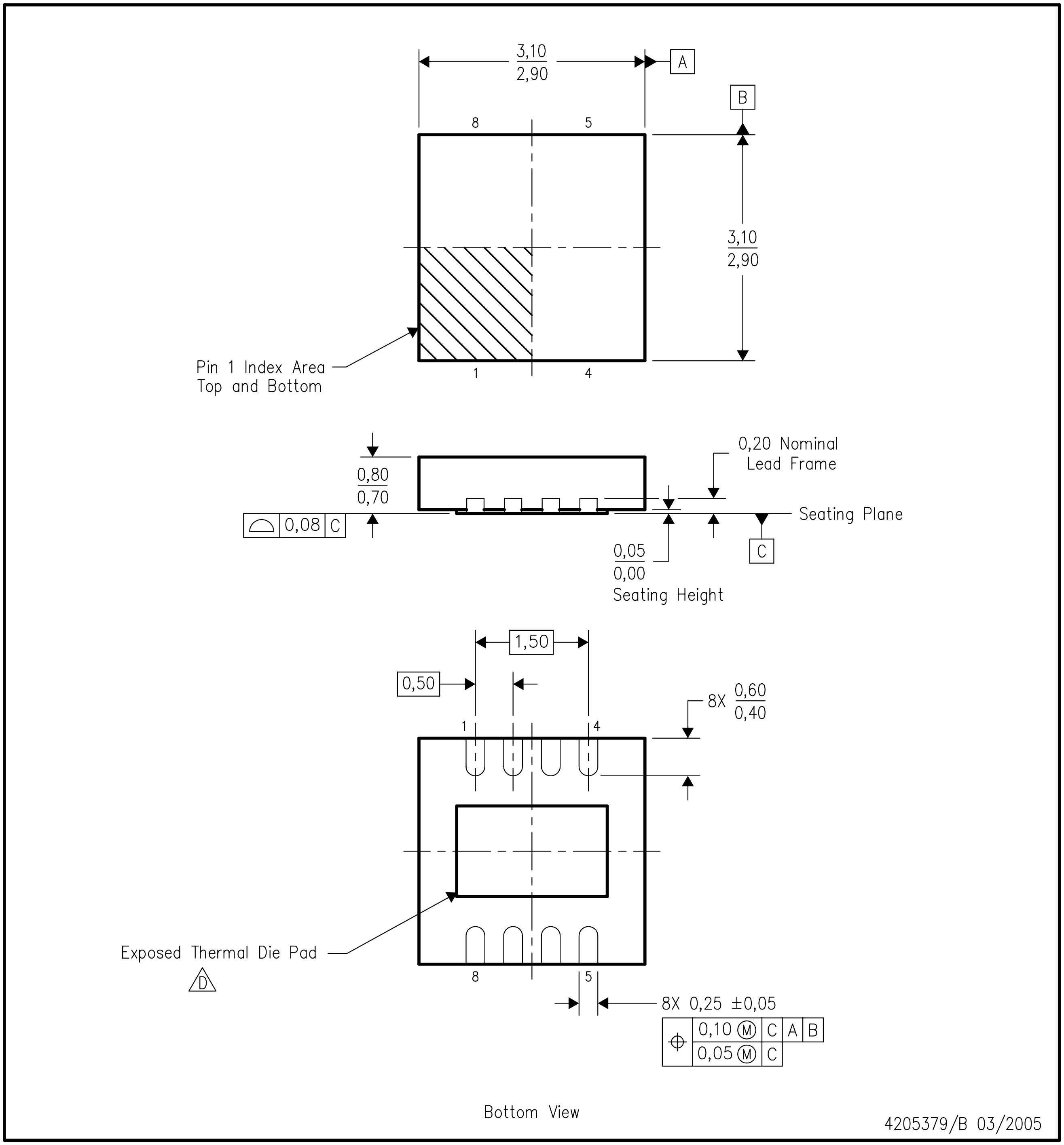
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22949ADRGR	SON	DRG	8	3000	346.0	346.0	29.0

DRG (S–PDSO–N8) PLASTIC SMALL OUTLINE



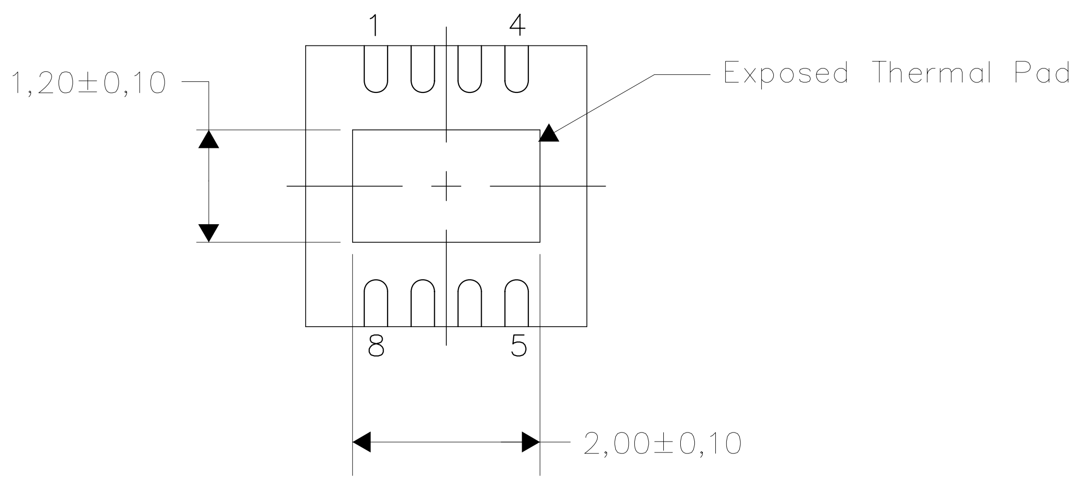
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

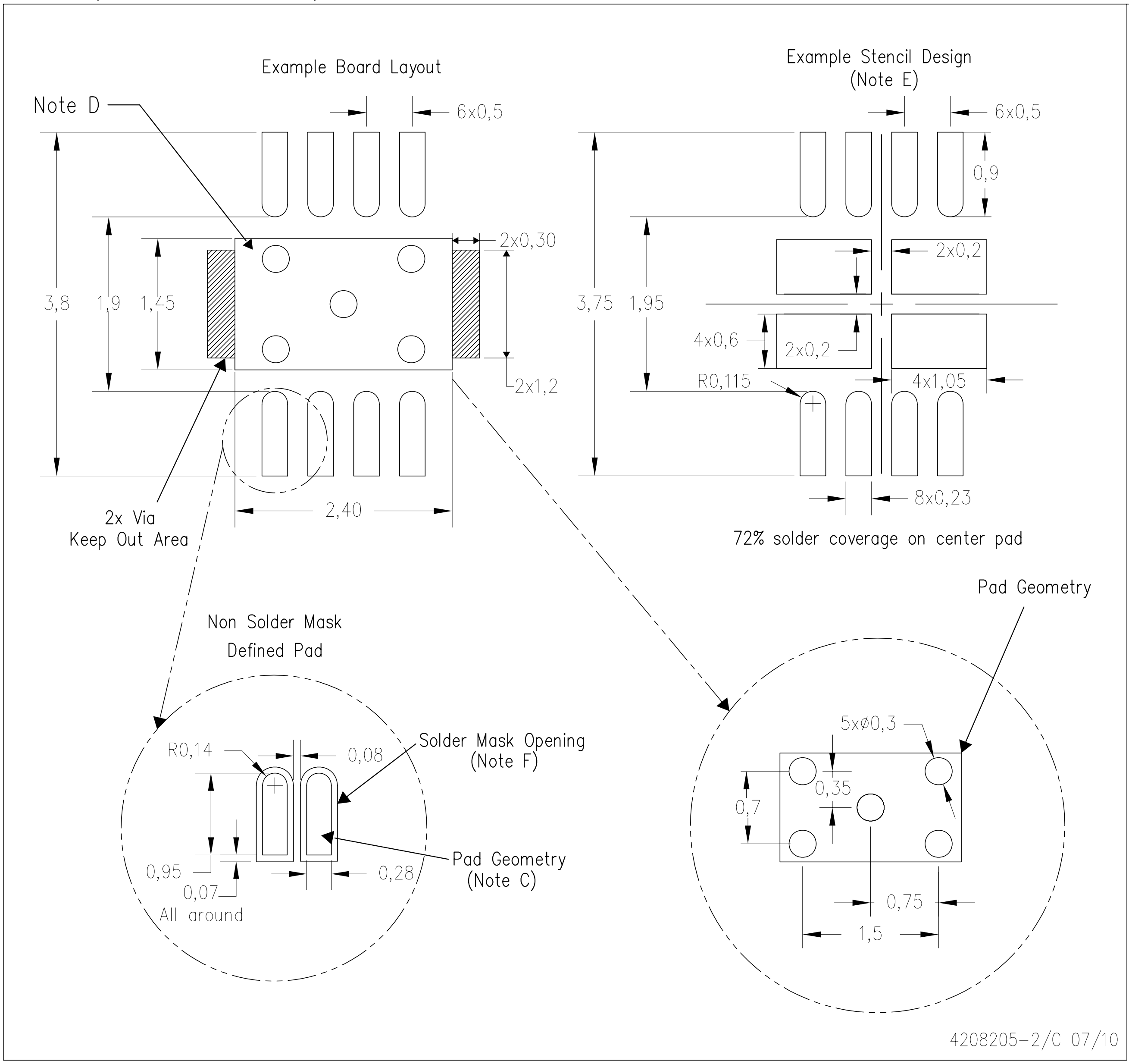


Bottom View

NOTE: All linear dimensions are in millimeters

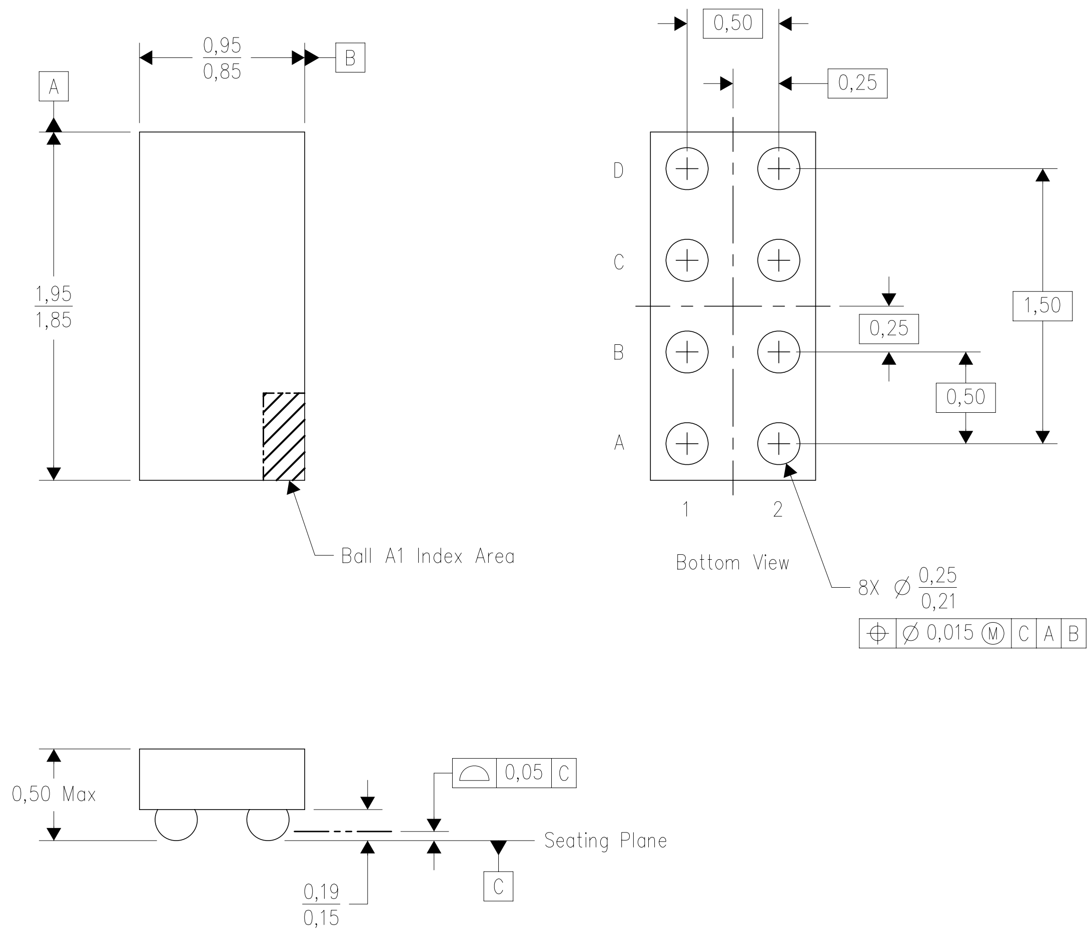
Exposed Thermal Pad Dimensions

DRG (S-PDSO-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



4204741–4/G 07/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

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