

# TPIC2701

## 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

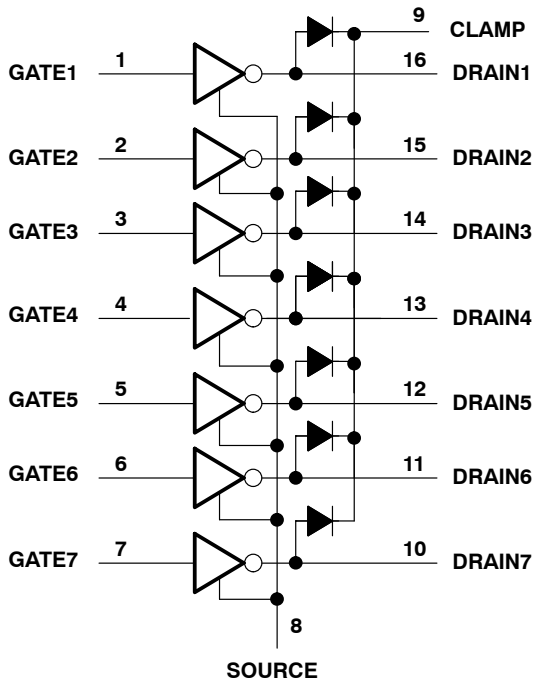
- Seven 0.5-A Independent Output Channels
- Integrated Clamp Diode With Each Output
- Low  $r_{DS(on)}$  . . . 0.5  $\Omega$  Typical
- Output Voltage . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Avalanche Energy . . . 22 mJ

### description

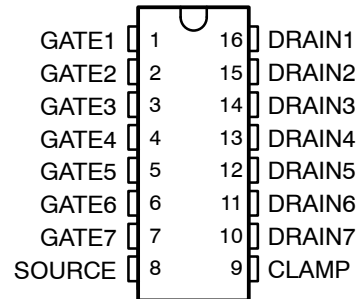
The TPIC2701 is a monolithic power DMOS transistor array that consists of seven independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains. The TPIC2701 is pin-for-pin functionally compatible with the Texas Instruments ULN2001A through ULN2004A.

The TPIC2701 is characterized for operation over a temperature range of 0°C to 125°C. The TPIC2701M is characterized for operation over the full military temperature range of -55°C to 125°C.

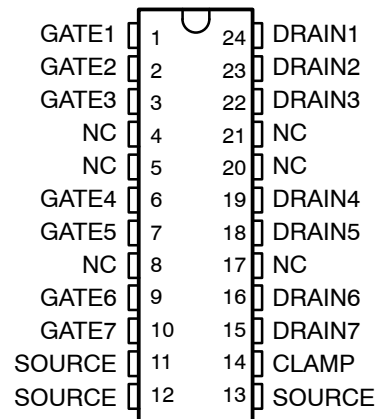
### logic diagram



**TPIC2701**  
**N PACKAGE**  
**(TOP VIEW)**



**TPIC2701M**  
**J PACKAGE†**  
**(TOP VIEW)**



NC – No internal connection

† Refer to the mechanical data for the JW package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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## 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

### absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, $V_{DS}$	60 V
Gate-source voltage, $V_{GS}$	$\pm 20$ V
Clamp-drain voltage, $V_{CD}$	60 V
Continuous source-drain diode current	0.5 A
Pulsed drain current, each output, $I_D$ (see Note 1 and Figure 17)	3 A
Pulsed clamp current, $I_{CL}$ (see Note 1 and Figure 18)	3 A
Continuous drain current, each output, all outputs on	0.5 A
Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)	22 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ : TPIC2701	$-40^\circ\text{C}$ to $150^\circ\text{C}$
TPIC2701M	$-55^\circ\text{C}$ to $150^\circ\text{C}$
Operating case temperature range, $T_C$ : TPIC2701	$-40^\circ\text{C}$ to $125^\circ\text{C}$
TPIC2701M	$-55^\circ\text{C}$ to $125^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N Package	$260^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J Package	$300^\circ\text{C}$

NOTE 1: Pulse duration = 10 ms, duty cycle = 6%.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
J	2660 mW	21.3 mW/ $^\circ\text{C}$	1701 mW	1382 mW	530 mW
N	1400 mW	11.0 mW/ $^\circ\text{C}$	905 mW	740 mW	300 mW

### electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
$V_{(BR)DS}$ Drain-source breakdown voltage	$I_D = 1 \mu\text{A}$ , $V_{GS} = 0$	60			V
$V_{TGS}$ Gate-source threshold voltage	$I_D = 1 \text{ mA}$ , $V_{DS} = V_{GS}$	1.2	1.75	2.4	V
$V_{DS(on)}$ Drain-source on-state voltage	$I_D = 0.5 \text{ A}$ , $V_{GS} = 15 \text{ V}$ , See Notes 2 and 3		0.25	0.4	V
$I_{DSS}$ Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$
		$T_C = 125^\circ\text{C}$	0.5	10	
$I_{GSSF}$ Forward gate current, drain short circuited to source	$V_{GS} = 20 \text{ V}$ , $V_{DS} = 0$		10	100	nA
$I_{GSSR}$ Reverse gate current, drain short circuited to source	$V_{GS} = -20 \text{ V}$ , $V_{DS} = 0$		10	100	nA
$r_{DS(on)}$ Forward drain-source on-state resistance	$V_{GS} = 15 \text{ V}$ , $I_D = 0.5 \text{ A}$ , See Notes 2 and 3 and Figures 5 and 6	$T_C = 25^\circ\text{C}$	0.5	0.8	$\Omega$
		$T_C = 125^\circ\text{C}$	0.8	1.3	
$g_{fs}$ Forward transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 0.5 \text{ A}$ , See Notes 2 and 3	0.5	0.8		S
$C_{iss}$ Short-circuit input capacitance, common source	$V_{DS} = 25 \text{ V}$ , $V_{GS} = 0$ , $f = 300 \text{ kHz}$		105		pF
$C_{oss}$ Short-circuit output capacitance, common source			65		
$C_{riss}$ Short-circuit reverse transfer capacitance, common source			15		

NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts with a single output transistor conducting.



# TPIC2701

## 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

**electrical characteristics over case temperature operating range (unless otherwise noted) (see Note 4)**

PARAMETER	TEST CONDITIONS	T <sub>C</sub> <sup>†</sup>	TPIC2701M			UNIT
			MIN	TYP	MAX	
V <sub>(BR)DS</sub> Drain-to-source breakdown voltage	I <sub>D</sub> = 1 μA, V <sub>GS</sub> = 0	25°C	60			V
	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	Full range				
V <sub>TGS</sub> Gate-to-source input threshold voltage	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = V <sub>GS</sub>	Full range	1.2	1.75	2.4	V
V <sub>DS(on)</sub> Drain-to-source on-state voltage	I <sub>D</sub> = 0.5 A, V <sub>GS</sub> = 15 V	25°C	0.25		0.45	V
		Full range			0.65	
I <sub>DSS</sub> Zero-gate-voltage drain current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0	25°C	0.05		1	μA
		Full range			10	
I <sub>GSSF</sub> Forward gate current, drain short-circuited to source	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0	25°C	10		100	nA
		Full range			10	μA
I <sub>GSSR</sub> Reverse gate current, drain short-circuited to source	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0	25°C	10		100	nA
		Full range			10	μA
r <sub>DS(on)</sub> Forward drain-source on-state resistance	V <sub>GS</sub> = 15 V, I <sub>D</sub> = 0.5 A	25°C	0.5		0.9	Ω
		Full range			1.3	
g <sub>fs</sub> Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.5 A	25°C	0.8			S
C <sub>iss</sub> Short-circuit input capacitance, common source	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0, f = 300 kHz	Full range	105		pF	
C <sub>oss</sub> Short-circuit output capacitance, common source			65			
C <sub>rss</sub> Short-circuit reverse transfer capacitance, common source			15			

<sup>†</sup> Full range is -55°C to 125°C.

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

### source-drain diode characteristics, T<sub>C</sub> = 25°C

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
V <sub>SD</sub> Forward On voltage	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0	0.9		1.4	V
t <sub>rr(SD)</sub> Reverse-recovery time	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0, V <sub>DS</sub> = 48 V, di/dt = 25 A/μs, See Figure 1	165			ns
Q <sub>RR</sub> Total source-drain diode charge		250			nC

### source-to-drain diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
V <sub>SD</sub> Forward On voltage	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0	0.9		1.4	V
t <sub>rr</sub> Reverse recovery time	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0, V <sub>DS</sub> = 48 V, di/dt = 25 A/μs, T <sub>C</sub> = 25°C, See Figure 1	165			ns
Q <sub>RR</sub> Total source-to-drain diode charge		250			nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.



# TPIC2701

## 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

### clamp diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
$V_F$ Forward on-voltage	$I_F = 0.5\text{ A}$		1	1.5	V
$V_{BR}$ Breakdown voltage	$I_R = 1\ \mu\text{A}$	60			V
$I_R$ Reverse leakage current	$V_R = 48\text{ V}$		0.05	1	$\mu\text{A}$
$t_{rr(CD)}$ Reverse-recovery time	$I_F = 0.1\text{ A}$ , $di/dt = 25\text{ A}/\mu\text{s}$ , $V_{CD} = 48\text{ V}$ , See Figure 1		90		ns
$Q_{RR}$ Total source-drain diode charge			100		nC

### clamp diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
$V_F$ Forward voltage	$I_F = 0.5\text{ A}$		1	1.5	V
$V_{(BR)}$ Breakdown voltage	$I_R = 1\ \mu\text{A}$ , $T_C = 25^\circ\text{C}$	60			V
	$I_R = 1\text{ mA}$				
$I_R$ Reverse leakage current	$V_R = 48\text{ V}$ , $T_C = 25^\circ\text{C}$		0.05	1	$\mu\text{A}$
				10	
$t_{rr(SD)}$ Reverse recovery time, source-to-drain	$I_F = 0.1\text{ A}$ , $di/dt = 25\text{ A}/\mu\text{s}$ , $T_C = 25^\circ\text{C}$ , $V_{CD} = 48\text{ V}$ , See Figure 1		90		ns
$Q_{RR}$ Total source-to-drain diode charge			100		nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

### resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$ , $R_L = 100\ \Omega$ , $t_{en} = 10\text{ ns}$ , $t_{dis} = 10\text{ ns}$ , See Figure 2		10		ns
$t_{d(off)}$ Turn-off delay time			30		
$t_r$ Rise time			15		
$t_f$ Fall time			5		
$Q_g$ Total gate charge	$V_{DS} = 48\text{ V}$ , $I_D = 0.25\text{ A}$ , $V_{GS} = 10\text{ V}$ , See Figure 3		2.8	3.6	nC
$Q_{gs}$ Gate-source charge			1.6	2	
$Q_{gd}$ Gate-drain charge			1.2	1.6	



# TPIC2701

## 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

**resistive-load switching characteristics over operating case temperature range (unless otherwise noted) (see Note 4)**

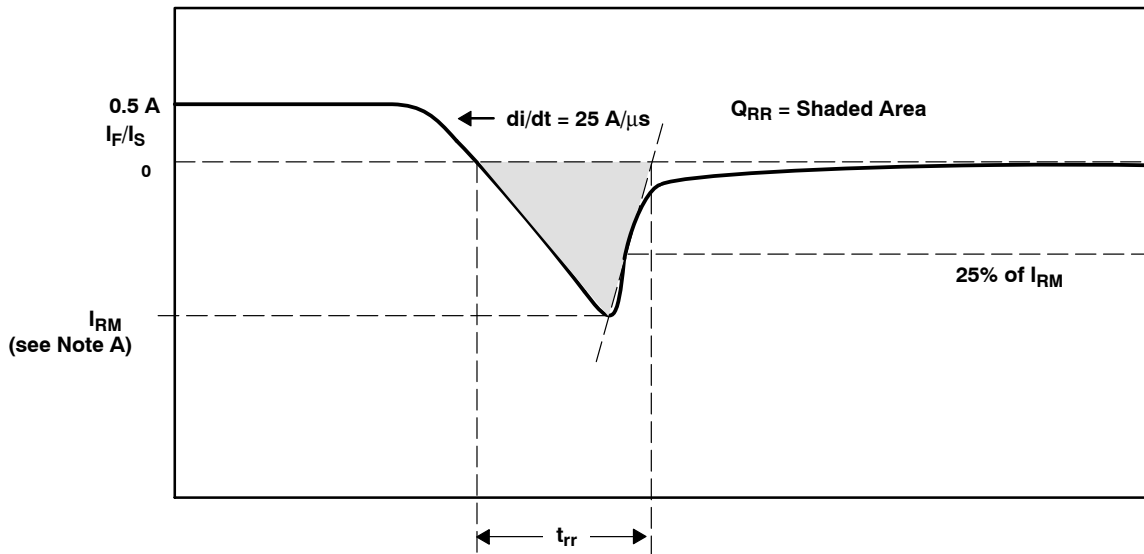
PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$ , $R_L = 100\ \Omega$ , $t_{en} = 10\text{ ns}$ , $t_{dis} = 10\text{ ns}$ , See Figure 2	10			ns
$t_{d(off)}$ Turn-off delay time		30			
$t_r$ Rise time		15			
$t_f$ Fall time		5			
$Q_g$ Total gate charge	$V_{DS} = 48\text{ V}$ , $I_D = 0.25\text{ A}$ , $V_{GS} = 10\text{ V}$ , See Figure 3	2.8			nC
$Q_{gs}$ Gate-to-source charge		1.6			
$Q_{gd}$ Gate-to-drain charge		1.2			

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

### thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	N package with all outputs at equal power			90	$^{\circ}\text{C/W}$
	J package with all outputs at equal power			66	

### PARAMETER MEASUREMENT INFORMATION



NOTE A:  $I_{RM}$  = maximum recovery current

**Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain and Clamp Diodes**



# TPIC2701 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

## PARAMETER MEASUREMENT INFORMATION

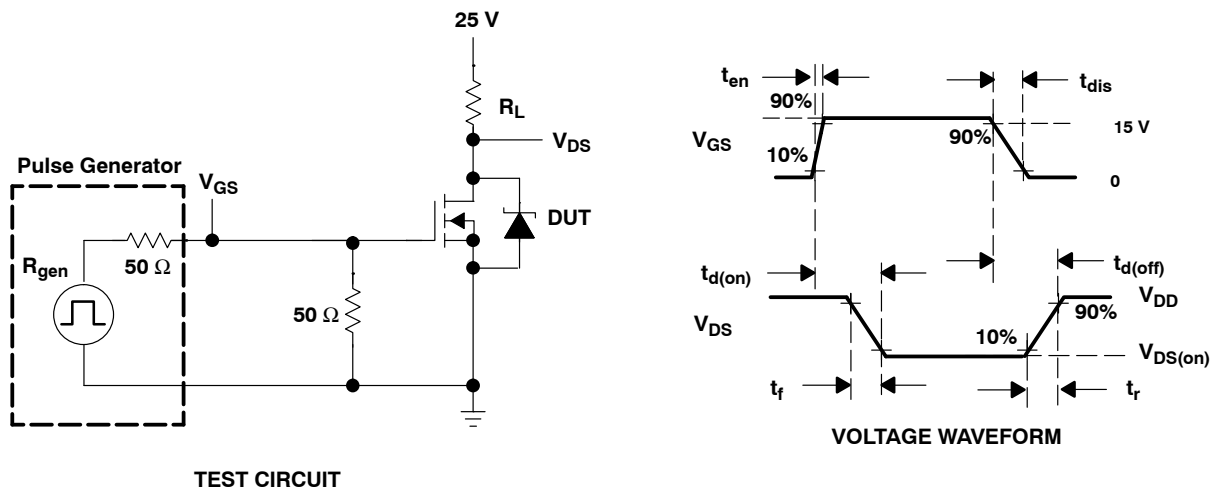


Figure 2. Resistive Switching

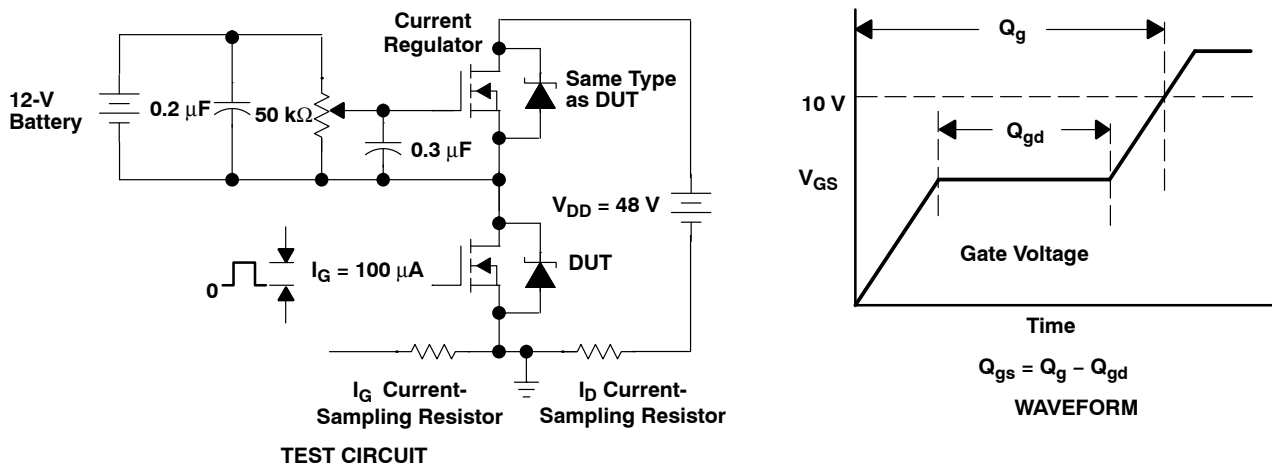
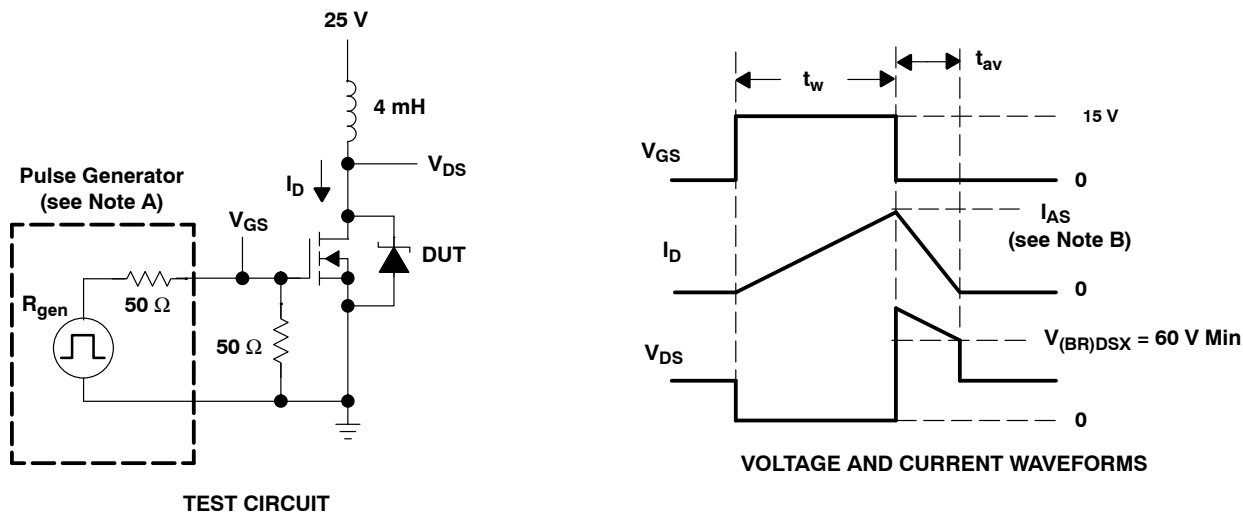


Figure 3. Gate Charge Test Circuit and Waveform

**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 2.5 \text{ A}$ .

Energy test level is defined as 
$$E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22 \text{ mJ min.}$$

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

# TPIC2701 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

## TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
FREE-AIR TEMPERATURE

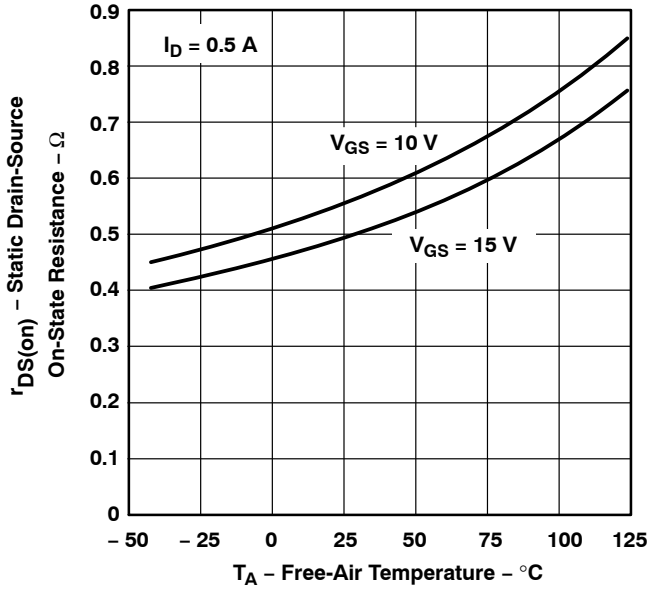


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

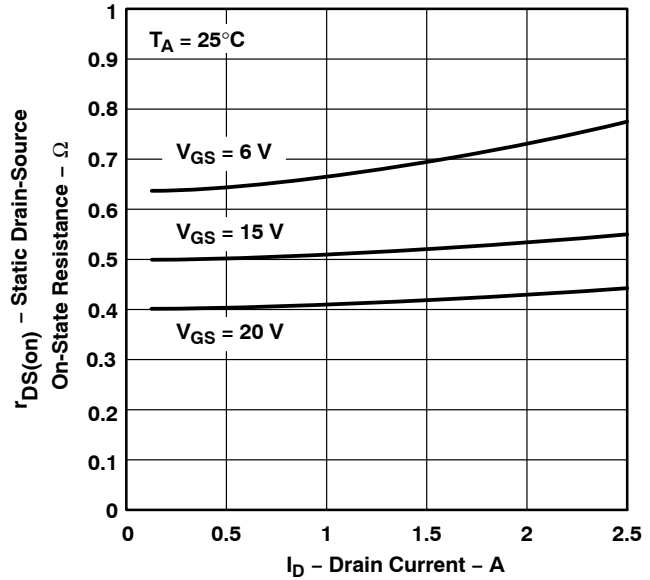


Figure 6

DISTRIBUTION OF  
FORWARD TRANSCONDUCTANCE

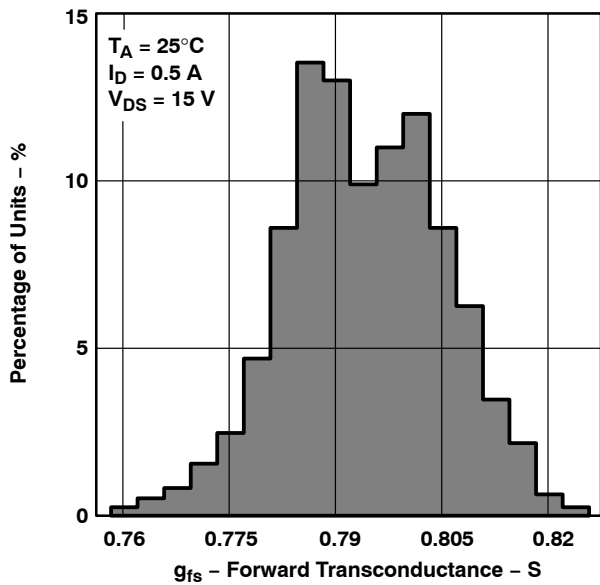


Figure 7

DRAIN-TO-SOURCE CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE

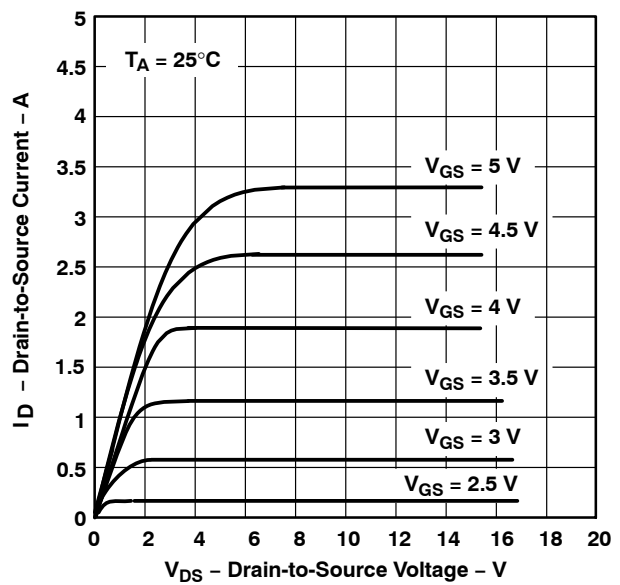
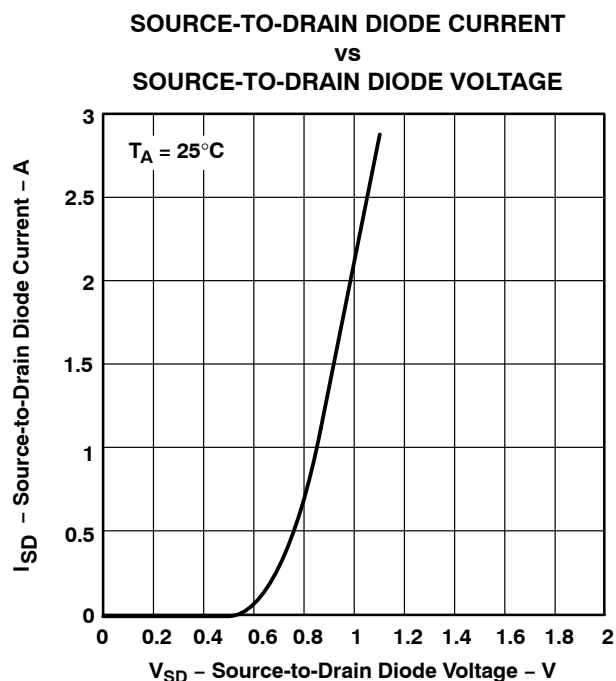
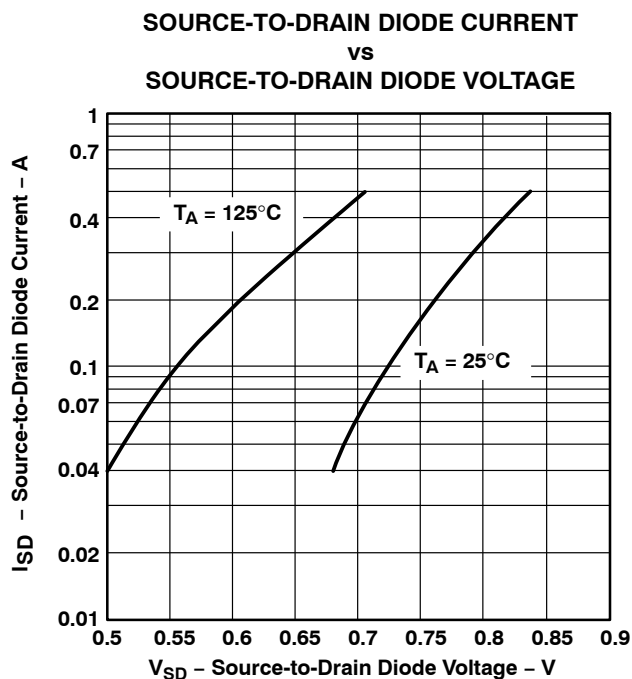
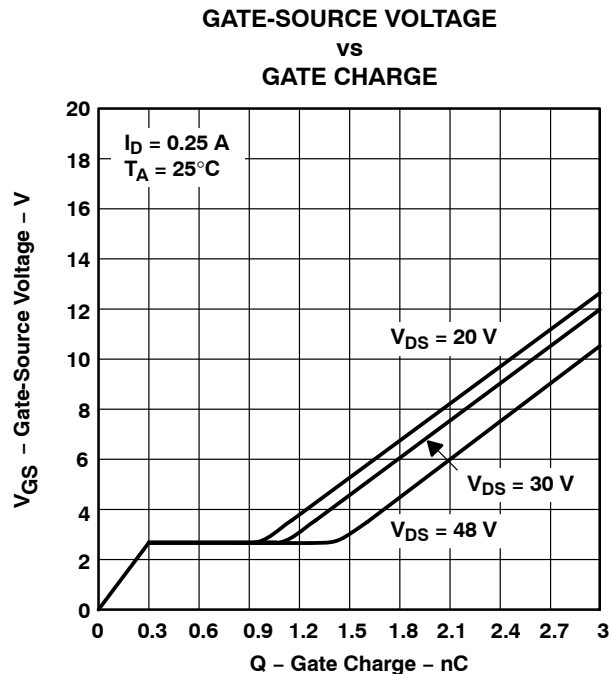
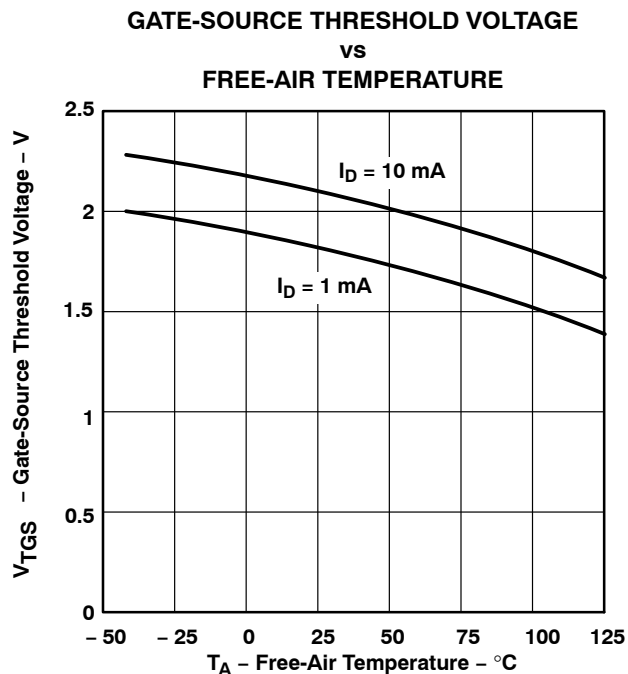


Figure 8



**TYPICAL CHARACTERISTICS**



# TPIC2701 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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## TYPICAL CHARACTERISTICS

CLAMP-DIODE CURRENT  
vs  
CLAMP-DIODE VOLTAGE

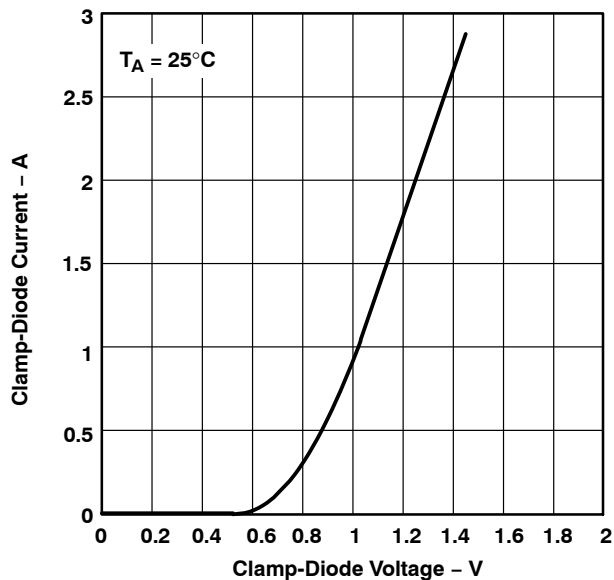


Figure 13

CLAMP-DIODE REVERSE RECOVERY TIME  
vs  
REVERSE di/dt

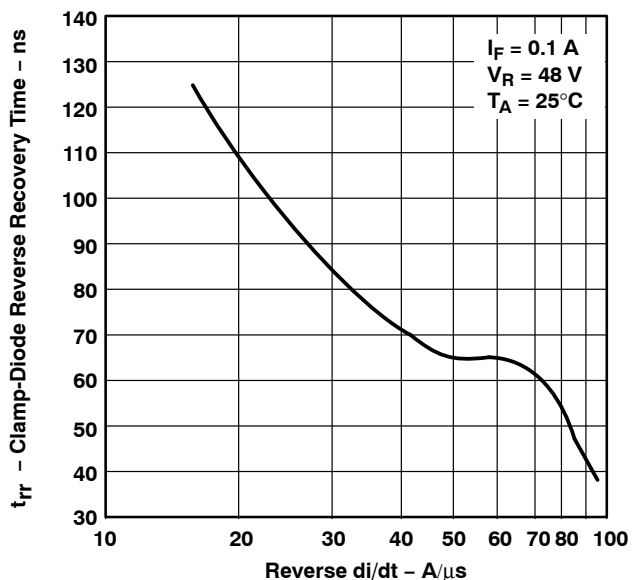
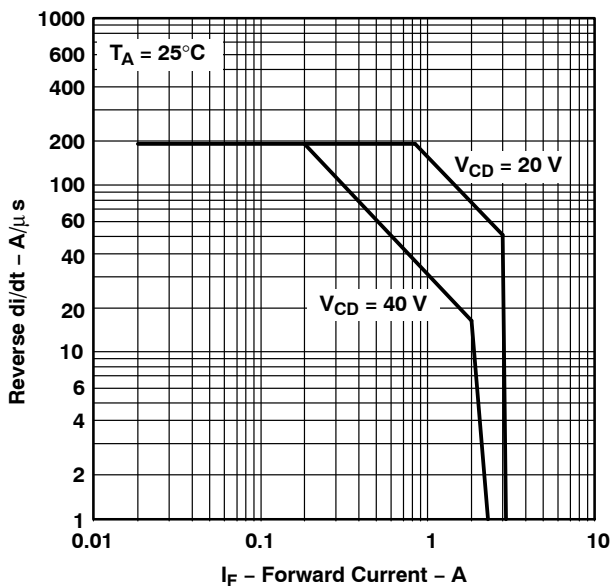


Figure 14

REVERSE di/dt  
vs  
FORWARD CURRENT



NOTE A:  $V_{CD} = V_{clamp} - V_{drain}$

Figure 15



TYPICAL CHARACTERISTICS

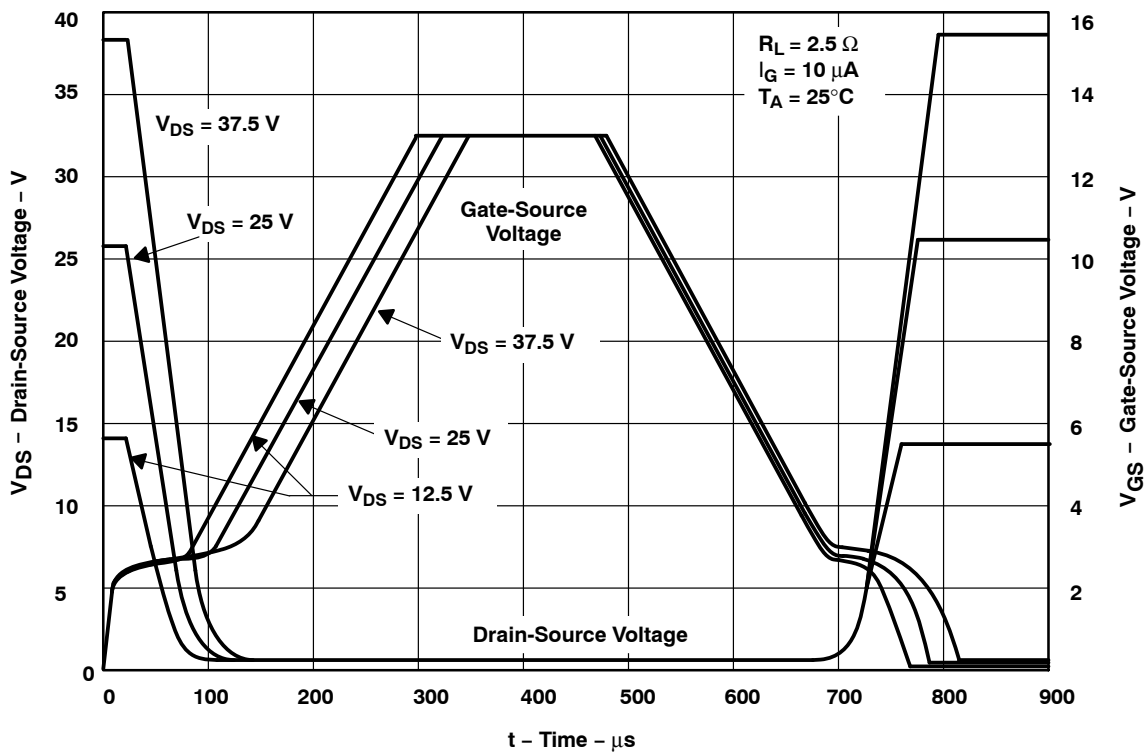


Figure 16. Resistive Switching Waveforms

# TPIC2701 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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## THERMAL INFORMATION

**MAXIMUM DRAIN CURRENT  
vs  
DUTY CYCLE**

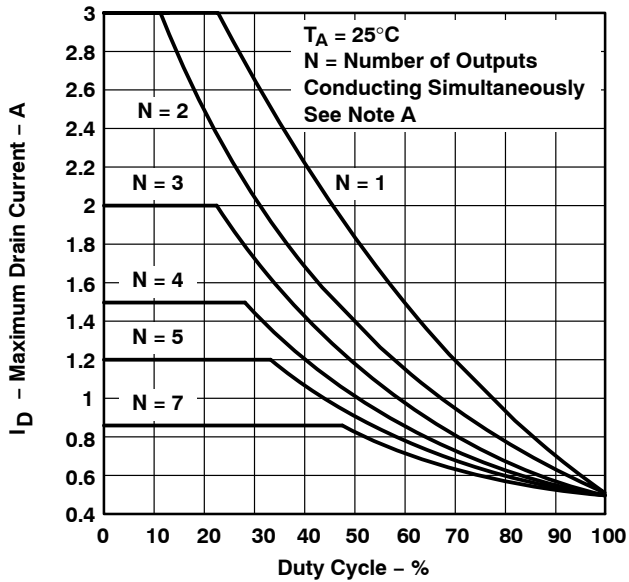


Figure 17

**MAXIMUM CLAMP-DIODE CURRENT  
vs  
DUTY CYCLE**

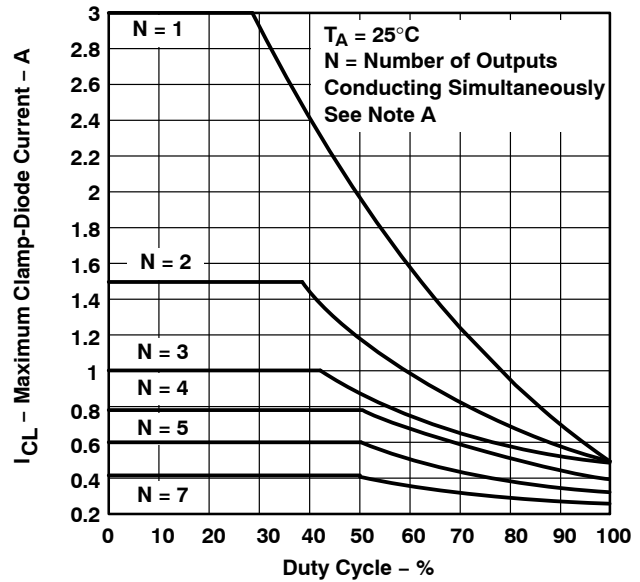
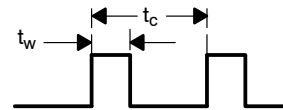


Figure 18

NOTE A: For Figures 17 and 18,  $d = t_w/t_c = 10 \text{ ms} / t_c$ , where  $t_w$  and  $t_c$  are defined by the following:



**PEAK AVALANCHE CURRENT  
vs  
TIME DURATION OF AVALANCHE**

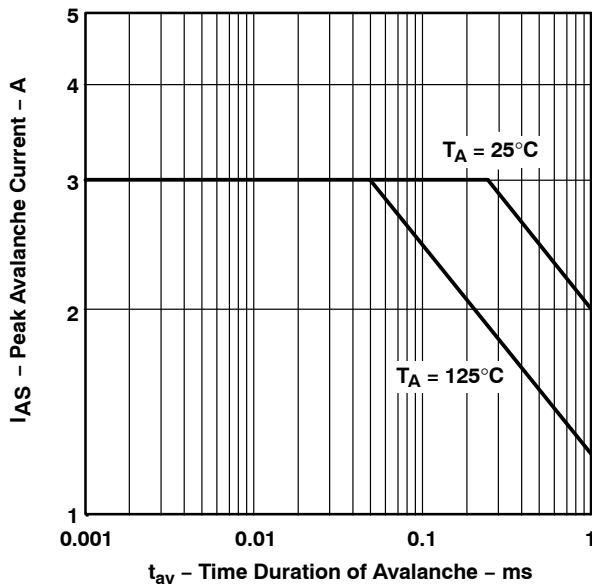


Figure 19

**MAXIMUM DRAIN CURRENT  
vs  
DRAIN-SOURCE VOLTAGE**

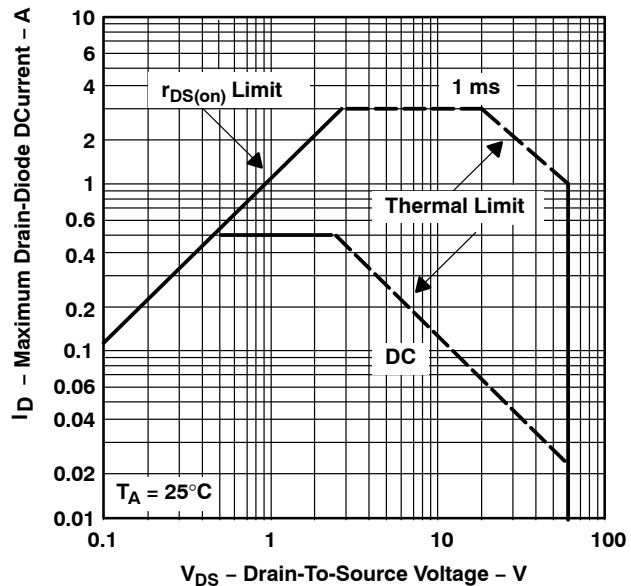


Figure 20

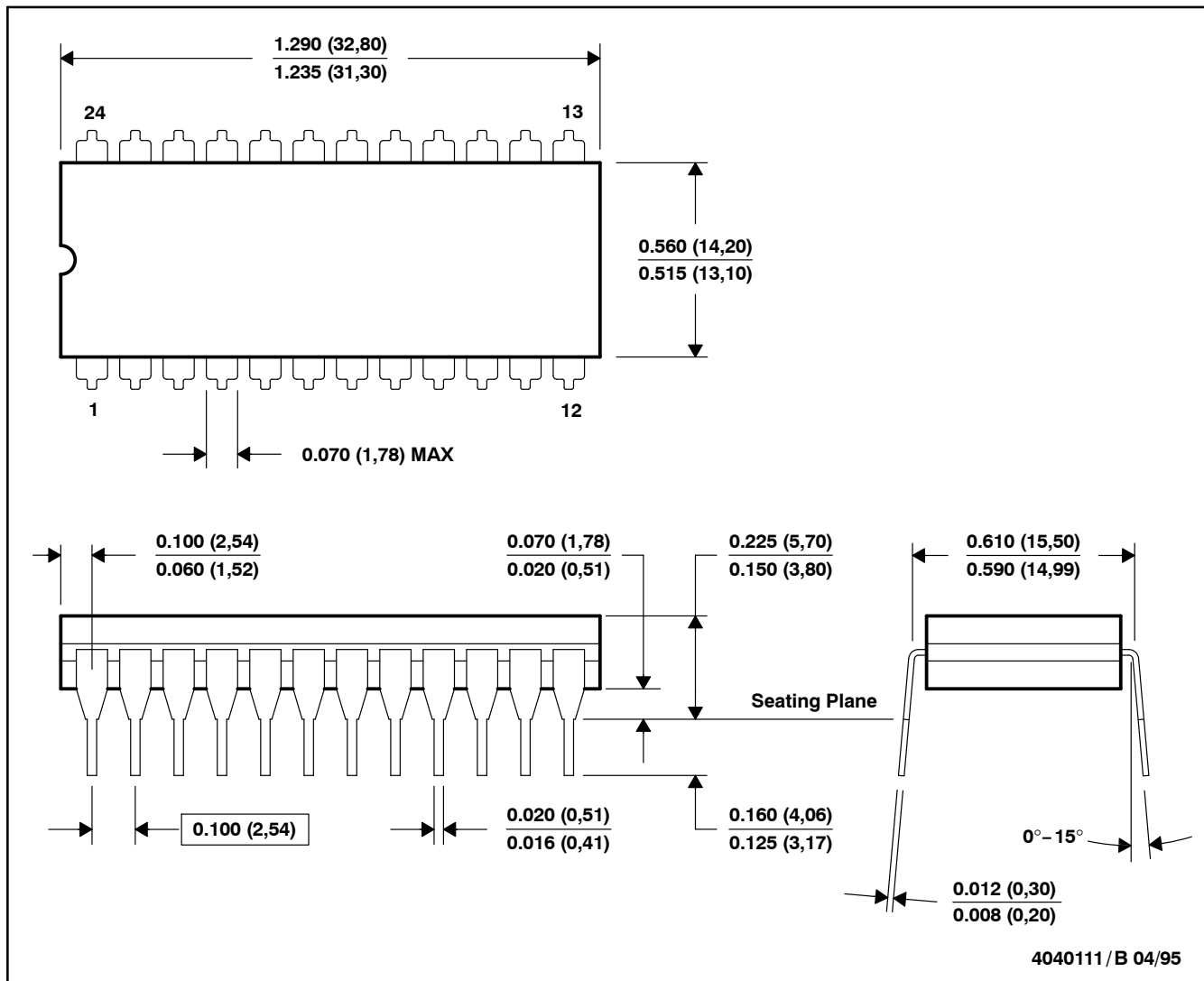
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## MECHANICAL INFORMATION

JW (R-GDIP-T24)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL-STD-1835 GDIP5-T24.

# TPIC2701 7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

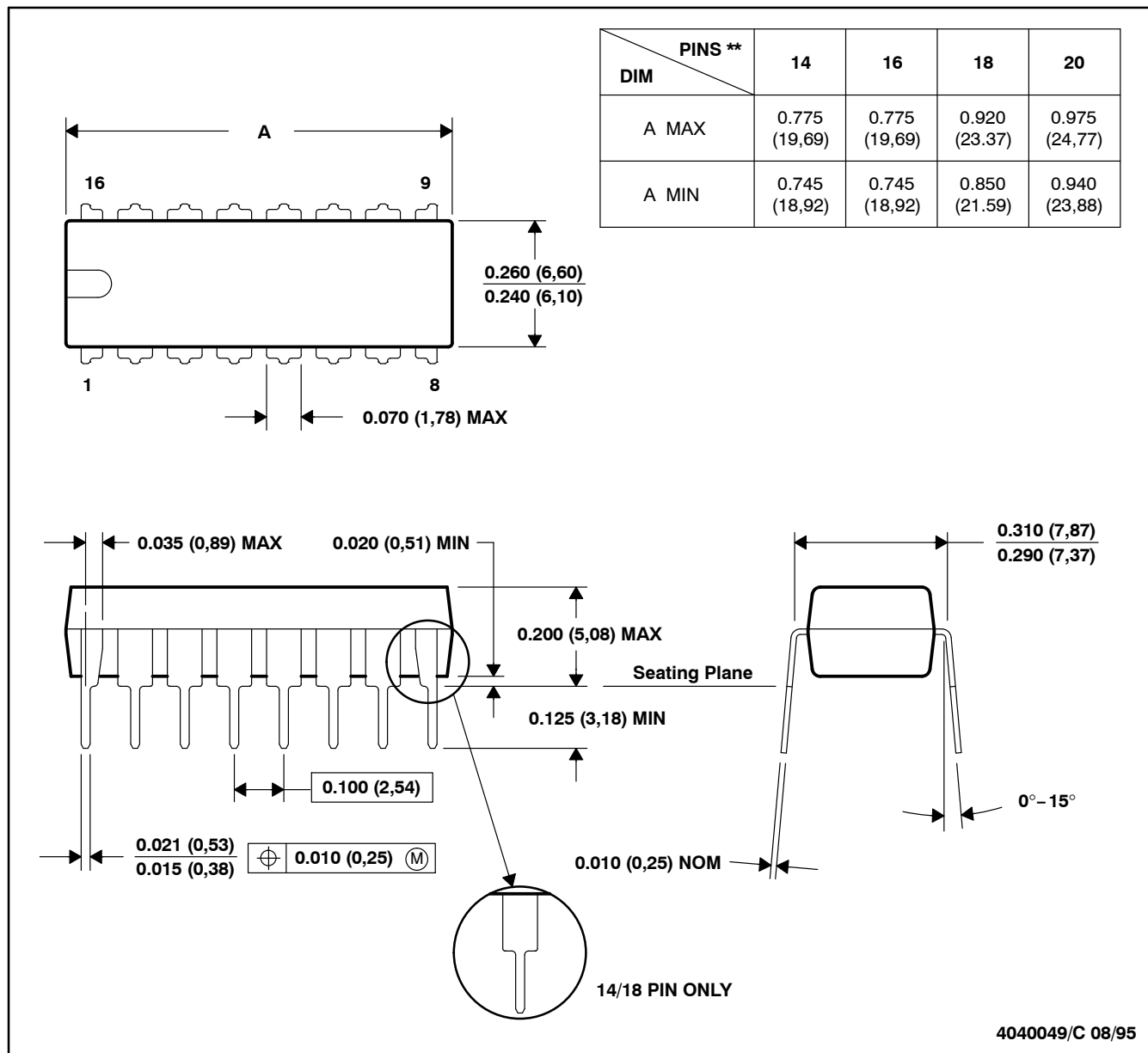
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## MECHANICAL INFORMATION

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC2701MJB	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
TPIC2701N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

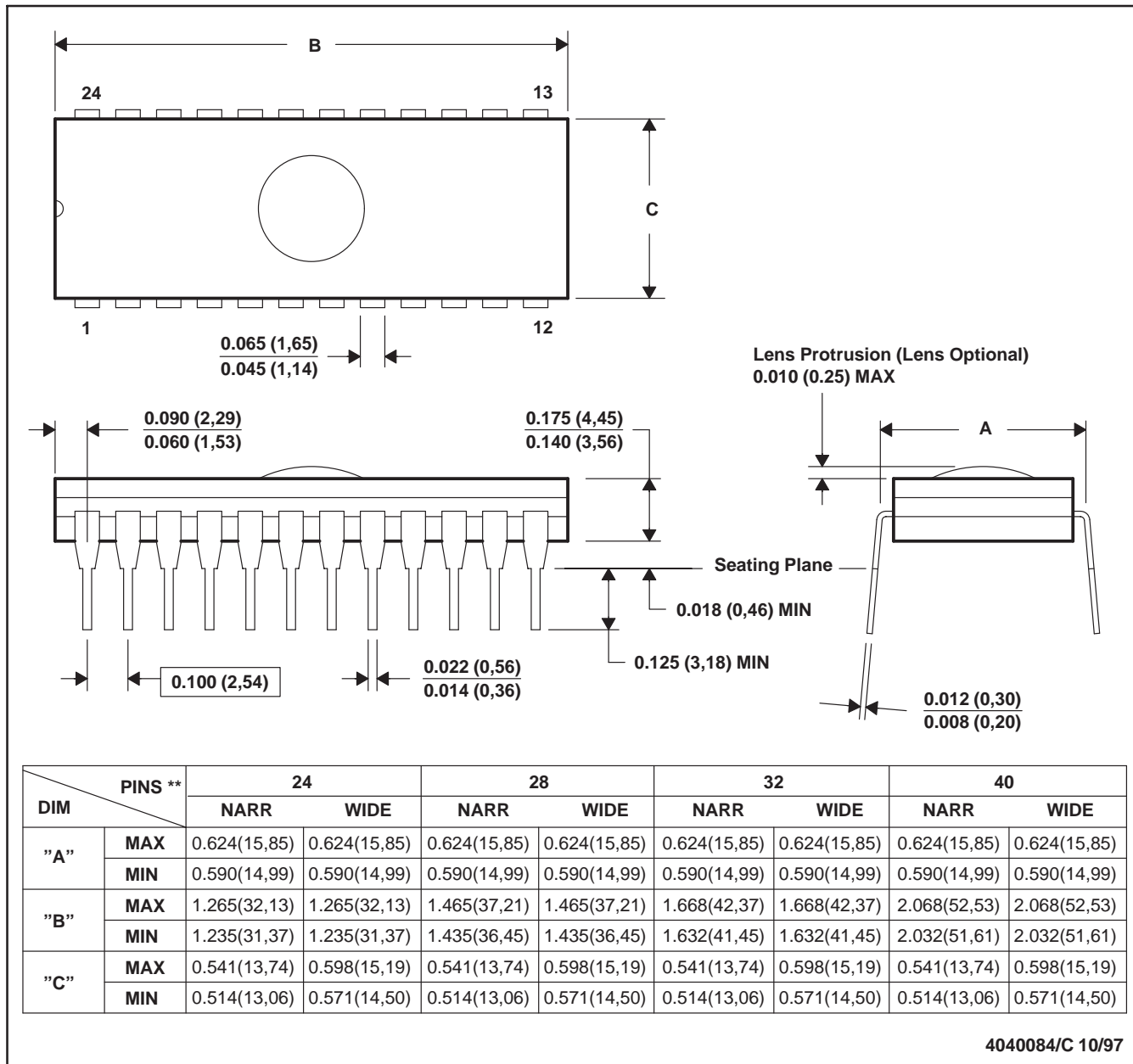
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J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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