TPD3S714-Q1 Automotive USB 2.0 Interface Protection with Short-to-Battery and Short-Circuit Protection

1 Features

- AEC-Q100 Qualified (Grade 1)
  - –40°C to 125°C Operating Temperature Range
- Short-to-Battery (up to 18 V) and Short-to-Ground Protection on V_{BUS_CON}
- Short-to-Battery (up to 18 V) and Short-to-V_{BUS} Protection on VD+, VD-
- IEC 61000-4-2 ESD Protection on V_{BUS_CON}, VD+, VD-
  - ±8 kV Contact Discharge
  - ±15 kV Air Gap Discharge
- ISO 10605 330pF, 330Ω ESD Protection on V_{BUS_CON}, VD+, VD-
  - ±8 kV Contact Discharge
  - ±15 kV Air Gap Discharge
- Low R_{ON} nFET V_{BUS} Switch (63 mΩ typ)
- High Speed Data Switches (1 GHz -3 dB Bandwidth)
- Hiccup Current Limit
  - 550 mA Overcurrent Limit (min)
- Fast Over-voltage Response Time
  - 2 µs typ (V_{BUS} switch)
  - 200 ns typ (Data switches)
- Integrated Input Enable for V_{BUS}, VD+, VD-
- Fault Output Signal
- Thermal Shutdown Feature
- 16-Pin SSOP Package (3.9 mm x 4.94 mm)

2 Applications

- End Equipment
  - Head Unit
  - Rear Seat Entertainment
  - Telematics
  - USB Hub
  - Navigation Module
  - Media Interface
- Interfaces
  - USB 2.0

3 Description

The TPD3S714-Q1 is a single-chip solution for short-to-battery, short-circuit, and ESD protection for high speed data and power lines in automotive USB hub, head unit, rear seat entertainment, telematics, and media interface applications. The integrated data switches provide best-in-class bandwidth for minimal signal degradation during USB short-to-battery events. The high bandwidth of 1 GHz allows for a clean USB2.0 high-speed (480 Mbps) eye diagram which helps pass stringent USB certification tests with the long captive cables that are common in the automotive USB environment.

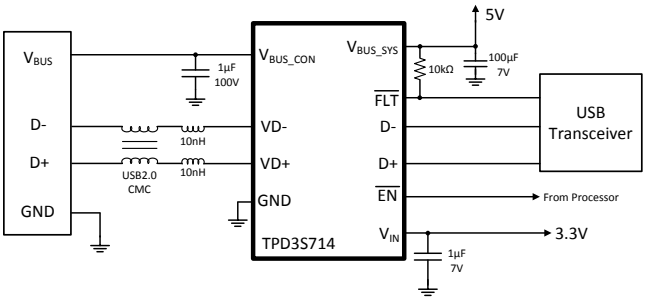
The short-to-battery protection isolates the internal system circuits from any over-voltage conditions at the V_{BUS_CON}, VD+, and VD- pins. On these pins, the TPD3S714-Q1 can handle over-voltages up to 18 V for hot plug and DC events. The over-voltage protection circuit provides the most reliable short-to-battery isolation in the industry, shutting off the switches and protecting the upstream transceiver from harmful voltage and current spikes. The V_{BUS_CON} pin also provides an accurate current limited load switch up to 0.5 A. The leading over-current protection automatically limits current to prevent drooping of the upstream rail during short-to-ground events. Additionally, this device also integrates system level IEC 61000-4-2 and ISO 10605 ESD protection on V_{BUS_CON}, VD+, and VD- pins which removes the need to provide external high-voltage, low capacitance ESD diodes

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3S714-Q1	SSOP (16)	3.90 mm × 4.94 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

DATE	REVISION	NOTES
January 2016	*	Initial release.

5 Device Logic Tables

Table 1. TPD3S714-Q1 V_{BUS} Logic Table

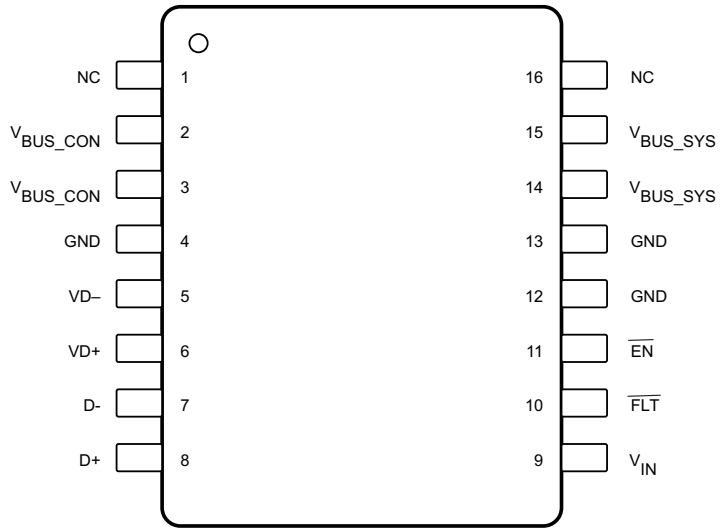
VOLTAGE CONDITION			CURRENT CONDITION		
V_{BUS_CON}	V_{BUS_SYS}	$\overline{EN}$	CURRENT FLOW	COMMENT	$\overline{FLT}$ PIN
X	<UVLO	X	No Flow	Switch off due to UVLO	High-Z
<OVP and >V_{SHRT}	>UVLO	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flows through the switch, normal host mode	High-Z
X	>UVLO	High	No Flow	Switch off	Low
<V_{SHRT}	>UVLO	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flow through switch, device detects short circuit, current limited to I_{SHRT}	Low
X	X	Low	>OCP	Device switches off due to overcurrent limit, will auto-retry until <OCP or thermal shutdown conditions occur	Low
>OVP	>UVLO	Low	No Flow	Switch off due to OVP	Low
X	X	X	No Flow	THERMAL SHUTDOWN CONDITION	Low

Table 2. TPD3S714-Q1 Data Line Logic Table

VOLTAGE CONDITION		CURRENT CONDITION		
VD+/VD–	$\overline{EN}$	Switches On?	Comment	$\overline{FLT}$ PIN
<OVP	Low	Yes	Device operates normally, data transfer can occur	High-Z
X	High	No	Switches off	Low
>OVP	Low	No	Switches off due to OVP limit	Low
X	X	No	THERMAL SHUTDOWN CONDITION	Low

6 Pin Configuration and Functions

DBQ Package
16-Pin SSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1, 16	NC	No connect, leave floating or connect to ground. Do not connect to V_{BUS_CON}
$\overline{EN}$	11	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the device. Drive $\overline{EN}$ high to disable the device.
$\overline{FLT}$	10	O	Open-Drain fault pin. Refer device description for operation.
V_{IN}	9	I	Connect to 3.3-V I/O. Controls the OVP threshold for VD+/VD-
D+/D–	8, 7	I/O	Connect to internal D+/D– transceiver
VD+/VD–	6, 5	I/O	Connect to USB connector D+, D–; provides IEC 61000-4-2 ESD protection
V_{BUS_CON}	2, 3	O	Connect to USB connector V_{BUS_CON}; provides IEC 61000-4-2 ESD protection
V_{BUS_SYS}	14, 15	I	Connect to internal V_{BUS} plane
GND	4, 12, 13	Ground	Connect to PCB ground plane

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage from USB connector	V_{BUS_CON}	–0.3	18	V
Internal Supply DC voltage Rail on the PCB	V_{BUS_SYS}	–0.3	6	V
Voltage range from connector-side USB data lines	VD+, VD–	–0.3	18	V
Voltage range for internal USB data lines	D+, D–	–0.3	V_{IN} + 0.3	V
Voltage range for V_{IN} supply input	V_{IN}	-0.3	4	V
Voltage on enable pin	$\overline{EN}$		7	V
Operating free air temperature	T_A	–40	125	°C
Storage temperature	T_{STG}	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), ESD stress voltage, all pins(1)	All pins	±4000	V
		Charged device model (CDM), ESD stress voltage, all pins(2)	All pins	±1500	
		IEC 61000-4-2 Contact Discharge(3)	V_{BUS_CON}, VD+, VD– pins	±8000	
		IEC 61000-4-2 Air-gap Discharge(3)	V_{BUS_CON}, VD+, VD– pins	±15000	
		ISO 10605 (330pF, 330Ω) Contact Discharge(3)	V_{BUS_CON}, VD+, VD– pins	±8000	
		ISO 10605 (330pF, 330Ω) Air-gap Discharge(3)	V_{BUS_CON}, VD+, VD– pins	±15000	

(1) The passing level per AEC-Q100 Classification H3.
(2) The passing level per AEC-Q100 Classification C6.
(3) Refer to ESD Test Setup diagram for details on system level ESD testing setup.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.25	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB		4.75		5.25	V
VD+, VD–	Voltage range from connector-side USB data lines		0		V_{IN}+0.3	V
D+, D–	Voltage range for internal USB data lines		0		V_{IN}+0.3	V
V_{IN}	Voltage range for V_{IN} supply		3		3.6	V
I_{BUS}	Current through V_{BUS} switch				500	mA
$\overline{EN}$	Voltage range for enable		0		5.9	V
C_{SYS}	Input capacitance(1)	V_{BUS_SYS} pin		100		µF
C_{LOAD}	Output load capacitance(1)	V_{BUS_CON} pin	1			µF
C_{VIN}	V_{IN} capacitance(1)	V_{IN} pin	1			µF

(1) See typical application diagram for configuration details

7.4 Thermal Information

THERMAL METRIC(1)		TPD3S714-Q1 DBQ (16 PIN)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	98.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	48.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	41.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD-/D+/D-/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT CONSUMPTION							
I_{VBUS_SLEEP}	V_{BUS} Sleep current consumption		Measured at V_{BUS_SYS} pin, $\overline{EN}$ = 5 V		45	150	µA
I_{VBUS}	V_{BUS} Operating current consumption		Measured at V_{BUS_SYS} pin		285	380	µA
I_{VIN}	Leakage current for V_{IN}		Measured at V_{IN} pin, V_{IN} = 3.6 V		12	25	µA
$I_{ON(LEAK)}$	Leakage through V_{BUS} while shorted to battery and powered on		Measured flowing in to V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, V_{BUS_CON} = 18 V			120	µA
$I_{OFF(LEAK)}$	Leakage through V_{BUS} while shorted to battery and unpowered		Measured flowing out of V_{BUS_SYS} pin, V_{BUS_SYS} = 0 V, V_{BUS_CON} = 18 V			50	µA
$I_{VD(OFF\_LEAK)}$	Leakage into data path while shorted to battery and unpowered		Measured flowing in to VD+ or VD- pins, V_{BUS_SYS} = 0 V, VD+ or VD- = 18 V, V_{IN} = 0 V, D+/D- = 0 V			80	µA
$I_{VD(ON\_LEAK)}$	Leakage into data path while shorted to battery and powered on		Measured flowing in to VD+ or VD- pins, V_{BUS_SYS} = 5 V, VD+ or VD- = 18 V, D+/D- = 0 V			80	µA
V_{IN} PIN							
$V_{UVLO(RISING)}$	Undervoltage lockout rising for V_{IN}	V_{IN}	Ramp V_{IN} down until $\overline{FLT}$ is deasserted, $\overline{EN}$ = 5 V	2.6	2.7	2.9	V
$V_{UVLO(FALLING)}$	Undervoltage lockout falling for V_{IN}		Ramp V_{IN} until $\overline{FLT}$ is asserted, $\overline{EN}$ = 5 V	2.5	2.6	2.8	
$\overline{EN}$, $\overline{FLT}$ PINS							
V_{IH}	High-level input voltage	$\overline{EN}$	Set $\overline{EN}$ = 0 V; Sweep $\overline{EN}$ to 1.4 V; Measure when $\overline{FLT}$ is asserted	1.2			V
V_{IL}	Low-level input voltage	$\overline{EN}$	Set $\overline{EN}$ = 3.3 V; Sweep $\overline{EN}$ from 3.3 V to 0.5 V; Measure when $\overline{FLT}$ is disasserted			0.8	V
I_{IL}	Input Leakage Current	$\overline{EN}$	$V_{(EN)}$ = 3.3 V ; Measure Current into EN pin			1	µA
V_{OL}	Low-level output voltage	$\overline{FLT}$	I_{OL} = 3 mA			0.4	V
OCP CIRCUIT - V_{BUS}							
I_{LIM}	Overcurrent limit	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	550	700	850	mA
OVER TEMPERATURE PROTECTION							
T_{SD_RISING}	The rising over-temperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped up until $\overline{FLT}$ is asserted	150	165	180	℃
$T_{SD(FALLING)}$	The falling over-temperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped down from $T_{SD(RISING)}$ until $\overline{FLT}$ is deasserted	125	130	140	℃
$T_{SD(HYST)}$	The over-temperature protection shutdown threshold hysteresis		$T_{SD(RISING)}$ - $T_{SD(FALLING)}$	10	35	55	℃
OVP CIRCUIT - V_{BUS}							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	V_{BUS_CON}	Increase V_{BUS_CON} from 5 V to 7 V. Measure when $\overline{FLT}$ is asserted	5.4	5.6	5.8	V
$V_{HYS(OVP)}$	Hysteresis on OVP	V_{BUS_CON}	Difference between rising and falling OVP thresholds on V_{BUS_CON}		50		mV
$V_{OVP\_FALLING}$	Input overvoltage protection threshold	V_{BUS_CON}	Decrease V_{BUS_CON} from 7 V to 5 V. Measure when $\overline{FLT}$ is deasserted	5.36		5.74	V
$V_{UVLO(SYS\_RISING)}$	Undervoltage lockout rising for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.3	3.6	V
$V_{HYS(UVLO\_SYS)}$	V_{BUS_SYS} UVLO Hysteresis	V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}	50	75	100	mV
$V_{UVLO(SYS\_FALLING)}$	Undervoltage lockout falling for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7 V to 3 V	3	3.2	3.5	V
$V_{SHRT(RISING)}$	Short-to-ground comparator rising threshold	V_{BUS_CON}	Increase V_{BUS_CON} voltage from 0 V until the device transitions from the short-circuit to over-current mode of operation	2.5	2.6	2.7	V
$V_{SHRT(FALLING)}$	Short-to-ground comparator falling threshold	V_{BUS_CON}	Set V_{BUS_SYS} = 5 V; V_{IN} = 3.3 V; $\overline{EN}$ = 0 V; Decrease V_{BUS_CON} voltage from 5 V until the device transitions from the over-current to short-circuit mode of operation	2.4	2.5	2.6	V
$V_{SHRT(HYST)}$	Short-to-ground comparator hysteresis	V_{BUS_CON}	Difference between $V_{SHRT(RISING)}$ and $V_{SHRT(FALLING)}$	100	125	150	mV

Electrical Characteristics (continued)

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD-/D+/D-/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHRT}	Short-to-ground current source	V_{BUS_CON}	Current sourced from V_{BUS_SYS} when device is in short-circuit mode	150		350	mA
OVP CIRCUIT – VD+/VD–							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	VD+/VD–	Increase VD+ or VD- (with D+ and D-) from 3.3 V to 4.5 V. Measure the value at which $\overline{FLT}$ is asserted	V_{IN} + 0.6	V_{IN} + 0.8	V_{IN} + 1	V
$V_{HYS(OVP)}$	Hysteresis on OVP	VD+/VD–	Difference between rising and falling OVP thresholds on VD+/VD-		50		mV
$V_{OVP(FALLING)}$	Input overvoltage protection threshold	VD+/VD–	Decrease VD+ or VD- (with D+ or D-) from 4.5 V to 2 V. Measure the value at $\overline{FLT}$ is deasserted	V_{IN} + 0.525	V_{IN} + 0.75	V_{IN} + 0.975	V
SHORT TO BATTERY							
$V_{(VBUS\_STB)}$	V_{BUS} hotplug short-to-battery tolerance	V_{BUS_CON}	Charge battery-equivalent capacitor to test voltage then discharge to pin under test through a 1 meter, 18ga wire. (See the STB Test Setup diagram for more details)			18	V
$V_{(DATA\_STB)}$	Data line hotplug short-to-battery tolerance	VD+/VD-				18	V
DATA LINE SWITCHES – VD+ to D+ or VD- to D-							
C_{ON}	Equivalent On Capacitance		Capacitance of D+/D- switches when enabled - measure on connector side across bias voltage		6.2		pF
R_{ON}	On Resistance		Measure resistance between D+ and VD+ or D- and VD-, voltage between 0 and 0.4 V		4	6.5	Ω
$R_{ON(Flat)}$	On Resistance flatness		Measure resistance between D+ and VD+ or D- and VD-, sweep voltage between 0 and 0.4 V		0.2	1	Ω
BW_{ON}	On Bandwidth (–3dB)		Measure S_{21} bandwidth from D+ to VD+ or D- to VD- with voltage swing = 400 mVpp, V_{CM}= 0.2 V		860		MHz
BW_{ON_DIFF}	On Bandwidth (–3dB)		Measure S_{DD21} bandwidth from D+ to VD+ and D- to VD- with voltage swing = 800 mVpp differential, V_{CM}= 0.2 V		1050		MHz
X_{talk}	Crosstalk		Measure S_{21} bandwidth from D+ to VD- or D- to VD+ with voltage swing = 400mVpp. Be sure to terminate open sides to 50 ohms. f = 480 MHz		-34		dB
nFET SWITCH - Vbus							
$R_{(DISCHARGE)}$	Output discharge resistance		$\overline{EN}$ = 5 V, Set V_{BUS_CON} = 5 V and measure current flow to ground			12500	Ω
R_{DS_ON}	Switch ON resistance		V_{BUS_CON} = 5 V, I_{OUT} = 0.5 A		63	150	mΩ

7.6 Timing Characteristics

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD-/D+/D-/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE PIN						
t_{ON}	Enable on time	Time between enable device until $\overline{FLT}$ deasserts		13		ms
OVER CURRENT PROTECTION						
t_{BLANK}	Overcurrent blanking time	Time from overcurrent condition until $\overline{FLT}$ assertion and V_{BUS} FET turn off			2	ms
t_{RETRY}	Overcurrent retry time	Time from overcurrent FET shut off until FET turns back on		100		ms
t_{RECV}	Overcurrent recovery time	Time from end of t_{RETRY} until $\overline{FLT}$ deassertion if overcurrent condition is removed		8		ms
OVER VOLTAGE PROTECTION						
$t_{OVP\_response}$	OVP Response time - V_{BUS}	Measured from OVP Condition to FET turn off		2	4	µs
$t_{OVP\_response}$	OVP Response time - data switches	Measured from OVP Condition to FET turn off		200		ns
SHORT TO GROUND PROTECTION						
t_{SHRT}	Short to ground response time	C_{LOAD} = 0 uF, Time from short condition until current falls below 120% of I_{SHRT}		2	4	µs

7.7 Typical Characteristics

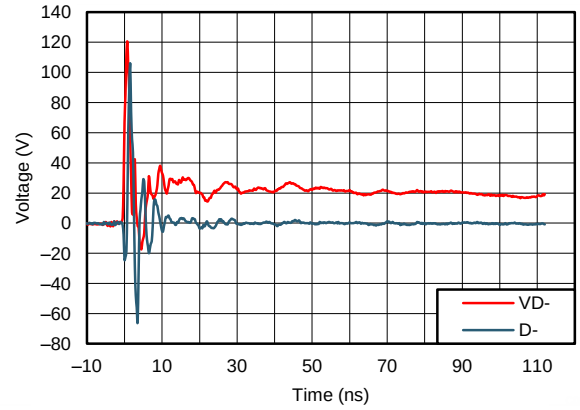


Figure 1. +8kV IEC Contact Waveform

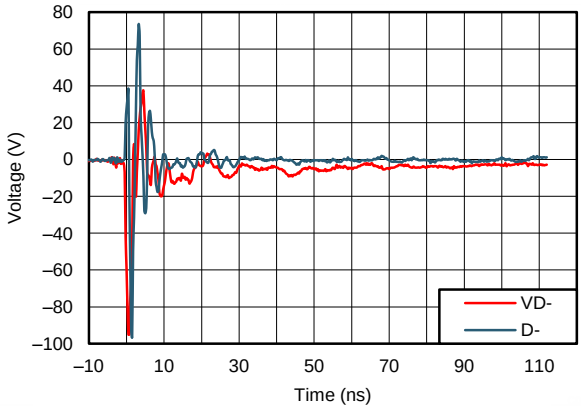


Figure 2. -8kV IEC Contact Waveform

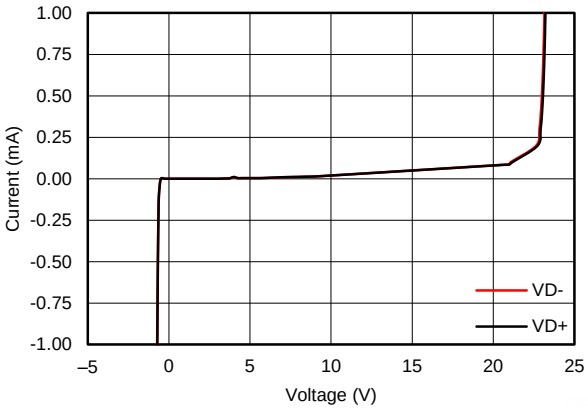


Figure 3. Data Line I-V Curve

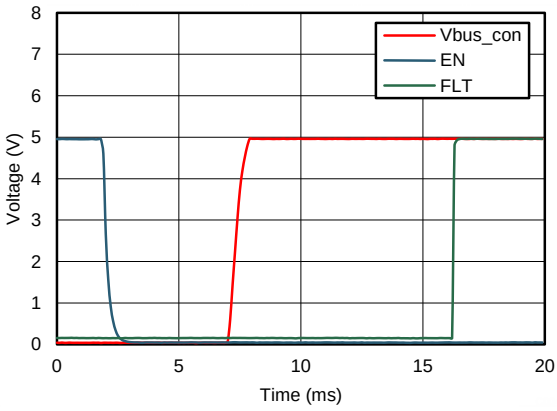


Figure 4. V_{BUS} t_{ON} Time

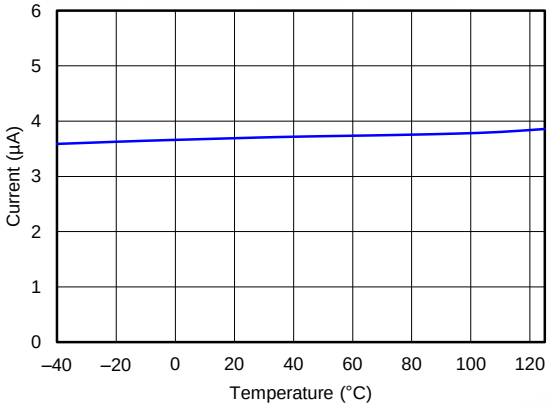


Figure 5. VD+/- Short-to-5V (while enabled) across temperature

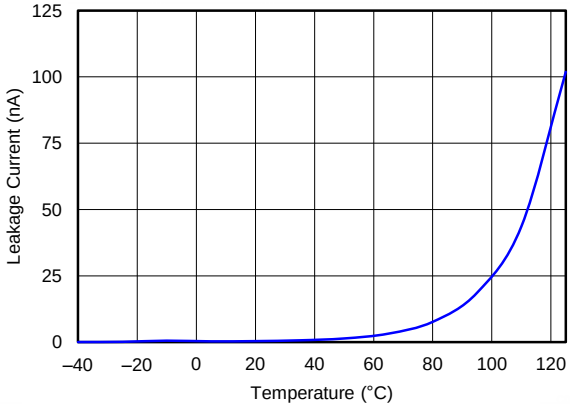


Figure 6. VD+/- Short-to-5V (while unpowered) Across Temperature

Typical Characteristics (continued)

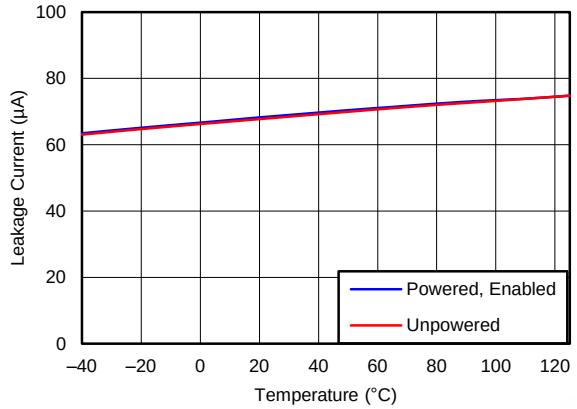


Figure 7. VD+/- Short-to-18 V Across Temperature

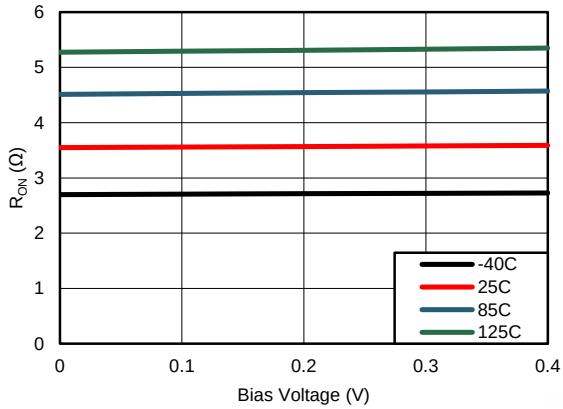


Figure 8. Data Switch R_{ON} vs. Bias Voltage

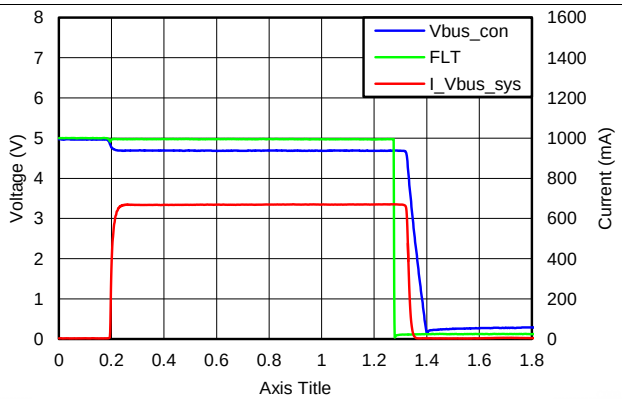


Figure 9. Overcurrent t_{BLANK} Response Waveform

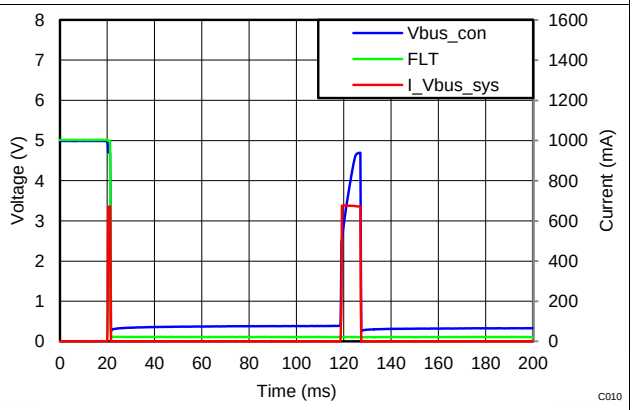


Figure 10. Overcurrent t_{BLANK_RETRY} Response Waveform

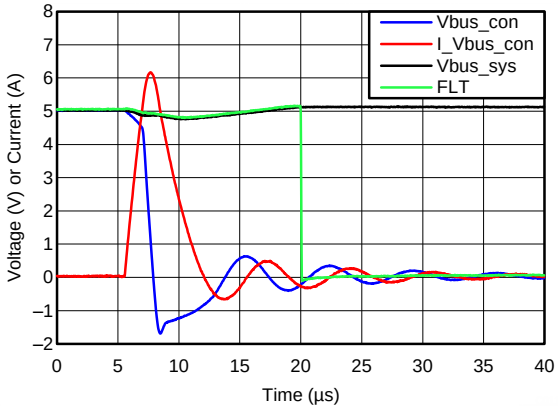


Figure 11. V_{BUS} Short-to-ground Response Waveform

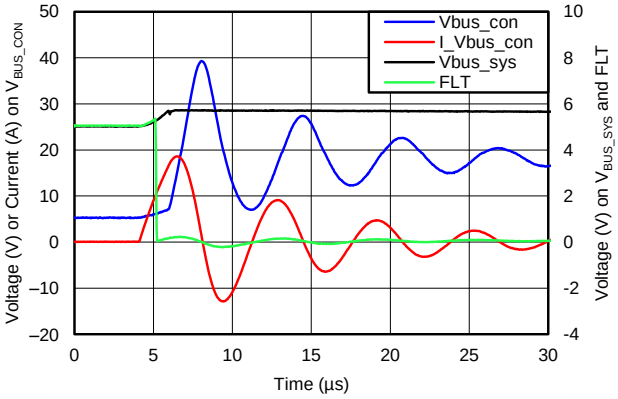


Figure 12. V_{BUS} Short-to-18 V Response Waveform

Typical Characteristics (continued)

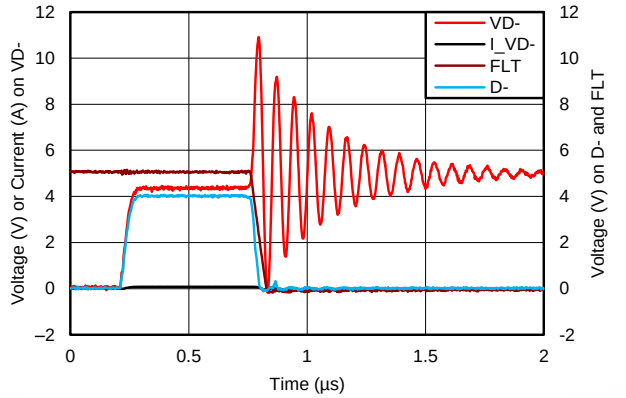


Figure 13. Data Switch Short-to-5 V Response Waveform

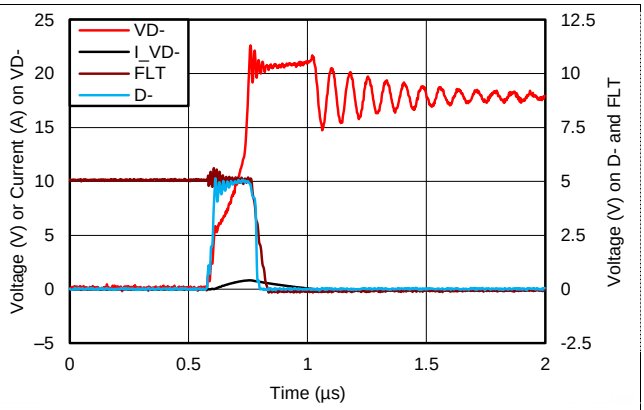


Figure 14. Data Switch Short-to-18 V Response Waveform

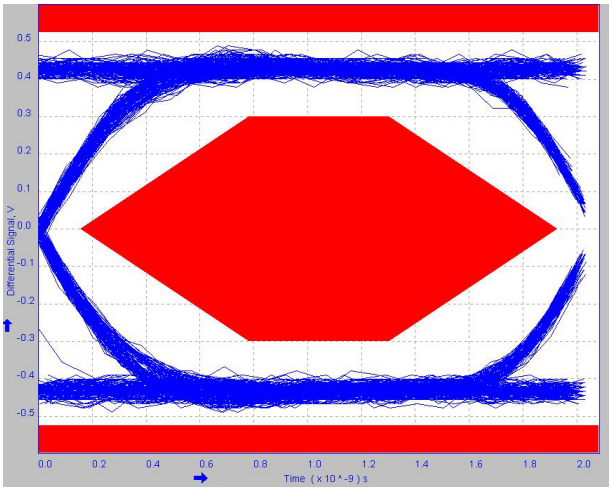


Figure 15. USB2.0 Eye Diagram (no TPD3S714-Q1)

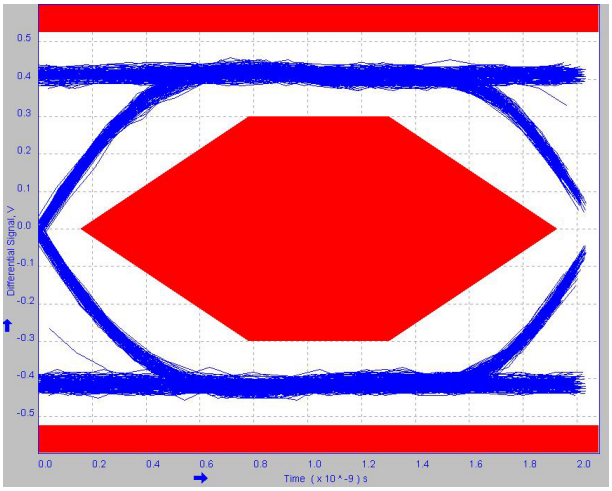


Figure 16. USB2.0 Eye Diagram (with TPD3S714-Q1)

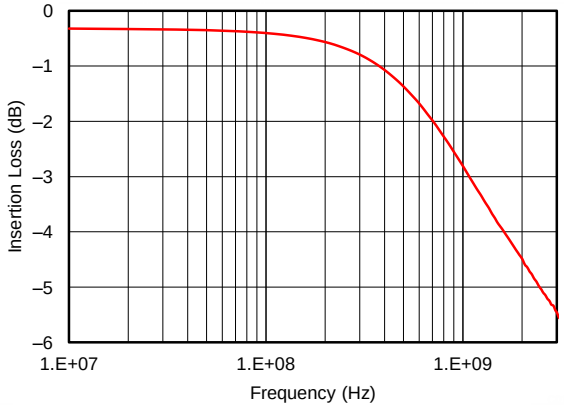


Figure 17. Data Switch Differential Bandwidth

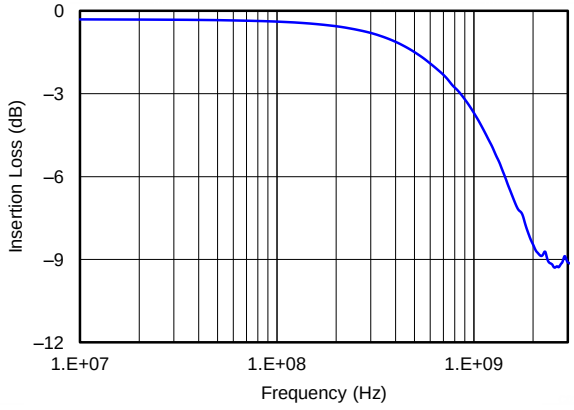


Figure 18. Data Switch Single-ended Bandwidth

Typical Characteristics (continued)

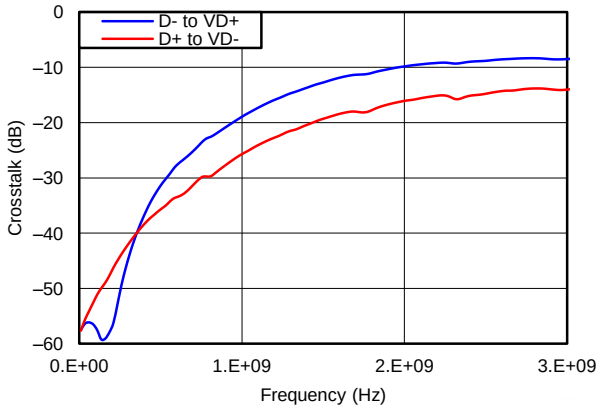


Figure 19. Data Switch Crosstalk

8 Parameter Measurement Information

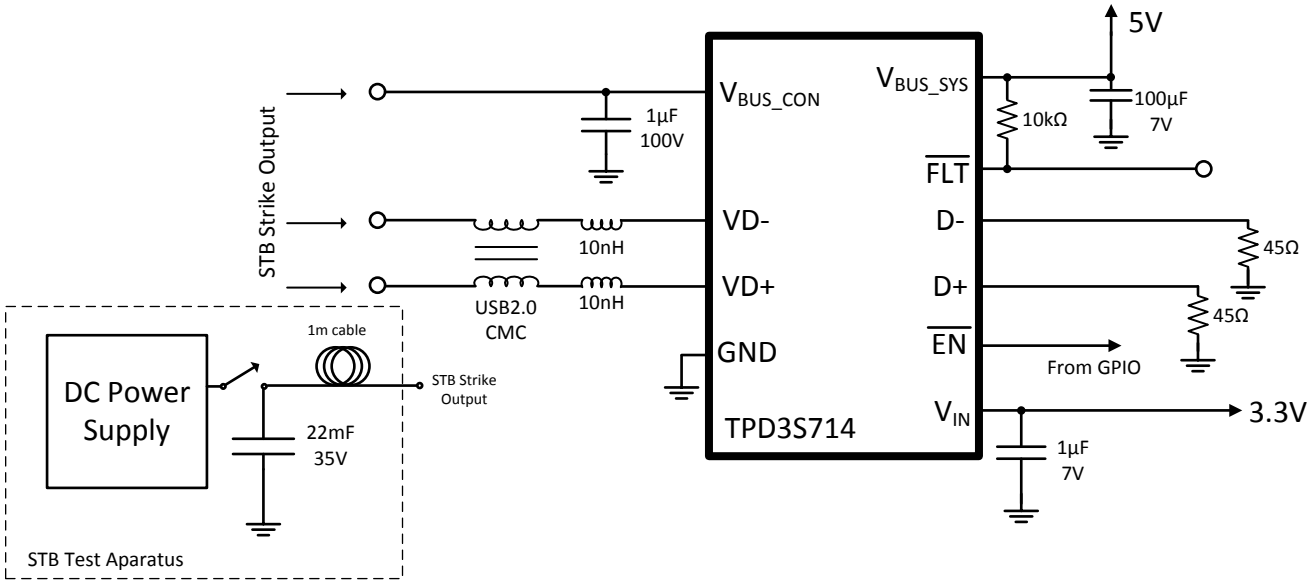


Figure 20. Short-to-battery System Test Setup

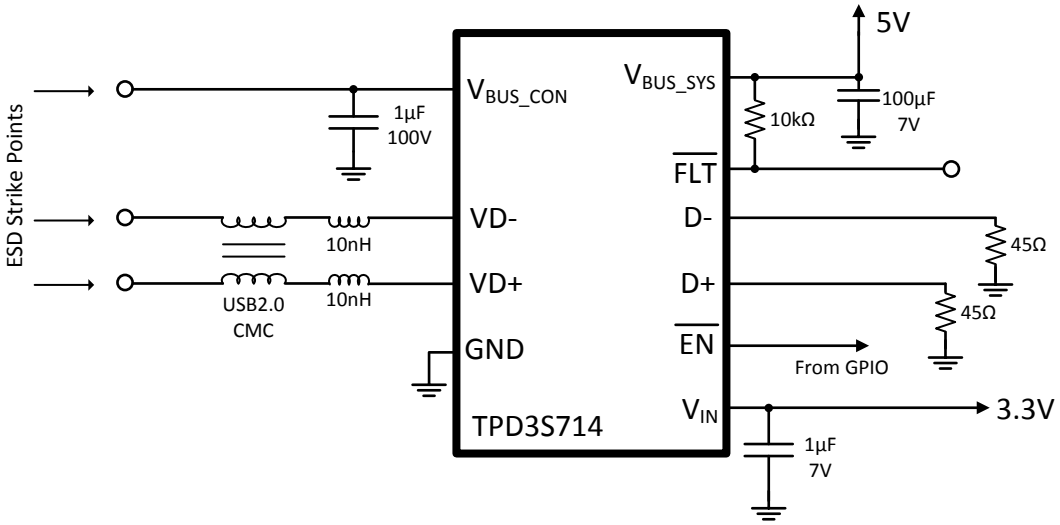


Figure 21. ESD System Test Setup

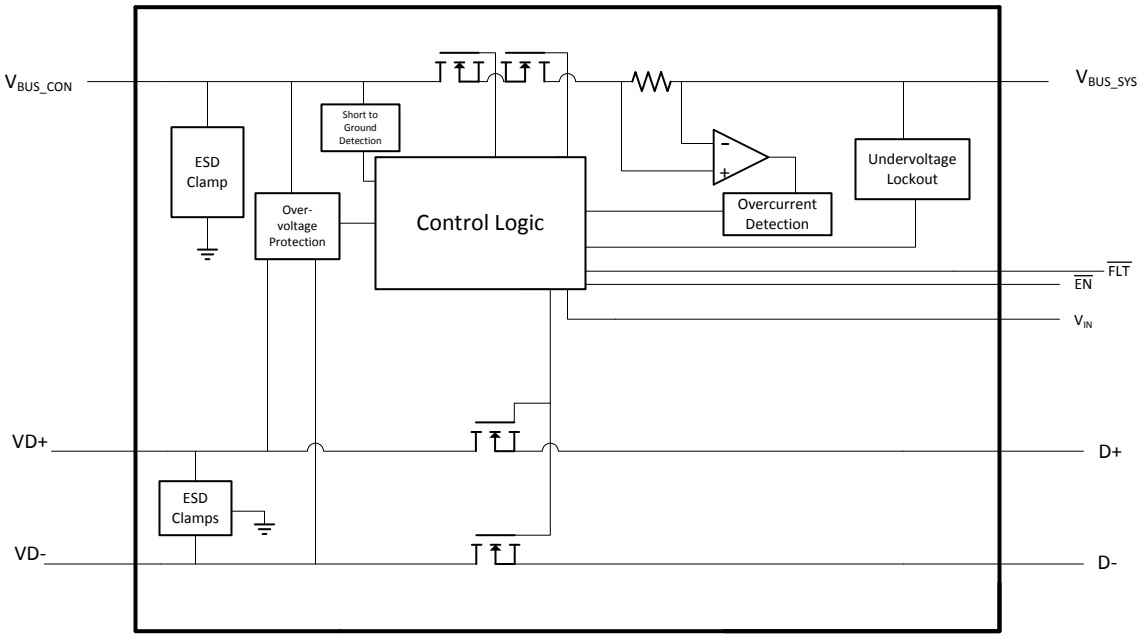
9 Detailed Description

9.1 Overview

The TPD3S714-Q1 provides a single-chip ESD protection and over voltage protection solution for automotive USB interfaces. It offers short to battery protection up to 18V and short to ground protection on V_{BUS_CON}. The TPD3S714-Q1 also provides a $\overline{FLT}$ pin that indicates to the system if a fault condition has occurred. The TPD3S714-Q1 offers ESD clamps on the V_{BUS_CON}, VD+, and VD– pins, thus eliminating the need for external TVS clamp circuits in the application.

The TPD3S714-Q1 has internal circuitry that controls the turn-on of the internal nFET switches. An internal oscillator controls the timers that enable the switches and resets the open-drain $\overline{FLT}$ output. If V_{BUS_CON} is less than V_{OVP}, the switches are enabled. After an internal delay, the charge-pump starts-up, turns on the internal nFET switch through a soft start. Once the nFET is completely turned ON, TPD3S714-Q1 releases $\overline{FLT}$ pin to HIGH. At any time, if any of the external pins rise above V_{OVP}, $\overline{FLT}$ pin will be pulled LOW. The nFET switches are turned OFF.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 AEC-Q100 Qualified

The TPD3S714-Q1 is an automotive qualified device according to the AEC-Q100 standards. This device is qualified to operate from -40 to 125°C ambient temperature.

9.3.2 Short-to-Battery and Short-to-Ground Protection on V_{BUS_CON}

The V_{BUS_CON} pin is protected against shorts to battery and shorts to ground.

Once a voltage on V_{BUS_CON} is detected as too low (below the V_{SHRT} threshold) after the device is enabled, the device will enter short-circuit protection mode and assert $\overline{FLT}$. It will source the I_{SHRT} current until it detects the voltage rising above the V_{SHRT} threshold, where it resumes standard operating mode and de-assert $\overline{FLT}$.

Once a voltage above the V_{OVP} threshold is detected by the device, it will shut off all FETs and asserts a fault on the $\overline{FLT}$ pin. Once the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ de-asserts (see *Timing Characteristics* for more details).

Feature Description (continued)

9.3.3 Short-to-Battery and Short-to-V_{BUS} Protection on VD+, VD-

The VD+ and VD- pins are protected against shorts to battery and shorts to bus. The OVP threshold on the VD+ and VD- pins is low enough that it protects against shorts to V_{BUS}.

Once a voltage above the V_{OVP} threshold is detected by the device, it shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. Once the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ de-asserts (see *Timing Characteristics* for more details).

9.3.4 ESD Protection on V_{BUS_CON}, VD+, VD-

The protected pins (V_{BUS_CON}, VD+, VD-) are tested to pass the IEC 61000-4-2 ESD standard up to Level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330 pF, 330 Ω equivalent network. This guarantees passing of at least ±8 kV contact discharge and ±15 kV air gap discharge according to both standards.

9.3.5 Low R_{ON} nFET V_{BUS} Switch

The V_{BUS} switch has a low R_{ON} that provides minimal voltage droop from system to connector. Typical resistance is 63 mΩ and is specified for 150 mΩ at 125°C ambient temperature.

9.3.6 High Speed Data Switches

The D+ and D- switches have a very low capacitance and a high bandwidth (1 GHz typ), allowing for a clean USB 2.0 eye diagram.

9.3.7 Hiccup Current Limit

The V_{BUS} path of this device has an integrated overcurrent protection circuit. Above the overcurrent threshold (550 mA min), the device goes into a fault state where it limits current to the threshold. After a short blanking time, the device will cycle on and off to try to check if the connected device is still in overcurrent.

9.3.8 Fast Over-voltage Response Time

The over-voltage FETs are designed to have a fast turn-off time to protect the upstream SoC as quickly as possible. Typical response time for complete turn-off is 2 µs for the V_{BUS} path and 200 ns for the data path.

9.3.9 Integrated Input Enable

The TPD3S714 has an enable input to turn on and off the device. The $\overline{EN}$ pin disables and enables the V_{BUS} and data paths.

9.3.10 Fault Output Signal

The TPD3S714 has a fault pin ($\overline{FLT}$) that indicates when there is any sort of fault condition due to OVP, OCP, or short-circuit.

9.3.11 Thermal Shutdown Feature

In the event that the device exceeds the maximum allowable junction temperature, it will shut down the device to prevent damage to itself and indicate via the fault pin.

9.3.12 16-pin SSOP Package

This device is packaged in a standard 16-pin SSOP leaded package.

9.4 Device Functional Modes

9.4.1 Normal Operation

The TPD3S714-Q1 operates normally (all FETs on) when enabled, both V_{BUS_SYS} and V_{IN} are above their UVLO thresholds, and the device is not in any fault conditions.

9.4.2 Overvoltage Condition

When the VD+, VD-, or V_{BUS_CON} pins exceed their OVP threshold, the device will enter the overvoltage state. All FETs will be disabled and the $\overline{FLT}$ pin will be asserted. Once the protected pins drop below their OVP threshold, the device will automatically turn back on.

9.4.3 Overcurrent Condition

When the current through the V_{BUS} path exceeds the I_{LIM} current threshold, the device will enter into the overcurrent state. The TPD3S714 limits current to the I_{LIM} threshold by dropping voltage across the V_{BUS} FET to maintain constant current. Once it continues to sense an overcurrent condition for the blanking time (t_{BLANK}), the device will disable itself for the retry time (t_{RETRY}) and then retry automatically for the retry time (t_{BLANK_RETRY}). In the event that the current is below the overcurrent threshold, the device will de-assert fault and resume normal operation.

9.4.4 Short-circuit Condition

When the voltage on the V_{BUS_CON} side drops below the V_{SHRT} threshold while enabled, the TPD3S714 will enter the short-circuit mode. It sources a constant current of I_{SHRT} until it rises above the V_{SHRT} threshold. Once that occurs, the device automatically re-enters normal operation and de-asserts fault.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPD3S714-Q1 offers fully featured automotive USB2.0 protection including short-to-battery, overcurrent, and ESD protection. Care must be taken during the implementation to make sure the device provides adequate protection to the system.

10.2 Typical Application

This application shows a fully featured USB2.0 high speed port, with an 18-V short-to-battery requirement on the connector side.

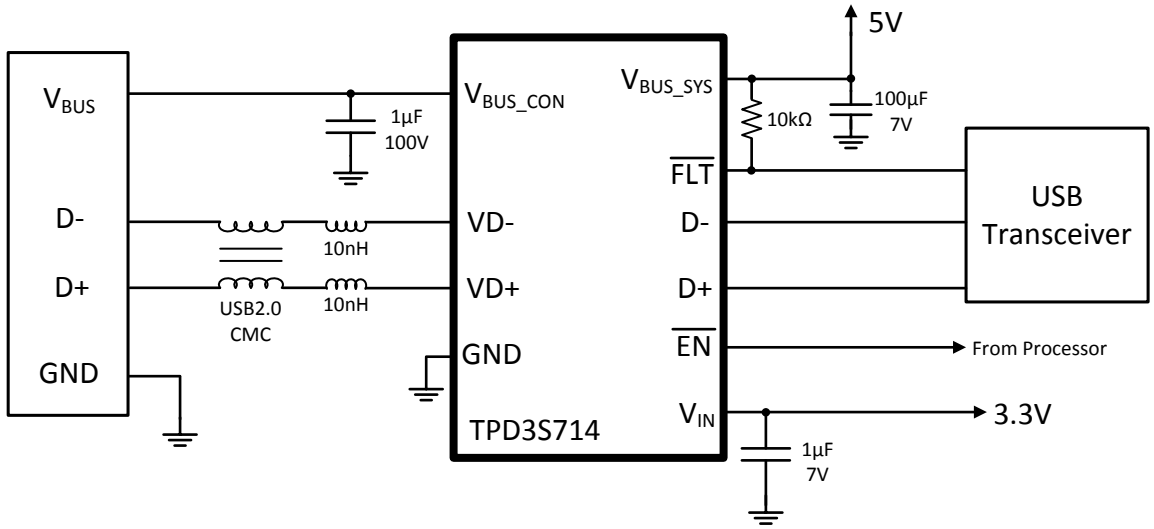


Figure 22. Typical Application Configuration for TPD3S714-Q1

10.3 Design Requirements

For this design example, use the following table as input parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Short-to-battery tolerance on VD+, VD-, V_{BUS_CON}	18 V
Max current in normal operation on V_{BUS}	500 mA
USB Data Rate	480 Mbps

10.4 Detailed Design Procedure

To begin the design process, the designer must know the following parameters:

- Short-to-battery tolerance on connector pins
- Max current in normal operation on V_{BUS}
- USB Data Rate

10.4.1 Short-to-battery Tolerance

The TPD3S714-Q1 is capable of handling up to 18 V DC on the VD+, VD-, and V_{BUS_CON} pins. In the event of a short-to-battery on V_{BUS_CON}, significant ringing would be expected due to the hot plug-like nature of the short-to-battery event. In typical ceramic capacitor configurations, a standard RLC response is expected which results in a ringing of nearly two times the applied DC voltage. The TPD3S714-Q1 is capable of withstanding the transient ringing from hot plug-like events, assuming some precautions are taken.

Careful capacitor selection on the V_{BUS_CON} pin needs to be observed. A capacitor with a low derating percentage under the applied voltages needs to be used to prevent excess ringing. In the example, a 1-µF 100-V tolerant ceramic X7R capacitor is used. It is best practice to carefully select the capacitors used in this circuit to prevent derating-based voltage spikes under hot plug events. See the application examples graphs to compare ringing from a 100-V capacitor to a 50-V capacitor.

Another alternative to a high rated ceramic capacitor is to implement either a standard R-C snubber circuit, or a small external TVS diode. Depending on the short-to-battery tolerance needed, no special precautions may be needed.

10.4.2 Max current on V_{BUS}

The TPD3S714-Q1 is capable of operating up to 550 mA of current (min) until going into current limit mode. In this example, the maximum current for USB2.0 of 500 mA has been chosen.

10.4.3 USB Data Rate

The TPD3S714-Q1 is capable of operating at the maximum USB2.0 High Speed data rate of 480 Mbps due to the high data switch bandwidth of 1 GHz (typ). In this design example the maximum data rate of 480 Mbps has been chosen.

10.5 Application Curves

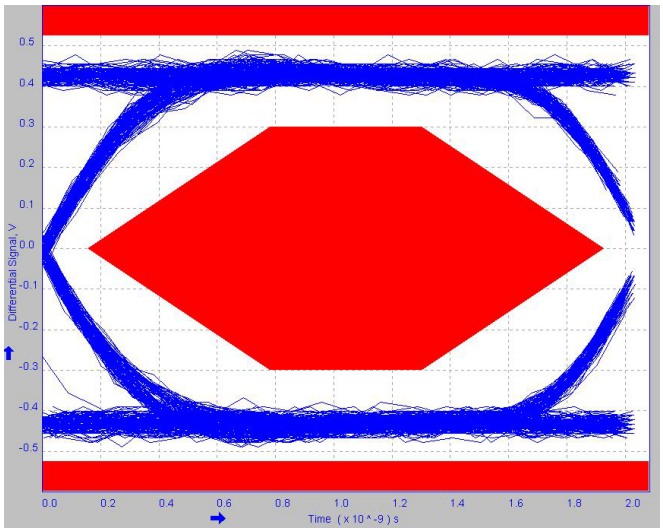


Figure 23. USB2.0 Eye Diagram (Board only, Through Path)

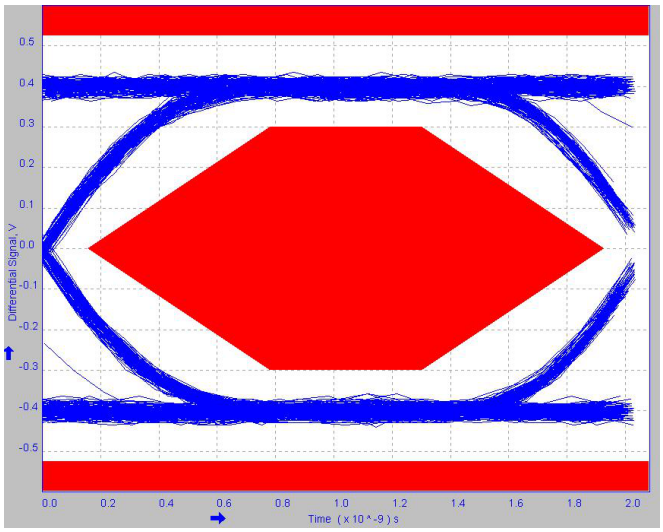


Figure 24. USB2.0 Eye Diagram (System from Typical Application Schematic)

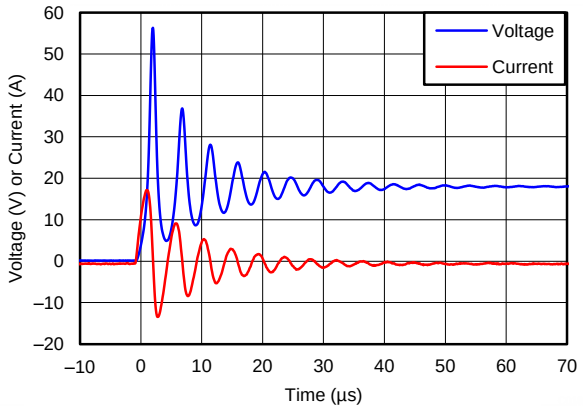


Figure 25. 50-V, 1-µF X7R Ceramic Shorted to 18-V

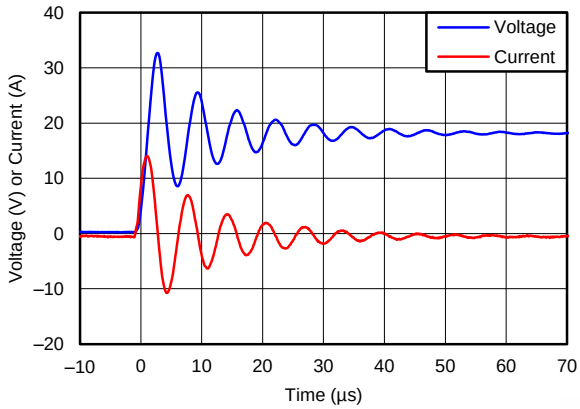


Figure 26. 100-V, 1-µF X7R Ceramic Shorted to 18 V

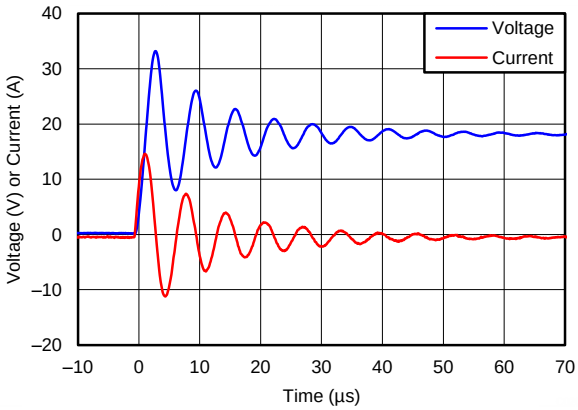


Figure 27. TPD3S714 and 100-V, 1-µF X7R Shorted to 18 V (Powered Off)

11 Power Supply Recommendations

11.0.1 V_{BUS} path

The V_{BUS_SYS} pins provide power to the chip and supply current through the load switch to V_{BUS_CON}. A 100-µF bulk capacitor is recommended on V_{BUS_SYS} to supply the USB port and maintain compliance. A 1-µF capacitor is recommended on the V_{BUS_CON} pin with adequate voltage rating to tolerate short-to-battery conditions. A supply voltage above the UVLO threshold for V_{BUS_SYS} must be supplied for the device to power on.

11.1 V_{IN} pin

The V_{IN} pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1-µF capacitor should be placed as close to the pin as possible and the supply should be set to be above the UVLO threshold for V_{IN}.

12 Layout

12.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high-speed signals. The following guidelines apply to the TPD3S714:

- Place the bypass capacitors as close as possible to the V_{IN}, V_{BUS_SYS}, and V_{BUS_CON} pins. Capacitors should be attached to a solid ground. This will minimize voltage disturbances during transient events such as short-to-battery, ESD, or overcurrent conditions.
- High speed traces (data switch path) should be routed as straight as possible and any sharp bends should be minimized.

Our standard ESD recommendations apply to the VD+, VD-, and V_{BUS_CON} pins as well:

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

12.2 Layout Example

The following figure shows a full layout for a standard USB2.0 port. A common mode choke and inductors are used on the high speed data lines, and the requisite bypassing caps are placed on V_{BUS_CON}, V_{BUS_SYS}, and V_{IN}.

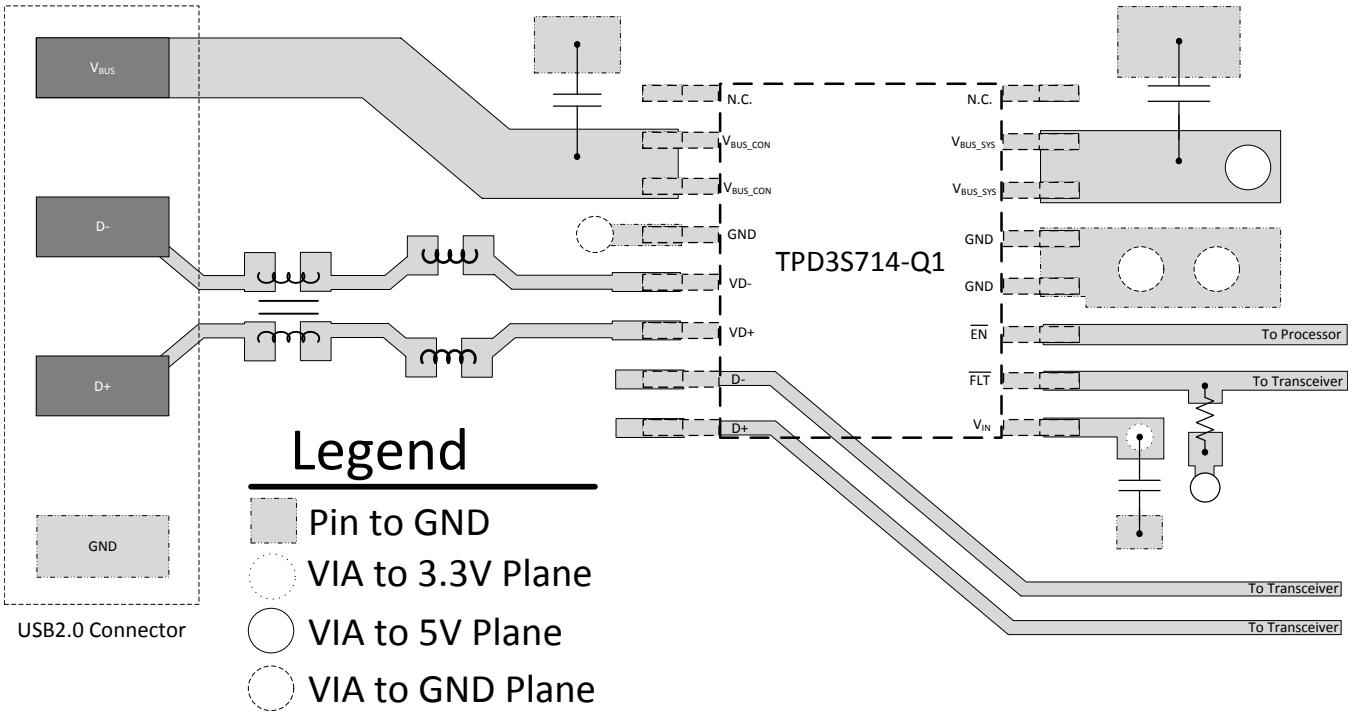


Figure 28. Typical Layout Example for TPD3S714-Q1

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

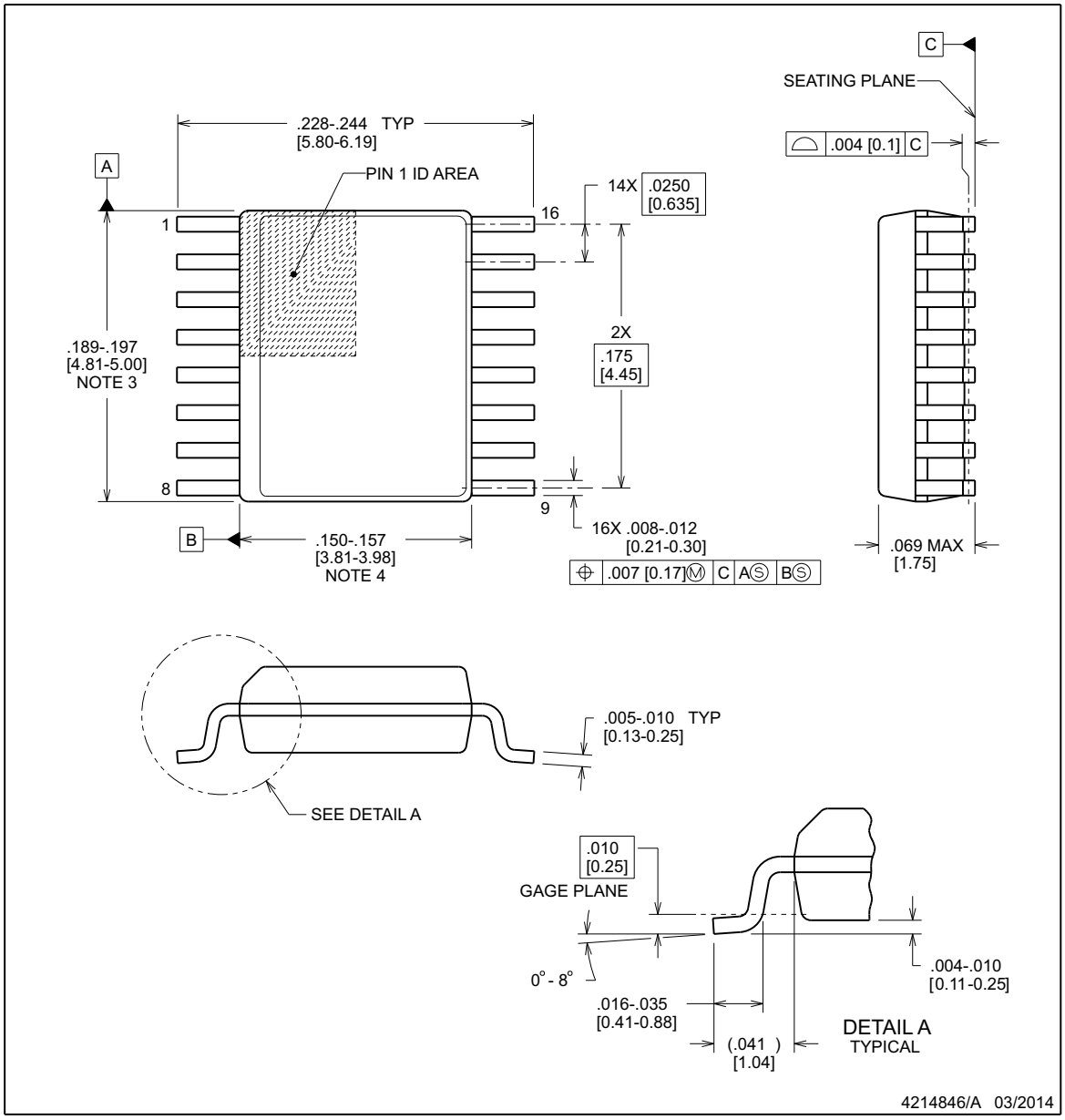
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

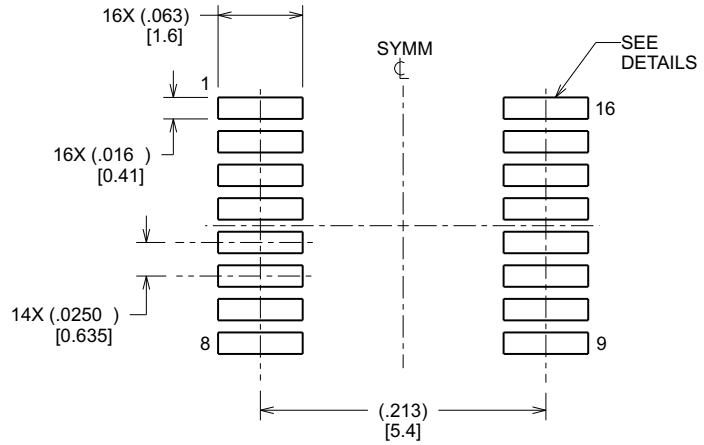
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

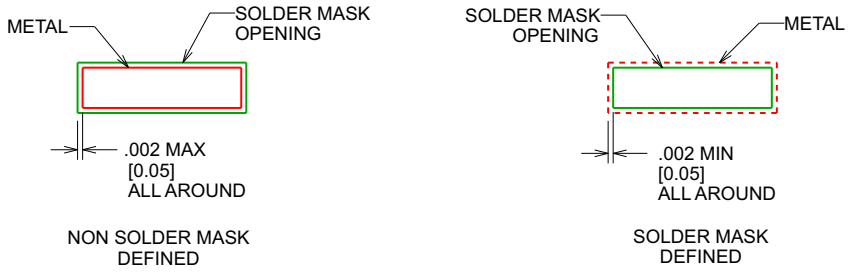
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

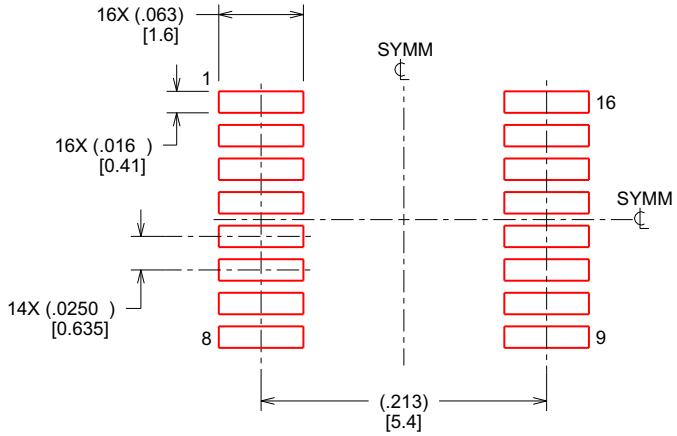
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S714QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ714Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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