# TPA3244 40-W Stereo, 100-W peak PurePath™ Ultra-HD Pad Down Class-D Amplifier

## 1 Features

- Differential Analog Inputs
- Total Output Power at 10%THD+N
  – 40-W Stereo Continuous into 8 Ω in BTL Configuration at 30 V
  – 100-W Stereo Peak into 4 Ω in BTL Configuration at 30 V
- Total Output Power at 1%THD+N
  – 35-W Stereo Continuous into 8 Ω in BTL Configuration at 30 V
  – 80-W Stereo Peak into 4 Ω in BTL Configuration at 30 V
- Advanced Integrated Feedback Design with High-speed Gate Driver Error Correction (PurePath™ Ultra-HD)
  – Signal Bandwidth up to 100 kHz for High Frequency Content From HD Sources
  – Ultra Low 0.005% THD+N at 1 W into 4 Ω and <0.01% THD+N to Clipping
  – 60 dB PSRR (BTL, No Input Signal)
  – <55 µV (A-Weighted) Output Noise
  – >110 dB (A Weighted) SNR
- Multiple Configurations Possible:
  – Stereo, Mono, 2.1 and 4xSE
- Click and Pop Free Startup and Stop
- 92% Efficient Class-D Operation (8 Ω)
- Wide 12-V to 30-V Supply Voltage Operation
- Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short Circuit Protection) With Error Reporting
- EMI Compliant When Used With Recommended System Design

## 2 Applications

- High End Soundbar
- Mini Combo Systems
- Blu-ray Disk™ / DVD Receivers
- Active Speakers

## 3 Description

The TPA3244 device is a high performance Class-D power amplifier that enables true premium sound quality with Class-D efficiency. It features an advanced integrated feedback design and proprietary high-speed gate driver error correction (PurePath™ Ultra-HD). This technology allows ultra low distortion across the audio band and superior audio quality. With a 30-V power supply the device can drive up to 2 x 100 W peak into 4-Ω load and 2 x 40 W continuous into 8-Ω load and features a 2-VRMS analog input interface that works seamlessly with high performance DACs such as TI's PCM5242. In addition to excellent audio performance, TPA3244 achieves both high power efficiency and very low power stage idle losses below 1 W. This is achieved through the use of 60 mΩ MOSFETs and an optimized gate driver scheme that achieves significantly lower idle losses than typical discrete implementations.

**Table 1. Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPA3244D2 | HTSSOP (44) | 6.10mm x 14.00mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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**Figure 1. Simplified Schematic**

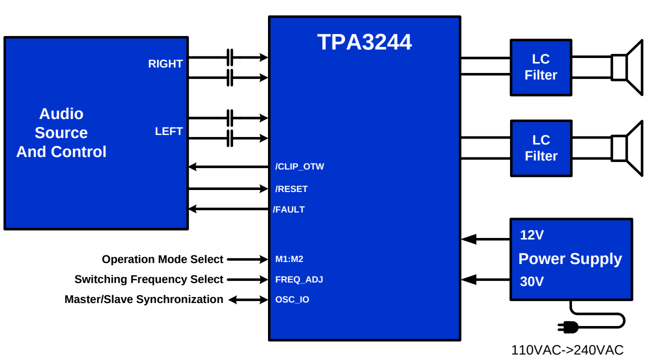
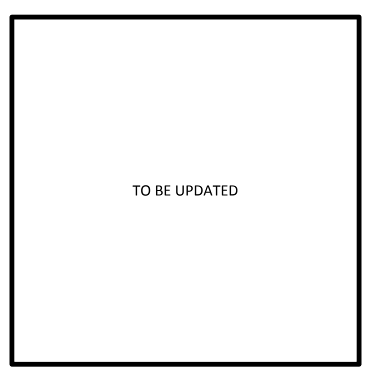



**Figure 2. Total Harmonic Distortion**

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## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| April 2016 | * | Initial release. |

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## 5 Device Comparison Table

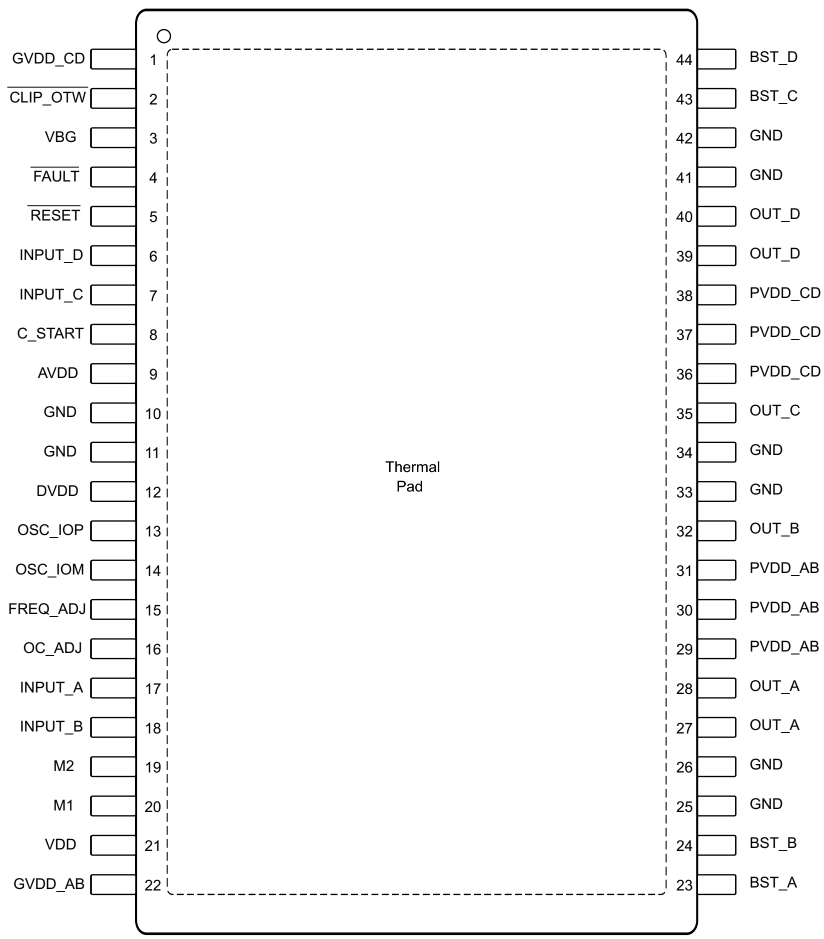
| DEVICE NAME | DESCRIPTION |
|---|---|
| TPA3251D2 | 175-W Stereo Class-D PurePath™ Ultra-HD Analog Input Audio Power Amplifier |
| TPA3116D2 | 50W Filter-Free Class-D Stereo Amplifier Family with AM Avoidance |
| TPA3118D2 | 30W Filter-Free Class-D Stereo Amplifier Family with AM Avoidance |

## 6 Pin Configuration and Functions

The TPA3244 device is available in a thermally enhanced TSSOP package.

The package type contains a PowerPad™ that is located on the bottom side of the device for thermal connection to the PCB.

**DDV Package**
**HTSSOP 44-Pin**
**(Top View)**



## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AVDD | 9 | P | Internal voltage regulator, analog section |
| BST_A | 23 | P | HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_A required. |
| BST_B | 24 | P | HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_B required. |
| BST_C | 43 | P | HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_C required. |
| BST_D | 44 | P | HS bootstrap supply (BST), external 0.033 µF capacitor to OUT_D required. |
| $\overline{\text{CLIP\_OTW}}$ | 2 | O | Clipping warning and Over-temperature warning; open drain; active low |
| C_START | 8 | O | Startup ramp, requires a charging capacitor to GND |
| DVDD | 12 | P | Internal voltage regulator, digital section |
| $\overline{\text{FAULT}}$ | 4 | O | Shutdown signal, open drain; active low |
| FREQ_ADJ | 15 | O | Oscillator frequency programming pin |
| GND | 10, 11, 25, 26, 33, 34, 41, 42 | P | Ground |
| GVDD_AB | 22 | P | Gate-drive voltage supply; AB-side, requires 0.1 µF capacitor to GND |
| GVDD_CD | 1 | P | Gate-drive voltage supply; CD-side, requires 0.1 µF capacitor to GND |
| INPUT_A | 17 | I | Input signal for half bridge A |
| INPUT_B | 18 | I | Input signal for half bridge B |
| INPUT_C | 7 | I | Input signal for half bridge C |
| INPUT_D | 6 | I | Input signal for half bridge D |
| M1 | 20 | I | Mode selection 1 (LSB) |
| M2 | 19 | I | Mode selection 2 (MSB) |
| OC_ADJ | 16 | I/O | Over-Current threshold programming pin |
| OSC_IOM | 14 | I/O | Oscillator synchronization interface |
| OSC_IOP | 13 | O | Oscillator synchronization interface |
| OUT_A | 27, 28 | O | Output, half bridge A |
| OUT_B | 32 | O | Output, half bridge B |
| OUT_C | 35 | O | Output, half bridge C |
| OUT_D | 39, 40 | O | Output, half bridge D |
| PVDD_AB | 29, 30, 31 | P | PVDD supply for half-bridge A and B |
| PVDD_CD | 36, 37, 38 | P | PVDD supply for half-bridge C and D |
| $\overline{\text{RESET}}$ | 5 | I | Device reset Input; active low |
| VDD | 21 | P | Power supply for internal voltage regulator requires a 10-µF capacitor with a 0.1-µF capacitor to GND for decoupling. |
| VBG | 3 | P | Internal voltage reference requires a 0.1-µF capacitor to GND for decoupling. |
| PowerPAD™ | | P | Ground, connect to PCB copper pour. Placed on bottom side of device. |

**Table 2. Mode Selection Pins**

| MODE PINS | | INPUT MODE | OUTPUT CONFIGURATION | DESCRIPTION |
|---|---|---|---|---|
| M2 | M1 | | | |
| 0 | 0 | 2N + 1 | 2 × BTL | Stereo BTL output configuration |
| 0 | 1 | 2N/1N + 1 | 1 x BTL + 2 x SE | 2.1 BTL + SE mode |
| 1 | 0 | 2N + 1 | 1 x PBTL | Parallelled BTL configuration. Connect INPUT_C and INPUT_D to GND. |
| 1 | 1 | 1N +1 | 4 x SE | Single ended output configuration |

# 7 Detailed Description

## 7.1 Overview

To facilitate system design, the TPA3244 needs only a 12-V supply in addition to the (typical) 32-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry, AVDD and DVDD. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

## Overview (continued)

The audio signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X). Power-stage supply pins (PVDD_X) and gate drive supply pins (GVDD_X) are separate for each full bridge. Although supplied from the same 12-V source, separating to GVDD_AB, GVDD_CD, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. It is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1-μF ceramic capacitor placed as close as possible to the supply pins. It is recommended to follow the PCB layout of the TPA3244 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 36-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artefacts. Moreover, the TPA3244 device is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range.

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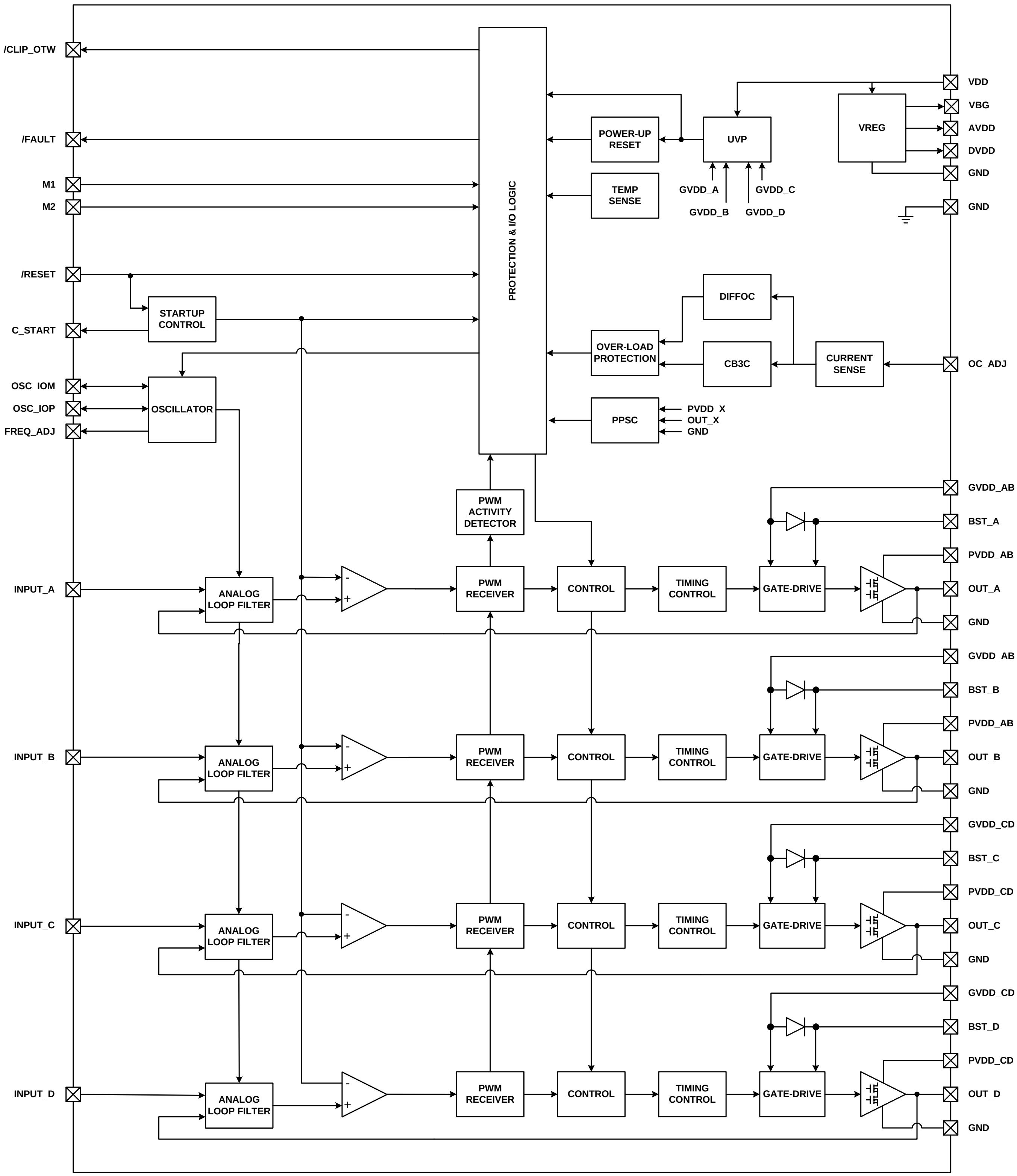
## 7.2 Functional Block Diagrams




FunctionalBlockDiagram.vsd

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## Functional Block Diagrams (continued)

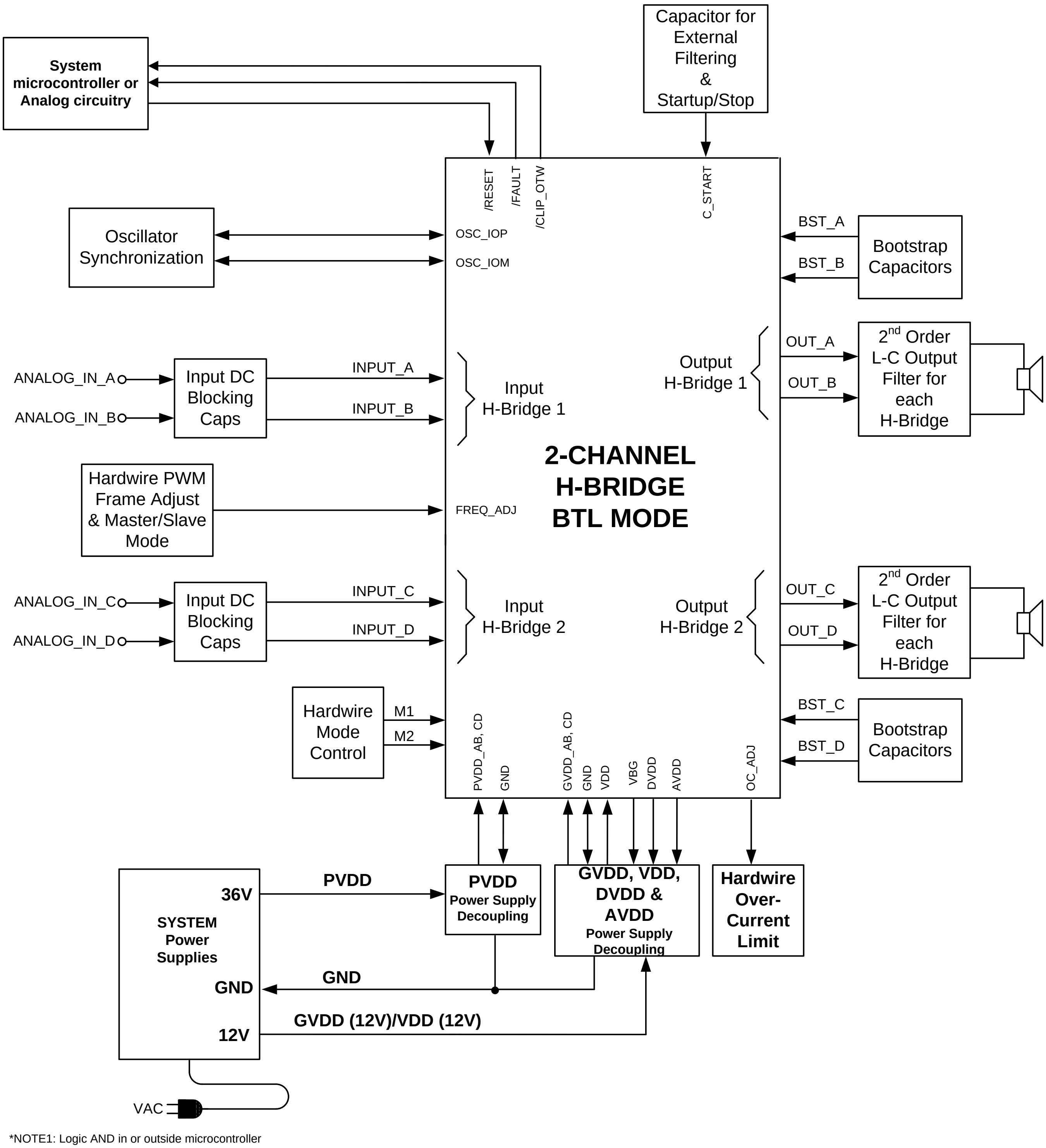


**Figure 3. System Block Diagram**

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## 7.3 Feature Description

### 7.3.1 Error Reporting

The FAULT, and CLIP_OTW, pins are active-low, open-drain outputs. The function is for protection-mode signaling to a system-control device.

Any fault resulting in device shutdown is signaled by the FAULT pin going low. Also, CLIP_OTW goes low when the device junction temperature exceeds 125°C (see Table 3).

**Table 3. Error Reporting**

| FAULT | CLIP_OTW | DESCRIPTION |
|---|---|---|
| 0 | 0 | Overtemperature (OTE) or overload (OLP) or undervoltage (UVP) Junction temperature higher than 125°C (overtemperature warning) |
| 0 | 0 | Overload (OLP) or undervoltage (UVP). Junction temperature higher than 125°C (overtemperature warning) |
| 0 | 1 | Overload (OLP) or undervoltage (UVP). Junction temperature lower than 125°C |
| 1 | 0 | Junction temperature higher than 125°C (overtemperature warning) |
| 1 | 1 | Junction temperature lower than 125°C and no OLP or UVP faults (normal operation) |

Note that asserting either RESET low forces the FAULT signal high, independent of faults being present. TI recommends monitoring the CLIP_OTW signal using the system microcontroller and responding to an overtemperature warning signal by, that is, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both FAULT and CLIP_OTW outputs.



## 7.4 Device Functional Modes

### 7.4.1 Device Protection System

The TPA3244 device contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TPA3244 device responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the FAULT pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will function on errors, as shown in Table 4.

**Table 4. Device Protection**

<table>
<tr><th>BTL</th><th>MODE</th><th>PBTL</th><th>MODE</th><th>SE</th><th>MODE</th></tr>
<tr><th>LOCAL ERROR IN</th><th>TURNS OFF</th><th>LOCAL ERROR IN</th><th>TURNS OFF</th><th>LOCAL ERROR IN</th><th>TURNS OFF</th></tr>
<tr><td>A</td><td rowspan="2">A+B</td><td>A</td><td rowspan="4">A+B+C+D</td><td>A</td><td rowspan="2">A+B</td></tr>
<tr><td>B</td><td>B</td><td>B</td></tr>
<tr><td>C</td><td rowspan="2">C+D</td><td>C</td><td>C</td><td rowspan="2">C+D</td></tr>
<tr><td>D</td><td>D</td><td>D</td></tr>
</table>

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert FAULT).

#### *7.4.1.1 Overload and Short Circuit Current Protection*

The TPA3244 device has fast reacting current sensors with a programmable trip threshold (OC threshold) on all high-side and low-side FETs. To prevent output current to increase beyond the programmed threshold, TPA3244 has the option of either limiting the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) or to perform an immediate shutdown of the output in case of excess output current (Latching Shutdown). CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a drop of real speaker's load impedance, and allows the output current to be limited to a maximum programmed level. If the maximum output current persists, i.e. the power stage being overloaded with too low load impedance, the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi- Z) state until a RESET cycle is initiated. CB3C works individually for each half bridge output. If an over current event is triggered, CB3C performs a state flip of the half bridge output that is cleared upon beginning of next PWM frame.

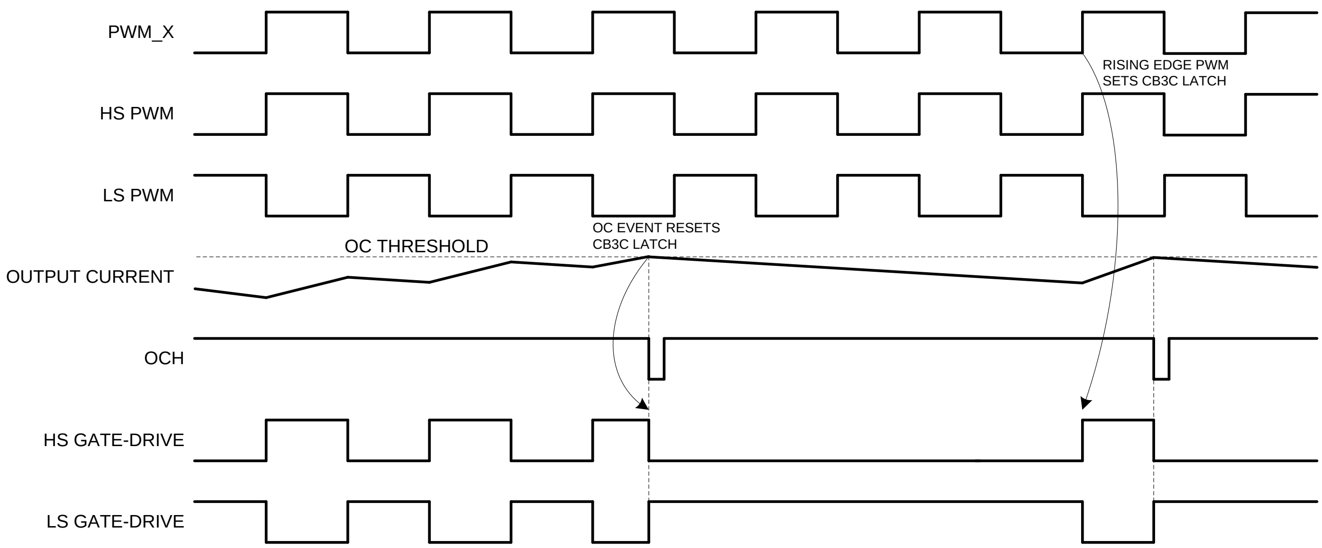


**Figure 4. CB3C Timing Example**

During CB3C an over load counter increments for each over current event and decrease for each non-over current PWM cycle. This allows full amplitude transients into a low speaker impedance without a shutdown protection action. In the event of a short circuit condition, the over current protection limits the output current by the CB3C operation and eventually shut down the affected output if the overload counter reaches its maximum value. If a latched OC operation is required such that the device shuts down the affected output immediately upon first detected over current event, this protection mode should be selected. The over current threshold and mode (CB3C or Latched OC) is programmed by the OC_ADJ resistor value. The OC_ADJ resistor needs to be within its intentional value range for either CB3C operation or Latched OC operation.

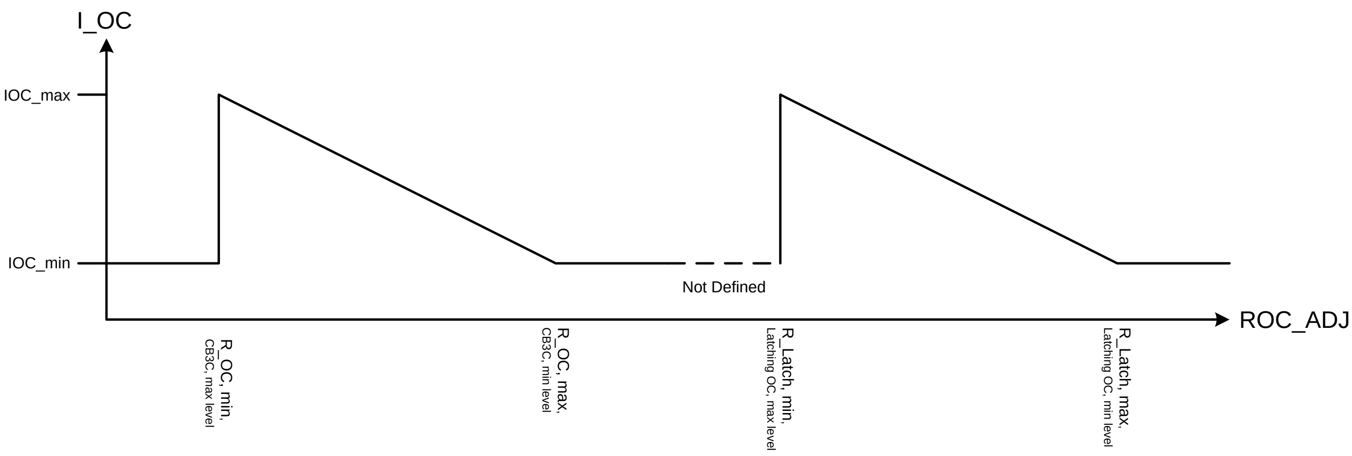


**Figure 5. OC Threshold versus OC_ADJ Resistor Value Example**

OC_ADJ values outside specified value range for either CB3C or latched OC operation will result in minimum OC threshold.

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**Table 5. Device Protection**

| OC_ADJ Resistor Value | Protection Mode | OC Threshold |
|---|---|---|
| 22kΩ | CB3C | 16.3A |
| 24kΩ | CB3C | 15.1A |
| 27kΩ | CB3C | 13.5A |
| 30kΩ | CB3C | 12.3A |
| 47kΩ | Latched OC | 16.3A |
| 51kΩ | Latched OC | 15.1A |
| 56kΩ | Latched OC | 13.5A |
| 64kΩ | Latched OC | 12.3A |

#### *7.4.1.2 DC Speaker Protection*

The output DC protection scheme protects a connected speaker from excess DC current caused by a speaker wire accidentally shorted to chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL output, and in the event of the unbalance exceeding a programmed threshold, the overload counter increments until its maximum value and the affected output channel is shut down. DC Speaker Protection is disabled in PBTL and SE mode operation.

#### *7.4.1.3 Pin-to-Pin Short Circuit Protection (PPSC)*

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup that is, when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low, and the device will not react to changes applied to the RESET pin. If no shorts are present the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert a resistive load to GND_X or PVDD_X.

#### *7.4.1.4 Overtemperature Protection OTW and OTE*

The TPA3244 device has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{CLIP\_OTW}}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

#### *7.4.1.5 Undervoltage Protection (UVP) and Power-on Reset (POR)*

The UVP and POR circuits of the TPA3244 device fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the Electrical Characteristics table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

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#### 7.4.1.6 Fault Handling

If a fault situation occurs while in operation, the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and will assert FAULT low. A global fault is a latching fault and clearing FAULT and restart operation requires resetting the device by toggling RESET. Toggling RESET should never be allowed with excessive system temperature, so it is advised to monitor RESET by a system microcontroller and only allow releasing RESET (RESET high) if the OTW signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channel(s). Note that asserting RESET low forces the FAULT signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system micro controller and responding to an over temperature warning signal by, that is, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

**Table 6. Error Reporting**

| Fault/Event | Fault/Event Description | Global or Channel | Reporting Method | Latched/Self Clearing | Action needed to Clear | Output FETs |
|---|---|---|---|---|---|---|
| PVDD_X UVP | Voltage Fault | Global | $\overline{\text{FAULT}}$ pin | Self Clearing | Increase affected supply voltage | HI-Z |
| VDD UVP | | | | | | |
| AVDD UVP | | | | | | |
| POR (DVDD UVP) | Power On Reset | Global | $\overline{\text{FAULT}}$ pin | Self Clearing | Allow DVDD to rise | HI-Z |
| BST_X UVP | Voltage Fault | Channel (Half Bridge) | None | Self Clearing | Allow BST cap to recharge (lowside ON, VDD 12V) | HighSide off |
| OTW | Thermal Warning | Global | $\overline{\text{OTW}}$ pin | Self Clearing | Cool below OTW threshold | Normal operation |
| OTE | Thermal Shutdown | Global | $\overline{\text{FAULT}}$ pin | Latched | Toggle $\overline{\text{RESET}}$ | HI-Z |
| OLP (CB3C>1.7ms) | OC Shutdown | Channel | $\overline{\text{FAULT}}$ pin | Latched | Toggle $\overline{\text{RESET}}$ | HI-Z |
| Latched OC (47kΩ<ROC_ADJ<68 kΩ) | OC Shutdown | Channel | $\overline{\text{FAULT}}$ pin | Latched | Toggle $\overline{\text{RESET}}$ | HI-Z |
| CB3C (22kΩ<ROC_ADJ<30 kΩ) | OC Limiting | Channel | None | Self Clearing | Reduce signal level or remove short | Flip state, cycle by cycle at fs/3 |
| Stuck at Fault(1) | No OSC_IO activity in Slave Mode | Global | None | Self Clearing | Resume OSC_IO activity | HI-Z |

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

#### 7.4.1.7 Device Reset

Asserting $\overline{\text{RESET}}$ low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active both in SE mode and BTL mode with $\overline{\text{RESET}}$ low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs.

Asserting reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPA3244 device can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

## 8.2 Typical Applications

### 8.2.1 Stereo BTL Application

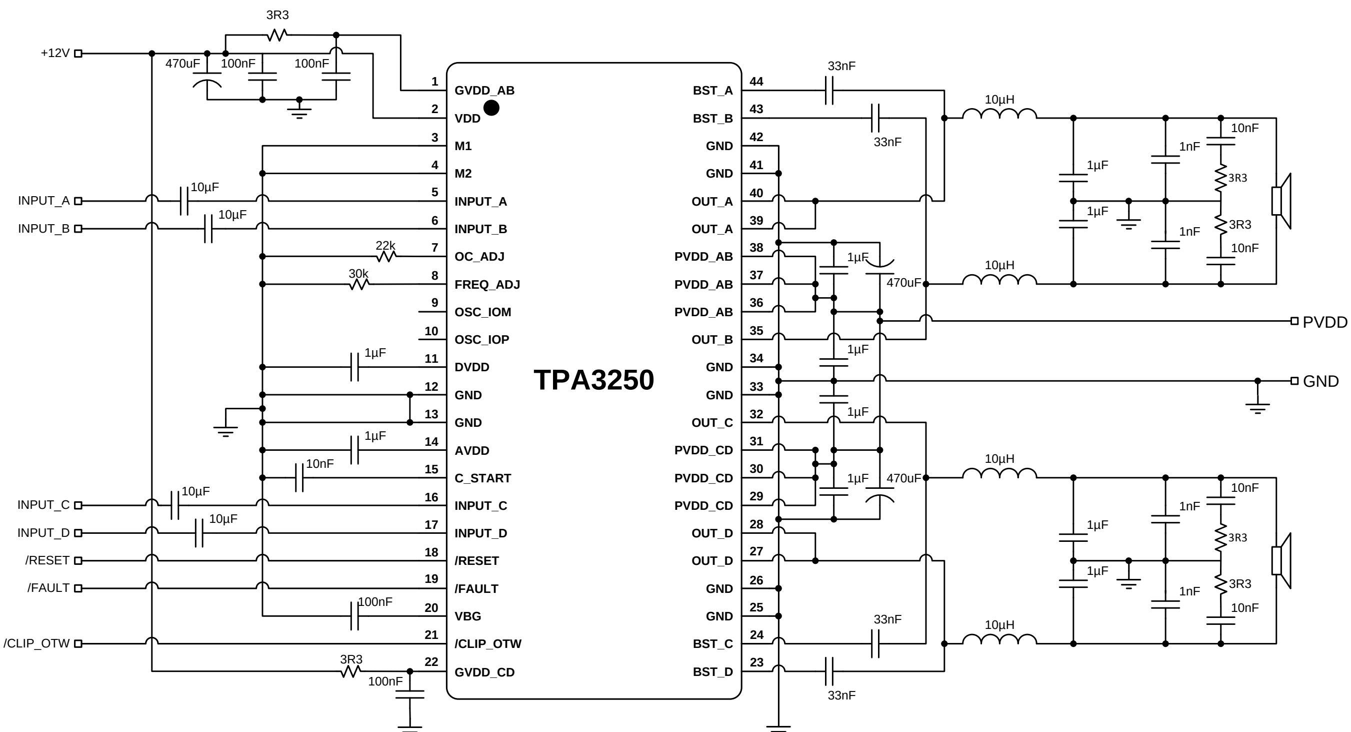


**Figure 6. Typical Differential Input BTL Application**

## Typical Applications (continued)

### *8.2.1.1 Design Requirements*

For this design example, use the parameters in Table 7.

**Table 7. Design Requirements, BTL Application**

| DESIGN PARAMETER | EXAMPLE |
| --- | --- |
| Low Power (Pull-up) Supply | 3.3 V |
| Mid Power Supply 12 V | 12 V |
| High Power Supply | 12 - 32 V |
| Mode Selection | M2 = L |
| | M1 = L |
| Analog Inputs | INPUT_A = ±3.9 V (peak, max) |
| | INPUT_B = ± 3.9V (peak, max) |
| | INPUT_C = ±3.9 V (peak, max) |
| | INPUT_D = ±3.9 V (peak, max) |
| Output Filters | Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF) |
| Speaker Impedance | 3-8 Ω |

### *8.2.1.2 Detailed Design Procedures*

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply nominally operating at a low rail adjusting to a higher supply rail.

The device is inverting the audio signal from input to output.

The DVDD and AVDD pins are not recommended to be used as a voltage sources for external circuitry.

#### 8.2.1.2.1 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 1µF that is placed on the power supply to each full-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50 V is required for use with a 32V power supply.

#### 8.2.1.2.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 50 V supports most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

#### 8.2.1.2.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper is recommended for use with the TPA3244 device. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

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#### 8.2.1.2.4 Oscillator

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

To reduce interference problems while using radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower value switching frequencies together results in the fewest cases of interference throughout the AM band. The oscillator frequency can be selected by the value of the FREQ_ADJ resistor connected to GND in master mode according to the description in the Recommended Operating Conditions table.

For slave mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to DVDD. This configures the OSC_I/O pins as inputs to be slaved from an external differential clock. In a master/slave system inter channel delay is automatically setup between the switching of the audio channels, which can be illustrated by no idle channels switching at the same time. This will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply to optimize audio performance and to get better operating conditions for the power supply. The inter channel delay will be setup for a slave device depending on the polarity of the OSC_I/O connection such that a slave mode 1 is selected by connecting the master device OSC_I/O to the slave 1 device OSC_I/O with same polarity (+ to + and - to -), and slave mode 2 is selected with the inverse polarity (+ to - and - to +).

### 8.2.2 Application Curves

Relevant performance plots for the TPA3244 device in BTL configuration are shown in

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**Table 8. Relevant Performance Plots, BTL Configuration**

| PLOT TITLE | FIGURE NUMBER |
|---|---|
| Total Harmonic Distortion+Noise vs Frequency | |
| Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW | |
| Total Harmonic Distortion + Noise vs Output Power | |
| Output Power vs Supply Voltage, 10% THD+N | |
| Output Power vs Supply Voltage, 10% THD+N | |
| System Efficiency vs Output Power | |
| System Power Loss vs Output Power | |
| Output Power vs Case Temperature | |
| Noise Amplitude vs Frequency | |

### 8.2.3 Typical Application, Single Ended (1N) SE

The TPA3244 device can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

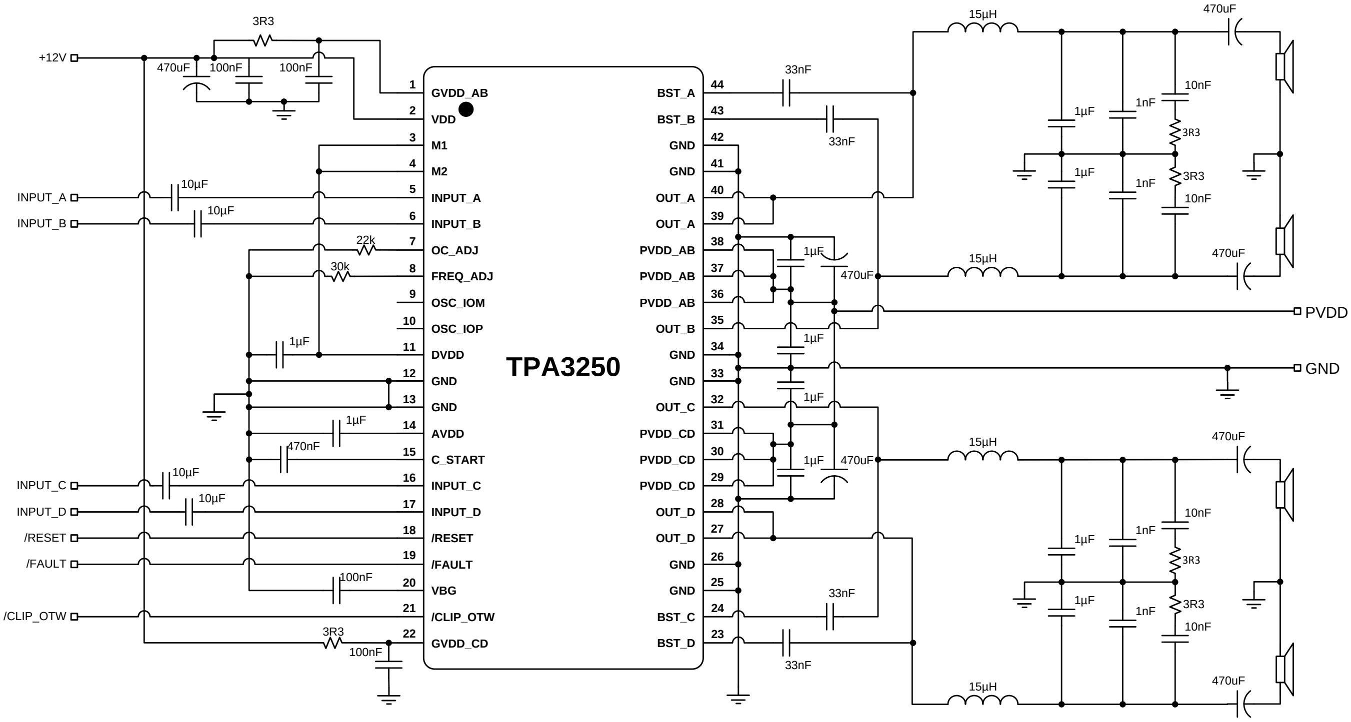


**Figure 7. Typical Single Ended (1N) SE Application**

#### *8.2.3.1 Design Requirements*

Refer to *Stereo BTL Application* for the Design Requirements.

**Table 9. Design Requirements, SE Application**

| DESIGN PARAMETER | EXAMPLE |
|---|---|
| Low Power (Pull-up) Supply | 3.3 V |
| Mid Power Supply 1 2V | 12 V |
| High Power Supply | 12 - 32 V |
| Mode Selection | M2 = H |
| | M1 = H |
| Analog Inputs | INPUT_A = ±3.9 V (peak, max) |
| | INPUT_B = ±3.9 V (peak, max) |
| | INPUT_C = ±3.9 V (peak, max) |
| | INPUT_D = ±3.9 V (peak, max) |
| Output Filters | Inductor-Capacitor Low Pass FIlter (15 µH + 680 nF) |
| Speaker Impedance | 2 - 8 Ω |

#### *8.2.3.2 Detailed Design Procedures*

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

#### 8.2.3.3 Application Curves

Relevant performance plots for the TPA3244 device in PBTL configuration are shown in

**Table 10. Relevant Performance Plots, SE Configuration**

| PLOT TITLE | FIGURE NUMBER |
|---|---|
| Total Harmonic Distortion+Noise vs Output Power | |
| Total Harmonic Distortion+Noise vs Frequency | |
| Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW | |
| Output Power vs Supply Voltage, 10% THD+N | |
| Output Power vs Supply Voltage, 1% THD+N | |
| Output Power vs Case Temperature | |

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### 8.2.4 Typical Application, Differential (2N) PBTL

The TPA3244 device can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

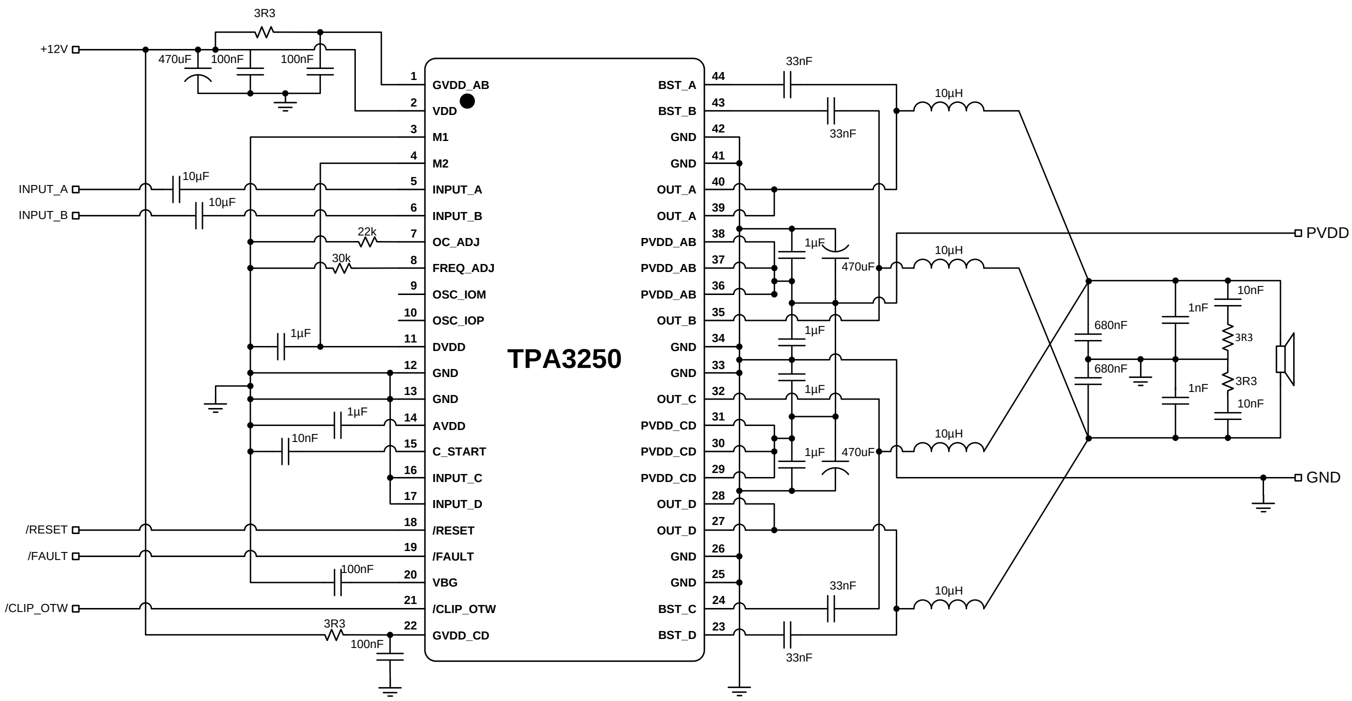


**Figure 8. Typical Differential (2N) PBTL Application**

#### 8.2.4.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

**Table 11. Design Requirements, PBTL Application**

| DESIGN PARAMETER | EXAMPLE |
|---|---|
| Low Power (Pull-up) Supply | 3.3 V |
| Mid Power Supply 12 V | 12 V |
| High Power Supply | 12 - 32 V |
| Mode Selection | M2 = H |
| | M1 = L |
| Analog Inputs | INPUT_A = ±3.9V (peak, max) |
| | INPUT_B = ±3.9V (peak, max) |
| | INPUT_C = Grounded |
| | INPUT_D = Grounded |
| Output Filters | Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF) |
| Speaker Impedance | 2 - 4 Ω |

#### 8.2.4.2 Detailed Design Procedures

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

#### 8.2.4.3 Application Curves

Relevant performance plots for the TPA3244 device in PBTL configuration are shown in

**Table 12. Relevant Performance Plots, PBTL Configuration**

| PLOT TITLE | FIGURE NUMBER |
|---|---|
| Total Harmonic Distortion+Noise vs Output Power | |
| Total Harmonic Distortion+Noise vs Frequency | |
| Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW | |
| Output Power vs Supply Voltage, 10% THD+N | |
| Output Power vs Supply Voltage, 1% THD+N | |
| Output Power vs Case Temperature | |

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# 9 Power Supply Recommendations

## 9.1 Power Supplies

The TPA3244 device requires two external power supplies for proper operation. A high-voltage supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one mid-voltage power supply for GVDD_X and VDD is required to power the gate-drive and other internal digital and analog portions of the device. The allowable voltage range for both the PVDD and the GVDD_X/VDD supplies are listed in the table. Ensure both the PVDD and the GVDD_X/VDD supplies can deliver more current than listed in the table.

### 9.1.1 VDD Supply

The VDD supply required from the system is used to power several portions of the device. It provides power to internal regulators DVDD and AVDD that are used to power digital and analog sections of the device, respectively. Proper connection, routing, and decoupling techniques are highlighted in the TPA3244 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3244 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3244 device. Some portions of the device also require a separate power supply which is a lower voltage than the VDD supply. To simplify the power supply requirements for the system, the TPA3244 device includes integrated low-dropout (LDO) linear regulators to create these supplies. These linear regulators are internally connected to the VDD supply and their outputs are presented on AVDD and DVDD pins, providing a connection point for an external bypass capacitors. It is important to note that the linear regulators integrated in the device have only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on these pins could cause the voltage to sag and increase noise injection, which negatively affects the performance and operation of the device.

### 9.1.2 GVDD_X Supply

The GVDD_X supply required from the system is used to power the gate-drives for the output H-bridges. Proper connection, routing, and decoupling techniques are highlighted in the TPA3244 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3244 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3244 device.

### 9.1.3 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TPA3244 device EVM User's Guide SLVUAG8 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TPA3244 device EVM User's Guide SLVUAG8. The lack of proper decoupling, like that shown in the EVM User's Guide, can results in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults.

## 9.2 Powering Up

The TPA3244 device does not require a power-up sequence, but it is recommended to hold $\overline{\text{RESET}}$ low minimum 400ms after PVDD supply voltage is turned ON. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

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### Powering Up (continued)

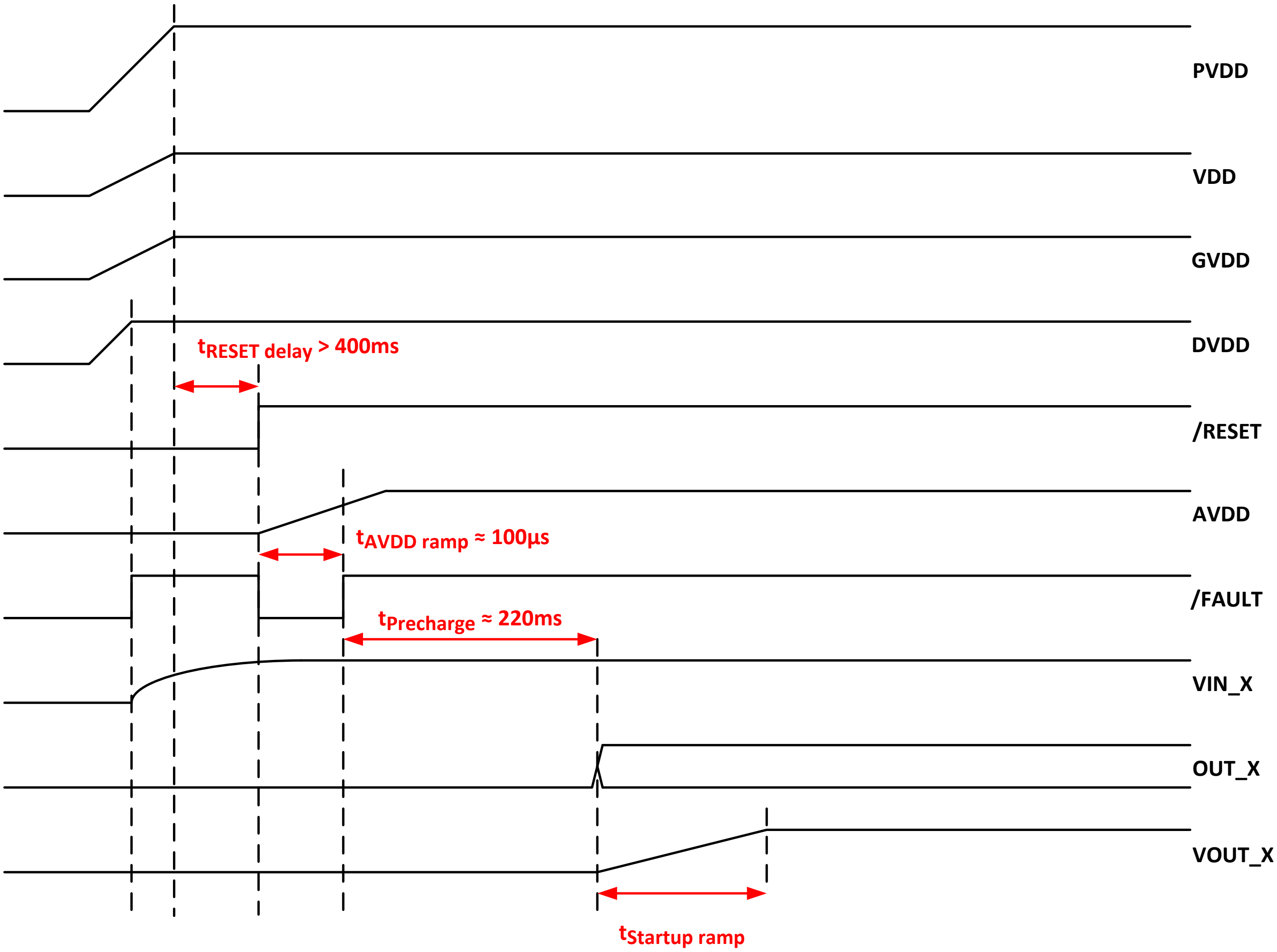


**Figure 9. Startup Timing**

When $\overline{\text{RESET}}$ is released to turn on the TPA3244 device, $\overline{\text{FAULT}}$ signal will turn low and AVDD voltage regulator will be enabled. $\overline{\text{FAULT}}$ will stay low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). After a precharge time to stabilize the DC voltage across the input AC coupling capacitors, before the ramp up sequence starts.

## 9.3 Powering Down

The TPA3244 device does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold. Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks by initiating a controlled ramp down sequence of the output voltage.

## 9.4 Thermal Design

### 9.4.1 Thermal Performance

The TPA3244 device thermal performance is dependent on the thermal design of the PCB. As a result, the maximum continuous output power attainable will be influenced by the PCB design. The continuous power rating is lower than the peak output power capability of the device. The peak power rating of the TPA3244 deviceis based on the burst capability of the device. The peak to average power ratio of the TPA3244 device is well suited to handle even demanding audio playback without thermal shutdown. Thermal performance with typical audio content (burst) versus sine wave content (continuous) should be considered when defining the thermal test requirements for the end product.

### 9.4.2 Thermal Performance with Continuous Output Power

It is recommended to operate the TPA3244 device below the OTW threshold, which in most systems will require the average output power to be below the maximum peak output power. The maximum continuous power, the TPA3244 device will deliver depends directly on the thermal design of the PCB and for the entire system (closed box with no air flow, or a fanned system etc.). Thermal performance is also impacted by PVDD voltage and switching frequency. The best configuration for a given application will often depend on the continuous output power requirements.

**Table 13. Device and PCB Temperatures with 8-Ω Load, $T_A$ = 40°C**

| $T_A$ = 40°C, TPA3244 EVM, No Airflow. Steady State Temperatures. | | | | | | |
|---|---|---|---|---|---|---|
| PVDD | Switching Frequency | Continuous Power [W] | | Device Top Temperature | Maximum PCB Temperature | Comment |
| 32V | 450kHz | 73W | 10% THD | 114°C | 89°C | |
| 32V | 450kHz | 18W | 1/4 of 10% THD power | 87°C | 71°C | |
| 32V | 450kHz | 9W | 1/8 of 10% THD power | 77°C | 65°C | |
| 32V | 600kHz | 72W | 10% THD | 128°C | 98°C | OTW after 236 seconds |
| 32V | 600kHz | 18W | 1/4 of 10% THD power | 105°C | 84°C | |
| 32V | 600kHz | 9W | 1/8 of 10% THD power | 85°C | 70°C | |
| 36V | 450kHz | 92W | 10% THD | 150°C | 113°C | OTW after 95 seconds |
| 36V | 450kHz | 23W | 1/4 of 10% THD power | 111°C | 87°C | |
| 36V | 450kHz | 11.5W | 1/8 of 10% THD power | 79°C | 71°C | |
| 36V | 600kHz | 91W | 10% THD | OTE(1) | | OTW after 3 seconds. Not recommended. |
| 36V | 600kHz | 22.5W | 1/4 of 10% THD power | 144°C | 109°C | OTW after 152 seconds |
| 36V | 600kHz | 11.5W | 1/8 of 10% THD power | 115°C | 90°C | |

(1) Steady state data is not available because device heats up to OTE in this condition.

**Table 14. Device and PCB Temperatures with 4-Ω Load, $T_A$ = 40°C**

| $T_A$ = 40°C, TPA3244 EVM, No Airflow. Steady State Temperatures. | | | | | | |
|---|---|---|---|---|---|---|
| PVDD | Switching Frequency | Continuous Power [W] | | Device Top Temperature | Maximum PCB Temperature | Comment |
| 32V | 450kHz | 130W | 10% THD | OTE | | OTW after 1 second.Not recommended. |
| 32V | 450kHz | 32.5W | 1/4 of 10% THD power | 147°C | 111°C | OTW after 92 seconds. Not recommended. |
| 32V | 450kHz | 16W | 1/8 of 10% THD power | 107°C | 85°C | |
| 32V | 600kHz | 130W | 10% THD | OTE(1) | | OTW after 1 second. Not recommended. |
| 32V | 600kHz | 32.5W | 1/4 of 10% THD power | OTE(1) | | OTW after 29 seconds. Not recommended. |
| 32V | 600kHz | 16W | 1/8 of 10% THD power | 147°C | 99°C | OTW after 92 seconds. Not recommended. |
| 36V | 450kHz | 165W | 10% THD | OTE(1) | | OTW after 0 seconds. Not recommended. |

(1) Steady state data is not available because device heats up to OTE in this condition.

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**Table 14. Device and PCB Temperatures with 4-Ω Load, $T_A$ = 40°C (continued)**

| $T_A$ = 40°C, TPA3244 EVM, No Airflow. Steady State Temperatures. | | | | | | |
|---|---|---|---|---|---|---|
| 36V | 450kHz | 41W | 1/4 of 10% THD power | OTE[1] | | OTW after 11 seconds. Not recommended. |
| 36V | 450kHz | 21W | 1/8 of 10% THD power | 142°C | 108°C | OTW after 134 seconds. Not recommended. |
| 36V | 600kHz | Not recommended | | | | |

### 9.4.3 Thermal Performance with Non-Continuous Output Power

As audio signals often have a peak to average ratio larger than one (average level below maximum peak output), the thermal performance for audio signals can be illustrated using burst signals with different burst ratios.

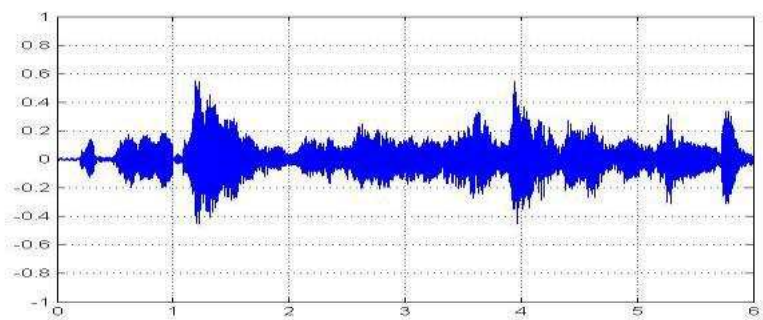


**Figure 10. Example of audio signal**

A burst signal is characterized by the high-level to low-level ratio as well as the duration of the high level and low level, e.g. a burst 1:4 stimuli is a single period of high level followed by 4 cycles of low level.

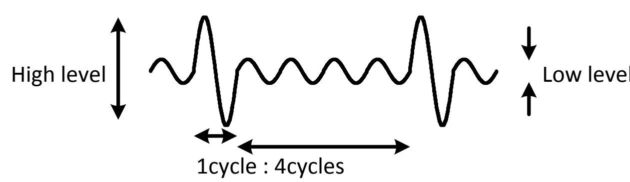


**Figure 11. Example of 1:4 Burst Signal**

The following analysis of thermal performance for the TPA3244 device is made with the TPA3244 EVM surrounded by still air (no airflow) with a controlled air temperature of 40°C. For 32-V operation the system is not thermally limited with 8Ω load, but depending on the burst stimuli for operation at 36V some thermal limitations may occur, depending on switching frequency and average to maximum power ratio. Low to maximum power ratio of the burst stimuli is given in the plots as for example P1:8 which equals 1 cycle of full power followed by 8 cycles of low power.

# 10 Layout

## 10.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible.
- A local ground area underneath the device is important to keep solid to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TPA3244 device, unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads.
- Avoid placing other heat producing components or structures near the TPA3244 device.
- Avoid cutting off the flow of heat from the TPA3244 device to the surrounding ground areas with traces or via strings, especially on output side of device.

Netlist for this printed circuit board is generated from the schematic in .

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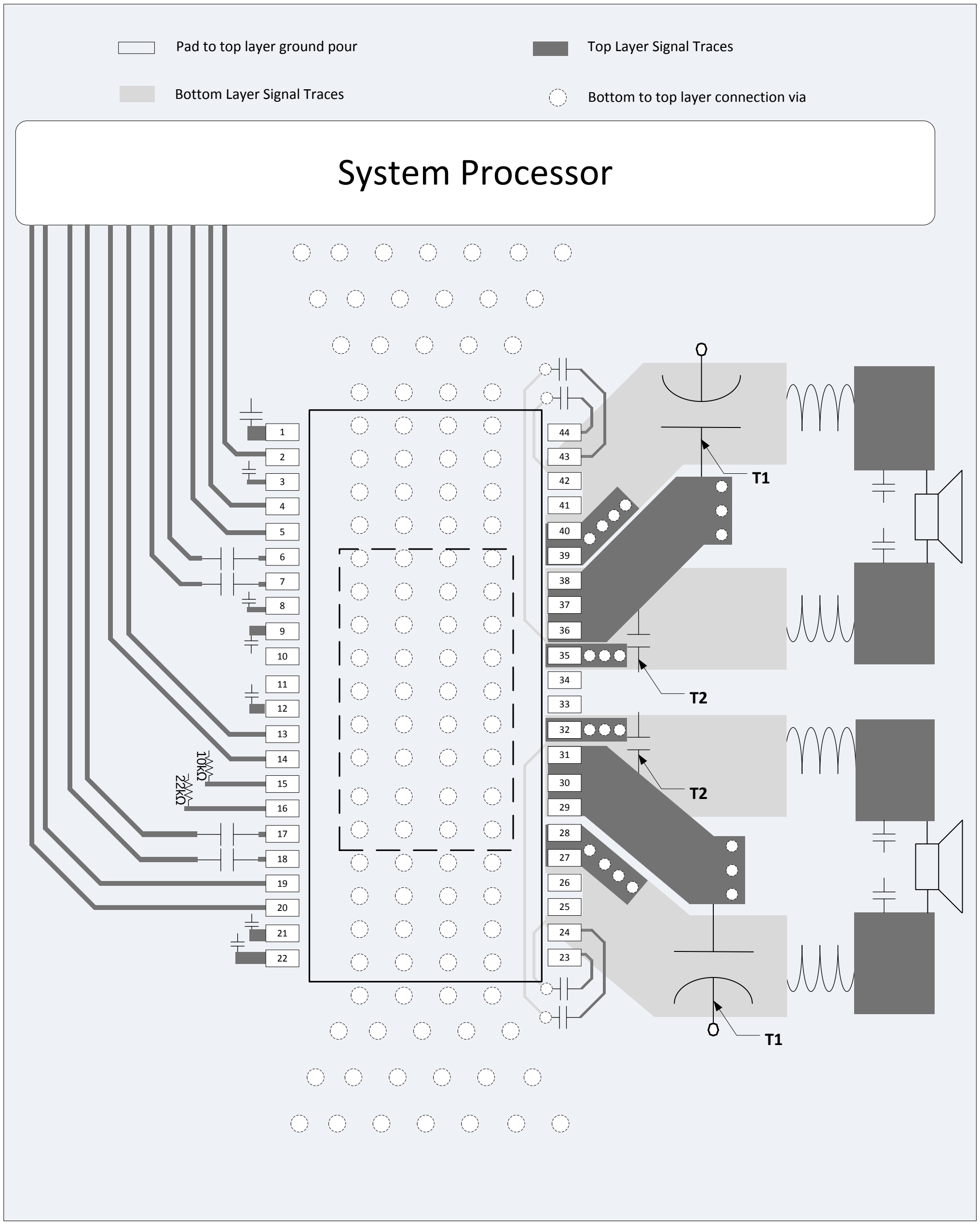
## 10.2 Layout Examples

### 10.2.1 BTL Application Printed Circuit Board Layout Example




A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

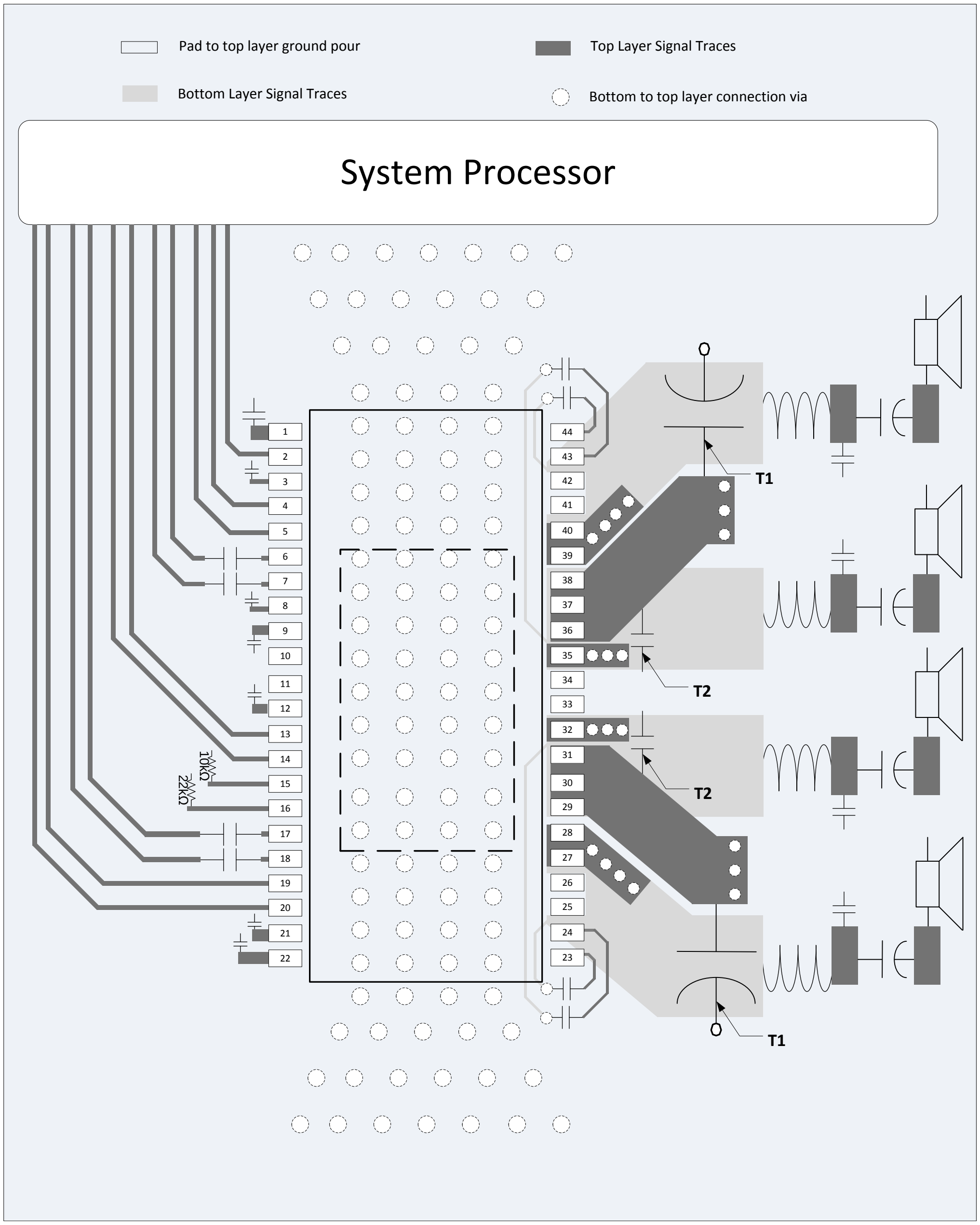
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors placed close to the pins.

D. **Note T3**: PowerPad™ needs to be soldered to PCB GND copper pour

**Figure 12. BTL Application Printed Circuit Board - Composite**

## Layout Examples (continued)

### 10.2.2 SE Application Printed Circuit Board Layout Example




A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

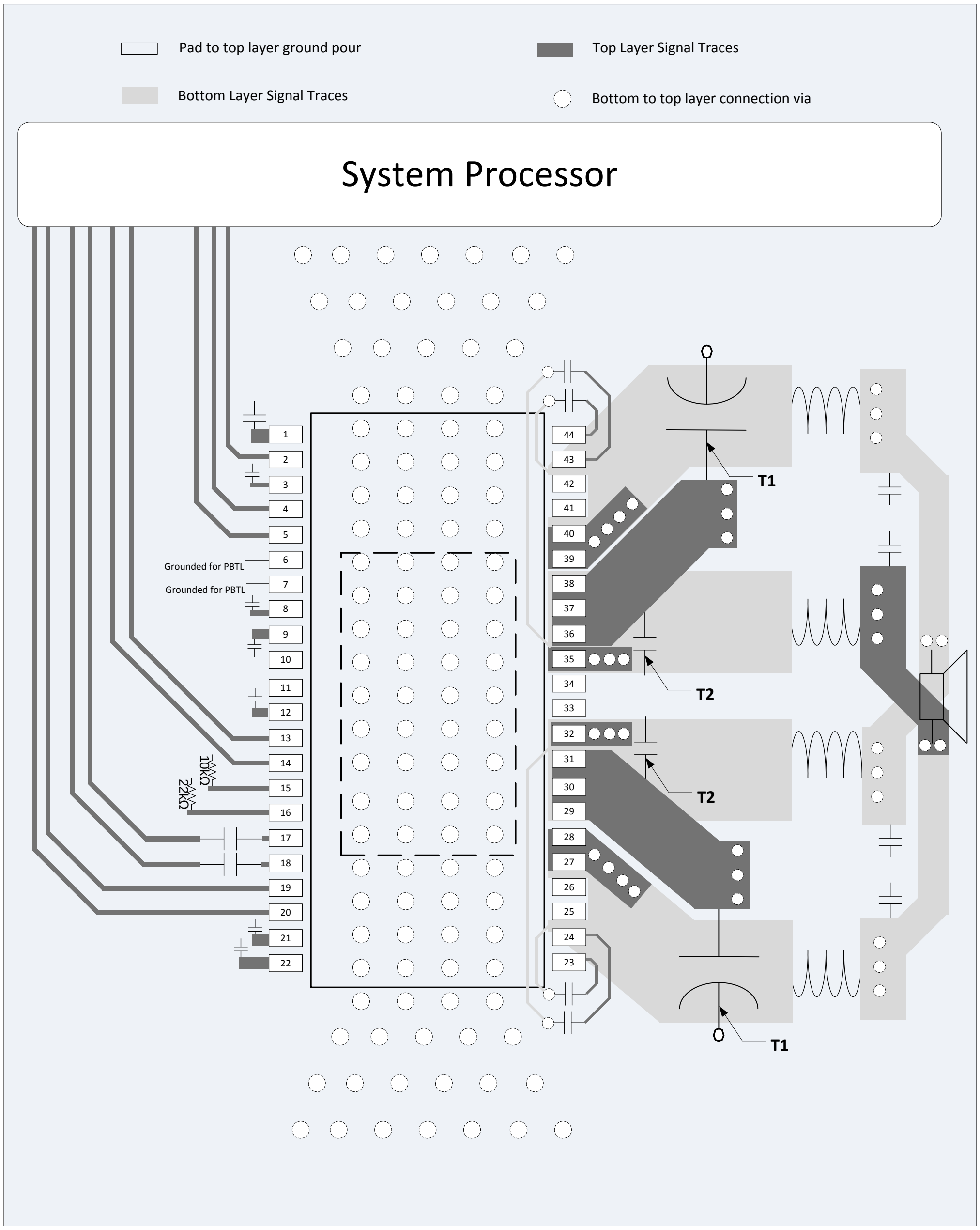
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed close to the pins.

D. **Note T3**: PowerPad™ needs to be soldered to PCB GND copper pour

**Figure 13. SE Application Printed Circuit Board - Composite**

## Layout Examples (continued)

### 10.2.3 PBTL Application Printed Circuit Board Layout Example




A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed close to the pins.

D. **ote T3**: PowerPad™ needs to be soldered to PCB GND copper pour

**Figure 14. PBTL Application Printed Circuit Board - Composite**

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# 11 Device and Documentation Support

## 11.1 Documentation Support

*TPA3250D2EVM User's Guide*, SLVUAG8

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

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Blu-ray Disk is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA3244DDW | PREVIEW | HTSSOP | DDW | 44 | 35 | TBD | Call TI | Call TI | 0 to 70 | | |
| TPA3244DDWR | PREVIEW | HTSSOP | DDW | 44 | 2000 | TBD | Call TI | Call TI | 0 to 70 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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