

## TPA SERIES

### Application :

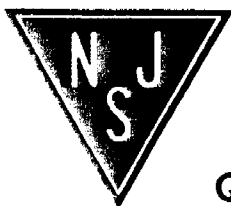
TPA series solid state Arrestor is optioned to perfect overvoltage Telecommunication equipment and other electric circuits.

### Electrical Parameter: Limit Value

Symbol	Parameter	Testcondition	Value	Unit
I <sub>PP</sub>	Impulse current	10/1000 $\mu$ s	50	A
		8/200 $\mu$ s	100	A
I <sub>sm</sub>	Surge current, half-period wave per time 50HZ	220V/ $\mu$ s	25	A
T <sub>STG</sub>	storage temperature		-40~150	C
T <sub>J</sub>	Junction temperature		150	C
T <sub>I</sub>	Maximum lead bonding temperature	10s	230	C
Dvdt	on state voltage critical rising rate	67%V <sub>BR</sub>	5	KV/us

### Electrical Parameter (Ta = 25°C)

Part Number	off-state current		breakdown voltage		beadover voltage		On State voltage		Hold Current	Capacity
	I <sub>RM</sub>	V <sub>RM</sub>	V <sub>BR</sub>	I <sub>R</sub>	V <sub>BO</sub>	I <sub>BO</sub>	V <sub>T</sub>	I <sub>T</sub>	I <sub>H</sub>	C <sub>50VIMHZ</sub>
	Max		Min		Max	Min	Max		Min	Max
	$\mu$ A	V	V	MA	V	MA	V	A	MA	Pf
TPA62	2	56	62	1	82	300	4	1	120	100
TPA100	2	90	100	1	133	300	4	1	120	100
TPA180	2	162	180	1	240	300	4	1	120	75
TPA200	2	180	200	1	267	300	4	1	120	75
TPA220	2	198	220	1	293	300	4	1	120	75
TPA240	2	216	240	1	320	300	4	1	120	75
TPA270	2	243	270	1	360	300	4	1	120	75



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Note: The surge of TPA type solid Arrestor  
Complies with the following standards.

CCITTK17-K20	10/700 $\mu$ s	1.5KV
	5/310 $\mu$ s	38A
VDE0433	10/700 $\mu$ s	2KV
	5/200 $\mu$ s	50A
CENT	0.5/700 $\mu$ s	1.5KV
	0.2/310 $\mu$ s	38A

3. Packaging Mode: Lead pin plastic capsulation

4. Outline :

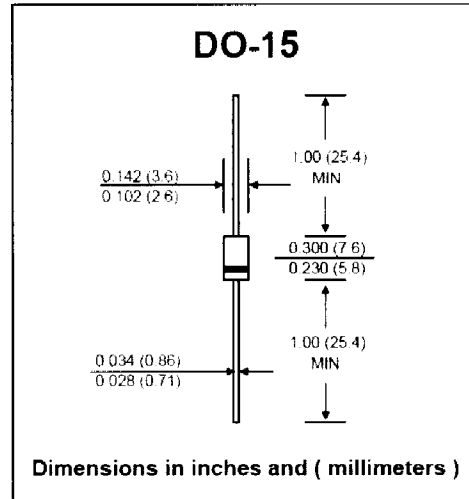


Table 1 Electrical characteristics-definitions (T=25°C)

Symbol	Parameter
$V_{RM}$	Stand-off voltage
$V_{BR}$	Breakdown voltage
$V_{BO}$	Breakover voltage
$I_{RM}$	Leakage current
$I_{PP}$	Peak pulse current
$I_{BO}$	Breakover current
$I_H$	Holding current
$V_R$	Continuous reverse voltage
$I_R$	Leakage current at $V_R$
C	Capacitance

Figure 1. Pulse waveform (10/1000  $\mu$ s)

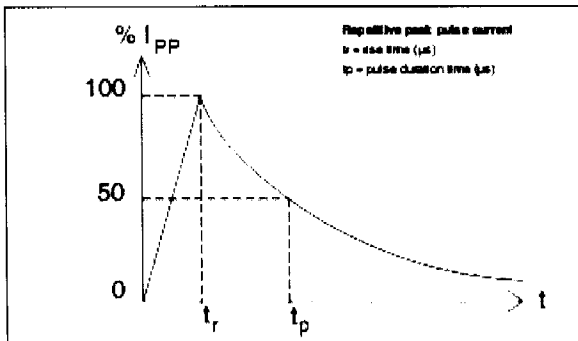


Figure 2. Non repetitive surge peak on-state current versus overload duration

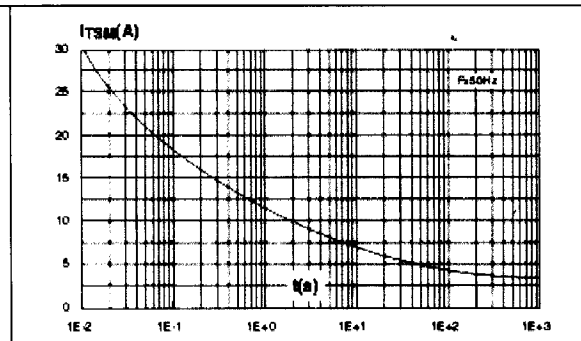


Figure 3. On-state voltage versus on-state current (typical values)

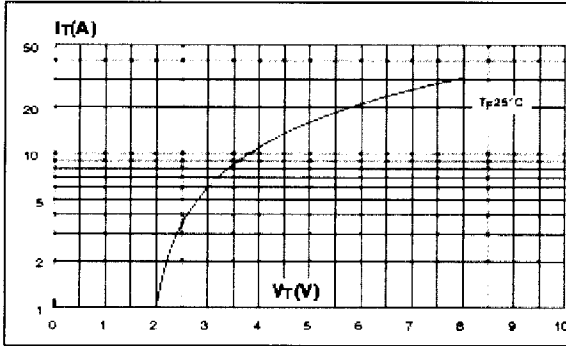


Figure 4. Relative variation of holding current versus junction temperature

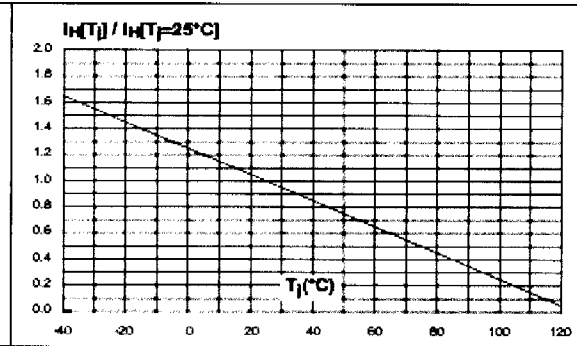


Figure 5. Relative variation of breakover voltage versus junction temperature

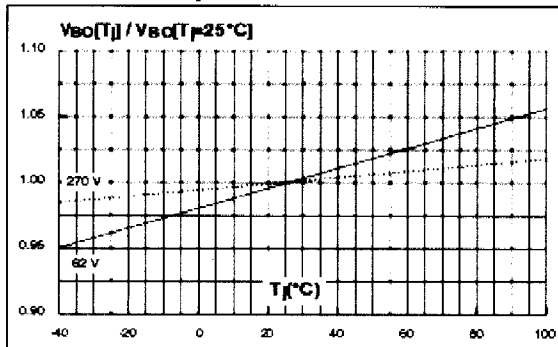


Figure 6. Relative variation of leakage current versus reverse voltage applied (typical values)

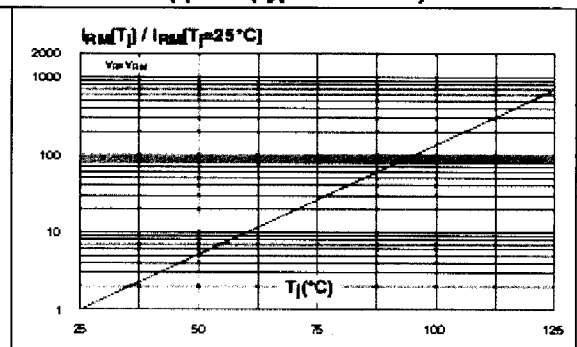


Figure 7. Variation of thermal impedance junction to ambient versus pulse duration (Printed circuit board FR4,  $S_{Cu} = 35 \mu\text{m}$ , recommended pad layout)

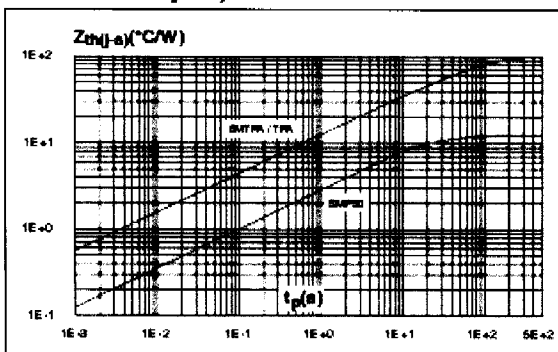
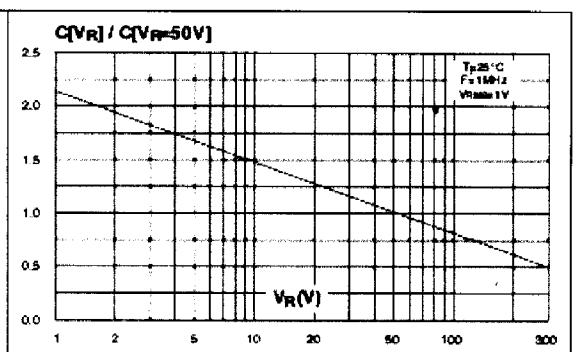
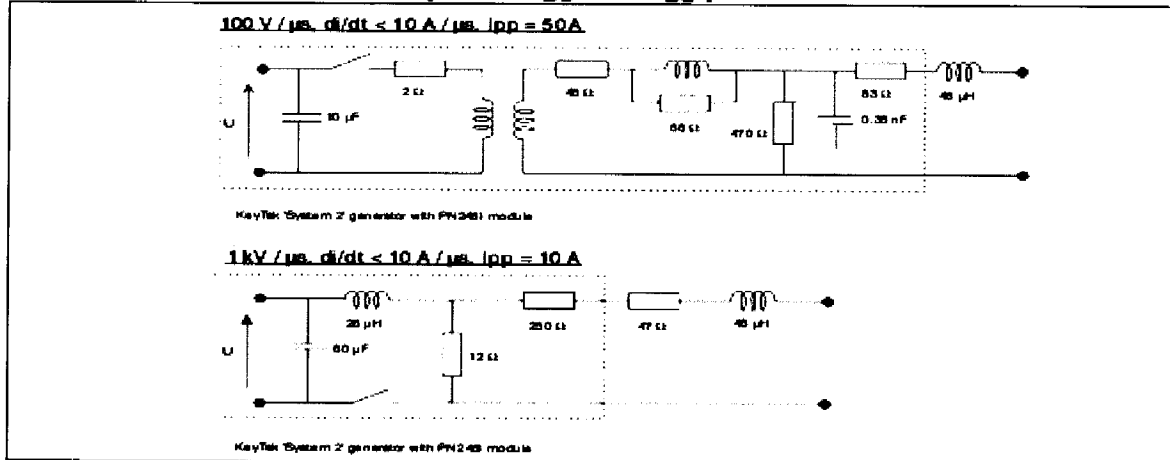


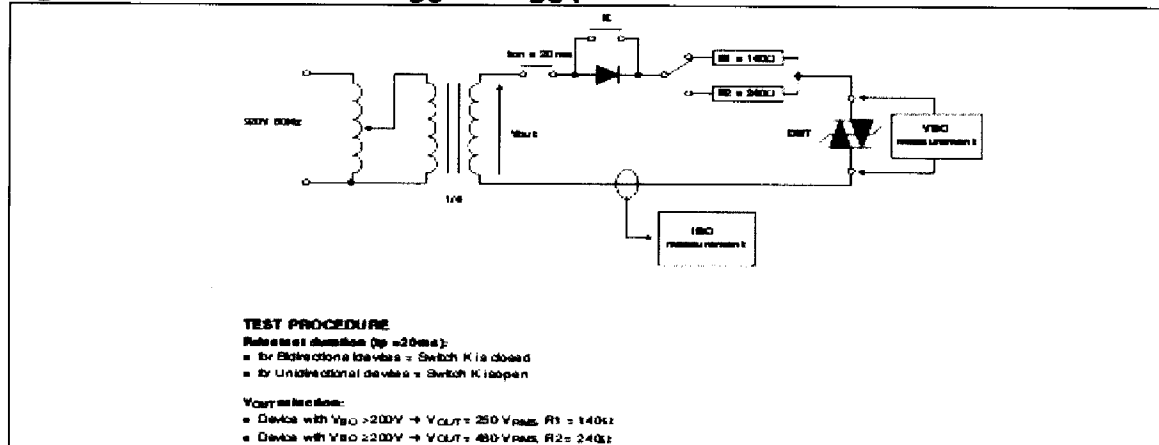
Figure 8. Relative variation of junction capacitance versus reverse voltage applied (typical values)



**Figure 9. Test circuit 1 for Dynamic  $I_{BO}$  and  $V_{BO}$  parameters**



**Figure 10. Test circuit 2 for  $I_{BO}$  and  $V_{BO}$  parameters**



**Figure 11. Test circuit 3 for dynamic  $I_H$  parameters**

