











TMP709-Q1

SBOS829-DECEMBER 2016

# TMP709-Q1 Automotive, Resistor-Programmable Temperature Switch in SOT Package

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
    Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Threshold Accuracy:
  - ±0.5°C Typical
  - ±3.5°C Maximum (60°C to 100°C)
- Temperature Threshold Set By 1% External Resistor
- Low Quiescent Current: 40 μA Typical
- · Open-Drain, Active-Low Output Stage
- Pin-Selectable 2°C or 10°C Hysteresis
- Reset Operation Specified at V<sub>CC</sub> = 0.8 V
- Supply Range: 2.7 V to 5.5 V
- Package: 5-Pin SOT-23

## 2 Applications

- Computers (Laptops and Desktops)
- Servers
- · Industrial and Medical Equipment
- Storage Area Networks
- Automotive

## 3 Description

The TMP709-Q1 is a fully-integrated, resistor-programmable temperature switch with a temperature threshold that is set by just one external resistor within the entire operating range. The TMP709-Q1 provides an open-drain, active-low output and has a 2.7-V to 5.5-V supply-voltage range.

The temperature threshold accuracy is typically  $\pm 0.5^{\circ}$ C, with a maximum of  $\pm 3.5^{\circ}$ C (60°C to 100°C). The quiescent current consumption is typically 40  $\mu$ A. Hysteresis is pin-selectable to 2°C or 10°C.

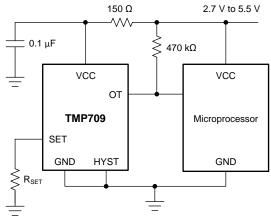
The TMP709-Q1 is available in a 5-pin, SOT-23 package.

### **Device Information**(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP709-Q1	SOT-23 (5)	2.90 mm x 1.60 mm

 For all available packages, see the package option addendum at the end of the datasheet.

## **Typical Application**



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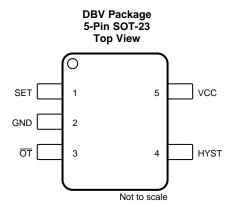
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# 4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

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# **5 Pin Configuration and Functions**



**Pin Functions** 

Pl	PIN TYPE		DESCRIPTION
NAME	NO.	ITPE	DESCRIPTION
GND	2	Analog power	Device ground
HYST	4	Digital input	Hysteresis selection. For 10°C, HYST = VCC; for 2°C, HYST = GND.
ŌT	3	Digital output	Open-drain, active low output
SET	1	Analog input	Temperature set point. Connect an external 1% resistor between SET and GND.
VCC	5	Analog power	Power-supply voltage (2.7 V to 5.5 V)

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### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
	Supply, VCC	-0.3	6	
Voltage	Input, SET and HYST	-0.3	V <sub>CC</sub> + 0.3	V
	Output, OT	-0.3	6	
Current	Input		20	Λ
	Output		20	mA
Temperature	Operating, T <sub>A</sub>	-40	125	
	Junction, T <sub>J</sub>		150	°C
	Storatge, T <sub>stg</sub>	-65	150	

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge		Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	V

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
$V_{CC}$	Supply voltage	2.7	5.5	V
T <sub>A</sub>	Operating temperature	0	125	°C

### 6.4 Thermal Information

		TMP709-Q1	
	THERMAL METRIC <sup>(1)</sup>	DBV (SOT-23)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	217.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	4.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	43.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



## 6.5 Electrical Characteristics

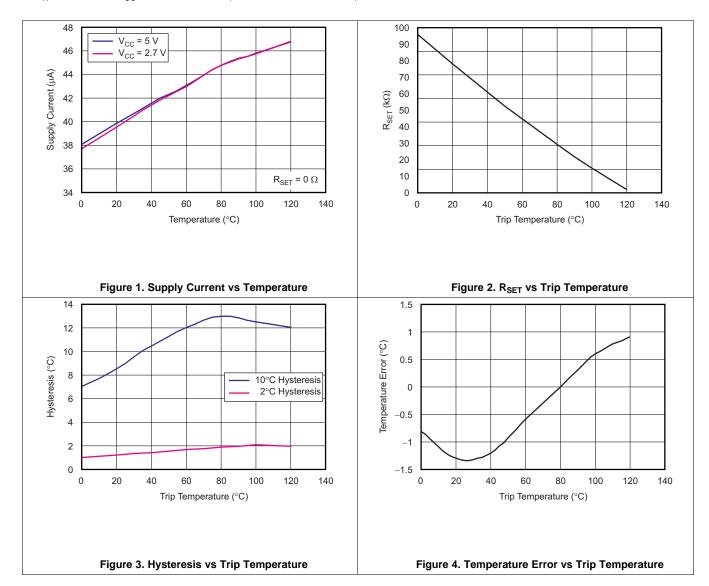
at  $T_A$  = 0°C to 125°C and  $V_{CC}$  = 2.7 V to 5.5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER S	UPPLY					
		V <sub>CC</sub> = 5 V		40	55	μΑ
I <sub>CC</sub> Supply current	V <sub>CC</sub> = 2.7 V		40	55	μΑ	
TEMPERA	TURE				·	
T <sub>E</sub>	Temperature error	T <sub>A</sub> = 60°C to 100°C		±0.5	±3.5	°C
DIGITAL II	NPUT (HYST)				·	
V <sub>IH</sub>	High-level input voltage		0.7 × V <sub>CC</sub>			V
V <sub>IL</sub>	Low-level input voltage				0.3 × V <sub>CC</sub>	V
C <sub>IN</sub>	Input capacitance			10		pF
ANALOG	NPUT (SET)				·	
V <sub>IN</sub>	Input voltage range		0		V <sub>CC</sub>	V
I <sub>lkg_in</sub>	Input leakage current			1		μΑ
DIGITAL C	PEN-DRAIN OUTPUT (OT)		•			
I <sub>(OT_SINK)</sub>	Output sink current	V <sub>OT</sub> = 0.3 V	5	12		mA
I <sub>lkg(OT)</sub>	Output leakage current	$V_{OT} = V_{CC}$		1		μΑ

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## 6.6 Typical Characteristics

at  $T_A = 25$ °C and  $V_{CC} = 2.7$  V to 5.5 V (unless otherwise noted)



### 7 Detailed Description

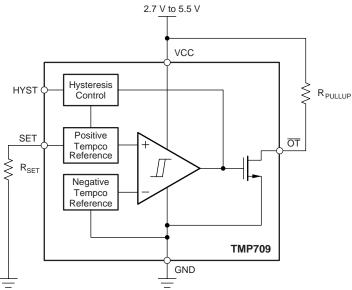
#### 7.1 Overview

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The TMP709-Q1 is a fully-integrated, resistor-programmable temperature switch that incorporates two temperature-dependent voltage references and one comparator. One voltage reference exhibits a positive temperature coefficient (tempco), and the other voltage reference exhibits a negative tempco. The temperature at which both voltage references are equal determines the temperature trip point.

The Functional Block Diagram shows the comparator, the NFET open-drain device connected to the  $\overline{\text{OT}}$  pin, the positive tempco reference using the external R<sub>SET</sub> resistor, the negative tempco reference, and the hysteresis control. The voltage of the positive tempco reference is controlled by external resistor R<sub>SET</sub>.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

### 7.3.1 Temperature Switch

The TMP709-Q1 temperature threshold is programmable from 0°C to 125°C and is set by an external 1% resistor from the SET pin to the GND pin. The TMP709-Q1 has an open-drain, active-low output structure that easily interfaces with a microprocessor.

The TMP709-Q1 reaches the temperature trip point when the voltage from the positive tempco reference exceeds the voltage from the negative tempco reference. This difference causes the output of the comparator to switch from logic 0 to logic 1. The comparator output drives the gate of the NFET open-drain device, and pulls the voltage on the  $\overline{OT}$  pin from logic 1 to logic 0 under these conditions; in other words, the output *trips*. Furthermore, the logic 1 output from the comparator causes the hysteresis control to increase the voltage of the positive tempco reference by an amount set by the logic setting on the HYST pin (10°C for logic 1 on the HYST pin; 2°C for logic 0 on the HYST pin). Increase the voltage of the positive tempco reference after the TMP709-Q1 trips to stop the TMP709-Q1 from untripping (voltage on the  $\overline{OT}$  pin changing from logic 0 to logic 1) until the local temperature reduces by the amount set by the HYST pin. After the local temperature reduces, and the voltage from the positive tempco reference is less than the voltage from the negative tempco reference, the output of the comparator switches from logic 1 to logic 0. This condition causes the voltage on the  $\overline{OT}$  pin to change from logic 0 to logic 1 (device untrips).

### 7.3.2 Hysteresis Input

The HYST pin is a digital input that allows the input hysteresis to be set at either 10°C (when HYST = VCC) or 2°C (when HYST = GND). The hysteresis function keeps the  $\overline{OT}$  pin from oscillating when the temperature is near the threshold. Thus, always connect the HYST pin to either VCC or GND. Other input voltages on this pin can cause abnormal supply currents or a device malfunction.

### 7.3.3 Set-Point Resistor (R<sub>SET</sub>)

Set the temperature threshold by connecting  $R_{SET}$  from the SET pin to GND. The value of  $R_{SET}$  is determined using either Figure 2 or Equation 1:

$$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

where

T = temperature threshold in degrees Celsius.

(1)

#### 7.4 Device Functional Modes

The TMP709-Q1 device has a single functional mode. Normal operation for the TMP709-Q1 device occurs when the power-supply voltage applied across the VCC and GND pins is within the specified operating range of 2.7 V to 5.5 V.

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## 8 Applications and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TMP709-Q1 device is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1- $\mu$ F capacitor placed as close as possible to the VCC supply pin. To minimize the internal power dissipation of the TMP709-Q1 family of devices, use a pullup resistor value greater than 10 k $\Omega$  from the  $\overline{OT}$  pin to the VCC pin. See the *Hysteresis Input* section for hysteresis configuration, and the *Set-Point Resistor* ( $R_{SET}$ ) section for configuring the temperature threshold.

## 8.2 Typical Application

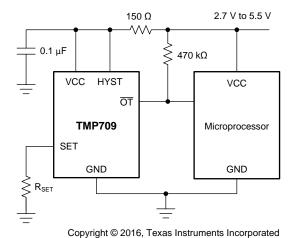


Figure 5. Overtemperature Protection for a 60°C Trip Point

### 8.2.1 Design Requirements

For this design example, a 2.7-V to 5.5-V power supply, 60°C trip point, and 10°C hysteresis are used.

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### **Typical Application (continued)**

### 8.2.2 Detailed Design Procedure

Connect the HYST pin to VCC for 10°C hysteresis. For a 60°C temperature threshold, see the *Set-Point Resistor* ( $R_{SET}$ ) section to compute an ideal  $R_{SET}$  resistor value of 44.619 k $\Omega$ . Select the closest standard value resistor available; in this case, 44.2 k $\Omega$ . Use a 10-k $\Omega$  pullup resistor from the  $\overline{OT}$  pin to the VCC pin. To minimize power, a larger-value pullup resistor can be used, but must not exceed 470 k $\Omega$ . Place a 0.1- $\mu$ F bypass capacitor close to the TMP709-Q1 device in order to reduce noise coupled from the power supply.

## 8.2.3 Application Curves

Figure 6 shows an example of the hysteresis feature. The HYST pin is connected to VCC, so the TMP709-Q1 device is configured for 10°C of hysteresis. The device is configured for a 60°C trip temperature by the R<sub>SET</sub> resistor value; therefore, the OT output asserts low when the 60°C threshold is exceeded. The OT output remains asserted low until the sensor reaches 50°C.

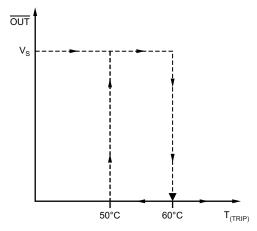


Figure 6. TMP709-Q1 Hysteresis Function

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9 Power Supply Recommendations

The TMP709-Q1 low supply current and supply range allow this device to be powered from many sources. Any significant noise on the VCC pin can result in a trip-point error. Minimize this noise by low-pass filtering the device supply ( $V_{CC}$ ) using a 150- $\Omega$  resistor and a 0.1- $\mu$ F capacitor.

### 10 Layout

### 10.1 Layout Guidelines

The TMP709-Q1 is extremely simple to lay out. Figure 7 shows the recommended board layout.

### 10.2 Layout Example

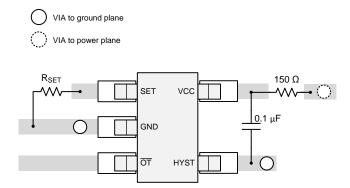


Figure 7. Recommended Layout

### 10.3 Thermal Considerations

The TMP709-Q1 quiescent current is typically 40  $\mu$ A. The device dissipates negligible power when the output drives a high-impedance load. Thus, the die temperature is the same as the package temperature. In order to maintain accurate temperature monitoring, provide a good thermal contact between the TMP709-Q1 package and the device being monitored. The rise in die temperature as a result of self-heating is given by Equation 2:

$$\Delta T_J = P_{DISS} \times \theta_{JA}$$

where

• P<sub>DISS</sub> = power dissipated by the device.

•  $\theta_{JA}$  = package thermal resistance. Typical thermal resistance for SOT-23 package is 217.9°C/W. (2)

To limit the effects of self-heating, keep the output current at a minimum level.

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### 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

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### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGE OPTION ADDENDUM

23-Dec-2016

### PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TMP709AQDBVRQ1	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR	0 to 125	709Q	
TMP709AQDBVTQ1	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	0 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# **PACKAGE OPTION ADDENDUM**

23-Dec-2016

In no event shall TI's liabilit	ty arising out of such information exceed the total	purchase price of the TI part(s) at issue in this of	document sold by TI to Customer on an annual basis.

## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP709AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP709AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



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