TLV717P 150-mA, Low-Dropout Regulator With Foldback Current Limit for Portable Devices

1 Features

- Very Low Dropout: 215 mV at 150 mA
- Accuracy: 0.5% (typical)
- Low I_Q: 35 µA
- Available in Fixed-Output Voltages: 1.2 V to 5 V
- High PSRR:
  - 70 dB at 1 kHz
  - 50 dB at 1 MHz
- Stable With Effective Output Capacitance: 0.1 µF
- Foldback Current Limit
- Package: 1-mm × 1-mm DQN

(1) See the Package Option Addendum at the end of this document for a complete list of available voltage options.

(2) See *Input and Output Capacitor Requirements* for more details.

2 Applications

- PCs and Notebooks
- Smart Phones
- Portable Electronics and Battery-Powered Devices
- Electronic Point of Sale

3 Description

The TLV717P series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 0.5%.

The TLV717P series offer current foldback that throttles down the output current with a decrease in load resistance. The typical value at which current foldback initiates is 350 mA; the typical value of the output short current limit value is 40 mA.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

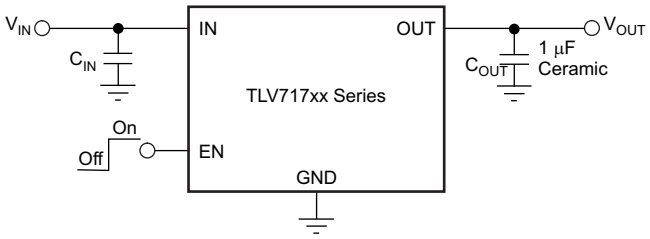
The TLV717P series is available in a 1-mm × 1-mm DQN package that makes them ideal for hand-held applications. The TLV717P provides an active pulldown circuit to quickly discharge output loads.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV717P	X2SON (4)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2012) to Revision B — **Page**

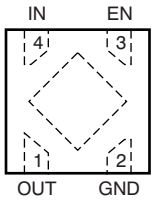
- Deleted all instances of TLV717xx; Replaced with generic part number, TLV717P ... 1
- Updated *Applications*. ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed T_J = –25°C to T_J = 25°C in the conditions statement in *Absolute Maximum Ratings* ... 4
- Changed T_A to T_J throughout *Electrical Characteristics* ... 5
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* ... 6
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* ... 7
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* ... 8
- Changed junction temperature range from –40°C to 125°C to –40°C to 85°C in *Overview* ... 9
- Deleted TLV717xx functional block diagram ... 9

Changes from Original (October 2011) to Revision A — **Page**

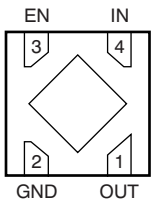
- Changed document status from Product Preview to Production Data ... 1

5 Pin Configuration and Functions

DQN Package
4-Pin X2SON
Top View



DQN Package
4-Pin X2SON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	—	Ground pin
IN	4	I	Input pin. A small capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application and Implementation* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application and Implementation* for more details.
Thermal pad	—	—	Connect to GND for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = 25°C, unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input range, V_{IN}	–0.3	6	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	
	Output range, V_{OUT}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation, P_{DISS}		See *Thermal Information*		
Temperature	Junction, T_J	–55	150	°C
	Storage junction, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1.7	5.5	V
V_{OUT}	Output voltage	1.2	5	V
I_{OUT}	Output current	0	150	mA
V_{EN}	Enable pin voltage	0	V_{IN}	V
T_J	Junction temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC		TLV717P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	393.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	140.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	330	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	329	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	147.5	°C/W

6.5 Electrical Characteristics

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.7		5.5	V
V_{OUT}	Output voltage range			1.2		5	V
I_{OUT}	Output current			150			mA
	DC output accuracy	T_J = +25°C			0.5%		
		V_{OUT} ≥ 1.2 V, –40°C ≤ T_J ≤ +85°C		–1.5%		1.5%	
		V_{OUT} ≤ 1.2 V				25	mV
$\Delta V_O/V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	20	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.5 V		330	500	mV
			1.5 V ≤ V_{OUT} < 1.8 V		330	450	
			1.8 V ≤ V_{OUT} ≤ 5 V		215	350	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			35	55	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V			0.1	0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 10 Hz		70		dB
			f = 100 Hz		70		
			f = 1 kHz		65		
			f = 10 kHz		60		
			f = 100 kHz		43		
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Start-up time	C_{OUT} = 1 µF, I_{OUT} = 150 mA			100		µs
I_{SC}	Short current limit	V_{IN} = min ($V_{OUT(NOM)}$ + 1 V, 5.5 V), V_{OUT} = 0 V			40		mA
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pulldown resistor				120		Ω
UVLO	Undervoltage lockout	V_{IN} rising			1.6		V

6.6 Typical Characteristics

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

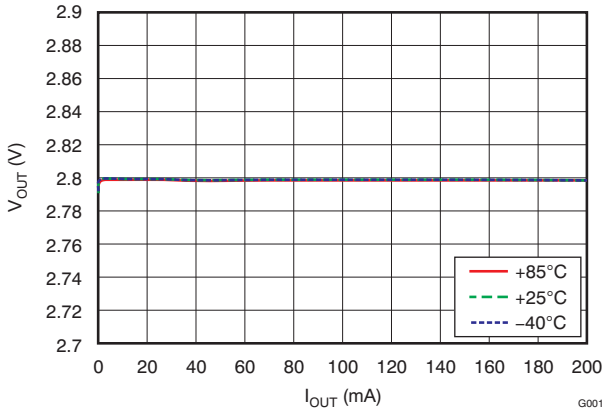


Figure 1. Load Regulation

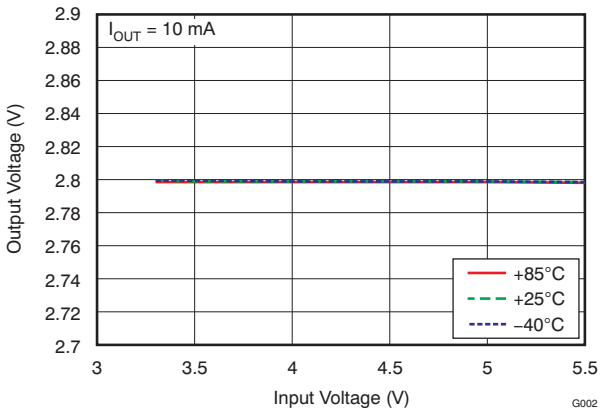


Figure 2. Line Regulation

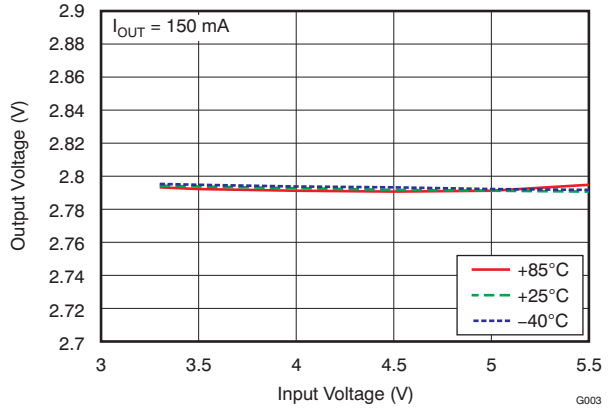


Figure 3. Line Regulation

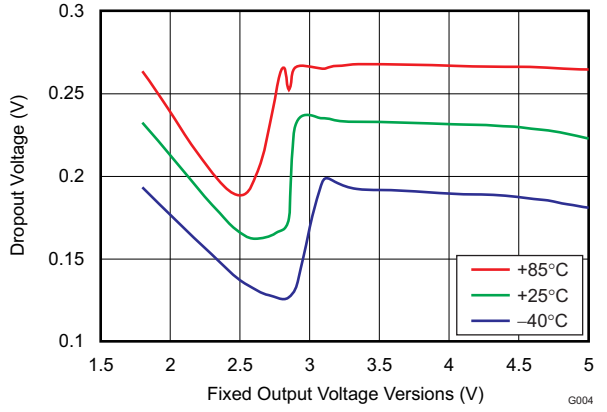


Figure 4. Dropout Voltage vs Fixed Output Voltage Versions

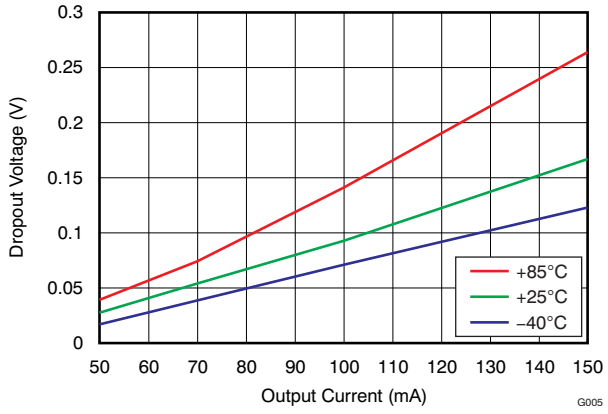


Figure 5. Dropout Voltage vs Output Current

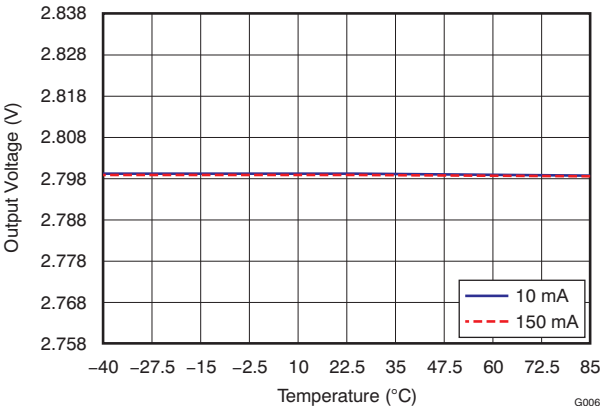


Figure 6. Output Voltage vs Temperature

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

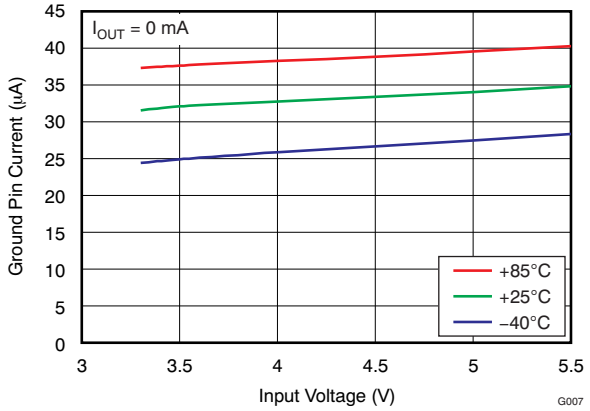


Figure 7. Ground Pin Current vs Input Voltage

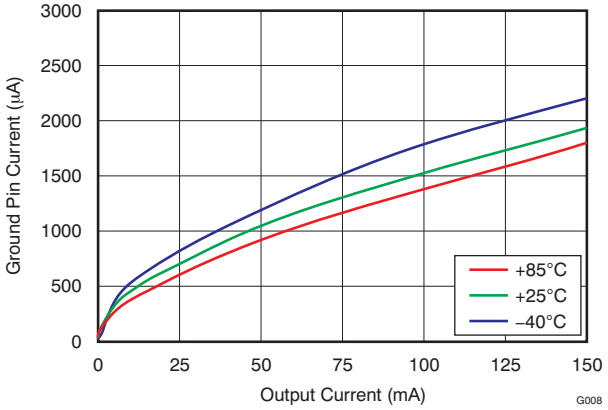


Figure 8. Ground Pin Current vs Output Current

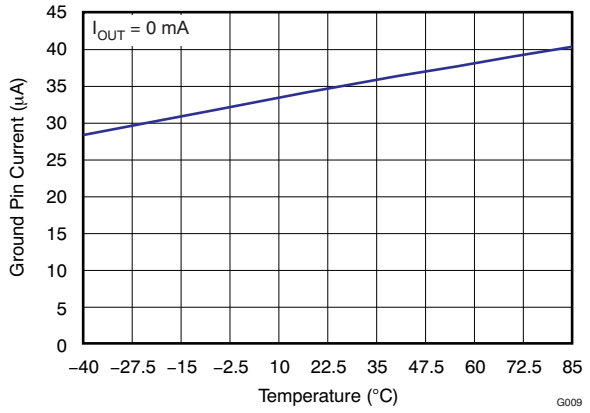


Figure 9. Ground Pin Current vs Temperature

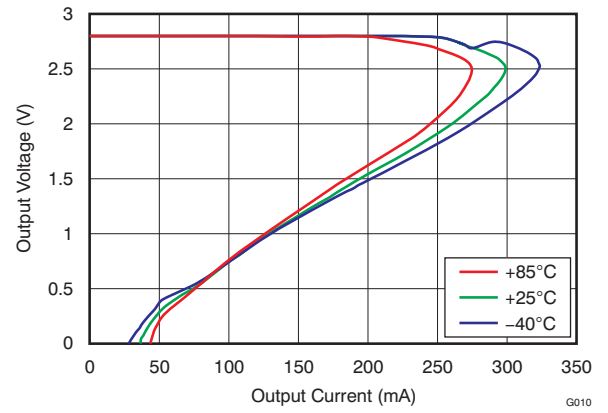


Figure 10. Output Voltage vs Output Current

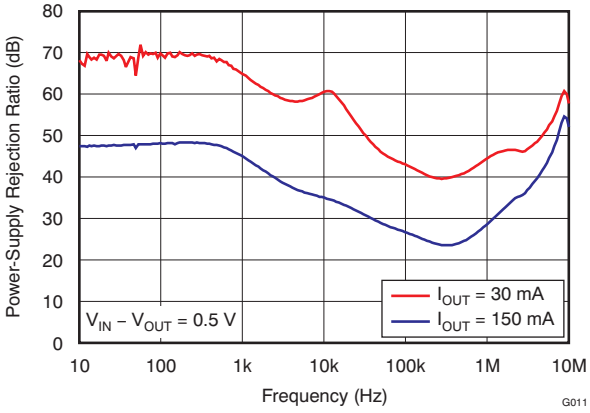


Figure 11. TLV71728PSRR vs Frequency

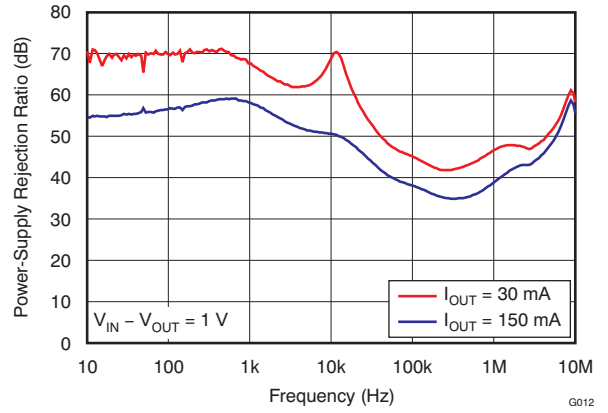


Figure 12. TLV71728PSRR vs Frequency

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

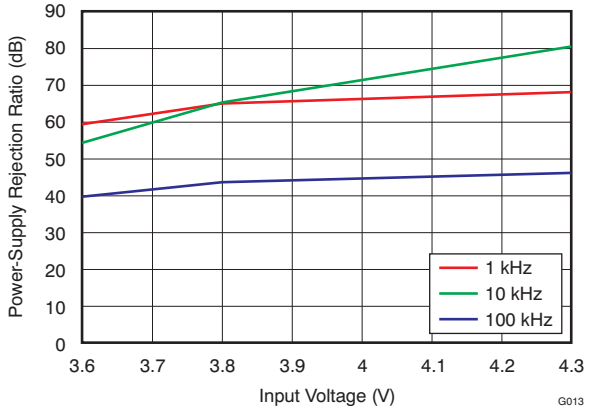


Figure 13. PSRR vs Input Voltage

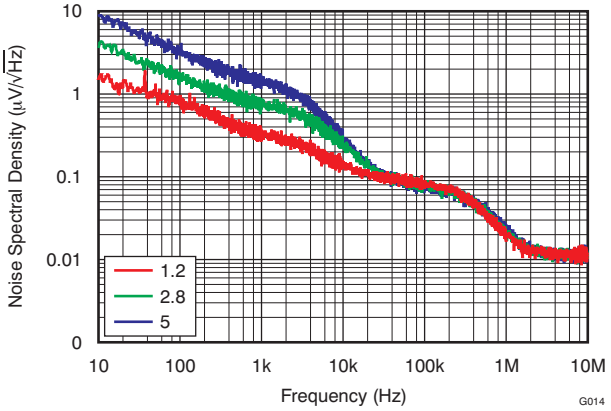


Figure 14. Output Spectral Noise Density vs Frequency

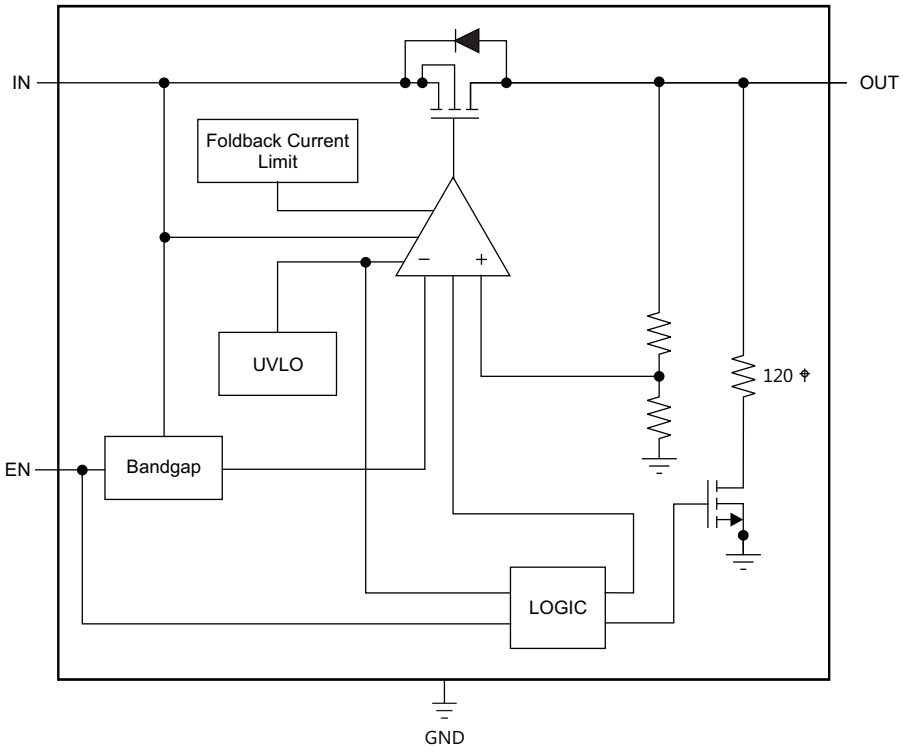
7 Detailed Description

7.1 Overview

The TLV717P belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current foldback. Device operating junction temperature is –40°C to 85°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV717P has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The advantage of foldback current limit is that the I_{LIMIT} value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates [($V_{IN} – V_{OUT}$) × I_{LIMIT}] is much less.

The TLV717P PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.3 Undervoltage Lockout (UVLO)

The TLV717P uses an undervoltage lockout circuit (UVLO = 1.6 V) to keep the output shut off until the internal circuitry operates properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	V_{EN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT}(nom) + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}(nom) + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV717P is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers a foldback current limit. The operating junction temperature of this device series is –40°C to 85°C.

8.2 Typical Application

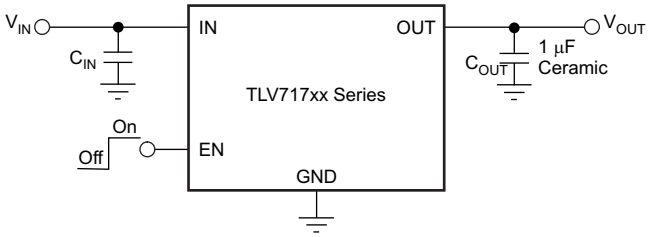


Figure 15. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the parameters for this application.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	2.8 V ±1%
Output current	30 to 150 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

TI recommends X5R- and X7R-type ceramic capacitors because they have minimal variation in value and equivalent series resistance (ESR) over temperature. The TLV717P is designed to be stable with an effective capacitance of 0.1 µF or larger at the output, though TI recommends a 1-µF ceramic capacitor for typical applications. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications. Using a 0.1-µF rated capacitor at the LDO output does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

8.2.2.2 Dropout Voltage

The TLV717P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves

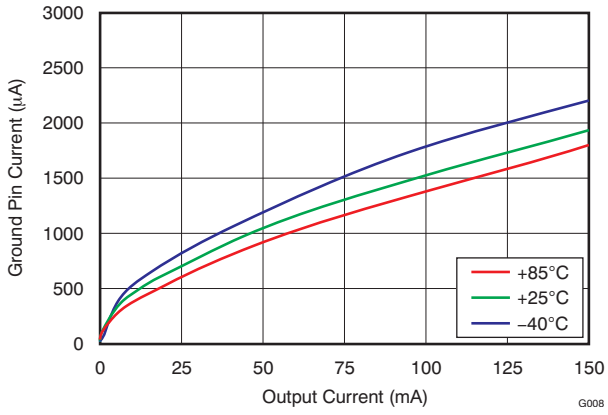


Figure 16. Ground Pin Current vs Output Current

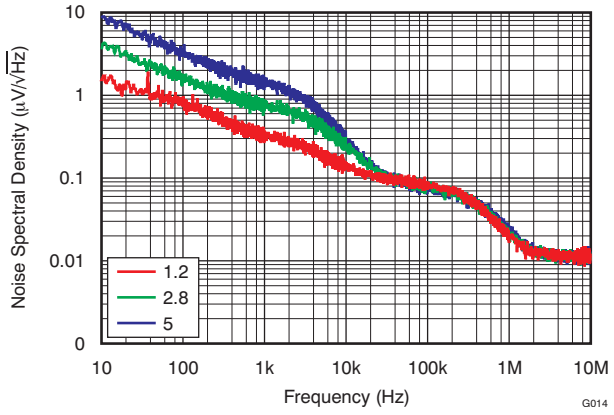


Figure 17. Output Spectral Noise Density vs Frequency

9 Power Supply Recommendations

Connect a low-output impedance power supply directly to the IN pin of the TLV717P. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.2 Layout Example

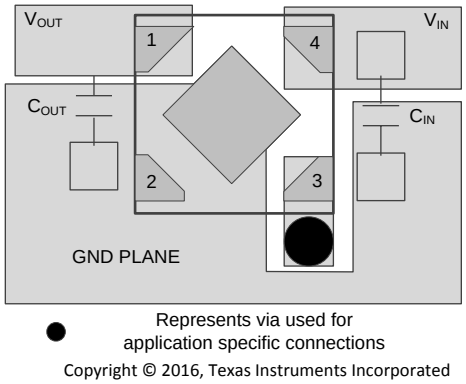


Figure 18. Recommended Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV717P. SLVU553 details the design kits and evaluation modules for TLV71733PEVM-072.

The EVM can be requested at the Texas Instruments website through the TLV717P product folder, or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

PRODUCT	V_{OUT}
TLV717**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** indicates an active output discharge feature. All members of TLV717P family will actively discharge the output when the device is disabled. **YYY** is the package designator. **Z** is the package quantity. R is for 3000 pieces, T is for 250 pieces.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

TLV71733PEVM-072 Evaluation Module user guide, SLVU553

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71712PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNR3	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71713PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71713PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71715PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV71715PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV717185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV717185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV71718PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71718PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71721PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71721PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71725PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71725PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71727PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV71727PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV717285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VE	Samples
TLV717285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VE	Samples
TLV71728PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNR3	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71729PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71729PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71730PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71730PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71733PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71733PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71736PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH	Samples
TLV71736PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

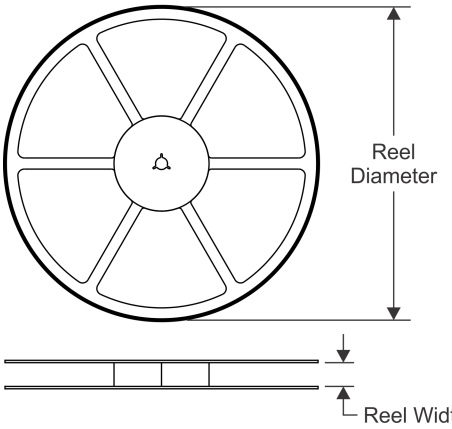
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

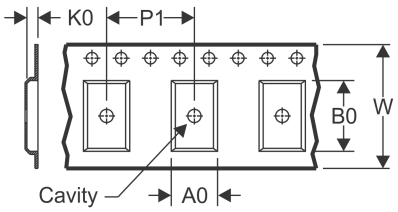
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

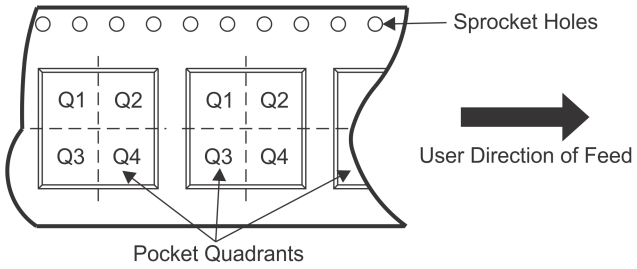


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

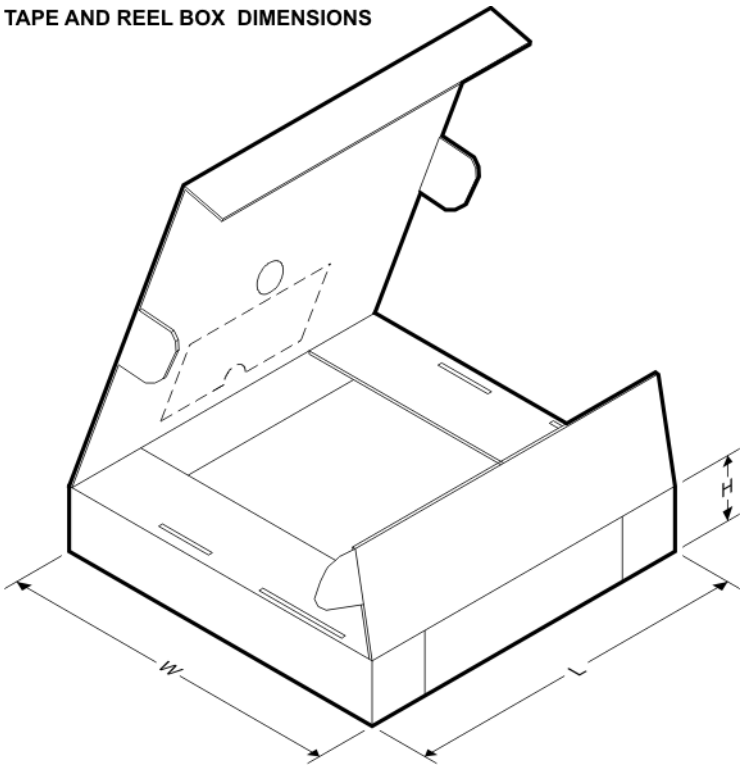


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71712PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

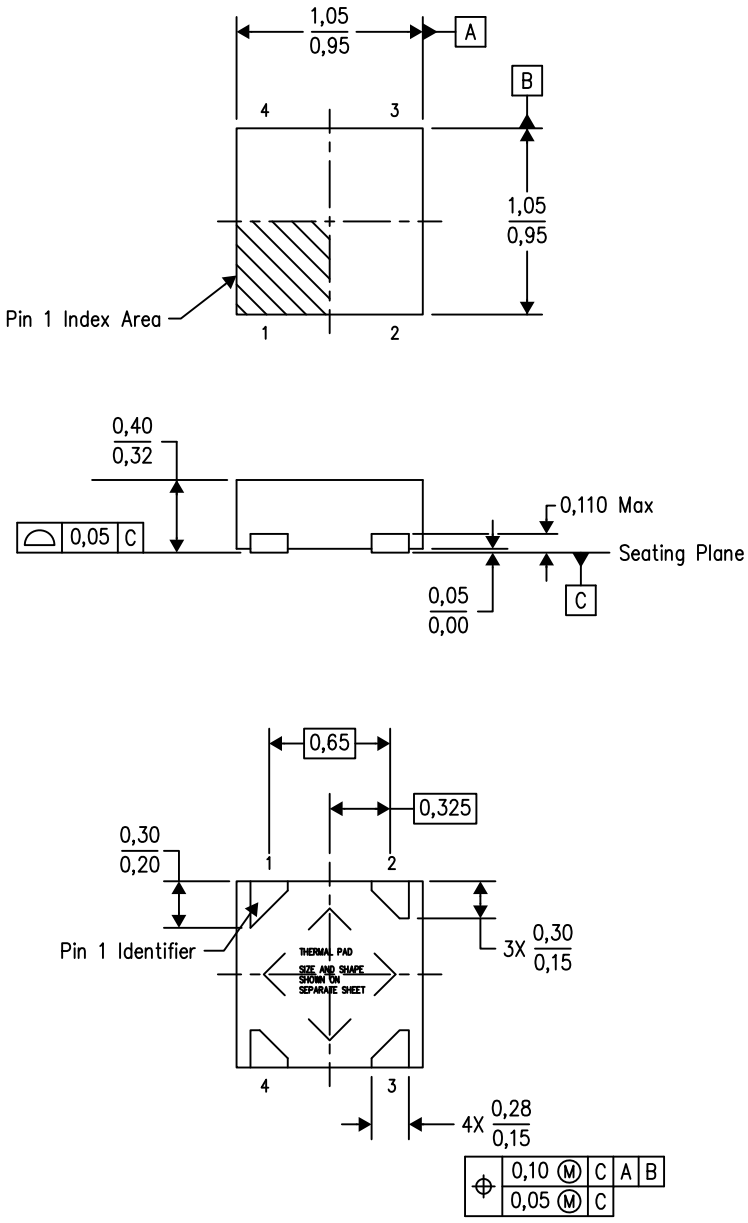


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71712PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71712PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71712PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71713PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71713PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71713PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71713PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71715PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71715PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV717185PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV717185PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717185PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71721PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71721PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71721PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71721PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71725PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71725PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71727PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71727PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71727PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71727PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV717285PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV717285PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717285PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71728PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71728PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71730PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71730PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71730PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71733PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71736PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71736PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71736PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71736PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

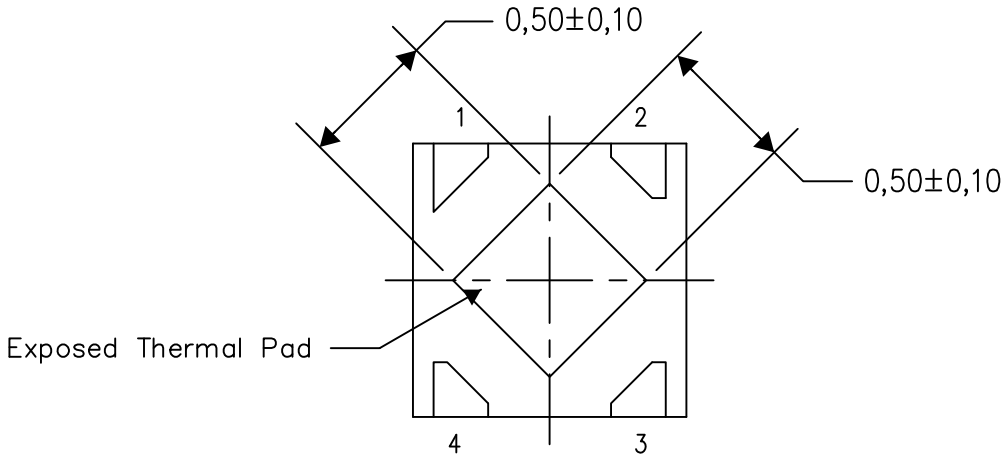
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



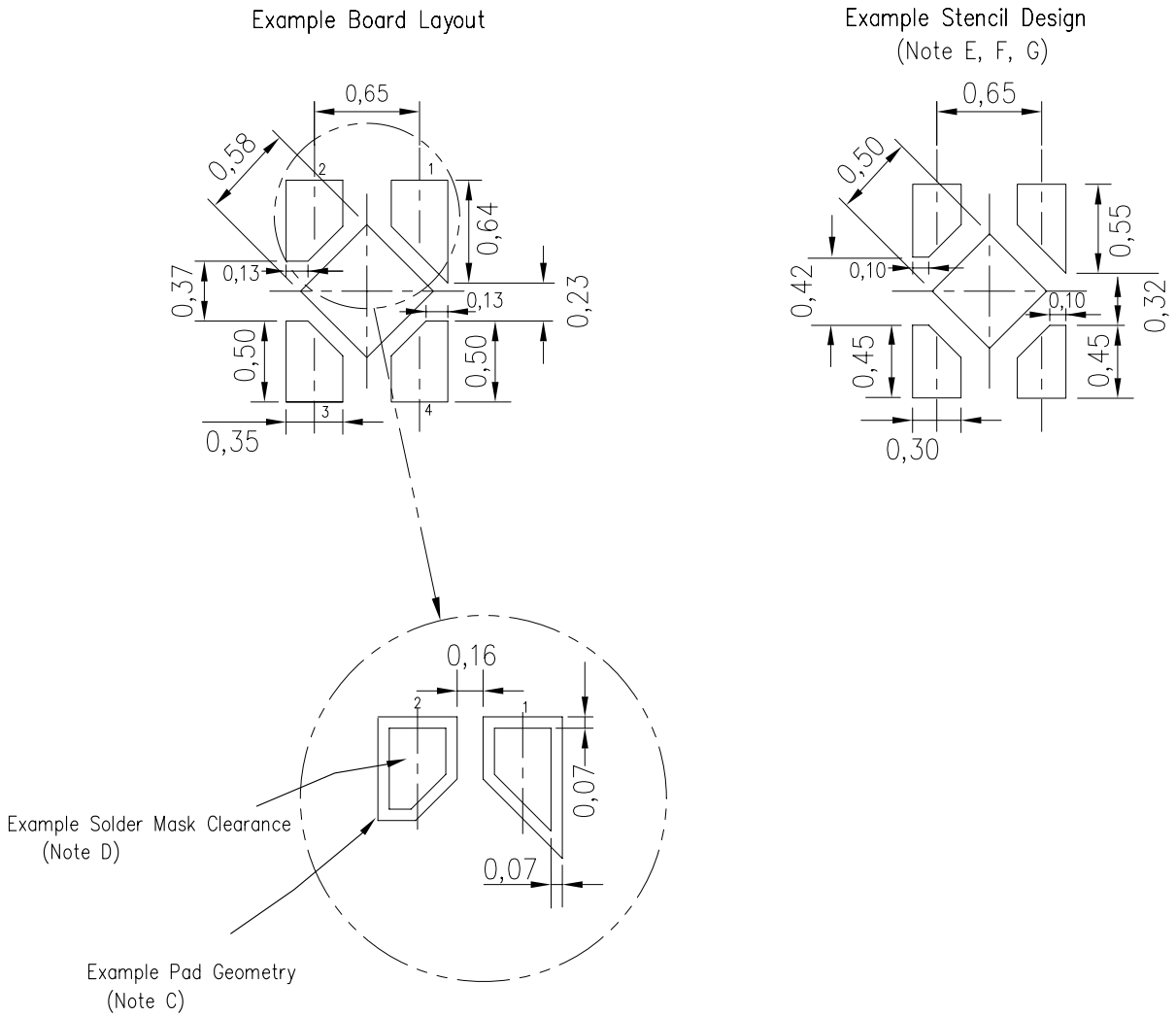
Bottom View

Exposed Thermal Pad Dimensions

4210393–2/F 05/15

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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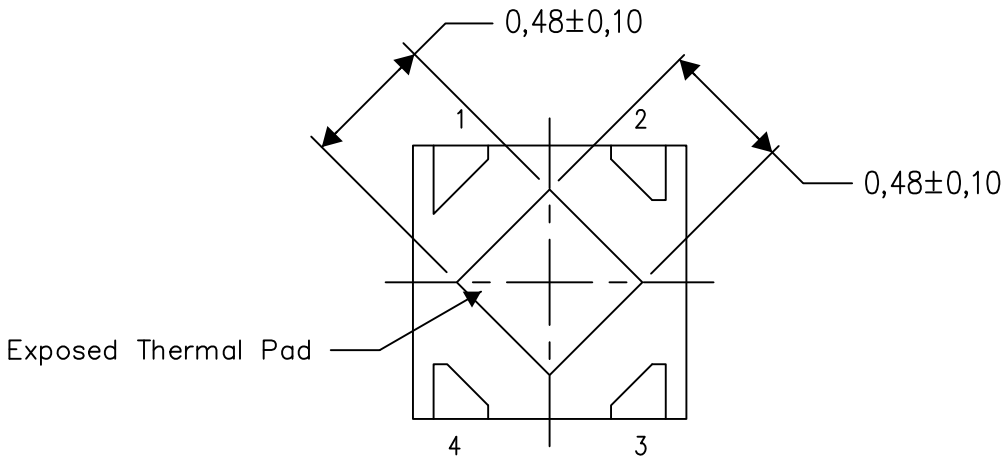
The exposed thermal pad dimensions for this package are shown in the following illustration.



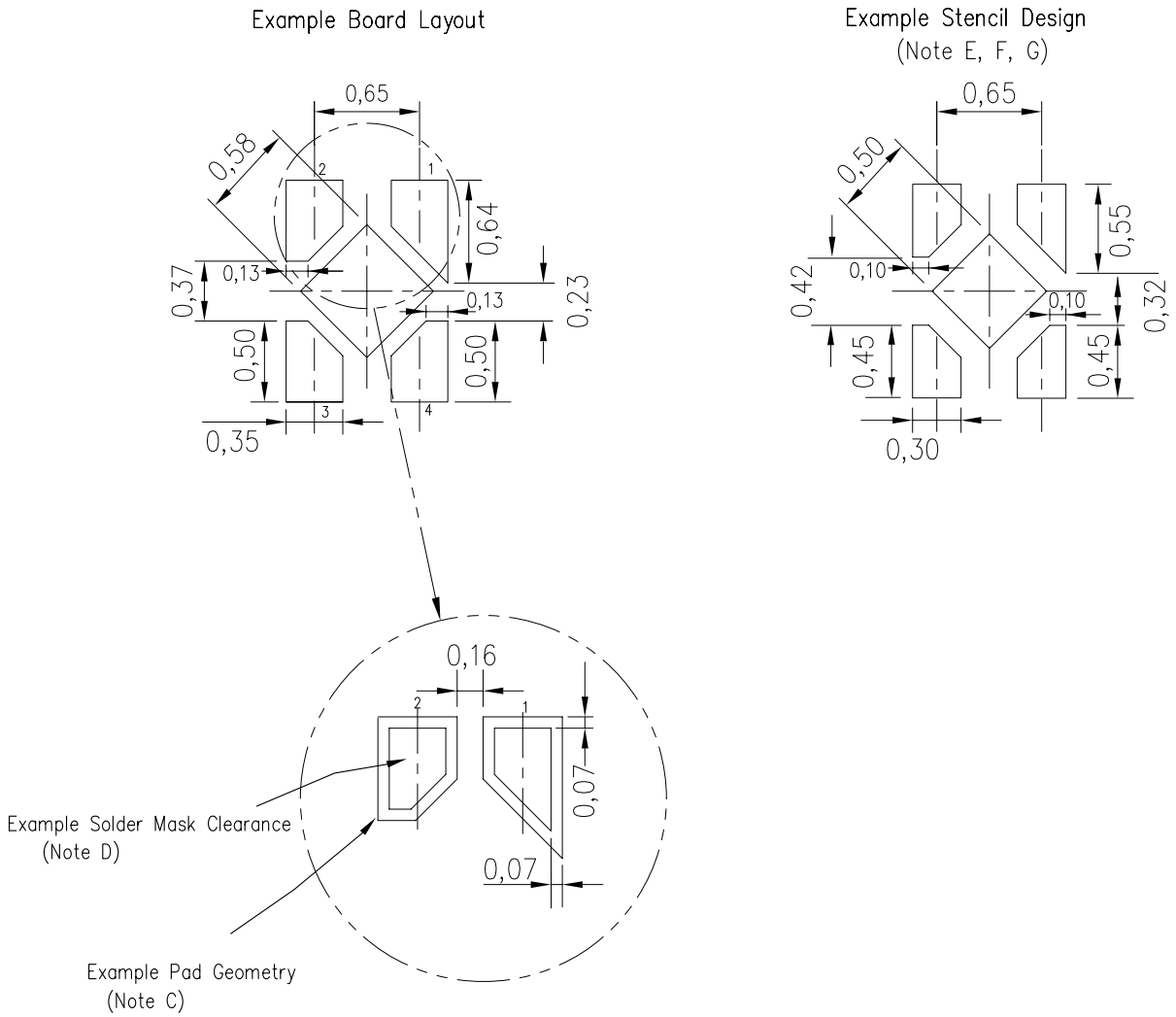
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/F 05/15

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
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G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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