TLVx369 Cost-Optimized, 800-nA, 1.8-V, Rail-to-Rail I/O Operational Amplifier with Zero-Crossover Distortion

1 Features

- Cost-Optimized Precision Amplifier *nano*Power: 800 nA/Ch (Typ)
- Low Offset Voltage: 400 µV (Typ)
- Rail-to-Rail Input and Output
- Zero-Crossover Distortion
- Low Offset Drift: 0.5 µV/°C (Typ)
- Gain-Bandwidth Product: 12 kHz
- Supply Voltage: 1.8 V to 5.5 V
- *micro*Size Packages: SC70-5, VSSOP-8

2 Applications

- Blood Glucose Meters
- Test Equipment
- Low-Power Sensor Signal Conditioning
- Portable Devices

3 Description

The TLV369 family of single and dual operational amplifiers represents a cost-optimized generation of 1.8-V nanopower amplifiers.

With the zero-crossover distortion circuitry, these amplifiers feature high linearity over the full common-mode input range with no crossover distortion, enabling true rail-to-rail input and operating from a 1.8-V to 5.5-V single supply. The family is also compatible with industry-standard nominal voltages of 3.0 V, 3.3 V, and 5.0 V.

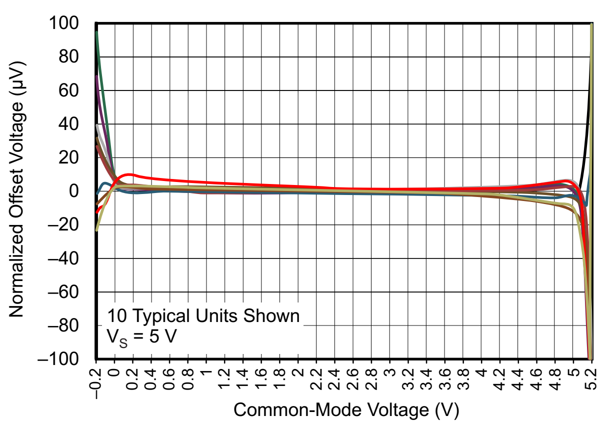
The TLV369 (single version) is offered in a 5-pin SC70 package. The TLV2369 (dual version) comes in 8-pin VSSOP and SOIC packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV369	SC70 (5)	2.00 mm × 1.25 mm
TLV2369	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TLV369 Family Eliminates Crossover Distortion Across the Full Supply Range



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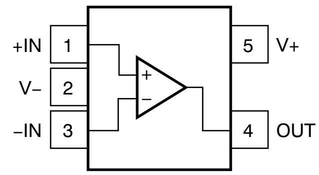
4 Revision History

DATE	REVISION	NOTES
May 2016	*	Initial release.

5 Pin Configuration and Functions

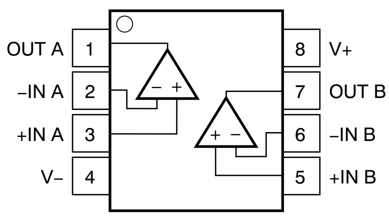
TLV369: DCK Package
5-Pin SC70
Top View



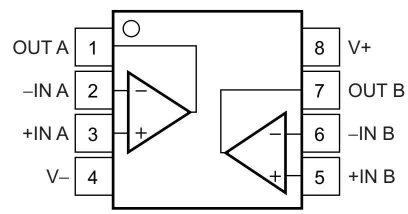
Pin Functions: TLV369

PIN		I/O	DESCRIPTION
NAME	TLV369 DCK (SC70)		
–IN	3	I	Negative (inverting) input
+IN	1	I	Positive (noninverting) input
OUT	4	O	Output
V–	2	—	Negative (lowest) power supply or ground (for single-supply operation)
V+	5	—	Positive (highest) power supply

TLV2369: D Package
8-Pin SOIC
Top View



TLV2369: DGK Package
8-Pin VSSOP
Top View



Pin Functions: TLV2369

PIN			I/O	DESCRIPTION
NAME	TLV2369			
	D (SOIC)	DGK (VSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) – (V–)	0	+7	V
	Signal input pin(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pin(2)	–10	10	mA
	Output short-circuit(3)	Continuous		mA
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to V_S / 2, one amplifier per package.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8		5.5	V
	Specified temperature	–40		85	°C

6.4 Thermal Information: TLV369

THERMAL METRIC[1]		TLV369	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: TLV2369

THERMAL METRIC[1]		TLV2369		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.5	168.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	88.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.8	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.9	87.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

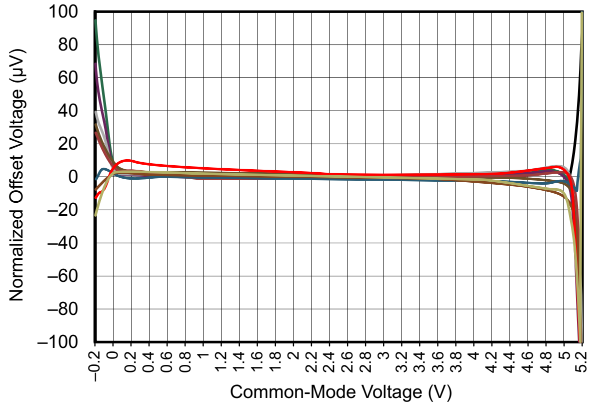
6.6 Electrical Characteristics

V_S (total supply voltage) = 1.8 V to 5.5 V; at T_A = 25°C, and R_L = 100 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	At T_A= 25°C		0.4	2	mV
		At T_A = –40°C to +85°C		0.85		
dV_{OS}/dT	Drift	At T_A = –40°C to +85°C		0.5		μV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5.5 V	80	94		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		V–		V+	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+)	80	110		dB
INPUT BIAS CURRENT						
I_B	Input bias current	At T_A= 25°C		10		pA
		At T_A= –40°C to +85°C		See Figure 8		
I_{OS}	Input offset current			10		pA
INPUT IMPEDANCE						
Z_{ID}	Differential			10^{13} || 3		Ω || pF
Z_{IC}	Common-mode			10^{13} || 6		Ω || pF
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		4		$μV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		300		nV/√Hz
i_n	Input current noise density	f = 1 kHz		1		fA/√Hz
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	At V_S = 5.5 V, 100 mV ≤ V_O ≤ (V+) – 100 mV, R_L = 100 kΩ		130		dB
		At V_S = 5.5 V, 500 mV ≤ V_O ≤ (V+) – 500 mV, R_L = 10 kΩ	80	120		
OUTPUT						
V_O	Voltage output swing from rail	R_L = 10 kΩ			25	mV
I_{SC}	Short-circuit current			10		mA
C_{LOAD}	Capacitive load drive			See Figure 10		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			12		kHz
SR	Slew rate	G = 1		0.005		V/μs
t_{OR}	Overload recovery time	V_{IN} × gain = V_S		250		μs
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current	I_O = 0 mA, at V_S = 5.5 V		800	1300	nA
TEMPERATURE						
	Specified range		–40		85	°C
T_A	Operating range		–40		125	°C

6.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, and R_L = 100 kΩ connected to V_S / 2 (unless otherwise noted)



10 typical units shown, V_S = 5 V

Figure 1. Normalized Offset Voltage vs Common-Mode Voltage

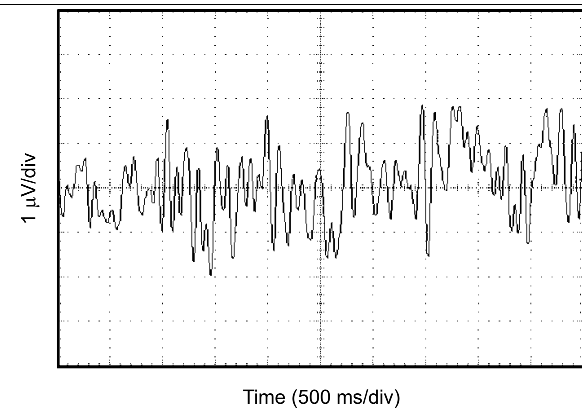
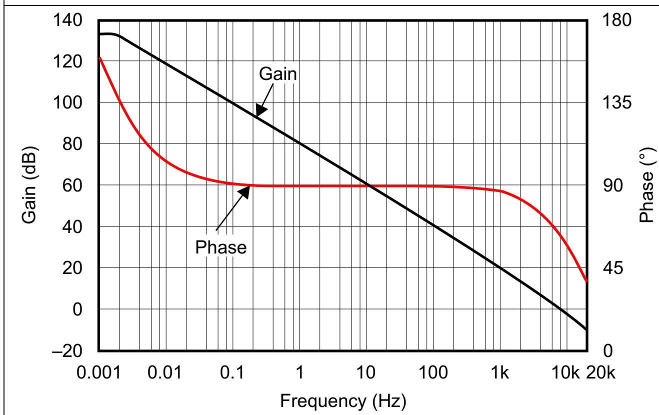


Figure 2. 0.1-Hz to 10-Hz Noise



V_S = 5.5 V

Figure 3. Open-Loop Gain and Phase vs Frequency

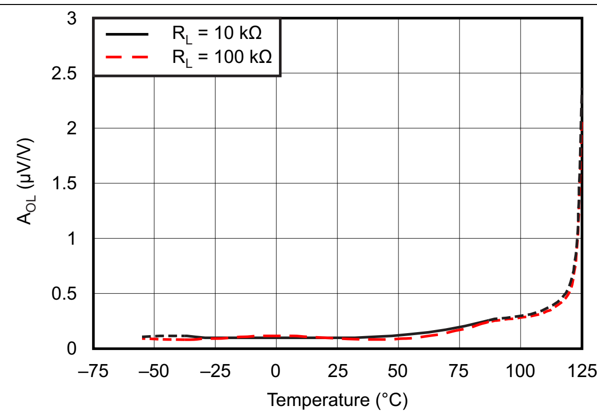


Figure 4. Open-Loop Gain vs Temperature

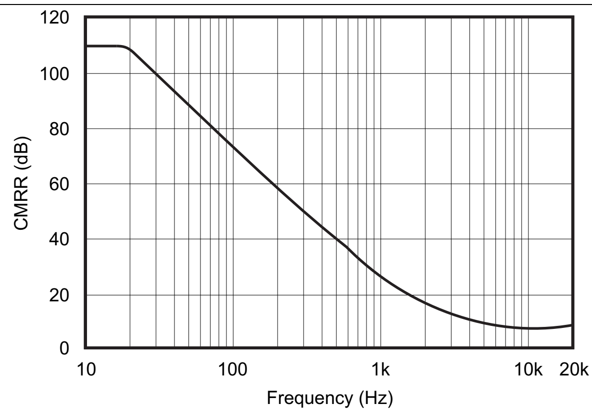


Figure 5. Common-Mode Rejection Ratio vs Frequency

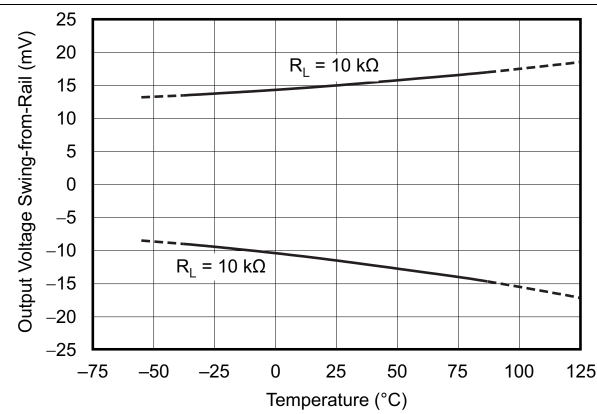


Figure 6. Output Voltage Swing from Rail vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and R_L = 100 kΩ connected to V_S / 2 (unless otherwise noted)

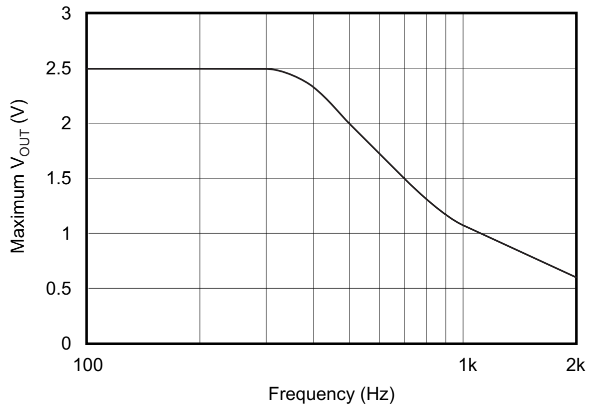


Figure 7. Maximum Output Voltage vs Frequency

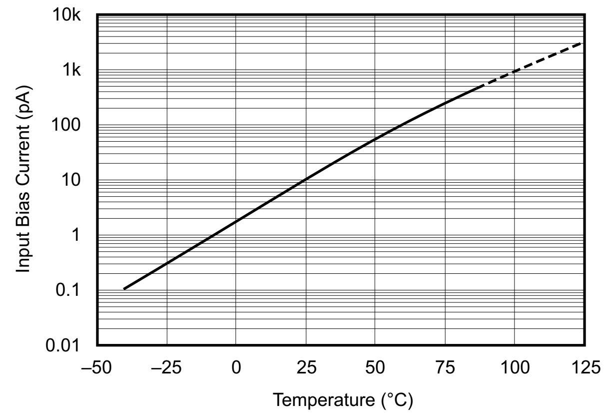


Figure 8. Input Bias Current vs Temperature

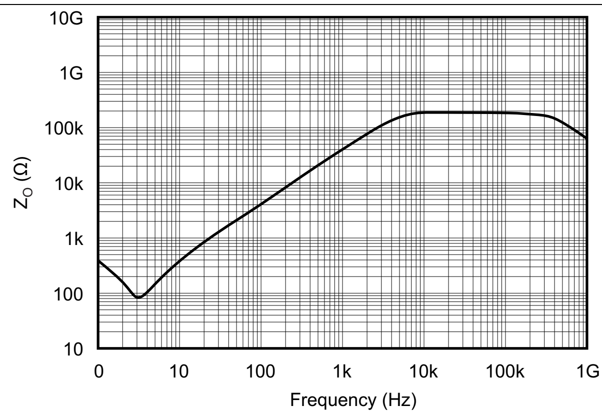


Figure 9. Open-Loop Output Impedance vs Frequency

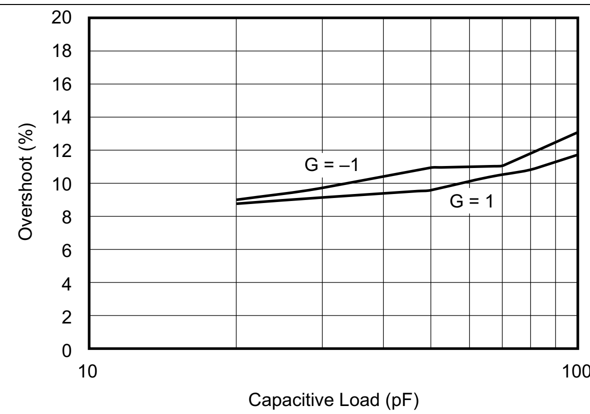
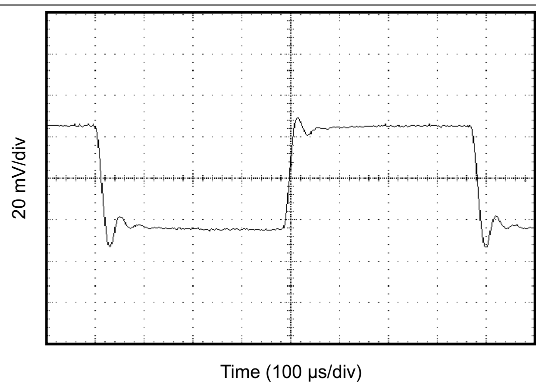


Figure 10. Small-Signal Overshoot vs Capacitive Load



C_L = 20 pF

Figure 11. Small-Signal Step Response

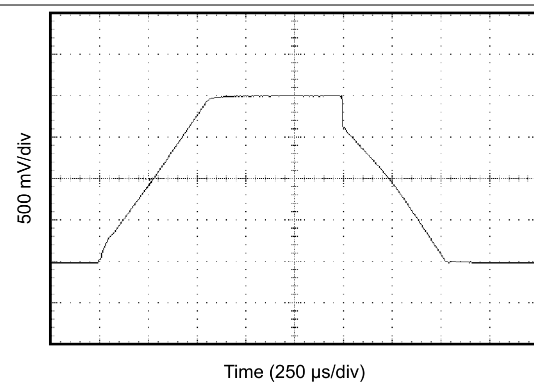


Figure 12. Large-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and R_L = 100 kΩ connected to V_S / 2 (unless otherwise noted)

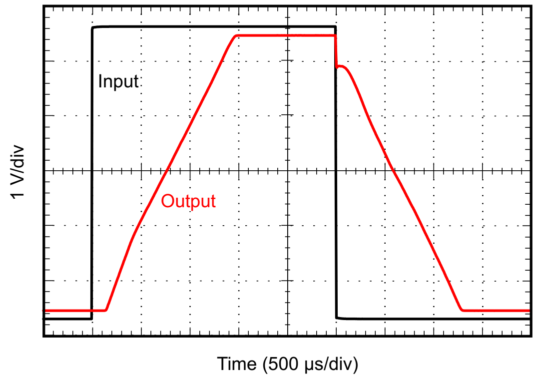


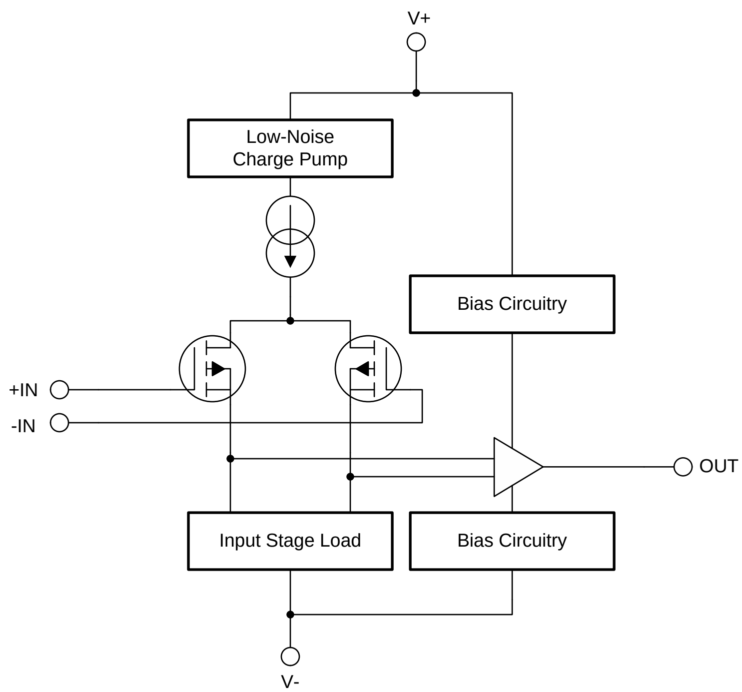
Figure 13. Overload Recovery

7 Detailed Description

7.1 Overview

The TLVx369 family of operational amplifiers minimizes power consumption and operates on supply voltages as low as 1.8 V. The zero-crossover distortion circuitry enables high linearity over the full input common-mode range, achieving true rail-to-rail input from a 1.8-V to 5.5-V single supply.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV369 series os op amps are fully specified and tested from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary significantly with supply voltage are described in the *Typical Characteristics* section.

7.3.2 Input Common-Mode Voltage Range

The TLV369 family is designed to eliminate the input offset transition region typically present in most rail-to-rail, complementary-stage operational amplifiers, allowing the TLV369 family of amplifiers to provide superior common-mode performance over the entire input range.

The input common-mode voltage range of the TLV369 family typically extends to each supply rail. CMRR is specified from the negative rail to the positive rail; see Figure 1, *Normalized Offset Voltage vs Common-Mode Voltage*.

7.3.3 Protecting Inputs from Overvoltage

Input currents are typically 10 pA. However, large inputs (greater than 500 mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, in addition to keeping the input voltage between the supply rails, the input current must also be limited to less than 10 mA. This limiting is easily accomplished with an input resistor, as shown in Figure 14.

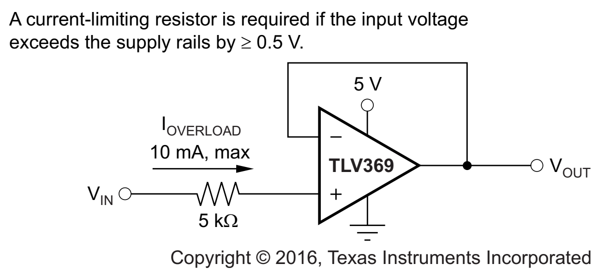


Figure 14. Input Current Protection for Voltages That Exceed the Supply Voltage

7.4 Device Functional Modes

The TLV369 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors can react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 15. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

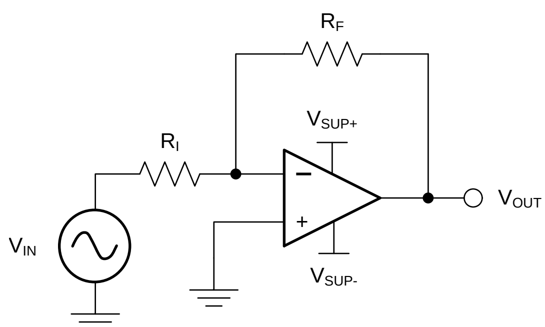


Figure 15. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

When the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures that the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Very small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, meaning 36 kΩ is used for R_F. These values are determined by Equation 3:

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

8.2.3 Application Curve

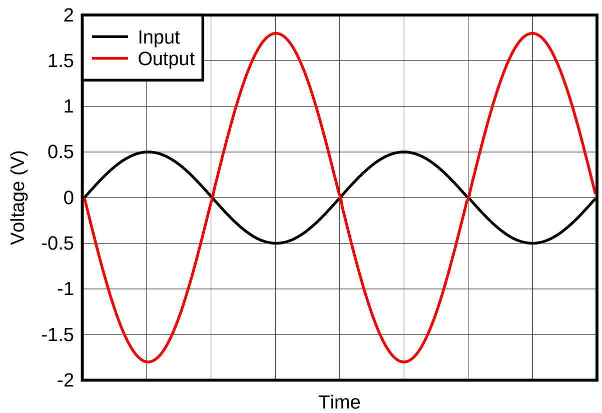


Figure 16. Inverting Amplifier Input and Output

8.3 System Examples

8.3.1 Battery Monitoring

The low operating voltage and quiescent current of the TLV369 series make the family an excellent choice for battery-monitoring applications, as shown in Figure 17.

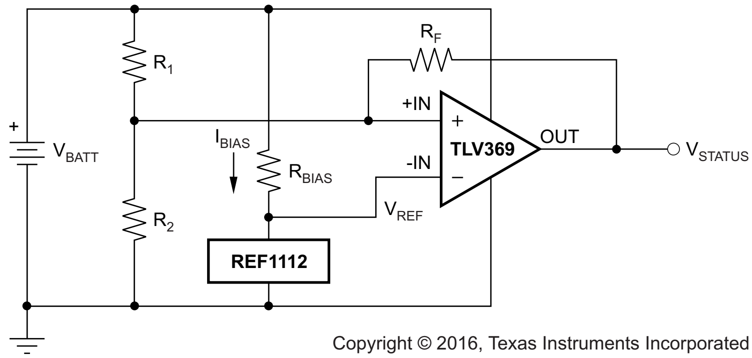


Figure 17. Battery Monitor

In this circuit, V_{STATUS} is high as long as the battery voltage remains above 2 V. A low-power reference is used to set the trip point. Resistor values are selected as follows:

1. Selecting R_F: Select R_F such that the current through R_F is approximately 1000 times larger than the maximum bias current over temperature, as given by Equation 4:

$$R_F = \frac{V_{REF}}{1000\,(I_{BMAX})} = \frac{1.2\ V}{1000\,(50\ pA)} = 24\ M\Omega \approx 20\ M\Omega \tag{4}$$

2. Choose the hysteresis voltage, V_{HYST}. For battery-monitoring applications, 50 mV is adequate.
3. Calculate R_1 as calculated by Equation 5:

$$R_1 = R_F\left[\frac{V_{HYST}}{V_{BATT}}\right] = 20\ M\Omega\left[\frac{50\ mV}{2.4\ V}\right] = 420\ k\Omega \tag{5}$$

4. Select a threshold voltage for V_{IN} rising (V_{THRS}) = 2.0 V.
5. Calculate R_2 as given by Equation 6:

$$R_2 = \frac{1}{\left[\left(\frac{V_{THRS}}{V_{BATT}}\right) - \frac{1}{R_1} - \frac{1}{R_1}\right]} = \frac{1}{\left[\left(\frac{2\ V}{1.2\ V \times 420\ k\Omega}\right) - \frac{1}{420\ k\Omega} - \frac{1}{20\ M\Omega}\right]} = 650\ k\Omega \tag{6}$$

6. Calculate R_{BIAS}: The minimum supply voltage for this circuit is 1.8 V. The REF1112 has a current requirement of 1.2 μA (max). Providing the REF1112 with 2 μA of supply current assures proper operation. Therefore, R_{BIAS} is as given by Equation 7.

$$R_{BIAS} = \frac{V_{BATTMIN}}{I_{BIAS}} = \frac{1.8\ V}{2\ \mu A} = 0.9\ M\Omega \tag{7}$$

System Examples (continued)

8.3.2 Window Comparator

Figure 18 shows the TLV2369 used as a window comparator. The threshold limits are set by V_H and V_L, with V_H greater than V_L. When V_{IN} is less than V_H, the output of A1 is low. When V_{IN} is greater than V_L, the output of A2 is low. Therefore, both op amp outputs are at 0 V as long as V_{IN} is between V_H and V_L. This architecture results in no current flowing through either diode, Q1 is in cutoff, with the base voltage at 0 V, and V_{OUT} forced high.

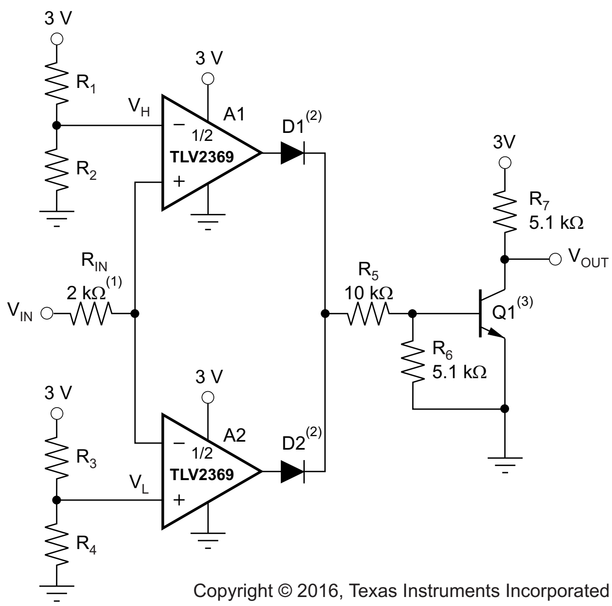


Figure 18. TLV2369 as a Window Comparator

If V_{IN} falls below V_L, the output of A2 is high, current flows through D2, and V_{OUT} is low. Likewise, if V_{IN} rises above V_H, the output of A1 is high, current flows through D1, and V_{OUT} is low. The window comparator threshold voltages are set as shown by Equation 8 and Equation 9:

$$V_H = \frac{R_2}{R_1 + R_2} \quad (8)$$

$$V_L = \frac{R_4}{R_3 + R_4} \quad (9)$$

9 Power Supply Recommendations

The TLV369 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input in order to minimize parasitic capacitance, as shown in Figure 19.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

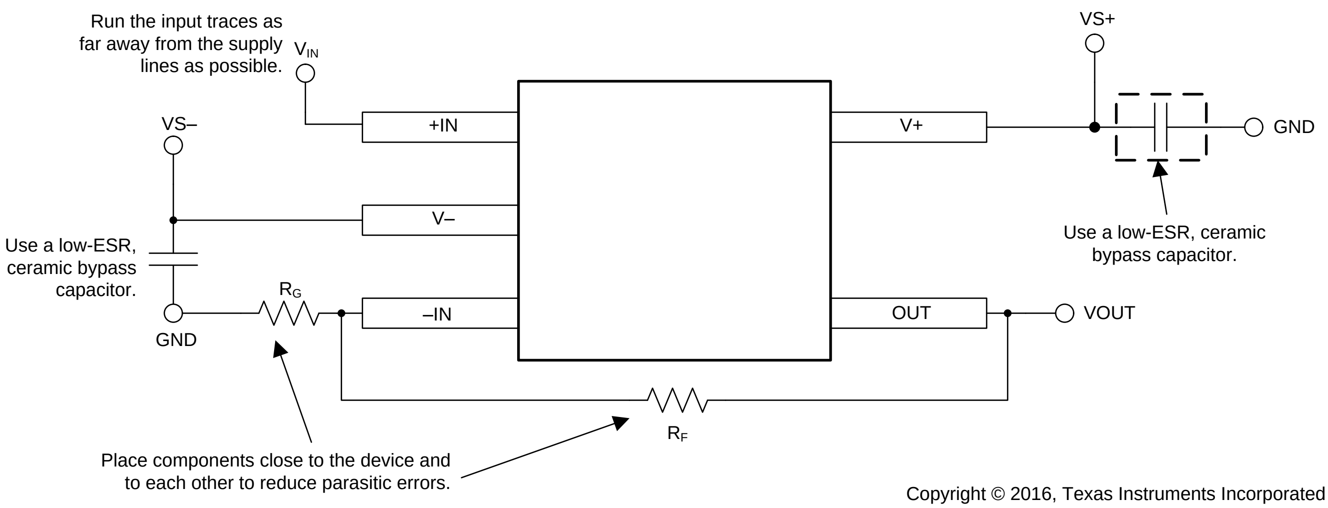


Figure 19. Operational Amplifier Board Layout for Noninverting Configuration

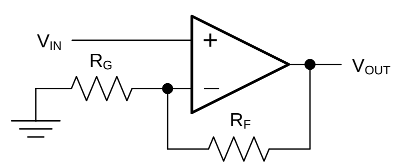


Figure 20. Schematic Representation of Figure 19

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

The following documents are relevant to using the TLVx369, and are recommended for reference and available for download at www.ti.com, unless otherwise noted.

- REF1112 Data Sheet, SBOS283
- *Circuit Board Layout Techniques*, SLOA089
- *Handbook of Operational Amplifier Applications*, SBOA092
- *Analog Engineer's Pocket Reference*, SLWY038

11.1.1.1 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV369	Click here	Click here	Click here	Click here	Click here
TLV2369	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2369IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	13JV	Samples
TLV2369IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	13JV	Samples
TLV2369IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
TLV369IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12K	Samples
TLV369IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12K	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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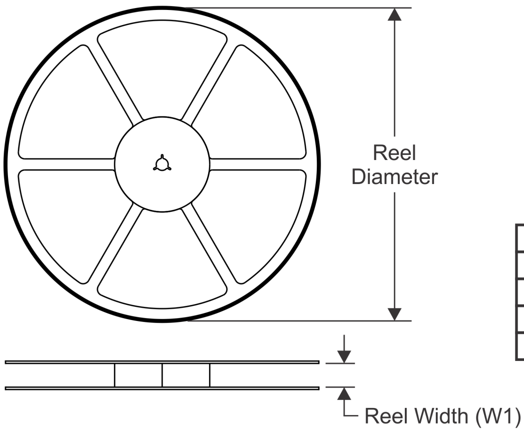
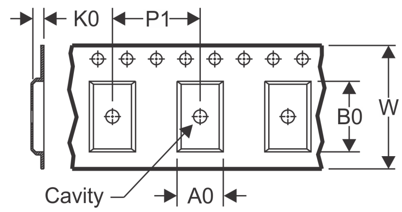
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

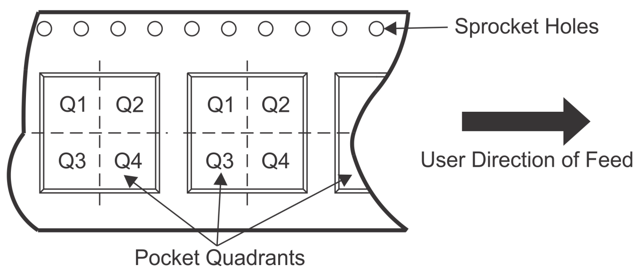


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

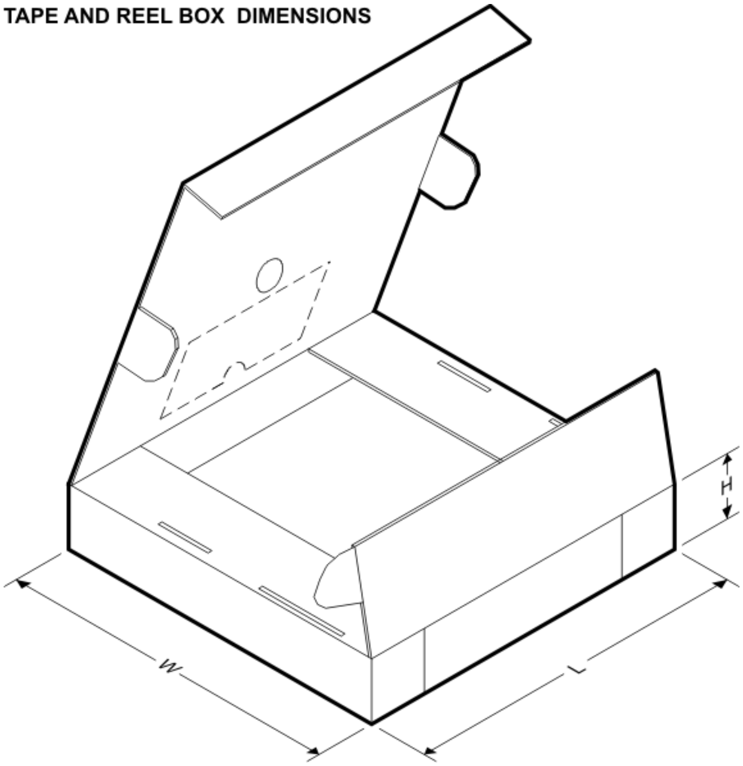
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2369IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2369IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV369IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV369IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

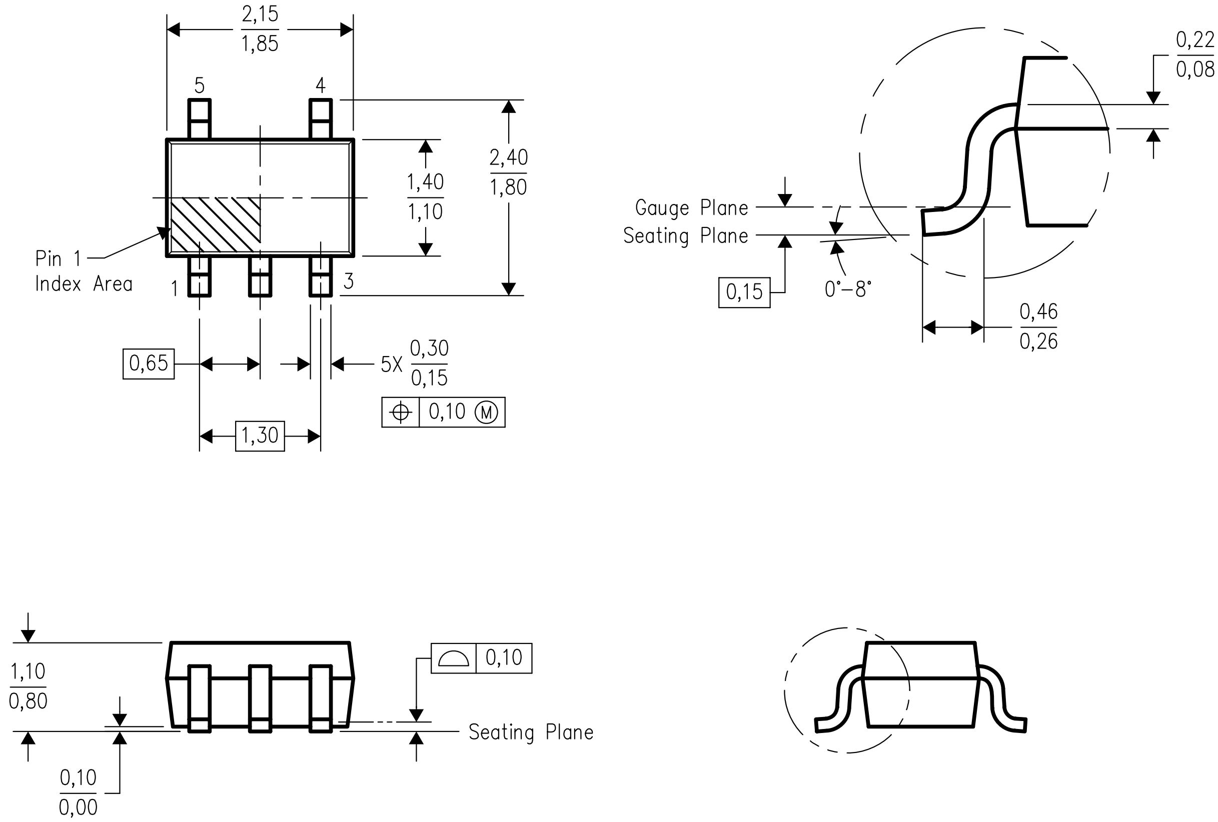
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2369IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2369IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV369IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV369IDCKT	SC70	DCK	5	250	180.0	180.0	18.0

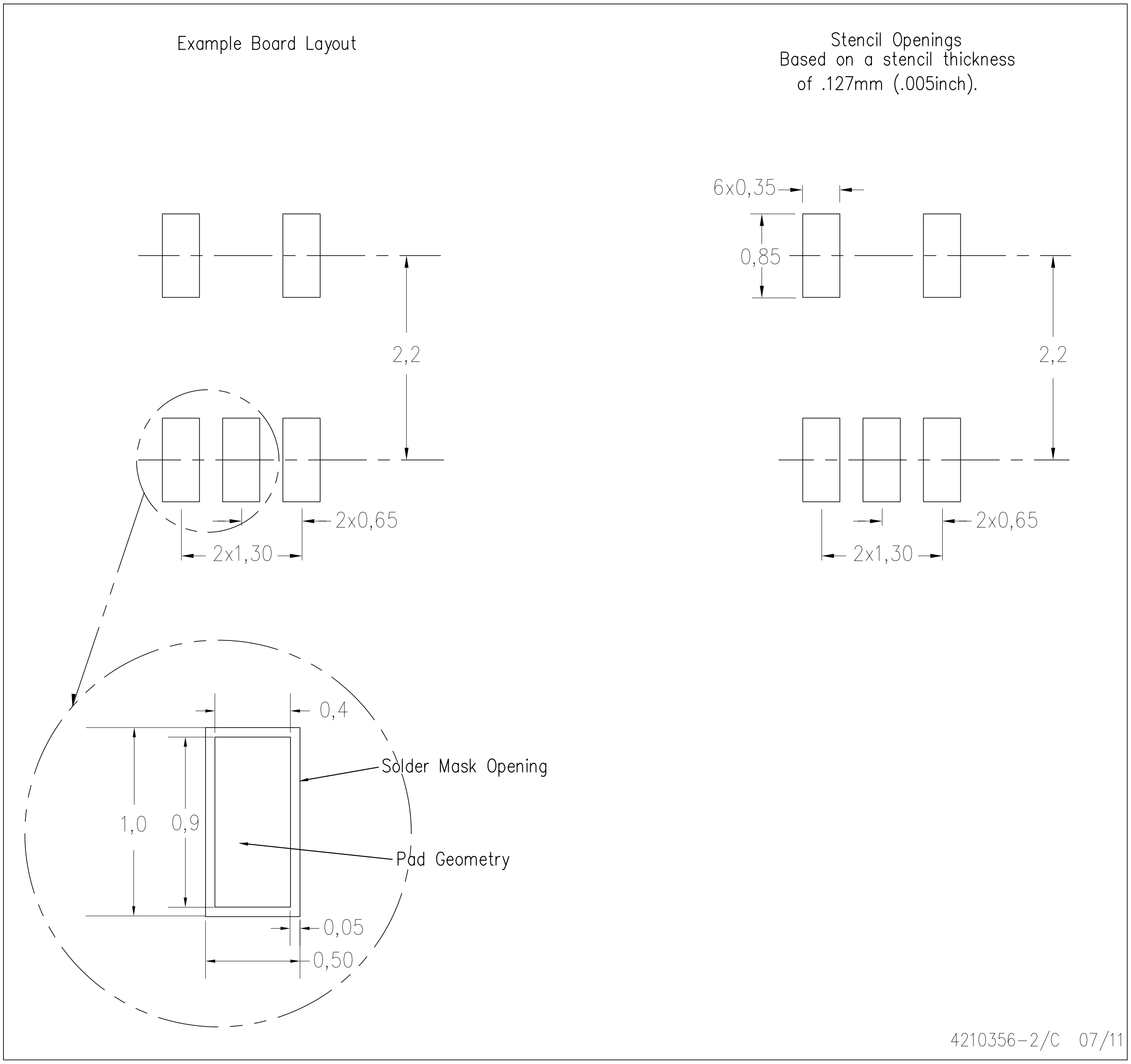
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

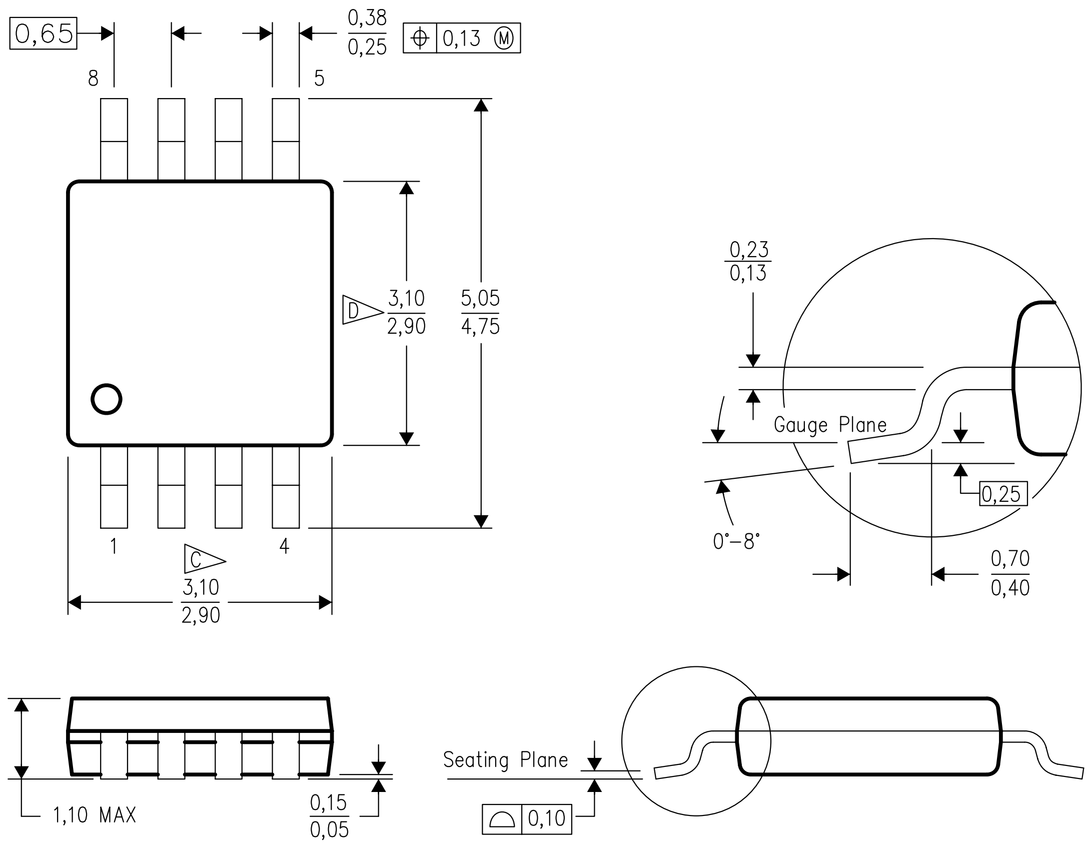
DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

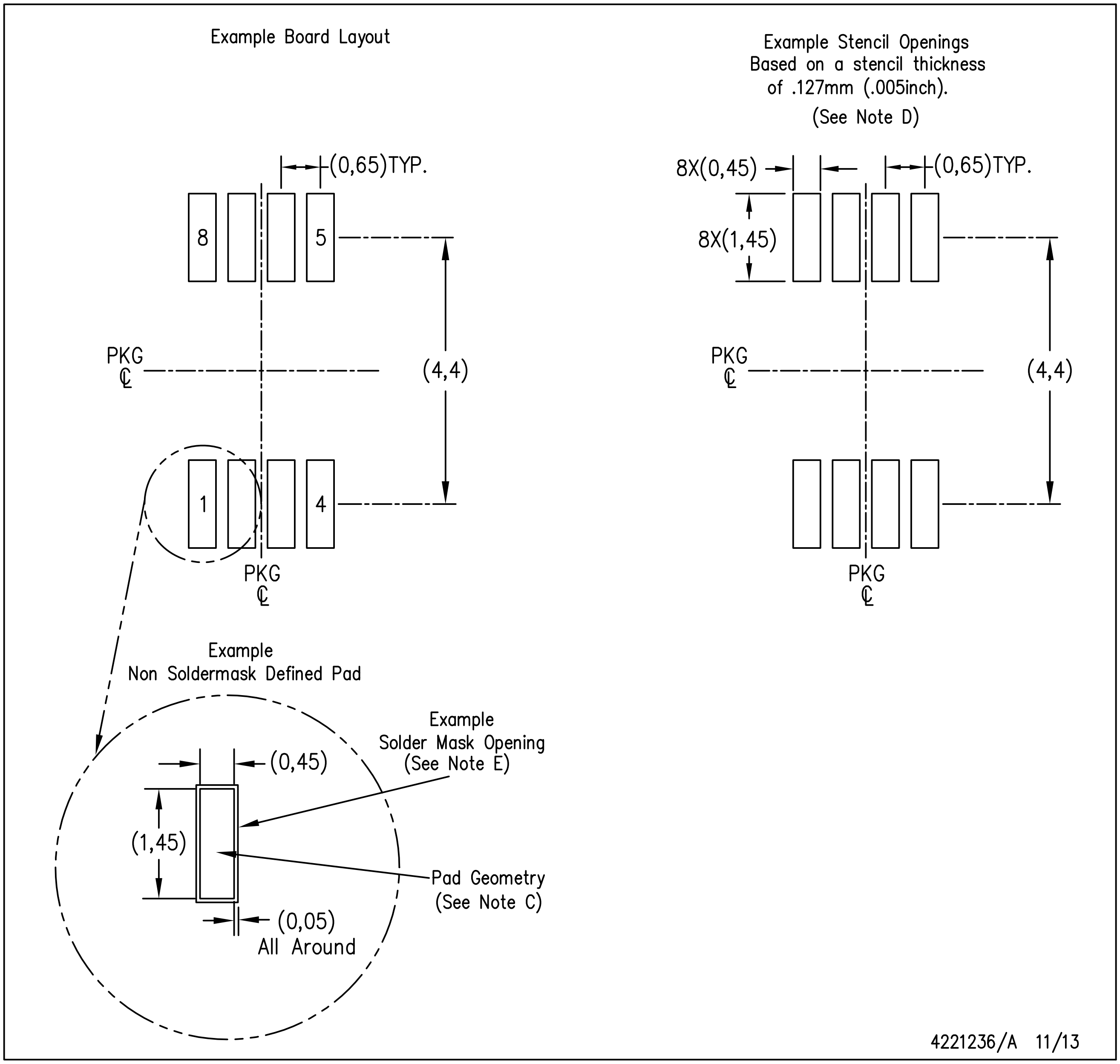
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

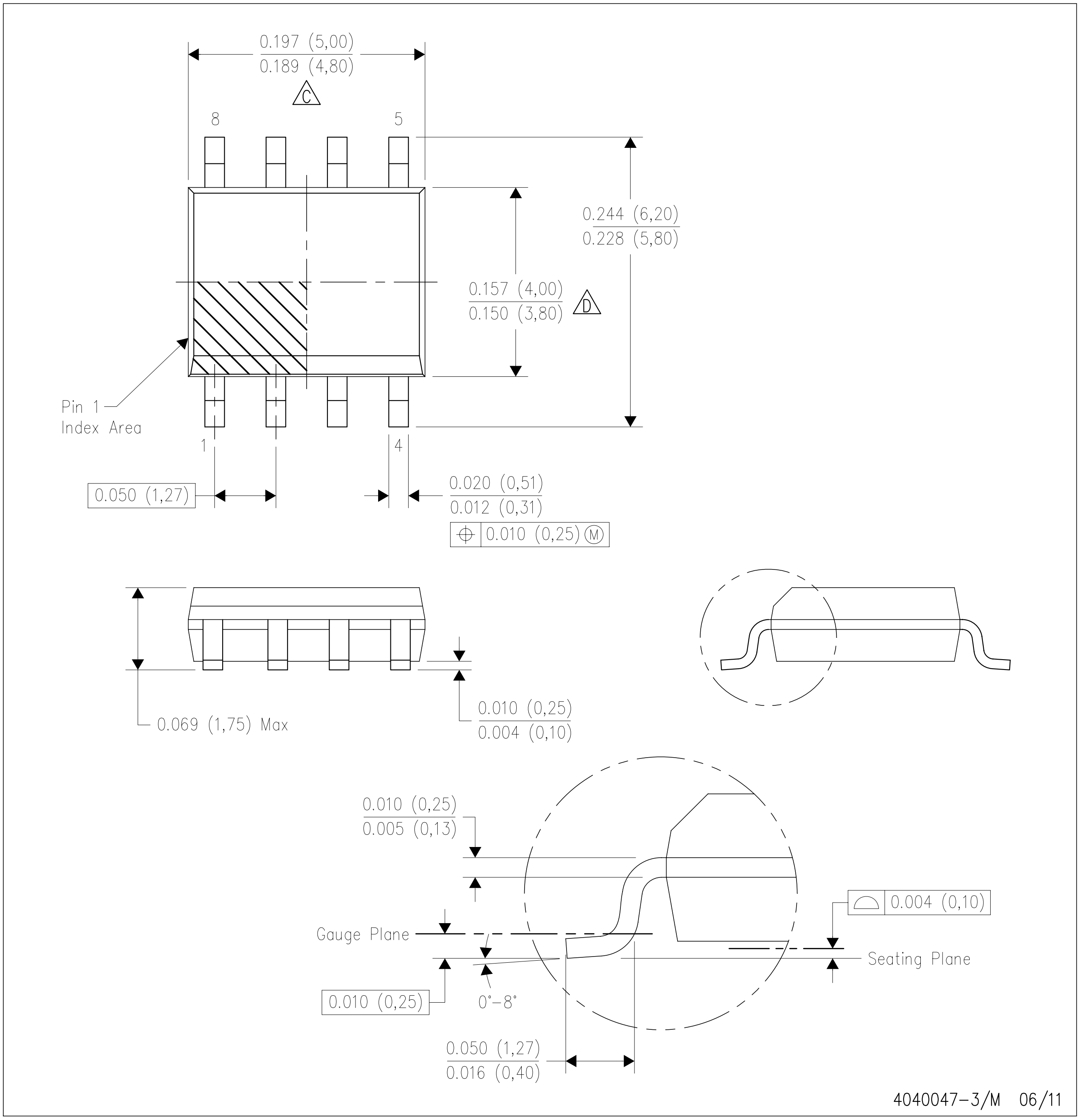
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.