TLV3501
TLV3502

SBOS321D − MARCH 2005 − REVISED JULY 2005

4.5ns Rail-to-Rail, High-Speed Comparator in Microsize Packages

FEATURES

- **HIGH SPEED: 4.5ns**
- **RAIL-TO-RAIL I/O**
- **SUPPLY VOLTAGE: +2.7V to +5.5V**
- **PUSH-PULL CMOS OUTPUT STAGE**
- **SHUTDOWN (TLV3501 only)**
- **MICRO PACKAGES:**
  SOT23-6 (single)
  SOT23-8 (dual)
- **LOW SUPPLY CURRENT: 3.2mA**

DESCRIPTION

The TLV350x family of push-pull output comparators feature a fast 4.5ns propagation delay and operation from +2.7V to +5.5V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

Microsize packages provide options for portable and space-restricted applications. The single (TLV3501) is available in SOT23-6 and SO-8 packages. The dual (TLV3502) comes in the SOT23-8 and SO-8 packages.

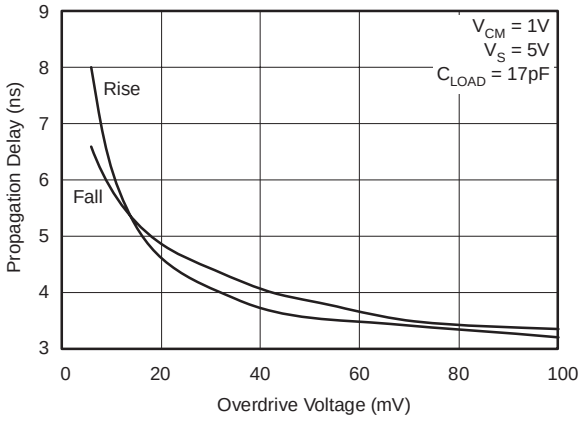
APPLICATIONS

- **AUTOMATIC TEST EQUIPMENT**
- **WIRELESS BASE STATIONS**
- **THRESHOLD DETECTOR**
- **ZERO-CROSSING DETECTOR**
- **WINDOW COMPARATOR**

TLV350x RELATED PRODUCTS

FEATURES	PRODUCT
Precision Ultra-Fast, Low-Power Comparator	TLC3016
Differential Output Comparator	TL712
High-Speed Op Amp, 16-Bit Accurate, 150MHz	OPA300
High-Speed Op Amp, Rail-to-Rail, 38MHz	OPA350
High-Speed Op Amp with Shutdown, 250MHz	OPA357

PROPAGATION DELAY vs OVERDRIVE VOLTAGE



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals, Voltage(2)	(V−) − 0.3V to (V+) + 0.3V
Signal Input Terminals, Current(2)	10mA
Output Short Circuit(3)	74mA
Operating Temperature	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model)	3000V
Charged-Device Model (CDM)	500V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one comparator per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

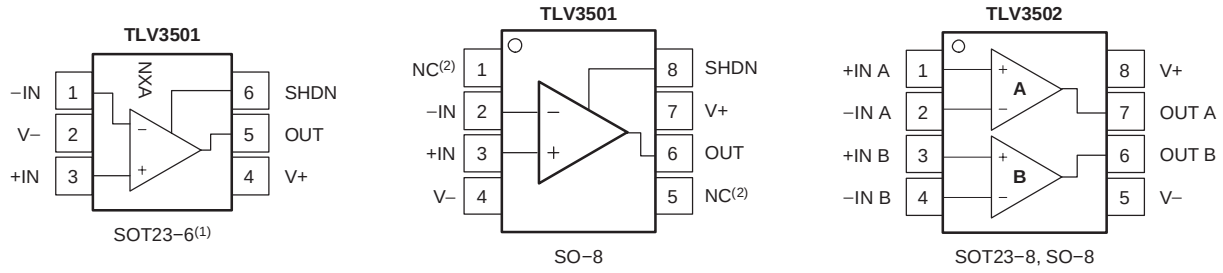
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TLV3501	SOT23-6	DBV	NXA
TLV3501	SO-8	D	TLV3501A
TLV3502	SOT23-8	DCN	NXC
TLV3502	SO-8	D	TLV3502A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS



(1) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated on the diagram.
(2) NC indicates no internal connection.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C and V_S = +2.7V to +5.5V, unless otherwise noted.

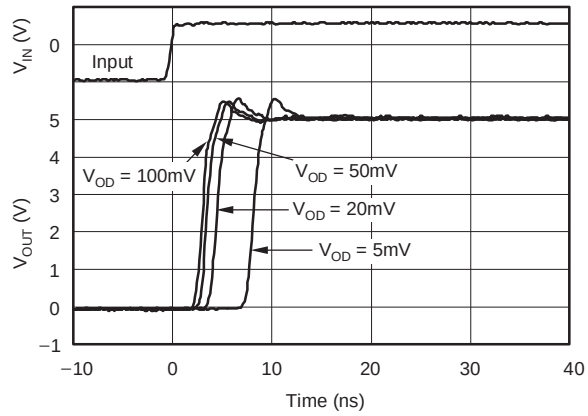
PARAMETER		CONDITION	TLV3501, TLV3502 MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage(1)	V_{OS}	V_{CM} = 0V, I_O = 0mA		±1	±6.5	mV
vs Temperature	**dV_{OS}/dT**	**T_A = −40°C to +125°C**		**±5**		**µV/°C**
vs Power Supply	PSRR	V_S = 2.7V to 5.5V		100	400	µV/V
Input Hysteresis				6		mV
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_{CC}/2		±2	±10	pA
Input Offset Current(2)	I_{OS}	V_{CM} = V_{CC}/2		±2	±10	pA
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.2V		(V+) + 0.2V	V
Common-Mode Rejection	CMRR	V_{CM} = −0.2V to (V+) + 0.2V	57	70		dB
		V_{CM} = −0.2V to (V+) + 0.2V	**55**			**dB**
INPUT IMPEDANCE						
Common-Mode				10^{13} ||2		Ω ||pF
Differential				10^{13} ||4		Ω ||pF
SWITCHING CHARACTERISTICS						
Propagation Delay Time(3)	$T_{(pd)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		4.5	6.4	ns
		ΔV_{IN} = 100mV, Overdrive = 20mV			**7**	**ns**
		ΔV_{IN} = 100mV, Overdrive = 5mV		7.5	10	ns
		ΔV_{IN} = 100mV, Overdrive = 5mV			**12**	**ns**
Propagation Delay Skew(4)	$\Delta t_{(SKEW)}$	ΔV_{IN} = 100mV, Overdrive = 20mV		0.5		ns
Maximum Toggle Frequency	f_{MAX}	Overdrive = 50mV, V_S = 5V		80		MHz
Rise Time(5)	t_R			1.5		ns
Fall Time(5)	t_F			1.5		ns
OUTPUT						
Voltage Output from Rail	V_{OH},V_{OL}	I_{OUT} = ±1mA		30	50	mV
SHUTDOWN						
t_{OFF}				30		ns
t_{ON}				100		ns
V_L (comparator is enabled)(6)					(V+) − 1.7V	V
V_H (comparator is disabled)(6)			(V+) − 0.9V			V
Input Bias Current of Shutdown Pin				2		pA
I_{QSD} (quiescent current in shutdown)				2		µA
POWER SUPPLY						
Specified Voltage	V_S		+2.7		+5.5	V
Operating Voltage Range				2.2 to 5.5		V
Quiescent Current	I_Q	V_S = 5V, V_O = High		3.2	5	mA
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Operating Range			−40		+125	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
SOT23-5				200		°C/W
SOT23-8				200		°C/W
SO-8				150		°C/W

(1) V_{OS} is defined as the average of the positive and the negative switching thresholds.
(2) The difference between I_B+ and I_B−.
(3) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization and testing at 100mV overdrive.
(4) The difference between the propagation delay going high and the propagation delay going low.
(5) Measured between 10% of V_S and 90% of V_S.
(6) When the shutdown pin is within 0.9V of the most positive supply, the part is disabled. When it is more than 1.7V below the most positive supply, the part is enabled.

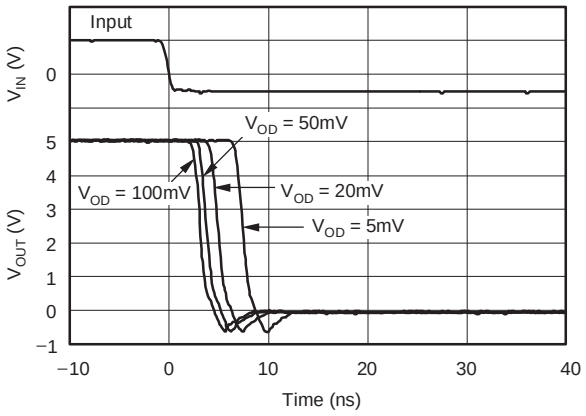
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and Input Overdrive = 100mV, unless otherwise noted.

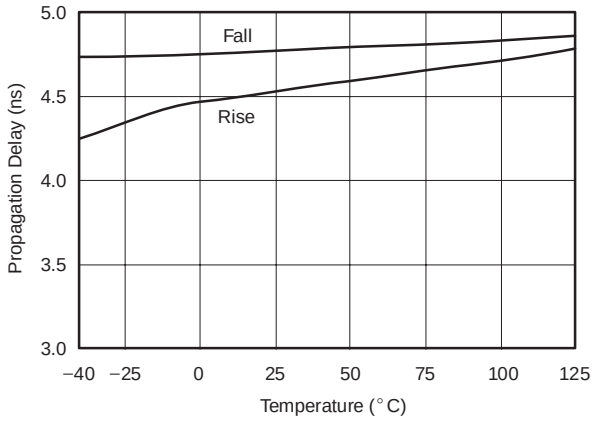
OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (rising)



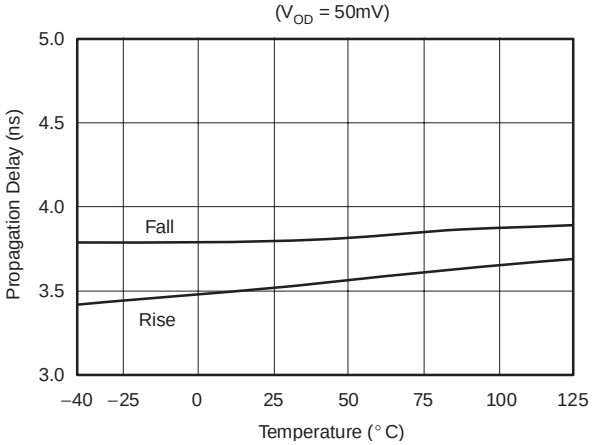
OUTPUT RESPONSE FOR VARIOUS OVERDRIVE VOLTAGES (falling)



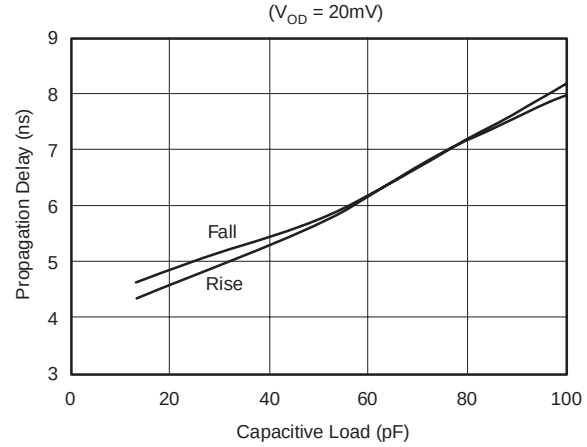
PROPAGATION DELAY vs TEMPERATURE (V_{OD} = 20mV)



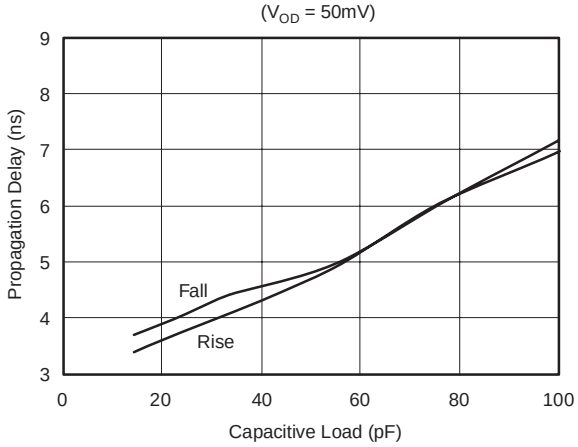
PROPAGATION DELAY vs TEMPERATURE (V_{OD} = 50mV)



PROPAGATION DELAY vs CAPACITIVE LOAD (V_{OD} = 20mV)



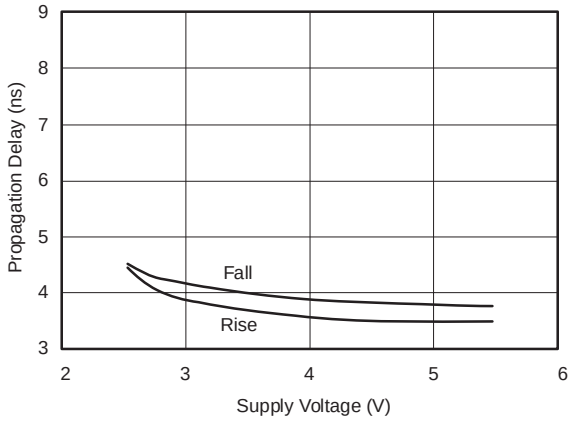
PROPAGATION DELAY vs CAPACITIVE LOAD (V_{OD} = 50mV)



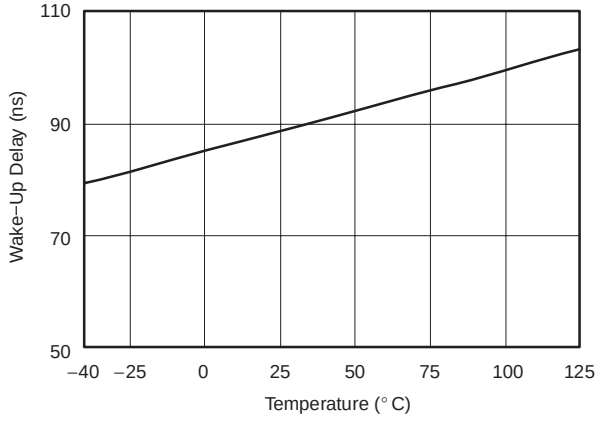
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and Input Overdrive = 100mV, unless otherwise noted.

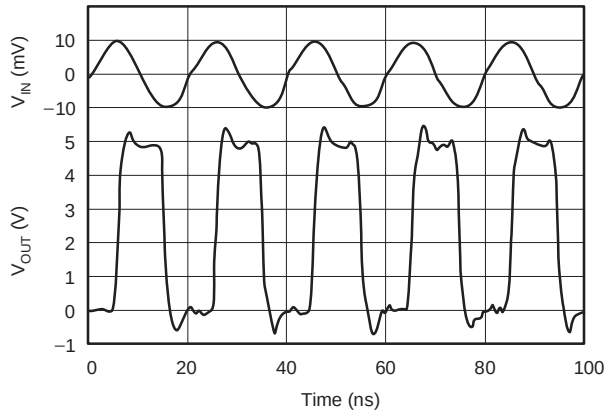
PROPAGATION DELAY vs SUPPLY VOLTAGE
(V_{CM} = 1V, V_{OD} = 20mV)



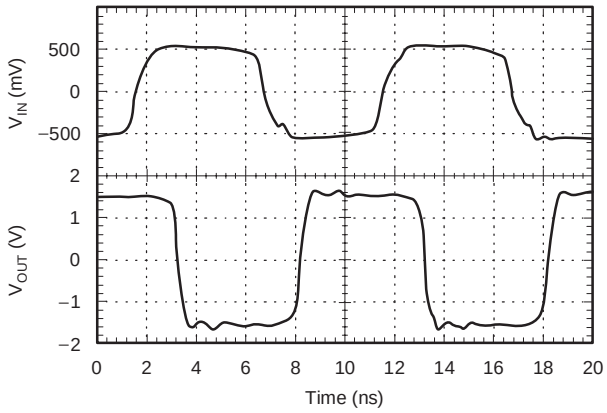
WAKE−UP DELAY vs TEMPERATURE



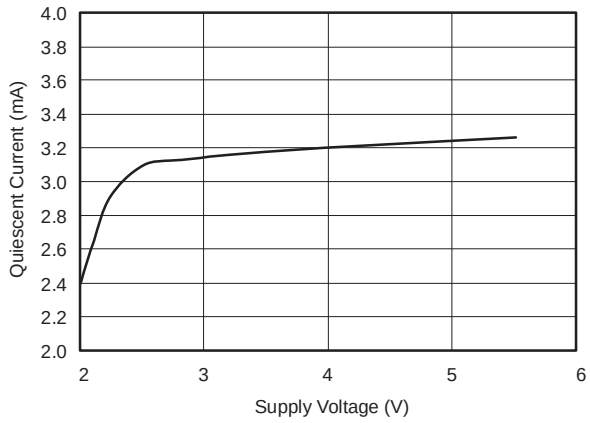
RESPONSE TO 50MHz SINE WAVE
(V_{DD} = 5V, V_{IN} = 20mV_{PP})



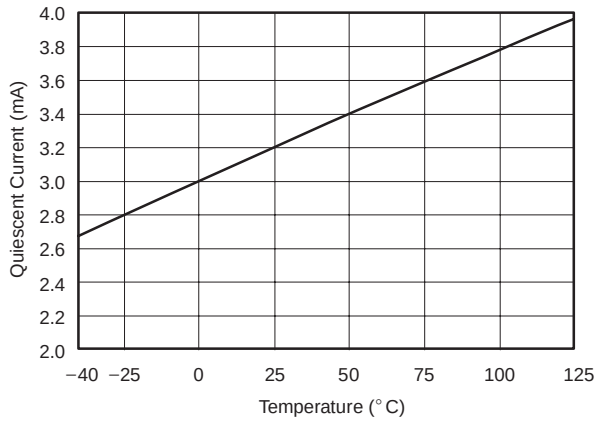
RESPONSE TO 100MHz SINE WAVE
(±2.5V dual supply into 50Ω oscilloscope input)



QUIESCENT CURRENT vs SUPPLY VOLTAGE

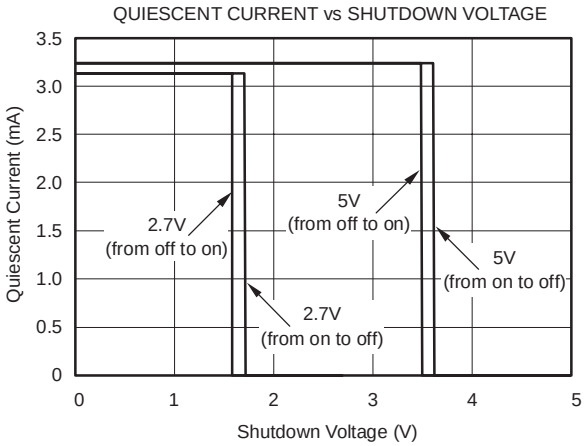


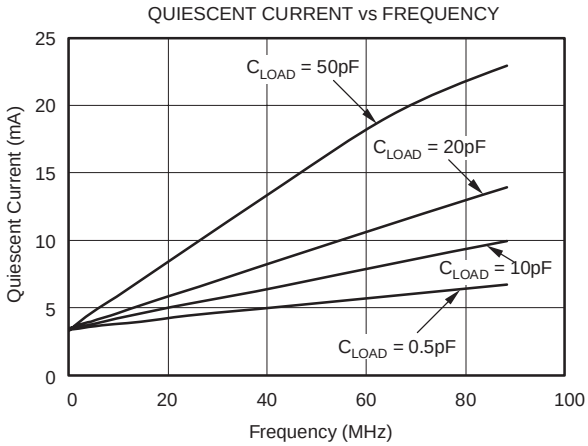
QUIESCENT CURRENT vs TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and Input Overdrive = 100mV, unless otherwise noted.





APPLICATIONS INFORMATION

The TLV3501 and TLV3502 both feature high-speed response and includes 6mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2V beyond the power-supply rails.

SHUTDOWN

A shutdown pin allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws about 2µA and the output goes to high impedance. When the shutdown pin is low, the TLV3501 is active. When the TLV3501 shutdown feature is not used, simply connect the shutdown pin to the most negative supply, as shown in Figure 1. It takes about 100ns to come out of shutdown mode. The TLV3502 does not have the shutdown feature.

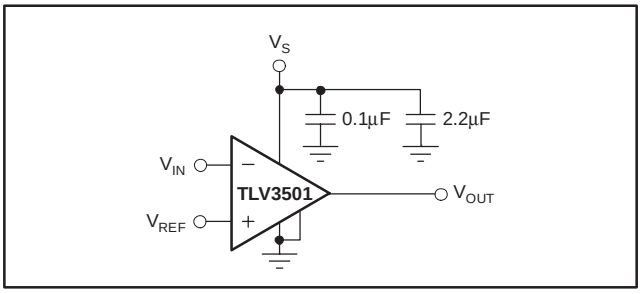


Figure 1. Basic Connections for the TLV3501

OPERATING VOLTAGE

TLV3501 comparators are specified for use on a single supply from +2.7V to +5.5V (or a dual supply from ±1.35V to ±2.75V) over a temperature range of −40°C to +125°C. The device continues to function below this range, but performance is not specified.

ADDING EXTERNAL HYSTERESIS

The TLV350x has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of specified offset voltage (±5mV). For slow moving or noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. In such applications, the 6mV of internal hysteresis of the TLV350x might not be sufficient. In cases where greater noise immunity is desired, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 2 shows a typical topology used to introduce 25mV of additional hysteresis, for a total of 31mV hysteresis when operating from a single 5V supply. Total hysteresis is approximated by Equation 1:

$$V_{HYST} = \frac{(V+) \times R_1}{R_1 + R_2} + 6mV \quad (1)$$

V_{HYST} sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.

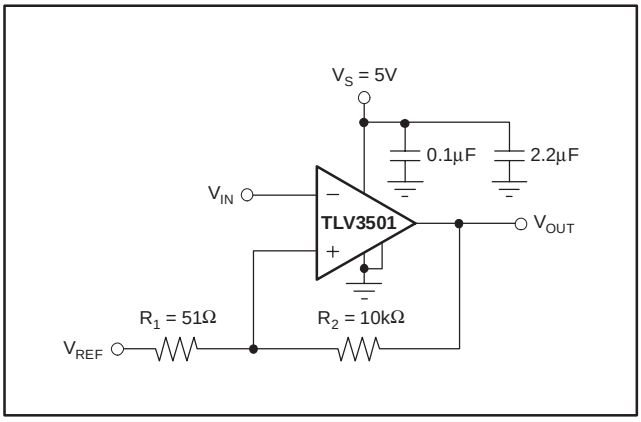


Figure 2. Adding Hysteresis to the TLV350x

INPUT OVER-VOLTAGE PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the input current is limited to 10mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 3.

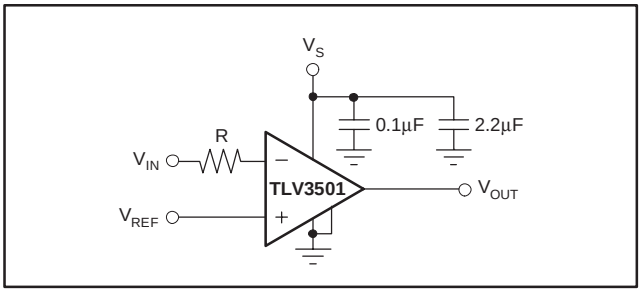


Figure 3. Input Current Protection for Voltages Exceeding the Supply Voltage

RELAXATION OSCILLATOR

The TLV350x can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 4, the R2 network sets the trip threshold at 1/3 and 2/3 of the supply. Since this is a high-speed circuit, the resistor values are rather low in order to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+ depending on whether the output is low or high. The time to charge (or discharge) is $0.69R_1C$. Therefore, the period is $1.38R_1C$. For 62pF and 1kΩ as shown in Figure 4, the output is calculated to be 10.9MHz. An implementation of this circuit oscillated at 9.6MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

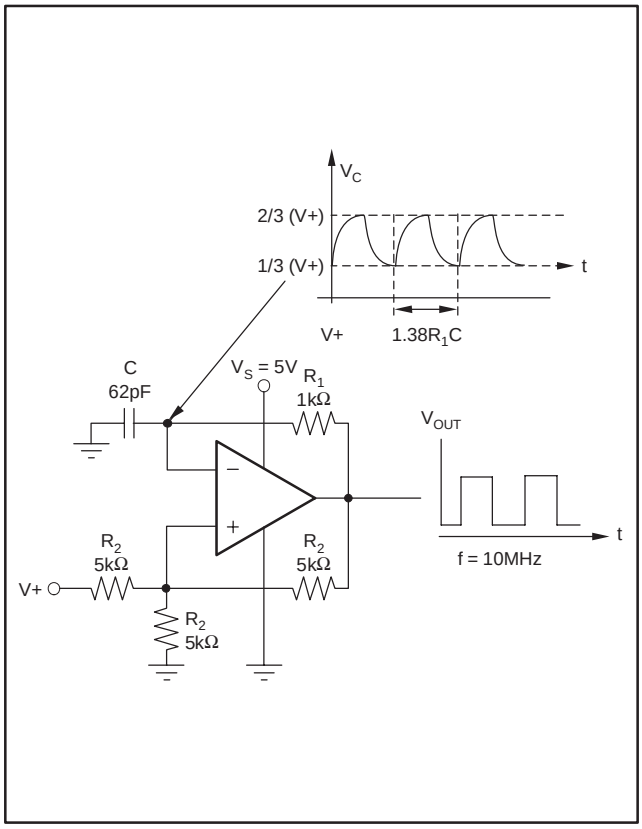


Figure 4. Relaxation Oscillator

HIGH-SPEED WINDOW COMPARATOR

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3502 can readily be used to create a high-speed window comparator. V_{HI} is the upper voltage threshold, and V_{LO} is the lower voltage threshold. When V_{IN} is between these two thresholds, the output in Figure 5 is high. Figure 6 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 5 and Figure 6. The operating voltage range of either circuit is 2.7V to 5.5V.

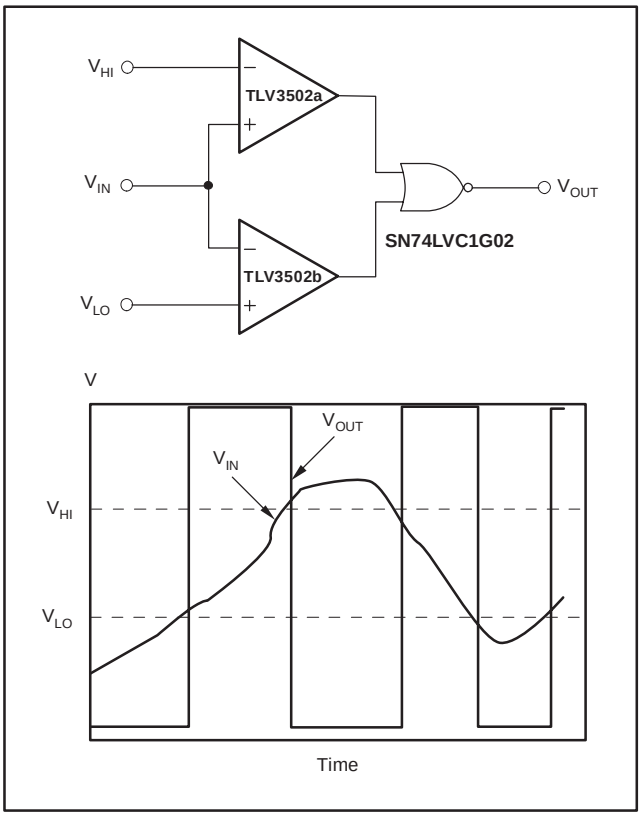


Figure 5. Window Comparator—Active High

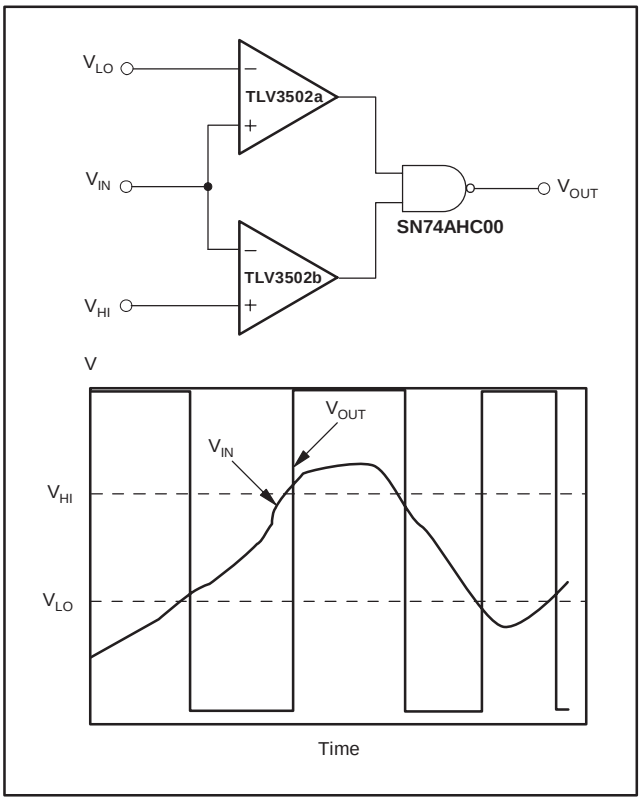


Figure 6. Window Comparator—Active Low

PCB LAYOUT

For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV350x along with stray capacitance from an input pin to ground results in several picofarads of capacitance.

The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2µF tantalum capacitor do not need to be as close to the device as the 0.1µF capacitor, and may be shared with other devices. The 2.2µF capacitor buffers the power-supply line against ripple, and the 0.1µF capacitor provides a charge for the comparator during high-frequency switching.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.

Figure 7 shows an evaluation layout for the TLV3501 SO-8 package; Figure 8 is for the SOT23-5 package. They are shown with SMA connectors bringing signals on and off the board. RT1 and RT2 are termination resistors for $+V_{IN}$ and $-V_{IN}$, respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1µF capacitor closest to the comparator. The ground plane is not shown, but the pads that the resistors and capacitors connect to are shown. Figure 9 shows a schematic of this circuit.

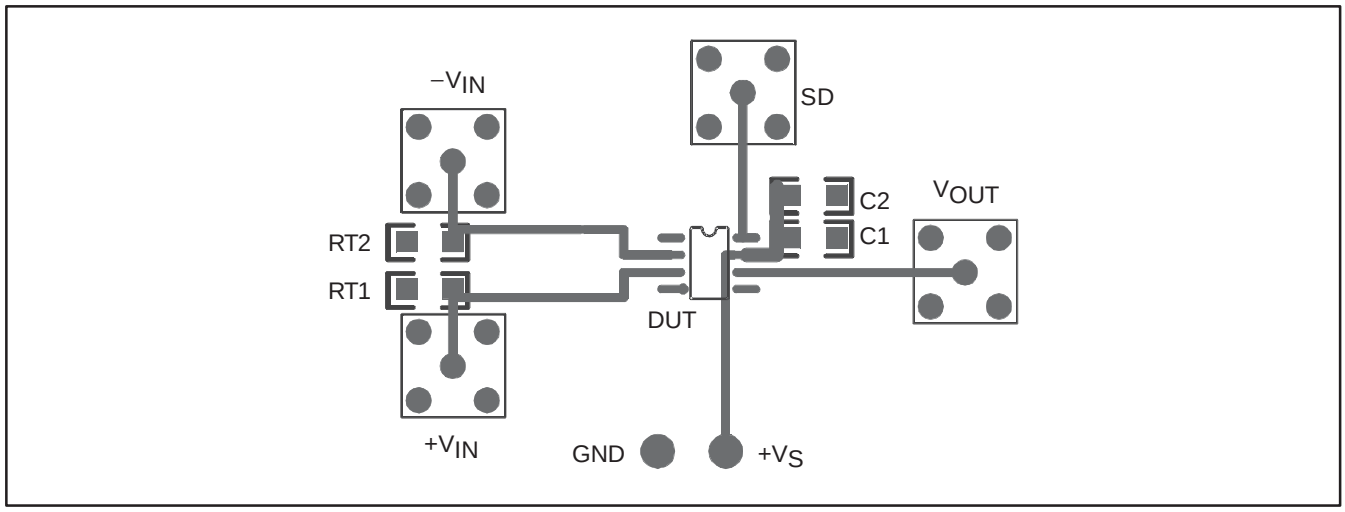


Figure 7. TLV3501D (SO-8) Sample Layout

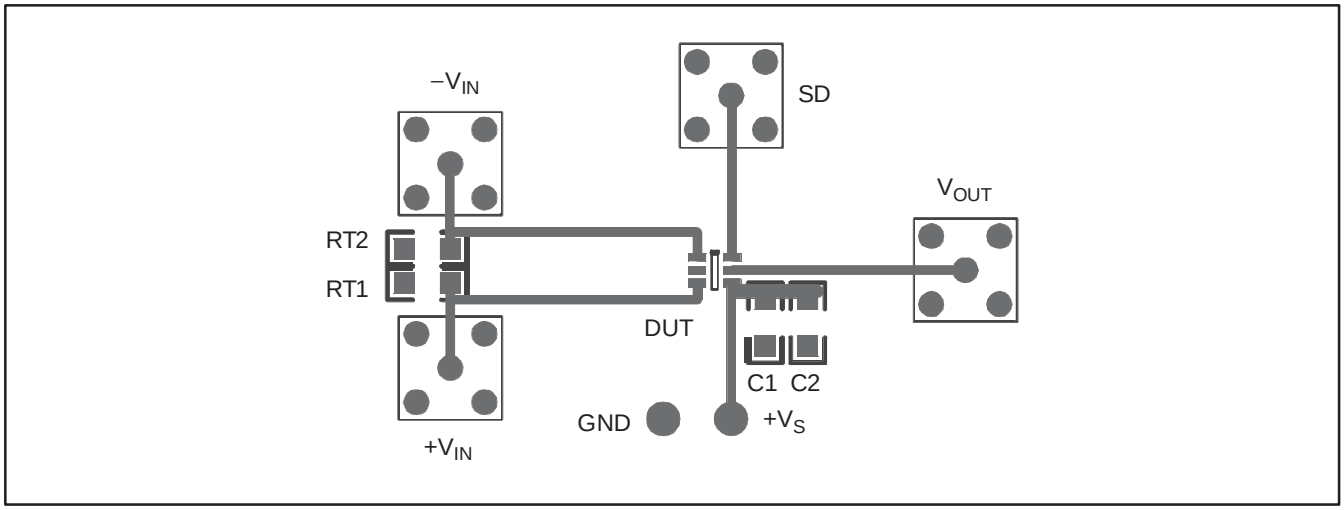


Figure 8. TLV3501DBV (SOT23) Sample Layout

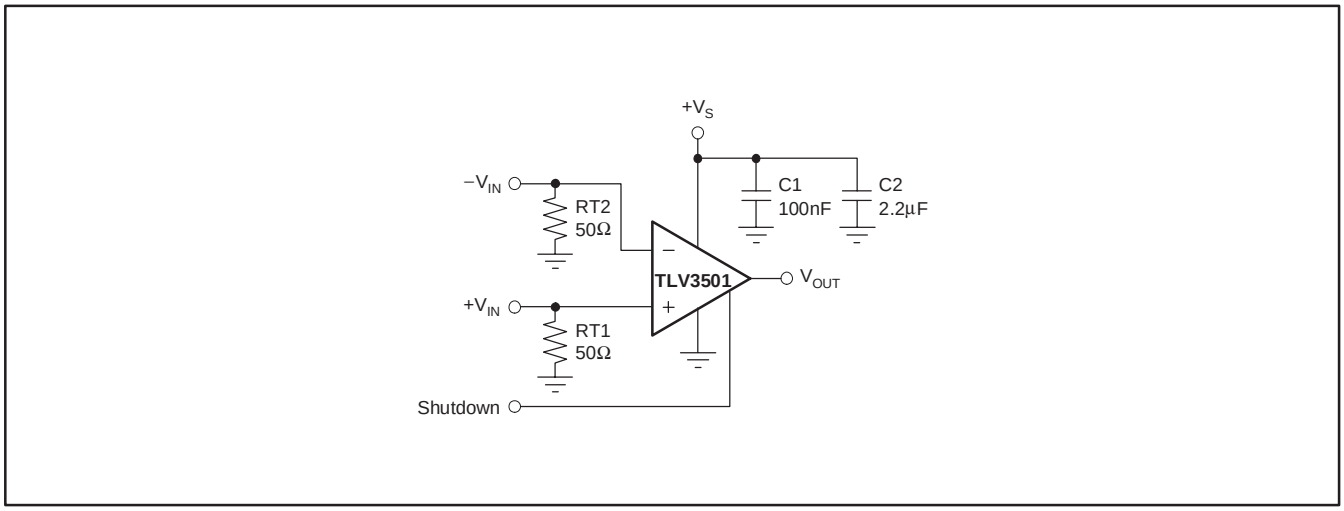


Figure 9. Schematic for Figure 7 and Figure 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV3501AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3501AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXA	Samples
TLV3501AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3501AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3501AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3501	Samples
TLV3502AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples
TLV3502AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	NXC	Samples
TLV3502AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples
TLV3502AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples
TLV3502AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3502	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF TLV3502 :

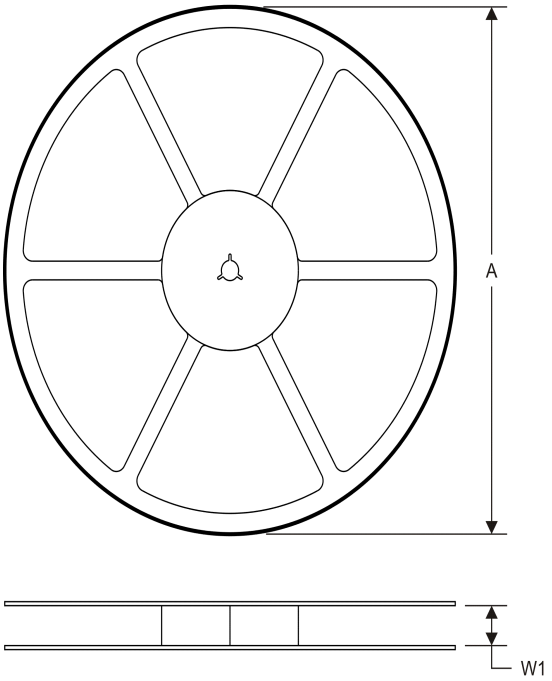
- Automotive: TLV3502-Q1

NOTE: Qualified Version Definitions:

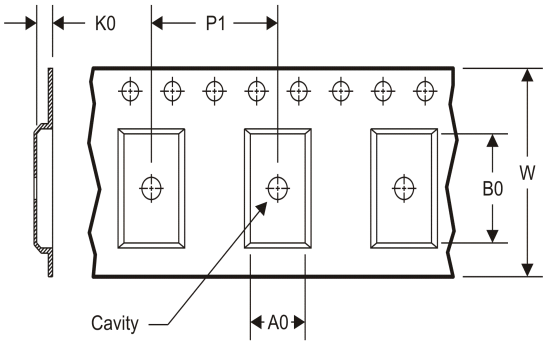
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



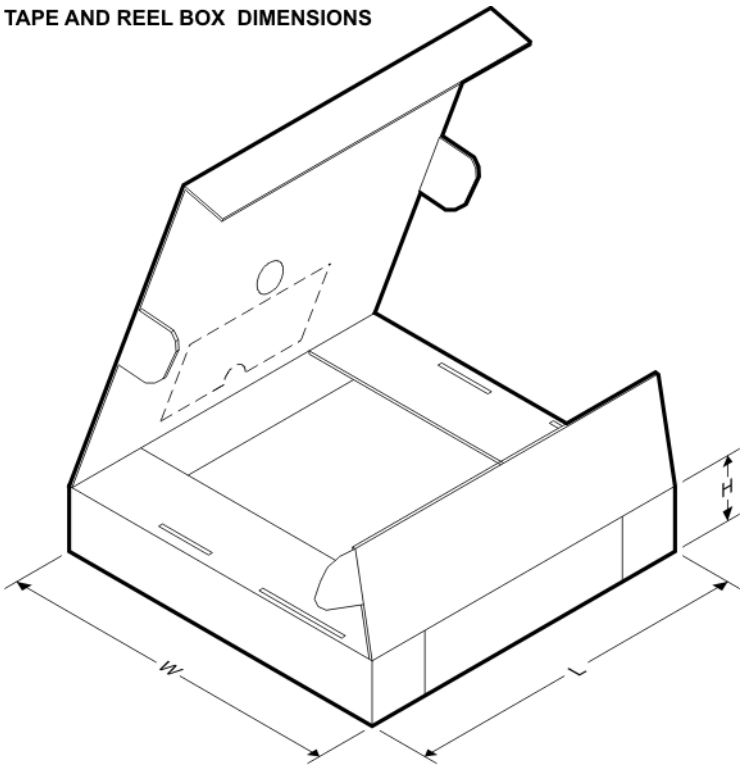
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3501AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3501AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3501AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3502AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3502AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

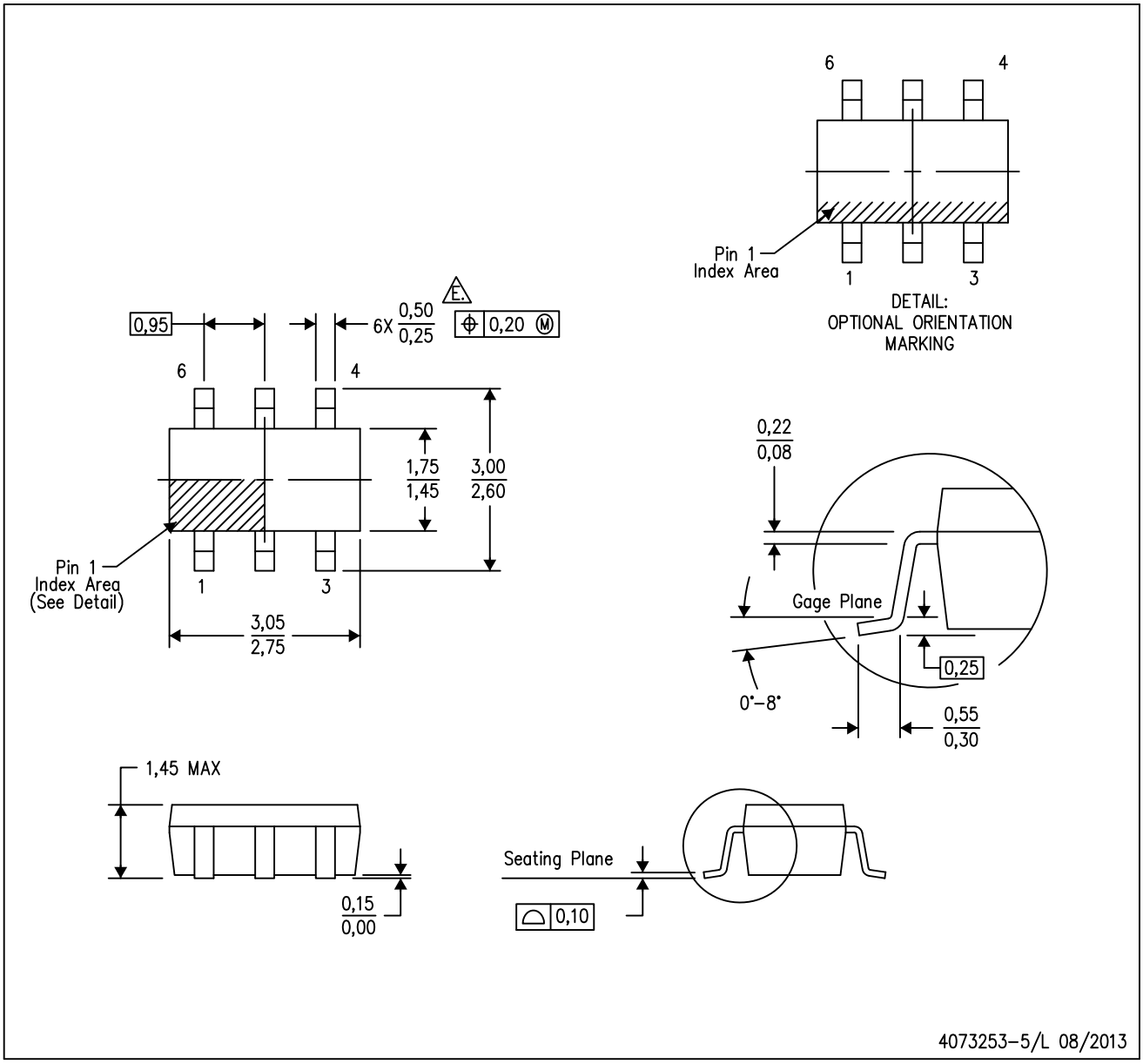
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

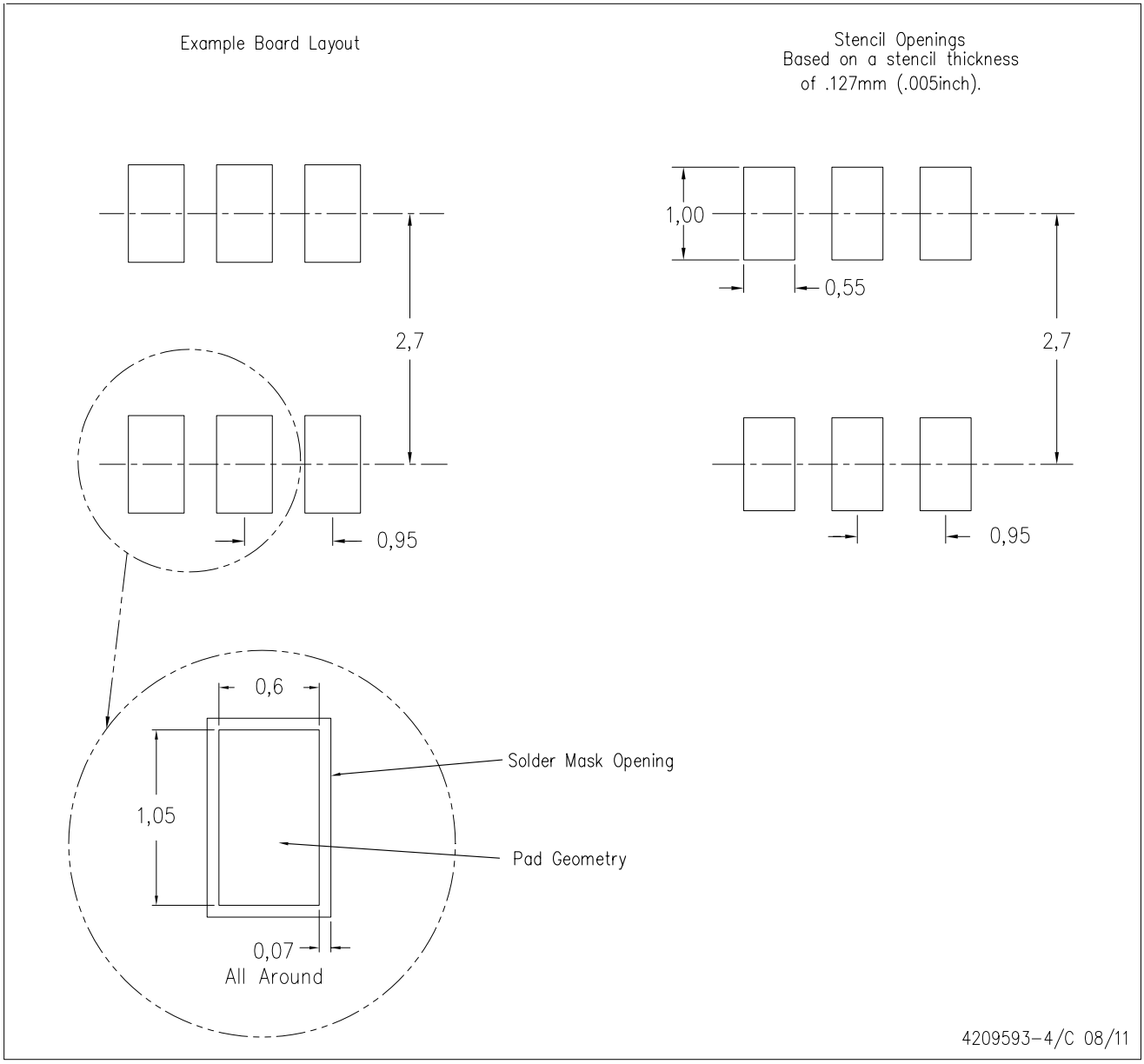
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3501AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV3501AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TLV3501AIDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV3502AIDCNR	SOT-23	DCN	8	3000	195.0	200.0	45.0
TLV3502AIDCNT	SOT-23	DCN	8	250	195.0	200.0	45.0
TLV3502AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



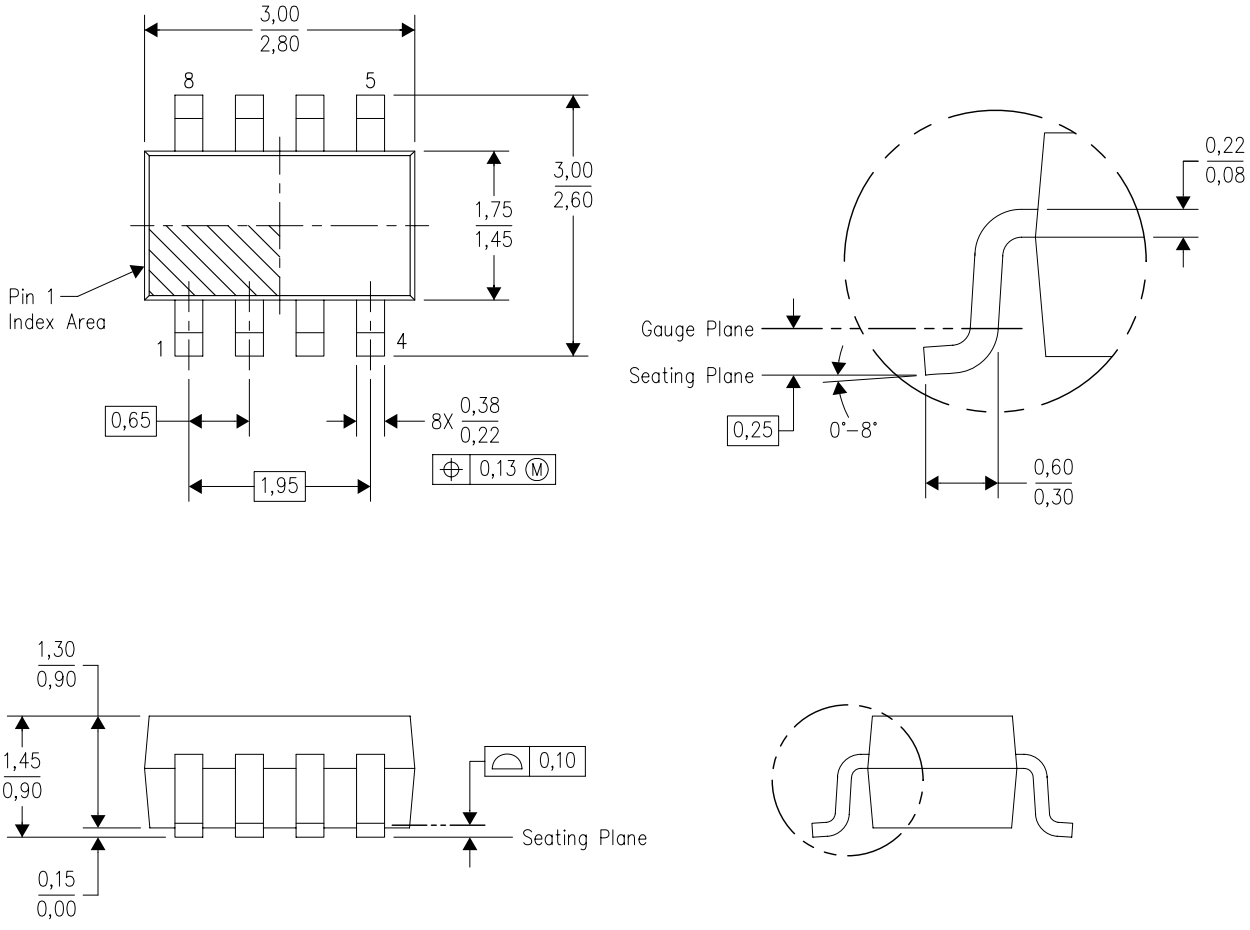
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



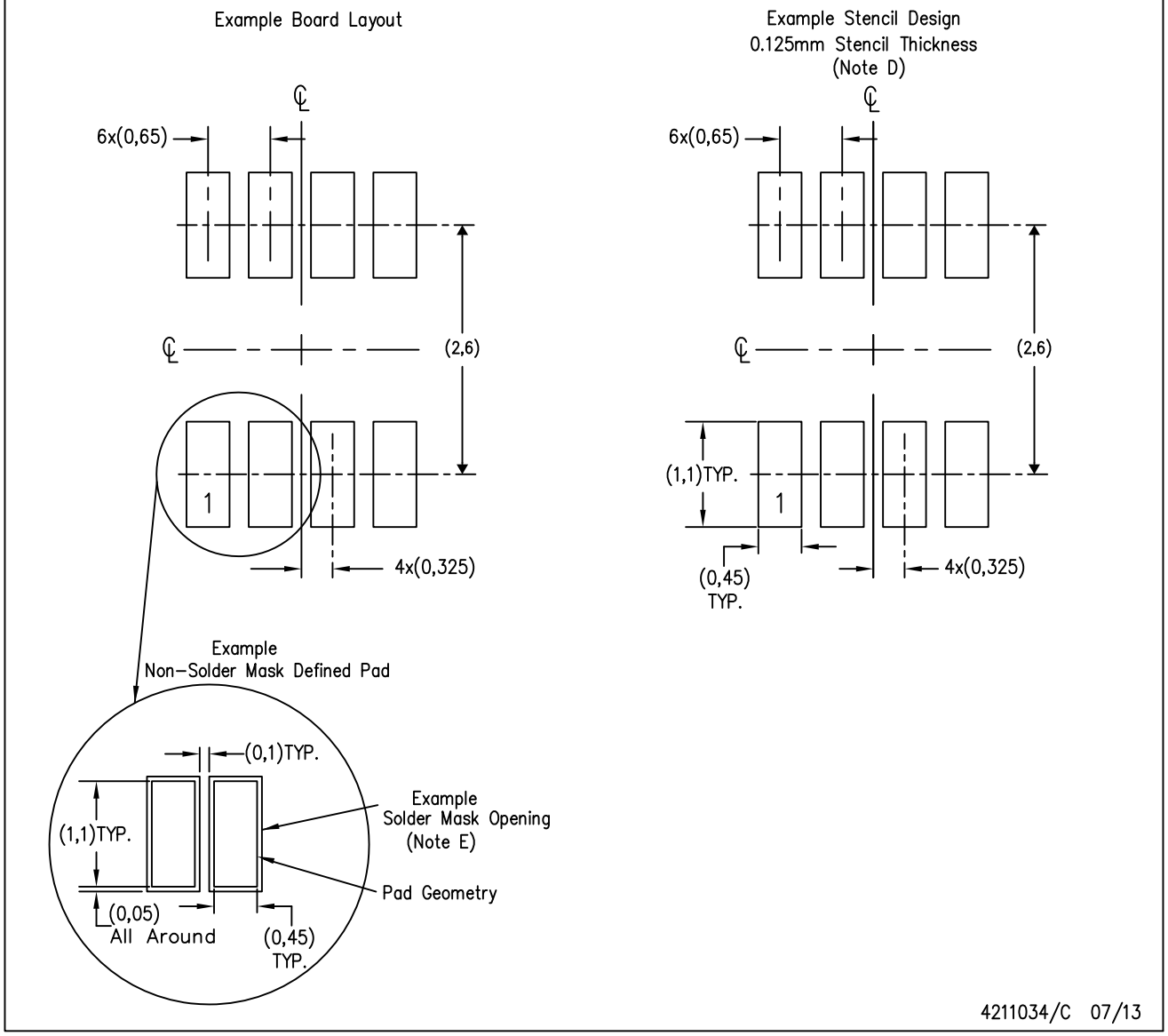
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



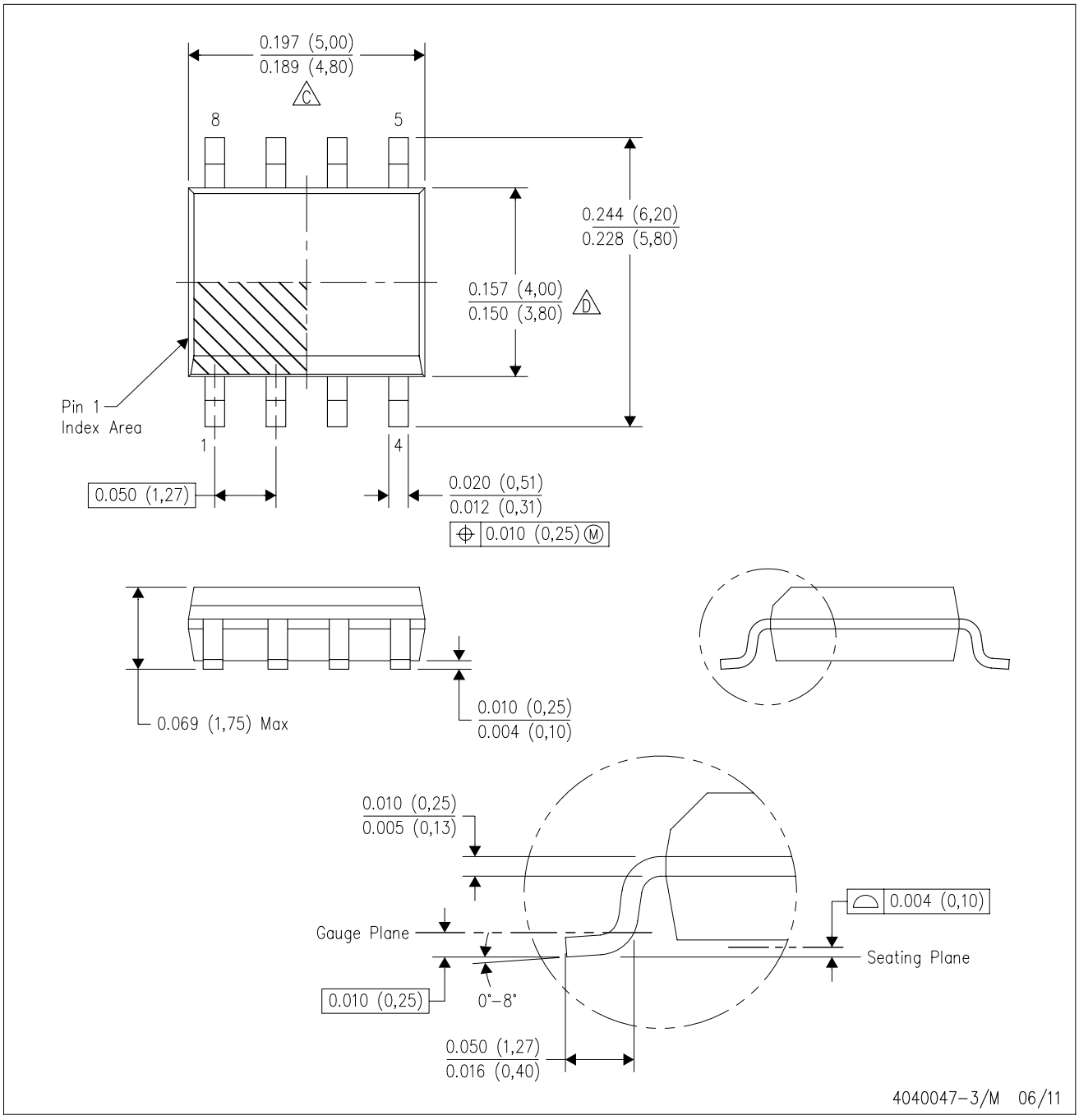
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



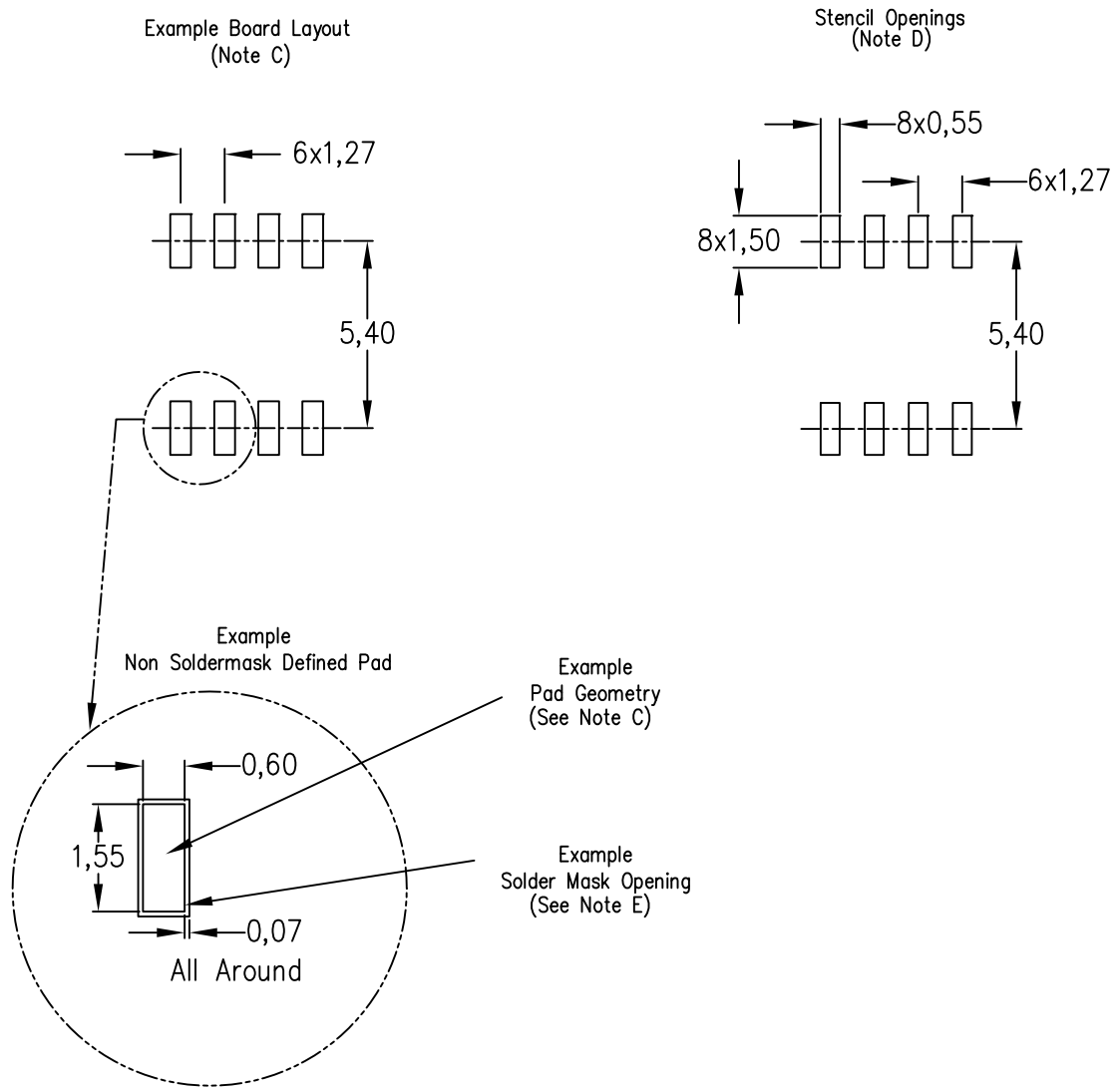
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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