

# Infineon<sup>®</sup> LITIX<sup>™</sup> Basic

## TLD1313EL

3 Channel High Side Current Source

Data Sheet

Rev. 1.1, 2015-03-24

Automotive

<b>1</b>	<b>Overview</b>	<b>3</b>
<b>2</b>	<b>Block Diagram</b>	<b>5</b>
<b>3</b>	<b>Pin Configuration</b>	<b>6</b>
3.1	Pin Assignment	6
3.2	Pin Definitions and Functions	7
<b>4</b>	<b>General Product Characteristics</b>	<b>8</b>
4.1	Absolute Maximum Ratings	8
4.2	Functional Range	9
4.3	Thermal Resistance	9
<b>5</b>	<b>EN Pin</b>	<b>10</b>
5.1	EN Function	10
5.2	Internal Supply Pin	11
5.3	EN Unused	12
5.3.1	EN - Pull Up to VS	12
5.3.2	EN - Direct Connection to VS	12
5.4	Electrical Characteristics Internal Supply / EN Pin	13
<b>6</b>	<b>IN_SET Pin</b>	<b>15</b>
6.1	Output Current Adjustment via RSET	15
6.2	Smart Input Pin	15
<b>7</b>	<b>ST Pin</b>	<b>18</b>
7.1	Diagnosis Selector	18
7.2	Diagnosis Output	18
7.3	Disable Input	18
<b>8</b>	<b>Load Diagnosis</b>	<b>20</b>
8.1	Open Load	20
8.2	Short Circuit to GND detection	21
8.3	Double Fault Conditions	23
8.4	Electrical Characteristics IN_SET Pin and Load Diagnosis	23
<b>9</b>	<b>Power Stage</b>	<b>25</b>
9.1	Protection	25
9.1.1	Over Load Behavior	25
9.1.2	Reverse Battery Protection	25
9.2	Electrical Characteristics Power Stage	26
<b>10</b>	<b>Application Information</b>	<b>28</b>
10.1	Further Application Information	28
<b>11</b>	<b>Package Outlines</b>	<b>29</b>
<b>12</b>	<b>Revision History</b>	<b>30</b>



## 1 Overview

### Features

- 3 Channel device with integrated output stages (current sources), optimized to drive LEDs
- Output current up to 120mA per channel
- Low current consumption in sleep mode
- PWM-operation supported via VS- and EN-pin
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection
- Overload protection
- Undervoltage detection
- Open load and short circuit to GND diagnosis
- Wide temperature range:  $-40\text{ °C} < T_j < 150\text{ °C}$
- PG-SSOP14 package with exposed heatslug
- Green Product (RoHS compliant)
- AEC Qualified



**PG-SSOP14**

### Description

The LITIX™ Basic TLD1313EL is a three channel high side driver IC with integrated output stages. It is designed to control LEDs with a current up to 120 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs per chain (total 9 LEDs) with a current up to 60mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

**Table 1 Product Summary**

Operating voltage	$V_{S(nom)}$	5.5 V... 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUTx(max)}$	40 V
Nominal output (load) current	$I_{OUTx(nom)}$	60 mA when using a supply voltage range of 8V - 18V (e.g. Automotive car battery). Currents up to $I_{OUT(max)}$ possible in applications with low thermal resistance $R_{thJA}$
Maximum output (load) current	$I_{OUTx(max)}$	120 mA; depending on thermal resistance $R_{thJA}$
Output current accuracy at $R_{SET} = 12\text{ k}\Omega$	$k_{LT}$	$750 \pm 7\%$
Current consumption in sleep mode	$I_{S(sleep,typ)}$	0.1 $\mu$ A

Type	Package	Marking
TLD1313EL	PG-SSOP14	TLD1313EL

**Protective functions**

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

**Diagnostic functions**

- OL detection
- SC to Vs (indicated by OL diagnosis)
- SC to GND detection

**Applications**

Designed for exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...

The device is also well suited for interior LED lighting applications such as ambient lighting, interior illumination and dash board lighting.

## 2 Block Diagram

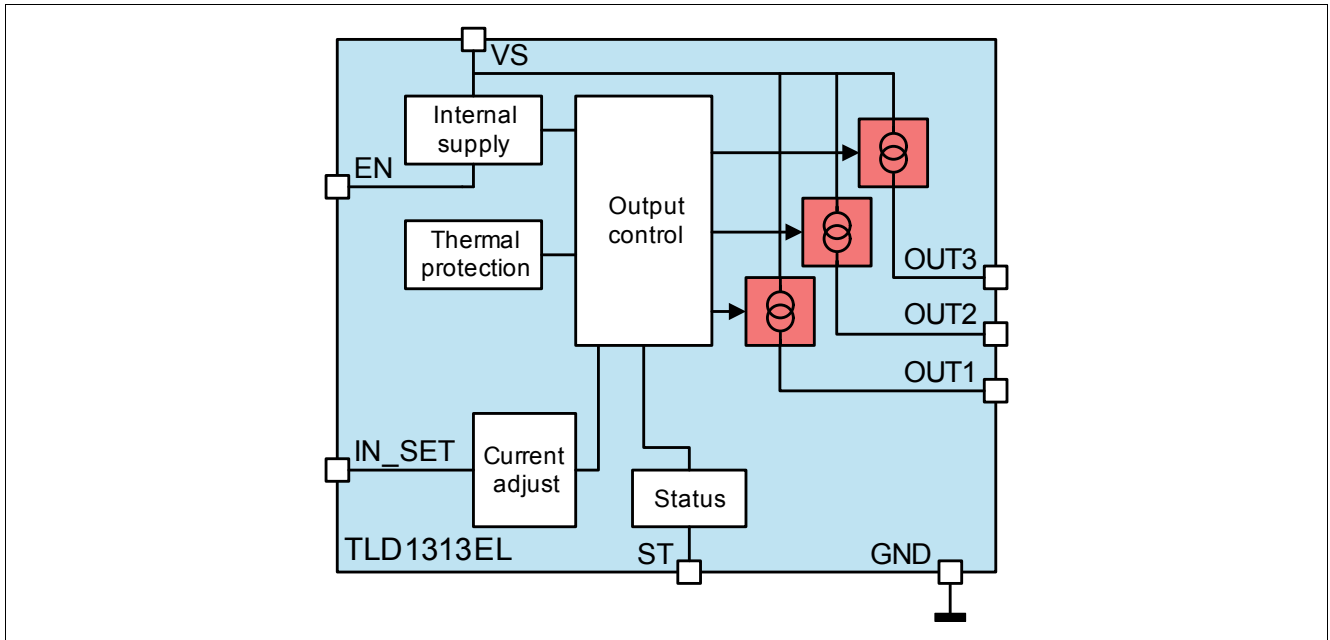


Figure 1 Basic Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment

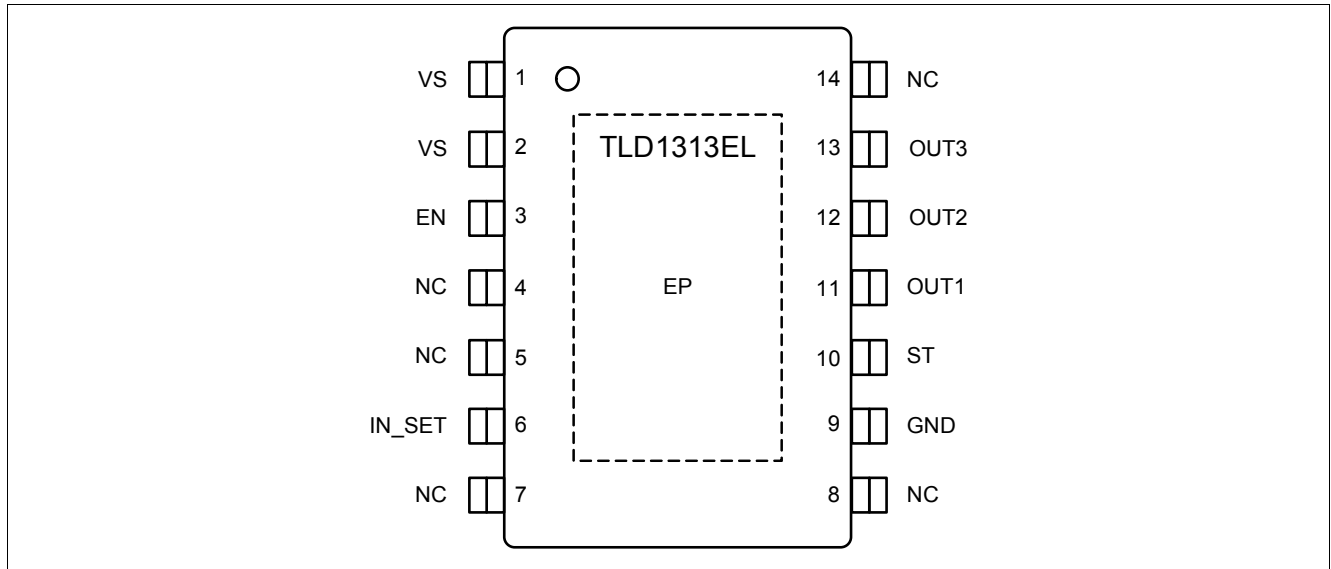


Figure 2 Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	<b>Supply Voltage</b> ; battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	EN	I	<b>Enable pin</b>
4	NC	–	<b>Pin not connected</b>
5	NC	–	<b>Pin not connected</b>
6	IN_SET	I/O	<b>Input / SET pin</b> ; Connect a low power resistor to adjust the output current
8	NC	–	<b>Pin not connected</b>
9	GND	–	<sup>1)</sup> <b>Ground</b>
10	ST	I/O	<b>Status pin</b>
11	OUT1	O	<b>Output 1</b>
12	OUT2	O	<b>Output 2</b>
13	OUT3	O	<b>Output 3</b>
14	NC	–	<b>Pin not connected</b>
Exposed Pad	GND	–	<sup>1)</sup> <b>Exposed Pad</b> ; connect to GND in application

1) Connect all GND-pins together.

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Supply voltage	$V_S$	-16	40	V	–
4.1.2	Input voltage EN	$V_{EN}$	-16	40	V	–
4.1.3	Input voltage EN related to $V_S$	$V_{EN(VS)}$	$V_S - 40$	$V_S + 16$	V	–
4.1.4	Input voltage EN related to $V_{OUTx}$	$V_{EN} - V_{OUTx}$	-16	40	V	–
4.1.5	Output voltage	$V_{OUTx}$	-1	40	V	–
4.1.6	Power stage voltage	$V_{PS} = V_S - V_{OUTx}$	-16	40	V	–
4.1.7	IN_SET voltage	$V_{IN\_SET}$	-0.3	6	V	–
4.1.8	Status voltage	$V_{ST}$	-0.3	6	V	–
<b>Currents</b>						
4.1.9	IN_SET current	$I_{IN\_SET}$	–	2 8	mA	– Diagnosis output
4.1.10	Output current	$I_{OUTx}$	–	130	mA	–
<b>Temperatures</b>						
4.1.11	Junction temperature	$T_j$	-40	150	°C	–
4.1.12	Storage temperature	$T_{stg}$	-55	150	°C	–
<b>ESD Susceptibility</b>						
4.1.13	ESD resistivity to GND	$V_{ESD}$	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ) <sup>2)</sup>
4.1.14	ESD resistivity all pins to GND	$V_{ESD}$	-500	500	V	CDM <sup>3)</sup>
4.1.15	ESD resistivity corner pins to GND	$V_{ESD}$	-750	750	V	CDM <sup>3)</sup>

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model "HBM" according to ANSI/ESDA/JEDEC JS-001-2011

3) ESD susceptibility, Charged Device Model "CDM" according to JESD22-C101E

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*



## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.16	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.17	Power on reset threshold	$V_{S(POR)}$	–	5	V	$V_{EN} = V_S$ $R_{SET} = 12\text{ k}\Omega$ $I_{OUTx} = 80\% I_{OUTx(nom)}$ $V_{OUTx} = 2.5\text{ V}$
4.2.18	Junction temperature	$T_j$	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	$R_{thJC}$	–	8	10	K/W	<sup>1) 2)</sup>
4.3.2	Junction to Ambient 1s0p board	$R_{thJA1}$	–	61	–	K/W	<sup>1) 3)</sup> $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	56	–		
4.3.3	Junction to Ambient 2s2p board	$R_{thJA2}$	–	45	–	K/W	<sup>1) 4)</sup> $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	43	–		

- 1) Not subject to production test, specified by design. Based on simulation results.
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature).  $T_a = 85\text{ °C}$ , Total power dissipation 1.5 W.
- 3) The  $R_{thJA}$  values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 70µm Cu, 300 mm<sup>2</sup> cooling area. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.
- 4) The  $R_{thJA}$  values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogeneously over all power stages.

## 5 EN Pin

The EN pin is a dual function pin:

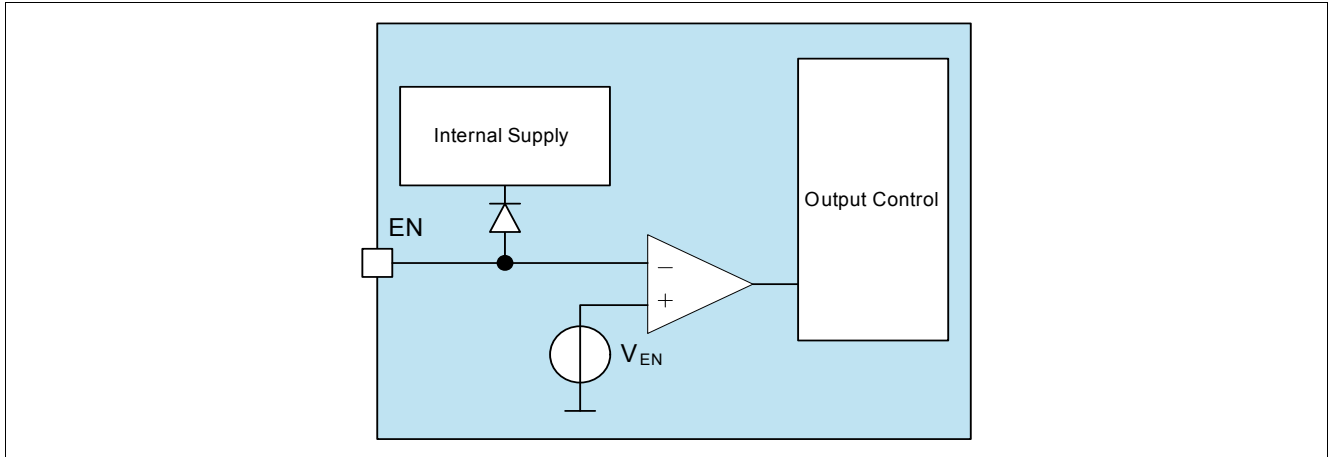


Figure 3 Block Diagram EN pin

Note: The current consumption at the EN-pin  $I_{EN}$  needs to be added to the total device current consumption. The total current consumption is the sum of the currents at the VS-pin  $I_S$  and the EN-pin  $I_{EN}$ .

### 5.1 EN Function

If the voltage at the pin EN is below a threshold of  $V_{EN(off)}$  the LITIX™ Basic IC will enter Sleep mode. In this state all internal functions are switched off, the current consumption is reduced to  $I_{S(sleep)}$ . A voltage above  $V_{EN(on)}$  at this pin enables the device after the Power on reset time  $t_{POR}$ .

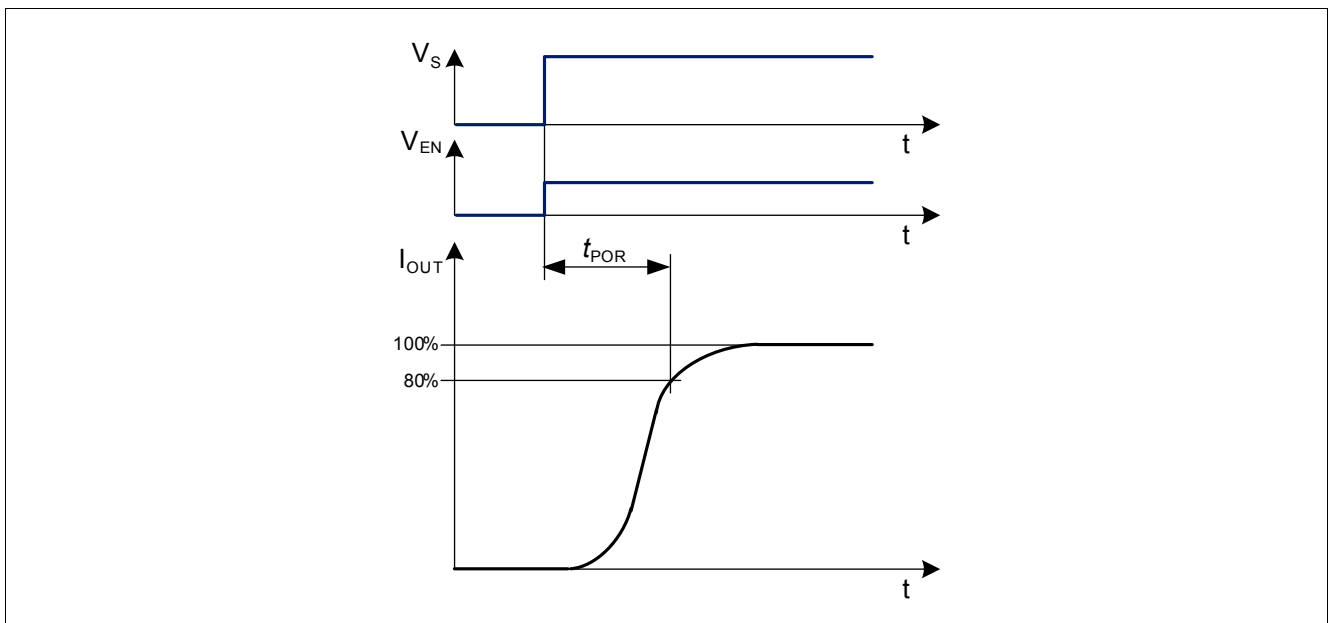


Figure 4 Power on reset

## 5.2 Internal Supply Pin

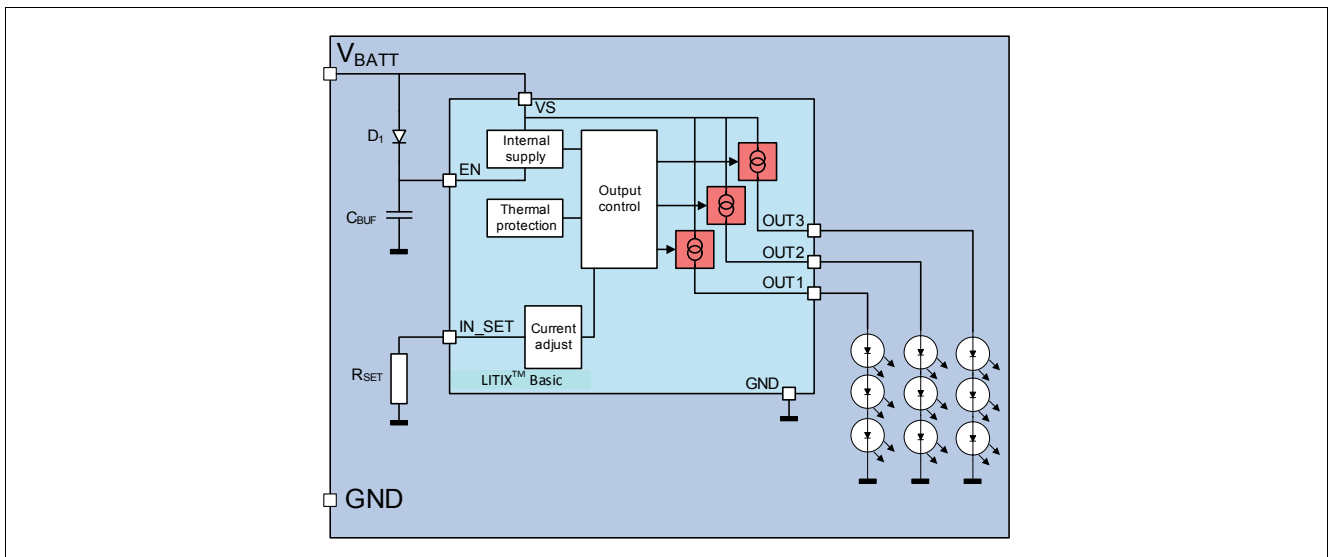
The EN pin can be used to supply the internal logic. There are two typical application conditions, where this feature can be used:

- 1) In “DC/DC control Buck” configurations, where the voltage  $V_s$  can be below 5.5V.
- 2) In configurations, where a PWM signal is applied at the Vbatt pin of a light module. The buffer capacitor  $C_{BUF}$  is used to supply the LITIX™ Basic IC during Vbatt low ( $V_s$  low) periods. This feature can be used to minimize the turn-on time to the values specified in **Pos. 9.2.13**. Otherwise, the power-on reset delay time  $t_{POR}$  (**Pos. 5.4.7**) has to be considered.

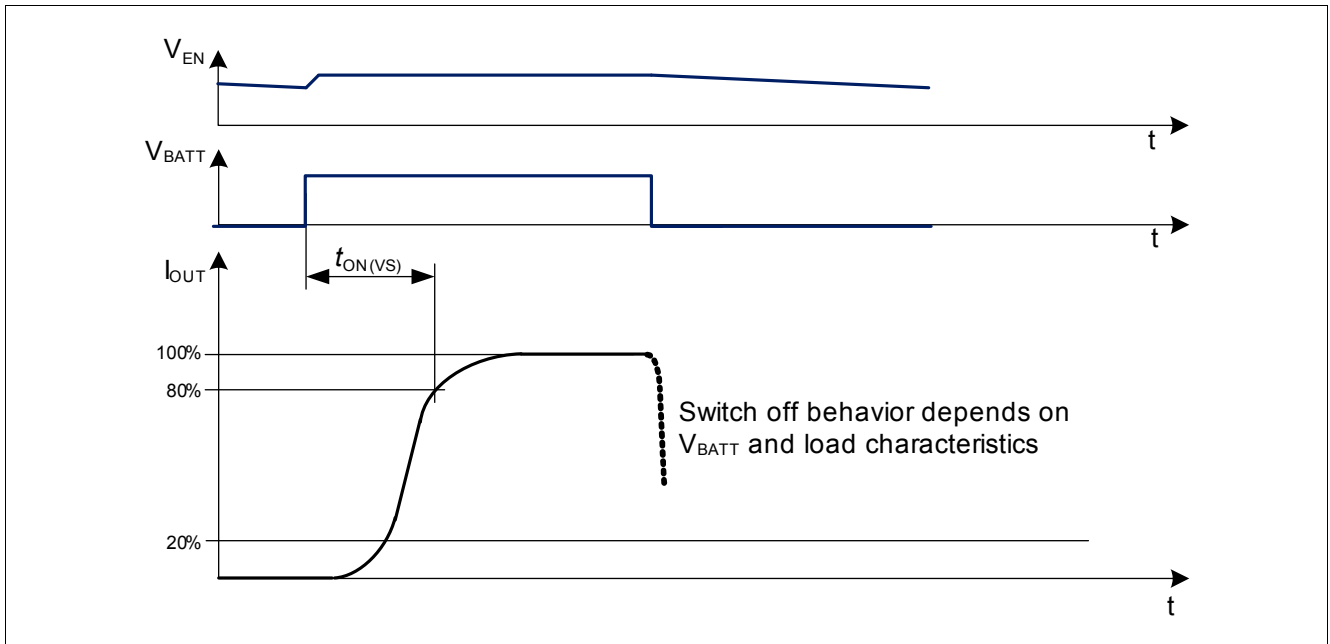
The capacitor can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(LS)}}{V_s - V_{D1} - V_{S(POR)}} \quad (1)$$

See also a typical application drawing in **Chapter 10**.



**Figure 5** External circuit when applying a fast PWM signal on  $V_{BATT}$



**Figure 6** Typical waveforms when applying a fast PWM signal on  $V_{BATT}$

The parameter  $t_{ON(VS)}$  is defined at [Pos. 9.2.13](#). The parameter  $t_{OFF(VS)}$  depends on the load and supply voltage  $V_{BATT}$  characteristics.

### 5.3 EN Unused

In case of an unused EN pin, there are two different ways to connect it:

#### 5.3.1 EN - Pull Up to VS

The EN pin can be connected with a pull up resistor (e.g. 10 k $\Omega$ ) to  $V_s$  potential. In this configuration the LITIX™ Basic IC is always enabled.

#### 5.3.2 EN - Direct Connection to VS

The EN pin can be connected directly to the VS pin (IC always enabled). This configuration has the advantage (compared to the configuration described in [Chapter 5.3.1](#)) that no additional external component is required.

## 5.4 Electrical Characteristics Internal Supply / EN Pin

### Electrical Characteristics Internal Supply / EN pin

Unless otherwise specified:  $V_S = 5.5 \text{ V to } 40 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ,  $R_{SET} = 12 \text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Current consumption, sleep mode	$I_{S(\text{sleep})}$	–	0.1	2	$\mu\text{A}$	<sup>1)</sup> $V_{EN} = 0.5 \text{ V}$ $T_j < 85 \text{ }^\circ\text{C}$ $V_S = 18 \text{ V}$ $V_{OUTx} = 3.6 \text{ V}$
5.4.2	Current consumption, active mode	$I_{S(\text{on})}$	–	–	–	$\text{mA}$	<sup>2)</sup> $I_{IN\_SET} = 0 \text{ }\mu\text{A}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_S = 18 \text{ V}$ $V_{OUTx} = 3.6\text{V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ <sup>1)</sup> $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
5.4.3	Current consumption, device disabled via ST	$I_{S(\text{dis,ST})}$	–	–	–	$\text{mA}$	<sup>2)</sup> $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{ST} = 5 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ <sup>1)</sup> $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
5.4.4	Current consumption, device disabled via IN_SET	$I_{S(\text{dis,IN\_SET})}$	–	–	–	$\text{mA}$	<sup>2)</sup> $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{IN\_SET} = 5 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ <sup>1)</sup> $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
5.4.5	Current consumption, active mode in single fault detection condition with ST-pin unconnected	$I_{S(\text{fault,STu})}$	–	–	–	$\text{mA}$	<sup>2)</sup> $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $R_{SET} = 12 \text{ k}\Omega$ $V_{OUTx} = 18 \text{ V or } 0 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ <sup>1)</sup> $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin

**Electrical Characteristics Internal Supply / EN pin (cont'd)**

Unless otherwise specified:  $V_S = 5.5\text{ V to }40\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $R_{SET} = 12\text{ k}\Omega$  all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.6	Current consumption, active mode in single fault detection condition with ST-pin connected to GND	$I_{S(\text{fault,STG})}$	–	–	6.0 4.9 5.9	mA	<sup>2)</sup> $V_S = 18\text{ V}$ $T_j < 105\text{ °C}$ $R_{SET} = 12\text{ k}\Omega$ $V_{OUTx} = 18\text{ V or }0\text{ V}$ $V_{ST} = 0\text{ V}$ $V_{EN} = 5.5\text{ V}$ $V_{EN} = 18\text{ V}$ <sup>1)</sup> $R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin
5.4.7	Power-on reset delay time <sup>3)</sup>	$t_{POR}$	–	–	25	$\mu\text{s}$	<sup>1)</sup> $V_S = V_{EN} = 0 \rightarrow 13.5\text{ V}$ $V_{OUTx(\text{nom})} = 3.6 \pm 0.3\text{ V}$ $I_{OUTx} = 80\% I_{OUTx(\text{nom})}$
5.4.8	Required supply voltage for output activation	$V_{S(\text{on})}$	–	–	4	V	$V_{EN} = 5.5\text{ V}$ $V_{OUTx} = 3\text{ V}$ $I_{OUTx} = 50\% I_{OUTx(\text{nom})}$
5.4.9	Required supply voltage for current control	$V_{S(\text{CC})}$	–	–	5.2	V	$V_{EN} = 5.5\text{ V}$ $V_{OUTx} = 3.6\text{ V}$ $I_{OUTx} \geq 90\% I_{OUTx(\text{nom})}$
5.4.10	EN turn on threshold	$V_{EN(\text{on})}$	–	–	2.5	V	–
5.4.11	EN turn off threshold	$V_{EN(\text{off})}$	0.8	–	–	V	–
5.4.12	EN input current during low supply voltage	$I_{EN(\text{LS})}$	–	–	1.8	mA	<sup>1)</sup> $V_S = 4.5\text{ V}$ $T_j < 105\text{ °C}$ $V_{EN} = 5.5\text{ V}$
5.4.13	EN high input current	$I_{EN(\text{H})}$	–	–	0.1 0.1 1.65 0.45	mA	$T_j < 105\text{ °C}$ $V_S = 13.5\text{ V}, V_{EN} = 5.5\text{ V}$ $V_S = 18\text{ V}, V_{EN} = 5.5\text{ V}$ $V_S = V_{EN} = 18\text{ V}$ <sup>1)</sup> $V_S = 18\text{ V}, R_{EN} = 10\text{ k}\Omega$ between VS and EN-pin

1) Not subject to production test, specified by design

2) The total device current consumption is the sum of the currents  $I_S$  and  $I_{EN(\text{H})}$ , please refer to **Pos. 5.4.13**

3) See also **Figure 4**

## 6 IN\_SET Pin

The IN\_SET pin is a multiple function pin for output current definition, input and diagnostics:

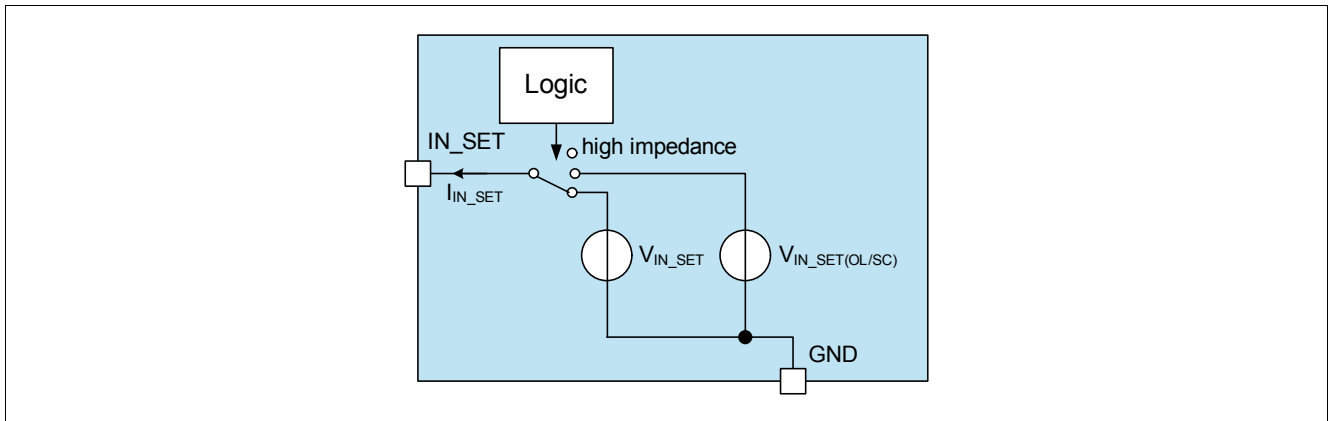


Figure 7 Block Diagram IN\_SET pin

### 6.1 Output Current Adjustment via RSET

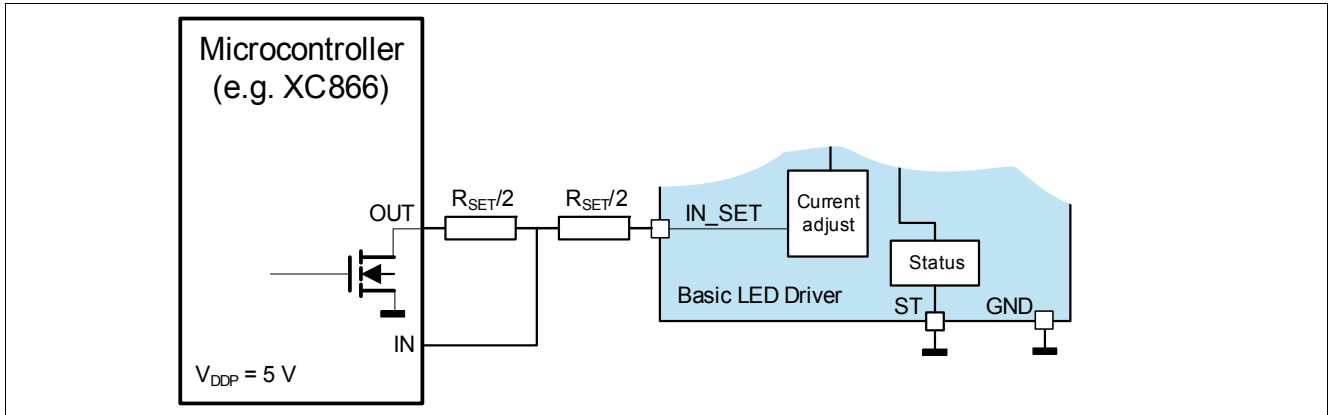
The output current for all three channels can only be adjusted simultaneously. The current adjustment can be done by placing a low power resistor ( $R_{SET}$ ) at the IN\_SET pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (2)$$

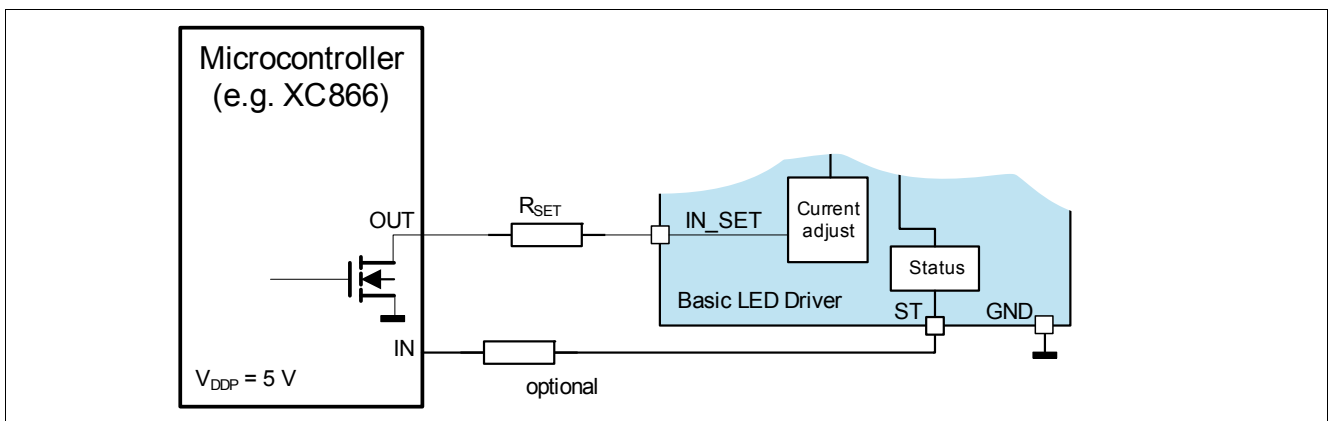
The gain factor  $k$  ( $R_{SET}$  \* output current) is specified in [Pos. 9.2.4](#) and [Pos. 9.2.5](#). The current through the  $R_{SET}$  is defined by the resistor itself and the reference voltage  $V_{IN\_SET(ref)}$ , which is applied to the IN\_SET during supplied device.

### 6.2 Smart Input Pin

The IN\_SET pin can be connected via  $R_{SET}$  to the open-drain output of a  $\mu C$  or to an external NMOS transistor as described in [Figure 8](#). This signal can be used to turn off the output stages of the IC. A minimum IN\_SET current of  $I_{IN\_SET(act)}$  is required to turn on the output stages. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN\_SET pin, see [Figure 11](#) for details. In addition, the IN\_SET pin offers the diagnostic feedback information, if the status pin is connected to GND. Another diagnostic possibility is shown in [Figure 9](#), where the diagnosis information is provided via the ST pin (refer to [Chapter 7](#) and [Chapter 8](#)) to a micro controller. In case of a fault event with the ST pin connected to GND the IN\_SET voltage is increased to  $V_{IN\_SET(OL/SC)}$  [Pos. 8.4.2](#). Therefore, the device has two voltage domains at the IN\_SET-pin, which is shown in [Figure 12](#).

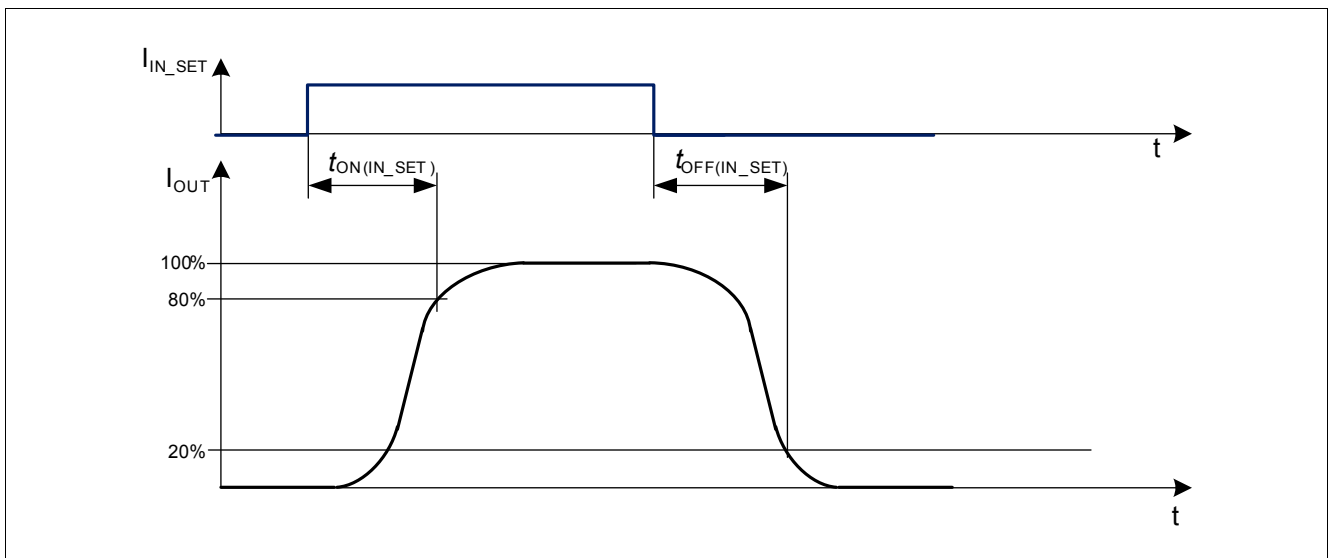


**Figure 8** Schematics IN\_SET interface to  $\mu$ C, diagnosis via IN\_SET pin



**Figure 9** Schematics IN\_SET interface to  $\mu$ C, diagnosis via ST pin

The resulting switching times are shown in [Figure 10](#):



**Figure 10** Switching times via IN\_SET



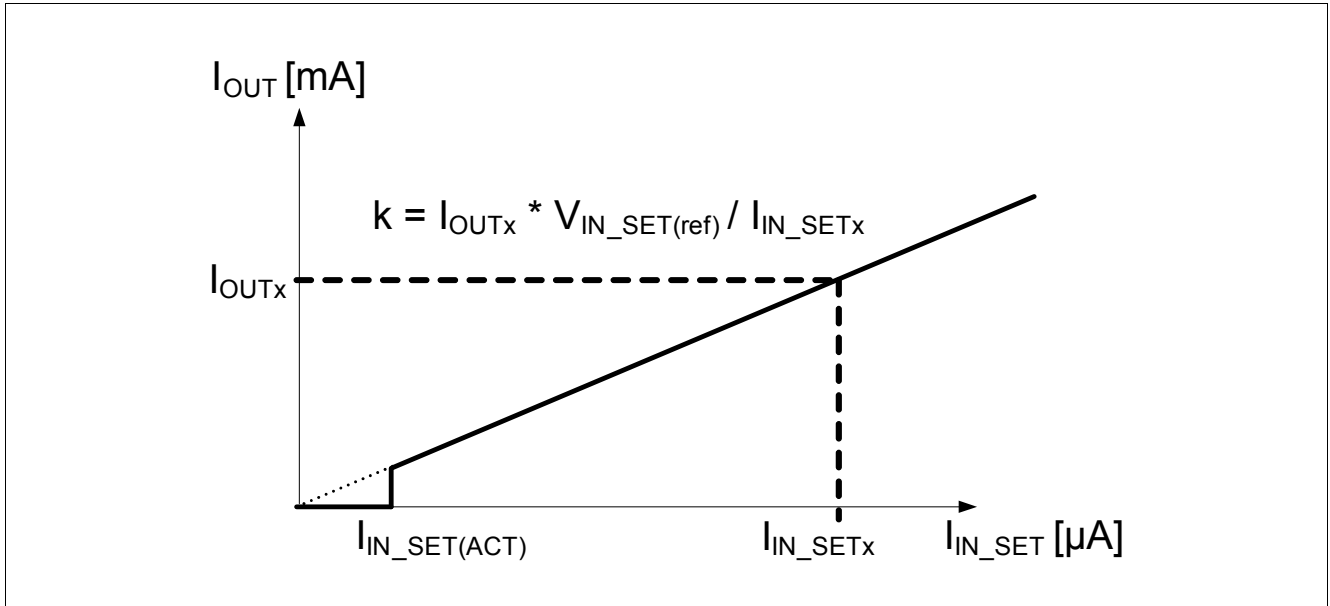


Figure 11  $I_{OUT}$  versus  $I_{INSET}$

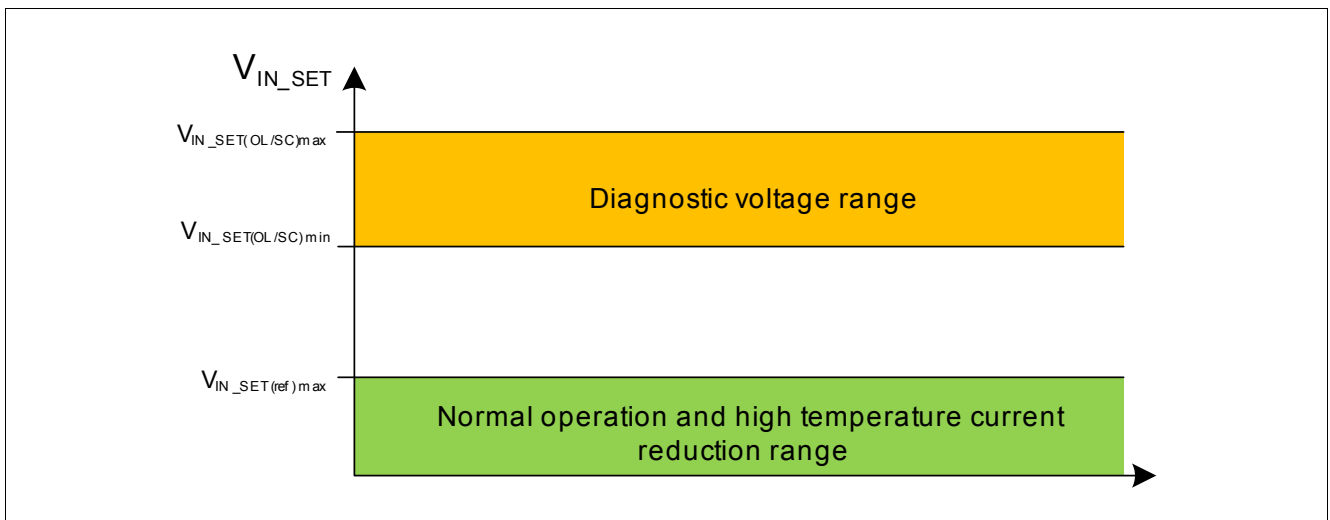


Figure 12 Voltage domains for IN\_SET pin, if ST pin is connected to GND

## 7 ST Pin

The ST pin is a multiple function pin.

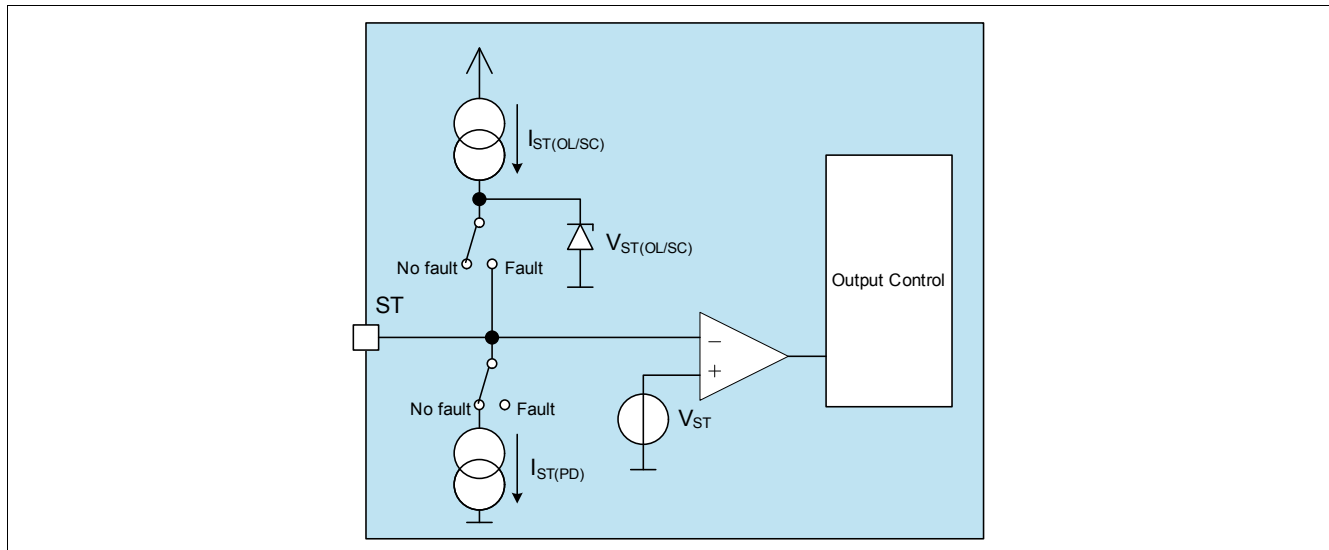


Figure 13 Block Diagram ST pin

### 7.1 Diagnosis Selector

If the status pin is unconnected or connected to GND via a high ohmic resistor ( $V_{ST}$  to be below  $V_{ST(L)}$ ), the ST pin acts as diagnosis output pin. In normal operation (device is activated) the ST pin is pulled to GND via the internal pull down current  $I_{ST(PD)}$ . In case of an open load or short circuit to GND condition the ST pin is switched to  $V_{ST(OL/SC)}$  after the open load or short circuit detection filter time (Pos. 8.4.9, Pos. 8.4.12).

If the device is operated in PWM operation via the VS and/or EN pins the ST pin should be connected to GND via a high ohmic resistor (e.g. 470k $\Omega$ ) to ensure proper device behavior during fast rising VS and/or EN slopes.

If the ST pin is shorted to GND the diagnostic feedback is performed via the IN\_SET-pin, which is shown in Chapter 6.2 and Chapter 8.

### 7.2 Diagnosis Output

If the status pin is unconnected or connected to GND via a high ohmic resistor ( $V_{ST}$  to be below  $V_{ST(L)}$ ), it acts as a diagnostic output. In case of a fault condition the ST pin rises its voltage to  $V_{ST(OL/SC)}$  (Pos. 8.4.7). Details are shown in Chapter 8.

### 7.3 Disable Input

If an external voltage higher than  $V_{ST(H)}$  (Pos. 8.4.5) is applied to the ST pin, the device is switched off. This function is used for applications, where multiple drivers should be used for one light function. It is possible to combine the drivers' fault diagnosis via the ST pins. If a single LED chain fails, the entire light function is switched off. In this scenario e.g. the diagnostic circuit on the body control module can easily distinguish between the two cases (normal load or load fault), because nearly no current is flowing into the LED module during the fault scenario - the drivers consume a current of  $I_{S(fault,STu)}$  (Pos. 5.4.5) or  $I_{S(dis,ST)}$  (Pos. 5.4.3).

As soon as one LED chain fails, the ST-pin of this device is switched to  $V_{ST(OL/SC)}$ . The other devices used for the same light function can be connected together via the ST pins. This leads to a switch off of all devices connected together. Application examples are shown in Chapter 10.

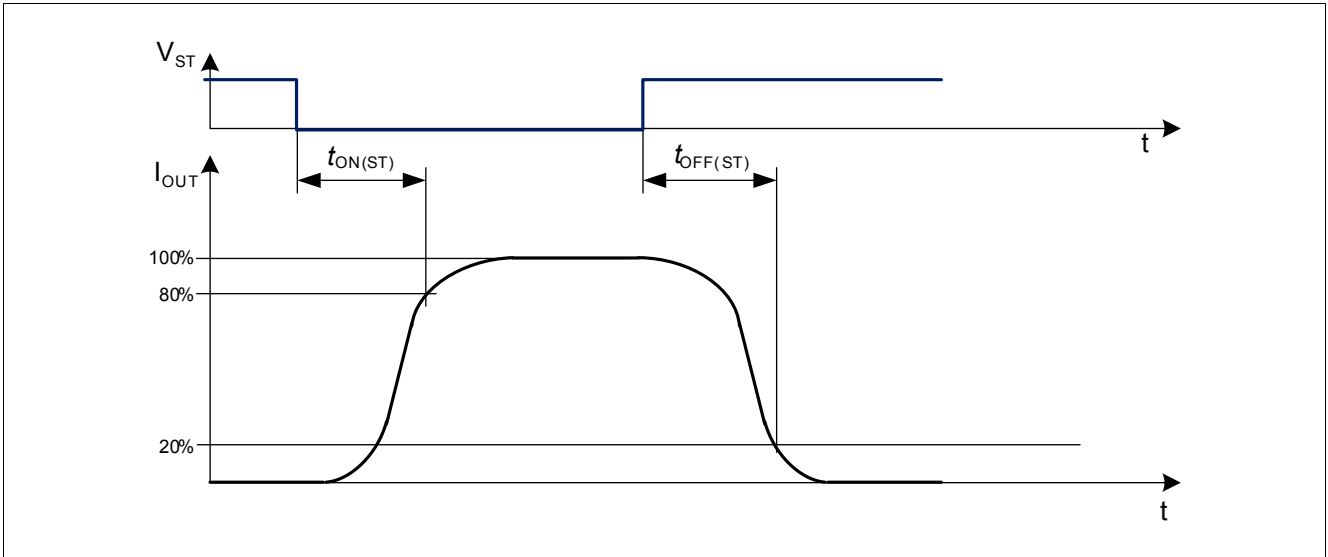


Figure 14 Switching times via ST Pin

## 8 Load Diagnosis

### 8.1 Open Load

An open load diagnosis feature is integrated in the TLD1313EL driver IC. If there is an open load on one of the outputs, the outputs are turned off. The potential on the IN\_SET pin rises up to  $V_{IN\_SET(OL/SC)}$ , if the ST is connected to GND. This high voltage can be used as input signal for a  $\mu C$  as shown in [Figure 9](#). If the ST pin is open or connected to GND via a high ohmic resistor, the ST pin rises to a high potential as described in [Chapter 7](#). More details are shown in [Figure 18](#). The open load status is not latched, as soon as the open load condition is no longer present, the output stage will be turned on again. An open load condition is detected, if the voltage drop over the output stage  $V_{PS}$  is below the threshold according [Pos. 8.4.10](#) and a filter time of  $t_{OL}$  is passed.

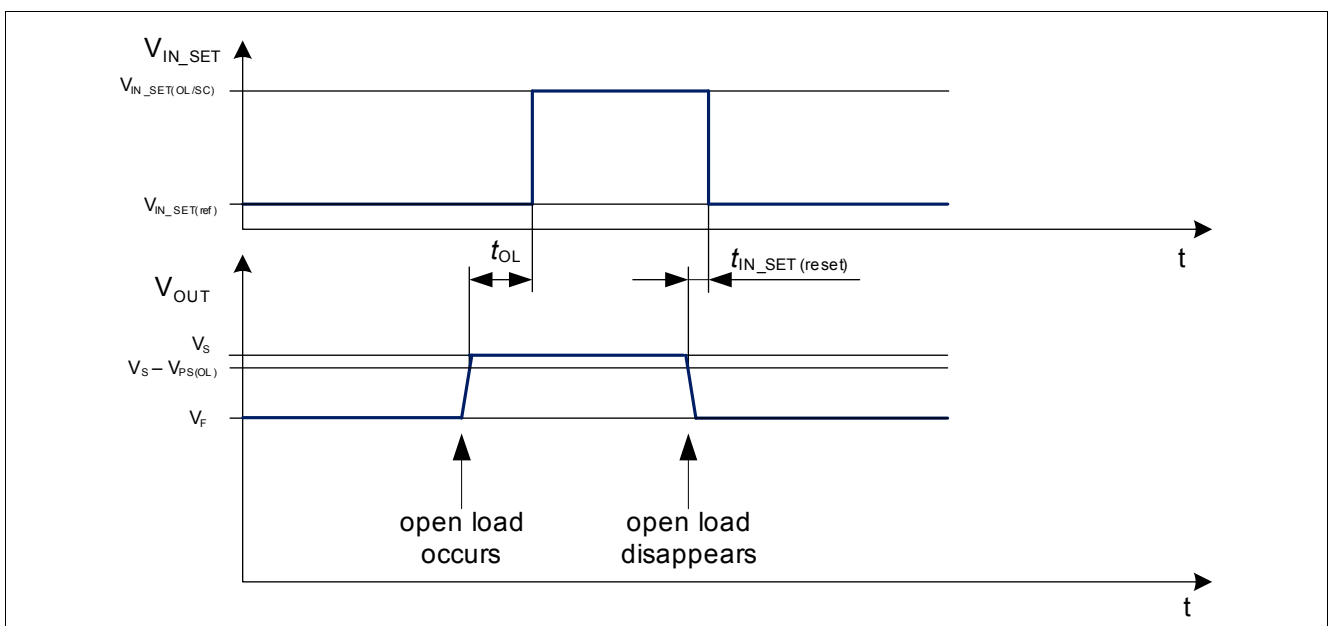


Figure 15 IN\_SET behavior during open load condition with ST pin connected to GND

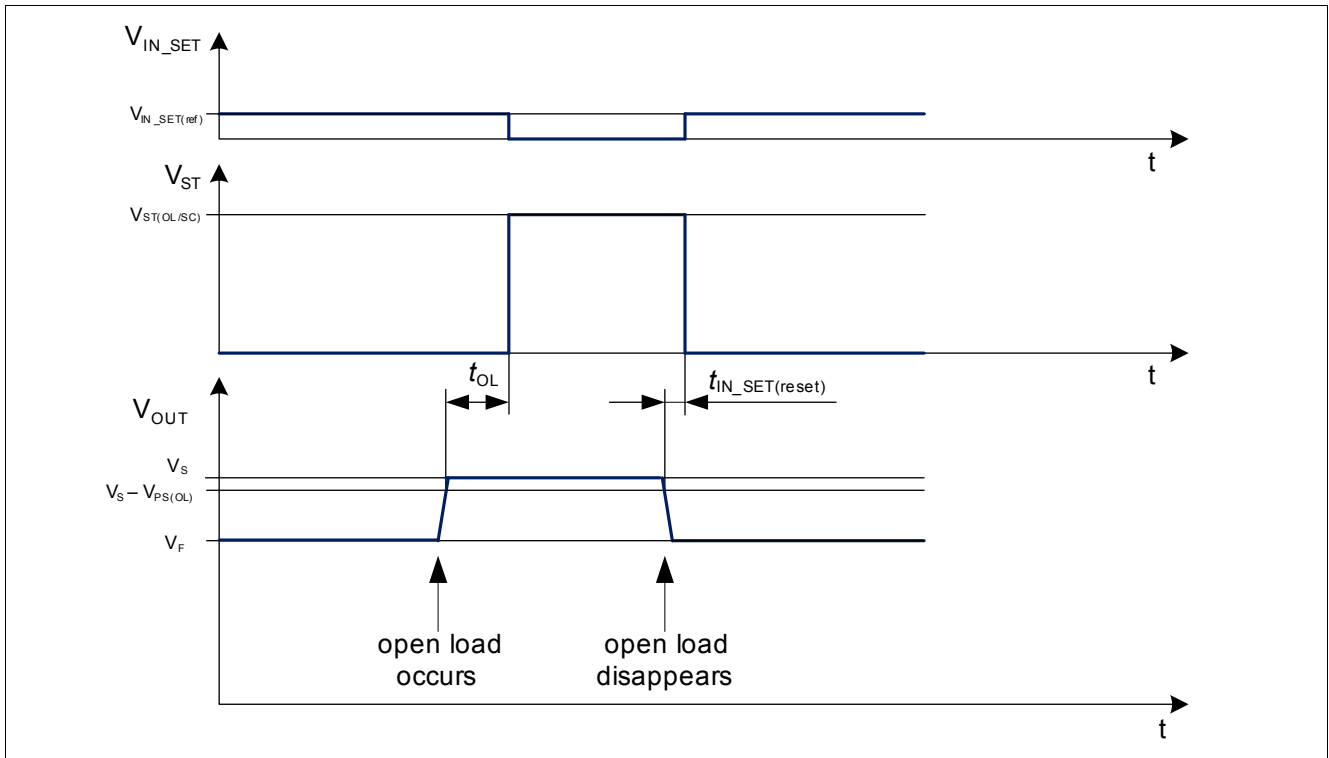


Figure 16 IN\_SET and ST behavior during open load condition (ST unconnected)

## 8.2 Short Circuit to GND detection

The TLD1313EL has an integrated SC to GND detection. If the output stage is turned on and the voltage at the output falls below  $V_{OUT(SC)}$  the potential on the IN\_SET pin is increased up to  $V_{IN\_SET(OL/SC)}$  after  $t_{SC}$ , if the ST pin is connected to GND. If the ST is open or connected to GND via a high ohmic resistor the fault is indicated on the ST pin according to [Chapter 7](#) after  $t_{SC}$ . More details are shown in [Figure 18](#). This condition is not latched. For detecting a normal condition after a short circuit detection an output current according to  $I_{OUT(SC)}$  is driven by the channel.

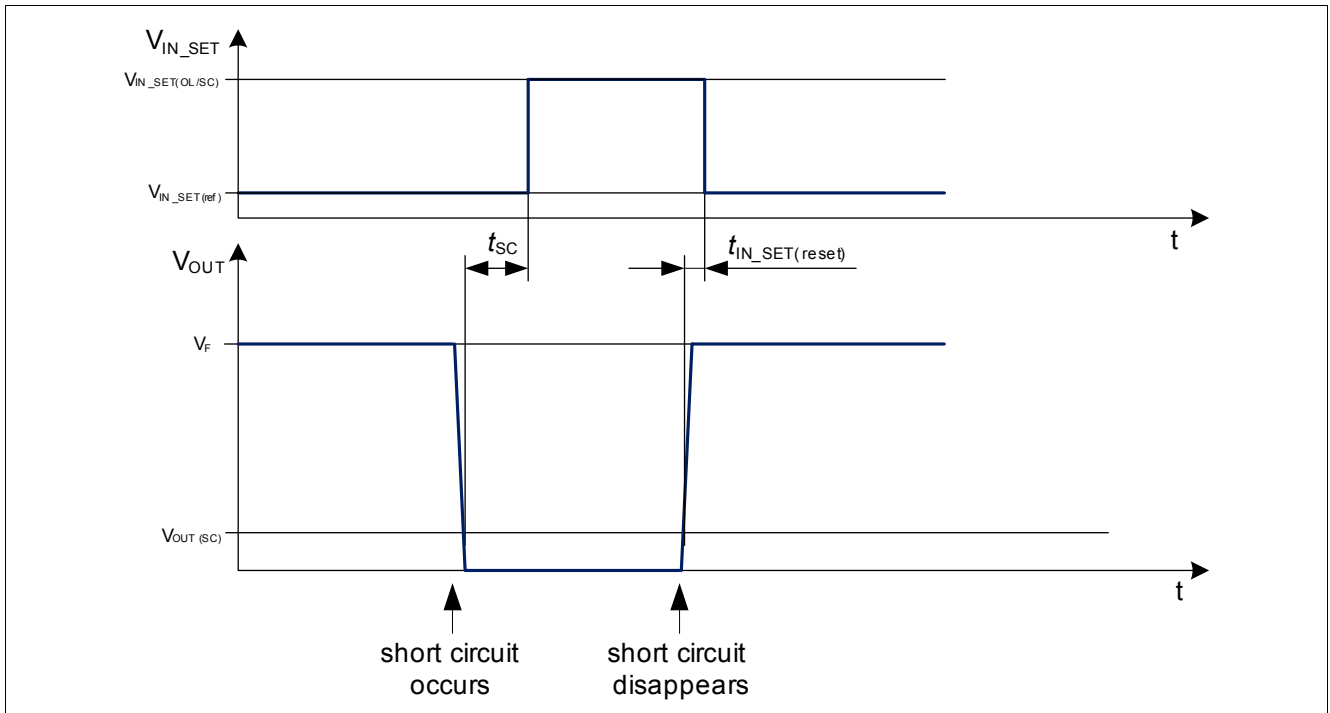


Figure 17  $V_{IN\_SET}$  behavior during short circuit to GND condition with ST connected to GND and  $V_{DEN} > V_{DEN(act)}$

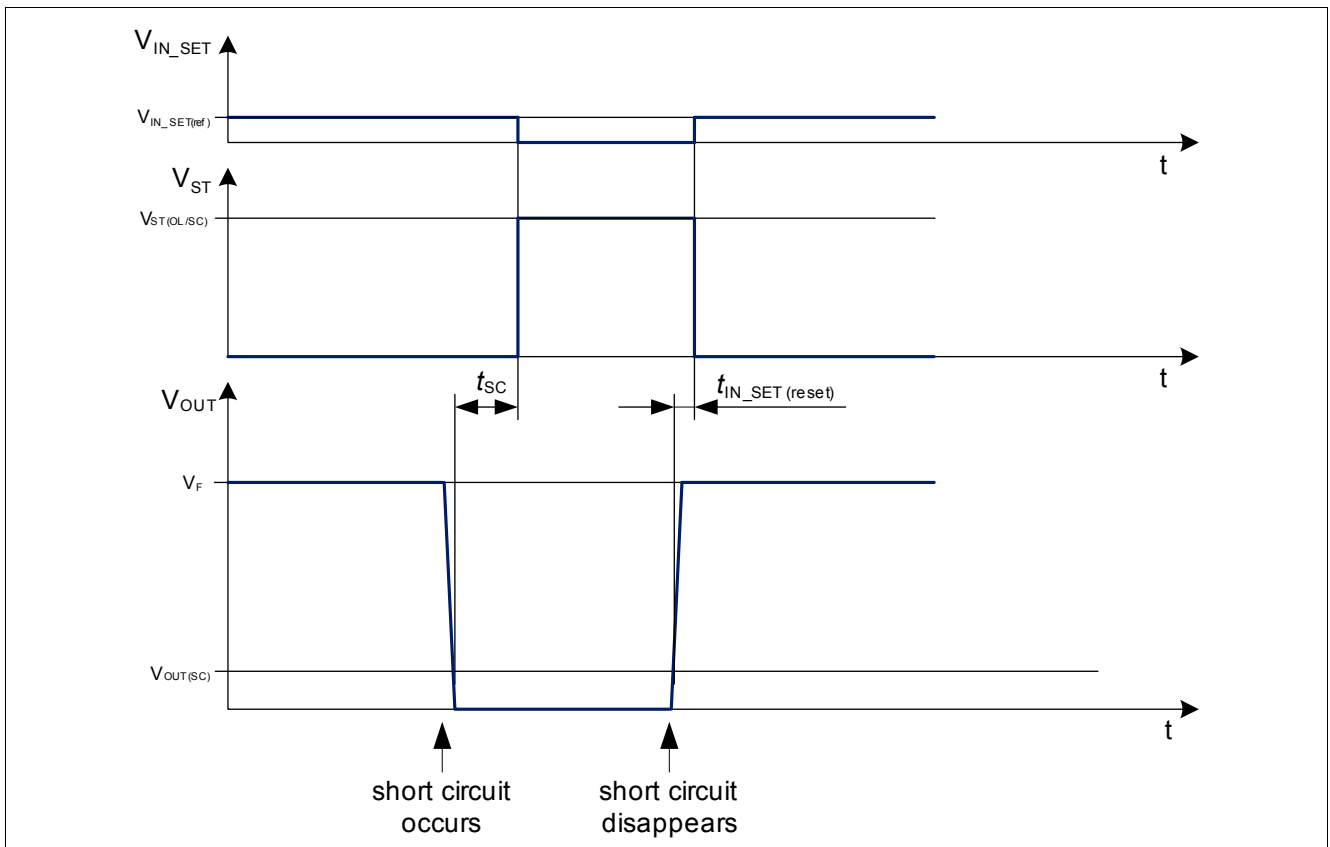


Figure 18  $V_{IN\_SET}$  and ST behavior during short circuit to GND condition (ST unconnected)

Note: In applications, where 1 output of the LITIX™ Basic IC is not used, a zener diode can be connected to the output to avoid unintended open load or short circuit conditions. The zener voltage should be in the range of the LEDs' forward voltage.

### 8.3 Double Fault Conditions

The TLD1313EL has an integrated double fault detection feature. This feature is implemented to detect significant supply voltage drops. During such supply voltage drops close to the forward voltage of the LEDs the drivers outputs remain active. In case of load faults on two or more outputs within the time period  $t_{OL}$  or  $t_{SC}$  (Pos. 8.4.9 and Pos. 8.4.12) the device disables the diagnosis to avoid any uncorrect open load diagnosis during low supply voltages close to the forward voltages of the connected LED chains. If the faults between two or three channels happen with a delay of longer than  $t_{OL}$  or  $t_{SC}$  the double fault detection feature is not active, i.e. the device is not turned on.

### 8.4 Electrical Characteristics IN\_SET Pin and Load Diagnosis

#### Electrical Characteristics IN\_SET pin and Load Diagnosis

Unless otherwise specified:  $V_S = 5.5 \text{ V to } 40 \text{ V}$ ,  $T_j = -40 \text{ °C to } +150 \text{ °C}$ ,  $R_{SET} = 12 \text{ k}\Omega$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.1	IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.19	1.23	1.27	V	<sup>1)</sup> $V_{OUTx} = 3.6 \text{ V}$ $T_j = 25...115 \text{ °C}$
8.4.2	IN_SET open load/short circuit voltage	$V_{IN\_SET(OL/SC)}$	4	–	5.5	V	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ °C}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.3	IN_SET open load/short circuit current	$I_{IN\_SET(OL/SC)}$	1.5	–	7.4	mA	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ °C}$ $V_{IN\_SET} = 4 \text{ V}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.4	ST device turn on threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(L)}$	0.8	–	–	V	–
8.4.5	ST device turn off threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(H)}$	–	–	2.5	V	–
8.4.6	ST pull down current	$I_{ST(PD)}$	–	–	15	$\mu\text{A}$	$V_{EN} = 5.5 \text{ V}$ $V_{ST} = 0.8 \text{ V}$

**Electrical Characteristics IN\_SET pin and Load Diagnosis (cont'd)**

Unless otherwise specified:  $V_S = 5.5 \text{ V to } 40 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$ ,  $R_{SET} = 12 \text{ k}\Omega$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.7	ST open load/short circuit voltage (ST-pin acting as diagnosis output)	$V_{ST(OL/SC)}$	4	–	5.5	V	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25 \dots 150 \text{ }^\circ\text{C}$ $R_{ST} = 470 \text{ k}\Omega$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.8	ST open load/short circuit current (ST-pin acting as diagnosis output)	$I_{ST(OL/SC)}$	100	–	220	$\mu\text{A}$	<sup>1)</sup> $V_S > 8 \text{ V}$ $T_j = 25 \dots 150 \text{ }^\circ\text{C}$ $V_{ST} = 2.5 \text{ V}$ $V_S = V_{OUTx} \text{ (OL) or } V_{OUTx} = 0 \text{ V (SC)}$
8.4.9	OL detection filter time	$t_{OL}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.10	OL detection voltage $V_{PS(OL)} = V_S - V_{OUTx}$	$V_{PS(OL)}$	0.2	–	0.4	V	$V_S > 8 \text{ V}$
8.4.11	Short circuit to GND detection threshold	$V_{OUT(SC)}$	0.8	–	1.4	V	$V_S > 8 \text{ V}$
8.4.12	SC detection filter time	$t_{SC}$	10	22	35	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.13	IN_SET diagnosis reset time	$t_{IN\_SET(reset)}$	–	5	20	$\mu\text{s}$	<sup>1)</sup> $V_S > 8 \text{ V}$
8.4.14	SC detection current in case of unconnected ST-pin	$I_{OUT(SC,STu)}$	100	200	300	$\mu\text{A}$	$V_S > 8 \text{ V}$ $V_{OUTx} = 0 \text{ V}$
8.4.15	SC detection current in case of ST-pin shorted to GND	$I_{OUT(SC,STG)}$	0.1	2	4.75	mA	$V_S > 8 \text{ V}$ $V_{OUTx} = 0 \text{ V}$ $V_{ST} = 0 \text{ V}$
8.4.16	IN_SET activation current without turn on of output stages	$I_{IN\_SET(act)}$	2	–	15	$\mu\text{A}$	See <a href="#">Figure 11</a>

1) Not subject to production test, specified by design



## 9 Power Stage

The output stages are realized as high side current sources with a current of 120 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

The maximum current of each channel is limited by the power dissipation and used PCB cooling areas (which results in the applications  $R_{thJA}$ ).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control  $V_{S(CC)}$ , **Pos. 5.4.9**
- Voltage drop over output stage during current control  $V_{PS(CC)}$ , **Pos. 9.2.6**
- Required output voltage for current control  $V_{OUTx(CC)}$ , **Pos. 9.2.7**

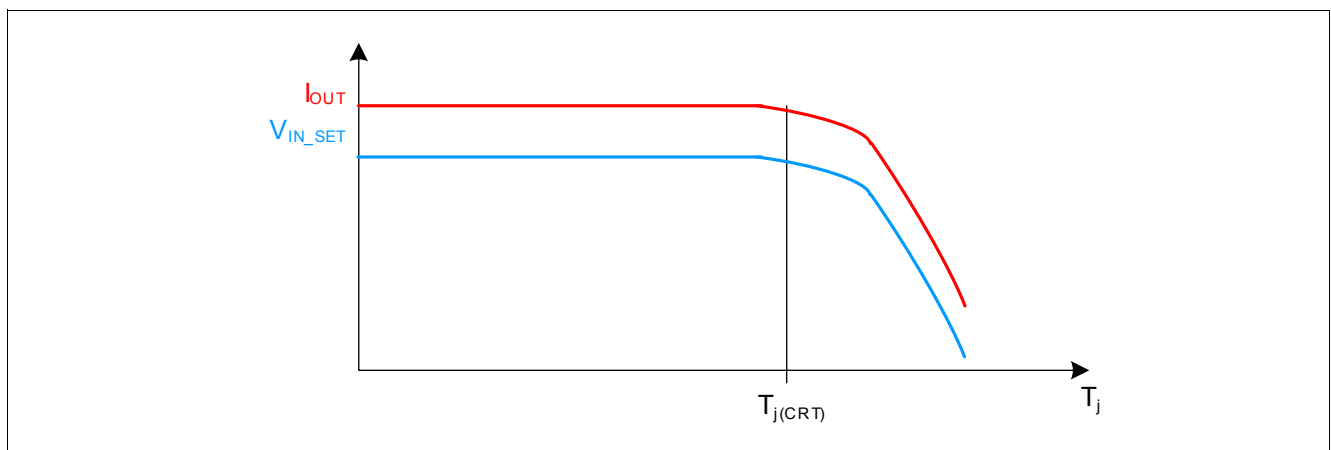
### 9.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

#### 9.1.1 Over Load Behavior

An over load detection circuit is integrated in the LITIX™ Basic IC. It is realized by a temperature monitoring of the output stages (OUTx).

As soon as the junction temperature exceeds the current reduction temperature threshold  $T_{j(CRT)}$  the output current will be reduced by the device by reducing the IN\_SET reference voltage  $V_{IN\_SET(ref)}$ . This feature avoids LED's flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the three output currents decrease close to 0 A. As soon as the device cools down the output currents rise again.



**Figure 19 Output current reduction at high temperature**

*Note: This high temperature output current reduction is realized by reducing the IN\_SET reference voltage (Pos. 8.4.1). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to  $I_{OUTx} = 0$  mA, after a slight cooling down the current increases again.*

#### 9.1.2 Reverse Battery Protection

The TLD1313EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to  $I_{OUTx(rev)}$  by the reverse battery protection.

Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.

## 9.2 Electrical Characteristics Power Stage

### Electrical Characteristics Power Stage

Unless otherwise specified:  $V_S = 5.5\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{OUTx} = 3.6\text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.1	Output leakage current	$I_{OUTx(leak)}$	– –	– –	7 3	μA	$V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\text{ μA}$ $V_{OUTx} = 2.5\text{ V}$ $T_j = 150\text{ °C}$ 1) $T_j = 85\text{ °C}$
9.2.2	Output leakage current in boost over battery setup	- $I_{OUTx(leak,B2B)}$	–	–	50	μA	1) $V_{EN} = 5.5\text{ V}$ $I_{IN\_SET} = 0\text{ μA}$ $V_{OUTx} = V_S = 40\text{ V}$
9.2.3	Reverse output current	$-I_{OUTx(rev)}$	–	–	1	μA	1) $V_S = -16\text{ V}$ Output load: LED with break down voltage < - 0.6 V
9.2.4	Output current accuracy limited temperature range	$k_{LT}$	697 645	750 750	803 855		1) $T_j = 25...115\text{ °C}$ $V_S = 8...18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SET} = 6...12\text{ k}\Omega$ $R_{SET} = 30\text{ k}\Omega$
9.2.5	Output current accuracy over temperature	$k_{ALL}$	697 645	750 750	803 855		1) $T_j = -40...115\text{ °C}$ $V_S = 8...18\text{ V}$ $V_{PS} = 2\text{ V}$ $R_{SET} = 6...12\text{ k}\Omega$ $R_{SET} = 30\text{ k}\Omega$
9.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUTx}$	$V_{PS(CC)}$	0.75	–	–	V	1) $V_S = 13.5\text{ V}$ $R_{SET} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.7	Required output voltage for current control	$V_{OUTx(CC)}$	2.3	–	–	V	1) $V_S = 13.5\text{ V}$ $R_{SET} = 12\text{ k}\Omega$ $I_{OUTx} \geq 90\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.8	Maximum output current	$I_{OUT(max)}$	120	–	–	mA	$R_{SET} = 4.7\text{ k}\Omega$ The maximum output current is limited by the thermal conditions. Please refer to <a href="#">Pos. 4.3.1 - Pos. 4.3.3</a>

**Electrical Characteristics Power Stage (cont'd)**

Unless otherwise specified:  $V_S = 5.5\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $V_{OUTx} = 3.6\text{ V}$ , all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.9	ST turn on time	$t_{ON(ST)}$	–	–	15	$\mu\text{s}$	<sup>2)</sup> $V_S = 13.5\text{ V}$ $R_{SET} = 12\text{ k}\Omega$ ST $\rightarrow$ L $I_{OUTx} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.10	ST turn off time	$t_{OFF(ST)}$	–	–	10	$\mu\text{s}$	<sup>2)</sup> $V_S = 13.5\text{ V}$ $R_{SET} = 12\text{ k}\Omega$ ST $\rightarrow$ H $I_{OUTx} = 20\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.11	IN_SET turn on time	$t_{ON(IN\_SET)}$	–	–	15	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $I_{IN\_SET} = 0 \rightarrow 100\text{ }\mu\text{A}$ $I_{OUTx} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.12	IN_SET turn off time	$t_{OFF(IN\_SET)}$	–	–	10	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $I_{IN\_SET} = 100 \rightarrow 0\text{ }\mu\text{A}$ $I_{OUTx} = 20\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.13	VS turn on time	$t_{ON(VS)}$	–	–	20	$\mu\text{s}$	<sup>1) 3)</sup> $V_{EN} = 5.5\text{ V}$ $R_{SET} = 12\text{ k}\Omega$ $V_S = 0 \rightarrow 13.5\text{ V}$ $I_{OUTx} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.14	Current reduction temperature threshold	$T_{j(CRT)}$	–	140	–	$^{\circ}\text{C}$	<sup>1)</sup> $I_{OUTx} = 95\%$ of $(k_{LT(typ)}/R_{SET})$
9.2.15	Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $(k_{LT(typ)}/R_{SET})$	–	–	A	<sup>1)</sup> $R_{SET} = 12\text{ k}\Omega$ $T_j = 150\text{ }^{\circ}\text{C}$

1) Not subject to production test, specified by design

2) see also [Figure 14](#)

3) see also [Figure 6](#)

## 10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

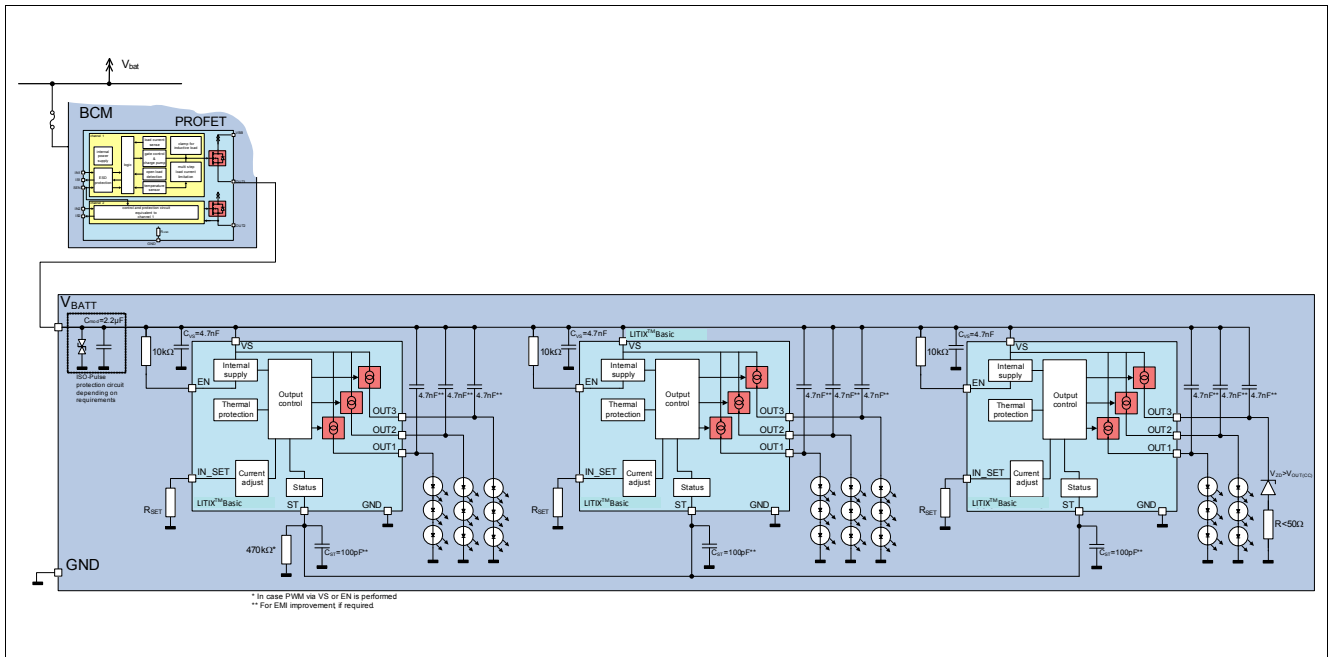


Figure 20 System Diagram TLD1313EL in combination with multiple devices and two channel usage for device at the right side

Note: This is a very simplified example of an application circuit. In case of high ISO-pulse requirements a reverse protection diode may be used for LED protection. The function must be verified in the real application.

### 10.1 Further Application Information

- For further information you may contact <http://www.infineon.com/>

## 11 Package Outlines

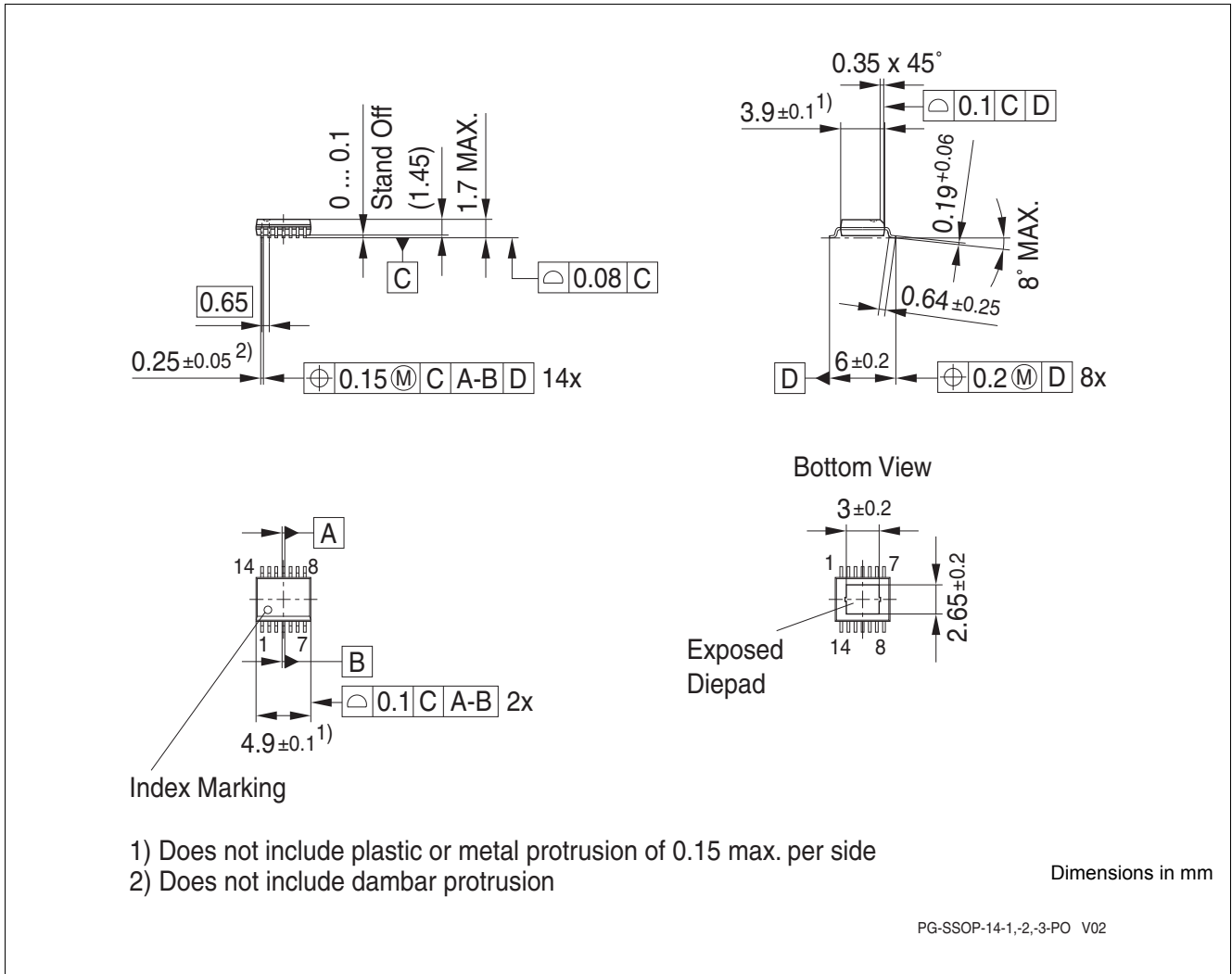


Figure 21 PG-SSOP14

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:

<http://www.infineon.com/packages>.

## 12 Revision History

Revision	Date	Changes
1.0	2013-08-08	Initial revision of data sheet
1.1	2015-03-19	Updated parameters $K_{LT}$ and $K_{ALL}$ in the chapter Power Stage.

**Edition 2015-03-24**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

**© 2015 Infineon Technologies AG  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.