TDP158 6-Gbps, AC-Coupled to TMDS™ or HDMI™ Redriver

1 Features

- AC-Coupled Receiver Supporting AC-Coupled HDMI or DP++ Signaling Data Rates up to 6 Gbps
- Transmitter is Compatible with HDMI TMDS Electrical Parameters up to 6 Gbps
- Support 4k2k60p and up to WUXGA 16-bit Color Depth or 1080p with Higher Refresh Rates.
- Programmable Fixed Receiver Equalizer up to 15 dB
- Global or Independent High Speed Lane Control
- I^2C or Pin Strap Programmable
- Transmitter Swing, Pre-emphasis, Slew Rate and Termination are Programmable by Pin Strapping or I^2C
- Configurable as a DisplayPort Redriver via I^2C
- 40-pin, 5 mm x 5 mm, 0.4 mm Pitch QFN Package
- Extended Commercial Temperature Support 0°C – 85°C (TDP158)
- Industrial Temperature support –40°C to 85°C (TDP158I)
- Pin Compatible to the SN65/75DP159RSB Retimer

2 Applications

- Notebook PC Market
- Audio/Video Equipment
- Blu-ray™ DVD
- Desktops/ All-in-Ones
- Tablet
- Gaming Systems

3 Description

The TDP158 device is an AC-Coupled HDMI signal to transition-minimized differential signal (TMDS) Redriver supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4b and 2.0b output signals. The TDP158 supports four TMDS channels and Digital Display Control (DDC) interfaces. The TDP158 supports signaling rates up to 6 Gbps to allow for the highest resolutions of 4k2k60p 24 bits per pixel and up to WUXGA 16-bit color depth or 1080p with higher refresh rates. The TDP158 can be configured to support the HDMI2.0 standard.

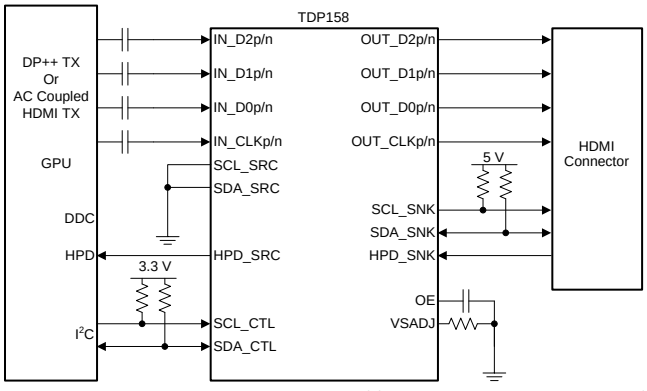
The TDP158 supports dual power supply rails of 1.1 V on V_{DD} and 3.3 V on V_{CC} for power reduction. Several methods of power management are implemented to reduce overall power consumption. TDP158 supports fixed receiver EQ gain using I^2C or pin strap to compensate for different lengths input cable or board traces.

Device Information[1]

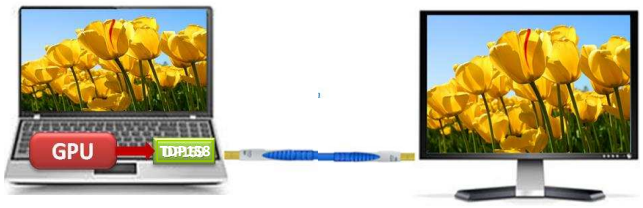
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TDP158	WQFN (40)	5.00 mm x 5.00 mm
TDP158I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Display



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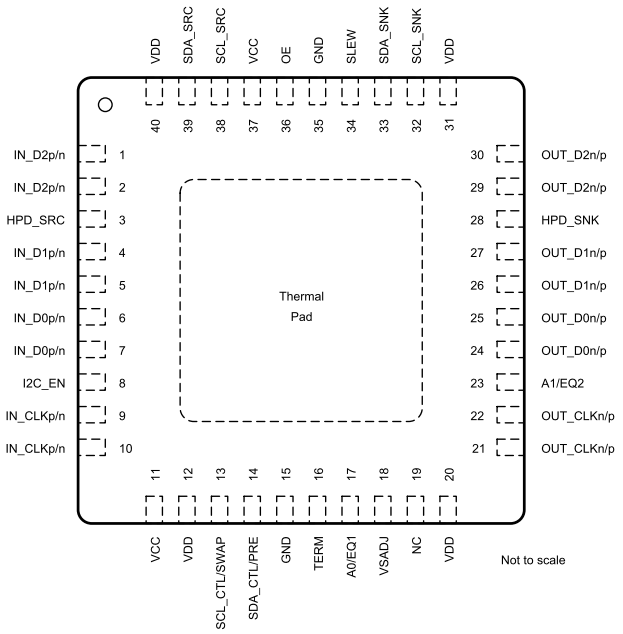
4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Pin Configuration and Functions

RSB Package
WQFN (40 Pins)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SUPPLY AND GROUND PINS			
VCC	11, 37	P	3.3V Power Supply
VDD	12,20,31,40	P	1.1V Power Supply
GND	15, 35 Thermal Pad	G	Ground
MAIN LINK INPUT PINS			
IN_D2p/n	1, 2	I	Channel 2 Differential Input
IN_D1p/n	4, 5	I	Channel 1 Differential Input
IN_D0p/n	6, 7	I	Channel 0 Differential Input
IN_CLKp/n	9, 10	I	Clock Differential Input
MAIN LINK OUTPUT PINS (FAIL SAFE)			
OUT_D2n/p	29, 30	O	TMDS Data 2 Differential Output
OUT_D1n/p	26, 27	O	TMDS Data 1 Differential Output
OUT_D0n/p	24, 25	O	TMDS Data 0 Differential Output
OUT_CLKn/p	21, 22	O	TMDS Data Clock Differential Output
HOT PLUG DETECT AND DDC PINS			
HPD_SRC	3	O	Hot Plug Detect Output to source side
HPD_SNK	28	I	Hot Plug Detect Input from sink side
SDA_SNK	33	I/O	Sink Side Bidirectional DDC Data Line
SCL_SNK	32	I/O	Sink Side Bidirectional DDC Clock Line
SDA_SRC	39	I/O	Source Side Bidirectional DDC Data Line

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SCL_SRC	38	I/O	Source Side Bidirectional DDC Clock Line
CONTROL PINS			
OE	36	I	Operation Enable/Reset Pin OE = L: Power Down Mode OE = H: Normal Operation Internal weak pull up: Resets device when transistions from H to L
I2C_EN	8	I	I2C_EN = High; Puts Device into I2C Control Mode I2C_EN = Low; Puts Device into Pin Strap Mode
SDA_CTL/PRE	14	I/0	I2C Data Signal: When I2C_EN = High; Pre-emphasis: When I2C_EN = Low: See *Pre-emphasis* DE = L: None 0 dB DE = H: 3.5 dB
SCL_CTL/SWAP	13	I	I2C Clock Signal: When I2C_EN = High; Lane SWAP: When I2C_EN = Low: See *Swap* HDMI Mode Only SWAP = L: Normal Operation SWAP = H: Lane Swap
VSADJ	18	I	TMDS Compliant Voltage Swing Control Nominal Typical: 6 KΩ Resistor to GND
A0/EQ1	17	I 3 Level	Address Bit 1 for I2C Programming when I2C_EN = High EQ1 Pin Setting when I2C_EN = Low; Works in conjunction with A1/EQ2; See *Main Link Inputs* for settings.
A1/EQ2	23	I 3 Level	Address Bit 2 for I2C Programming when I2C_EN = High EQ2 Pin Setting when I2C_EN = Low; Works in conjunction with A0/EQ1; See *Main Link Inputs* for settings
SLEW	34	I 3 Level	Clock Slew Rate Control: See *Slew Rate Control* SLEW = L: Slowest ~ 215 ps SLEW = NC (Default): Mid-range 1 ~ 155 p SLEW = H: Fastest ~ 125 ps
TERM	16	I 3 Level	Source Termination Cotnrol: See *Transmitter Impedance Control* TERM = H, 75 Ω ~ 150 Ω TERM = L, Transmit Termination impedance in 150 Ω ~ 300 Ω TERM = NC, No transmit Termination Note: When TMDS_CLOCK_RATIO_STATUS bit = 1 the TDP158 sets source termination to 75 Ω ~ 150 Ω Automatically
NC	19	NA	No Connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply Voltage Range(3)	VCC	–0.3	4	V
	VDD	–0.3	1.4	V
Voltage Range	Main Link Input Differential Voltage (IN_Dx)	–0.3	1.56	V
	Main Link Input Single Ended on Pin	–0.3	1.4	V
	TMDS Output (OUT_Dx)	–0.3	4	V
	HPD_SRC, VSADJ, SDA_CTL/PRE, OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW, SCL_CTL/SWAP, SDA_SRC, SCL_SRC	–0.3	4	V
	HDP_SNK, SDA_SNK, SCL_SNK	–0.3	6	V
Continuous power dissipation		See *Thermal Information*		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage Nominal Value 3.3 V		3		3.6	V
V_{DD}	Supply Voltage Nominal Value 1.1 V		1		1.27	V
T_J	Junction temperature		–40		105	°C
T_A	Operating free-air temperature (TDP158)		0		85	°C
	Operating free-air temperature (TDP158I)		–40		85	°C
MAIN LINK DIFFERENTIAL PINS						
$V_{ID(EYE)}$	Peak-to-peak input differential voltage See Figure 19		75		1200	mV
$V_{ID(DC)}$	The input differential voltage Peak-to peak DC level, See Figure 19		200		1200	mV
V_{IC}	Input Common Mode Voltage (Internally Biased)		0.5		0.9	V
d_R	Data rate		0.25		6	Gbps
VSADJ	TMDS compliant swing voltage bias resistor Nominal 6 kΩ		–1%		1%	
DDC, I2C, HPD, AND CONTROL PINS						
$V_{I(DC)}$	DC Input Voltage	HDP_SNK, SDA_SNK, SCL_SNK,	–0.3		5.5	V
		SDA_SRC, SCL_SRC; All other Local I2C, and control pins	–0.3		3.6	V
V_{IL}	Low-level input voltage at DDC				0.3 x V_{CC}	V
	Low-level input voltage at HPD				0.8	V
	Low-level input voltage at SDA_CTL/PRE, OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW, SCL_CTL/SWAP pins only				0.3	V
V_{IM}	Mid-Level input voltage at A1/EQ2, A0/EQ1, TERM, SLEW pins only		1.2		1.6	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage at OE, A1/EQ2, A0/EQ1, TERM, I2C_EN, SLEW pins only	2.2			V
	High-level input voltage at SDA_SRC, SCL_SRC, SDA_CTL/PRE, SCL_CTL/SWAP	0.7 x V_{CC}			V
	High-level input voltage at SDA_SNK, SCL_SNK	2.9			V
	High-level input voltage at HPD	2			V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.4			V
f_{SCL}	SCL clock frequency fast I^2C mode for local I2C control			400	kHz
$C_{(bus,DDC)}$	Total capacitive load for each bus line supporting 400 kHz (DDC terminals)			400	pF
$C_{(bus,I2C)}$	Total capacitive load for each bus line (local I2C terminals)			100	pF
$d_{R(DDC)}$	DDC Data rate			400	kbps
I_{IH}	High level input current	–30		30	µA
I_{IM}	Mid level input current	–20		20	µA
I_{IL}	Low level input current	–10		10	µA
I_{OZ}	High impedance outpupt current			10	µA
$R_{(OEPU)}$	Pull up resistance on OE pin	150		250	KΩ

6.4 Thermal Information

THERMAL METRIC[1]		TDP158 RSB (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	3.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics, Power Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX(2)	UNIT
P_{D1}	Device power Dissipation	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 1200 mV, 6 Gbps TMDS pattern, V_I = 3.3 V, I2C_EN = L, SDA_CTL/PRE = L, EQ1/EQ2 = H			200	350	mW
P_{D2}	Device power Dissipation in DP-Mode	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 400mV, 5.4 Gbps DP pattern, I2C_EN = H, V_{OD} = 400 mV PRE = 0 dB			330	680	mW
$P_{(STBY1)}$	Stage 1: Standby Power	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V , HPD = H, No input Signal: Stage 1 See Standby Power				25	mW
	Stage 2: Standby Power	OE = H, V_{CC} = 3.3 V/3.6 V, VDD = 1.1 V/1.27 V , HPD = H, Noise on input Signal: Stage 2 See Standby Power				55	mW
$P_{(SD1)}$	Device power in PowerDown	OE = L, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V			8	20	mW
$P_{(SD2)}$	Device power in PowerDown in DP-Mode	OE = L, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V			8	20	mW
I_{CC1}	V_{CC} Supply current	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 1200 mV, 6 Gbps TMDS pattern I2C_EN = L, SDA_CTL/PRE = L, EQ1/EQ2 = H,			8	20	mA
I_{CC2}	V_{CC} Supply current in DP-Mode	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 400 mV, 5.4 Gbps DP pattern, I2C_EN = H, V_{OD} = 400 mV PRE = 0 dB			45	110	mA
I_{DD1}	V_{DD} Supply current	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 1200 mV, 6 Gbps TMDS pattern I2C_EN = L, SDA_CTL/PRE = L, EQ1/EQ2 = H			160	220	mA
I_{DD2}	V_{DD} Supply current DP-Mode	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V IN_Dx: VID_PP = 400 mV, 5.4 Gbps DP pattern, I2C_EN = H, V_{OD} = 40mV PRE = dB			160	220	mA
$I_{(STBY1)}$	Stage 1: Standby current See Standby Power	OE = H, V_{CC} = 3.3V/3.6V, V_{DD} = 1.1 V/1.27 V , HPD = H: No signal on IN_CLK	3.3 V Rail			3	mA
			1.1 V Rail			10	mA
	Stage 2: Standby current See Standby Power	OE = H, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V , HPD = H: No valid signal on IN_CLK	3.3 V Rail			5	mA
			1.1 V Rail			27	mA
$I_{(SD11)}$	PowerDown current – HDMI Mode	OE = L, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V , or OE = H, HPD = L	3.3 V Rail		1	2	mA
			1.1 V Rail		4	10	mA
$I_{(SD2)}$	PowerDown current in DP-Mode	OE = L, V_{CC} = 3.3 V/3.6 V, V_{DD} = 1.1 V/1.27 V	3.3 V Rail		1	2	mA
			1.1 V Rail		4	10	mA

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.6 Electrical Characteristics, Differential Input

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$D_{R(RX\_DATA)}$	TMDS data lanes data rate		0.25		6	Gbps
$D_{R(RX\_CLK)}$	TMDS clock lanes clock rate		25		340	Mhz
t_{RX_DUTY}	Input clock duty circle		40%	50%	60%	
t_{CLK_JIT}	Input clock jitter tolerance				0.3	Tbit
t_{DATA_JIT}	Input data jitter tolerance	Test the TTP2 See Figure 10			150	ps
$R_{(INT)}$	Input differential termination impedance		80	100	120	Ω
$V_{(ITERM)}$	Input Termination Voltage	OE = H		0.7		V

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.7 Electrical Characteristics, TMDS Differential Output

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
V_{OH}	Single-ended high level output voltage Data rate ≤ 1.65 Gbps	SDA_CTL/PRE = L; TERML = NC; OE = H; D_R = 750 Mbps	V_{CC} - 10		V_{CC} + 10	V
	Single-ended high level output voltage Datarate >1.65 Gbps and < 3.4 Gbps	SDA_CTL/PRE = L ; TERM = L, NC; OE = H; D_R = 2.97 Gbps	V_{CC} - 200		V_{CC} + 10	V
	Single-ended high level output voltage Datarate > 3.4 Gbps and < 6 Gbps	SDA_CTL/PRE =L ; TERM = H; OE = H; D_R = 6 Gbps	V_{CC} - 400		V_{CC} + 10	V
V_{OL}	Single-ended low level output voltage Data rate ≤1.65 Gbps	SDA_CTL/PRE = L ; TERM = NC; OE = H; D_R = 750 Mbps	V_{CC} - 600		V_{CC} - 400	V
	Single-ended low level output voltage Datarate >1.65Gbps and <3.4Gbps	SDA_CTL/PRE = L ; TERM = L NC; OE = H; D_R = 2.97 Gbps	V_{CC} - 700		V_{CC} - 400	V
	Single-ended low level output voltage Datarate > 3.4 Gbps and < 6 Gbps	SDA_CTL/PRE = L ; TERM = H; OE = H; D_R = 6 Gbps	V_{CC} - 1000		V_{CC} - 400	V
$V_{(SWING\_DA)}$	Single-ended output voltage swing on data lane	SDA_CTL/PRE = L ; TERM = H/Z/L; OE = H; D_R = 750 Mbs, 2.97 Gbps, 6 Gbps V_{SADJ} = 5.5 kΩ;	400	500	600	mV
$V_{(SWING\_CLK)}$	Single-ended output voltage swing on clock lane	SDA_CTL/PRE = L ; TERM = L, NC; OE = H; Data rate ≤ 3.4 Gbps	400	500	600	mV
		SDA_CTL/PRE = L ; TERM = H; OE = H; Data rate > 3.4 Gbps	200	300	400	mV
$\Delta V_{(SWING)}$	Change in single-end output voltage swing per 100 Ω ΔV_{SADJ}			20		mV
$\Delta V_{OCM(SS)}$	Change in steady state output common mode voltage between logic levels		-5		5	mV
$V_{OD(PP)}$	Output differential voltage before Pre-emphasis; See Pre-emphasis	V_{SADJ} = 6 kΩ; SDA_CTL/PRE = H: See Figure 9	600		1000	mV
$V_{OD(SS)}$	Steady state output differential voltage See Pre-emphasis	V_{SADJ} = 6 kΩ; SDA_CTL/PRE = H, See Figure 9	350		720	mV
		V_{SADJ} = 5.5 kΩ; SDA_CTL/PRE = L, See Figure 8	350		1000	mV
$V_{OD(range)}$	Total TMDS data lanes output differential voltage for HDMI2.0 See Figure 11	3.4 Gbps < R_{bit} ≤ 3.712 Gps SLEW = H; TERM = H; SDA_CTL/PRE = L; OE = H	335			mV
		3.712 Gbps < R_{bit} < 5.94 Gbp SLEW = H; TERM = H; SDA_CTL/PRE = L; OE = H	-19.66 x (RBIT2) + (106.74 x R_{bit}) + 209.58			mV
		5.94 Gbps ≤ R_{bit} ≤ 6 Gbps SLEW = H; TERM = H; SDA_CTL/PRE = L; OE = H	150			mV
I_{OS}	Short circuit current limit	Main link output shorted to GND			50	mA
$R_{(TERM)}$	Source Termination resistance for HDMI2.0		75		150	Ω

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.8 Electrical Characteristics, DDC, I2C, HPD, and ARC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
DDC and I2C						
V_{IL}	SCL/SDA_CTL, SCL/SDA_SRC low level input voltage				0.3 x V_{CC}	V
V_{IH}	SCL/SDA_CTL, input voltage		0.7 x V_{CC}		V_{CC} + 0.5	V
V_{OL}	SCL/SDA_CTL, SCL/SDA_SRC low level output voltage	I_O = 3 mA and V_{CC} > 2 V			0.4	V
		I_O = 3 mA and V_{CC} > 2 V			0.2 x V_{CC}	V
HPD						
V_{IH}	High-level input voltage	HPD_SNK	2.1			V
V_{IL}	Low-level input voltage	HPD_SNK			0.8	V
V_{OH}	High-level output voltage	$_{IOH}$ = –500 µA; HPD_SRC,	2.4		3.6	V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA; HPD_SRC,	0		0.4	V
I_{LKG}	Failsafe condition leakage current	V_{CC} = 0 V; V_{DD} = 0 V; HPD_SNK = 5 V;			40	µA
$I_{H(HPD)}$	High level input current	Device powered; V_{IH} = 5 V; $I_{H(HPD)}$ includes $R_{(pdHPD)}$ resistor current			40	µA
		Device powered; V_{IL} = 0.8 V; $I_{L(HPD)}$ includes $R_{(pdHPD)}$ resistor current			30	µA
$R_{(pdHPD)}$	HPD input termination to GND	V_{CC} = 0 V	150	190	220	kΩ

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.9 Electrical Characteristics, TMDS Differential Output in DP-Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$V_{(TX\_DIFFPP\_LVL0)}$	Differential peak-to-peak output voltage level 0	Based on default state of V0_P0_VOD register		410		V
$V_{(TX\_DIFFPP\_LVL1)}$	Differential peak-to-peak output voltage level 1	Based on default state of V1_P0_VOD register		610		V
$V_{(TX\_DIFFPP\_LVL2)}$	Differential peak-to-peak output voltage level 2	Based on default state of V2_P0_VOD register		815		V
$\Delta V_{OD(L0L1)}$	Output peak-to-peak differential voltage delta	ΔV_{ODn} = 20×log($V_{ODL(n+1)}$ / $V_{ODL(n)}$)) measured in compliance with latest PHY CTS1	1		6	dB
$\Delta V_{OD(L1L2)}$			1		5	dB
$V_{(TX\_PRE\_RATIO\_0)}$	Pre-emphasis level 0	RBR, HBR and HBR2		0		dB
$V_{(TX\_PRE\_RATIO\_1)}$	Pre-emphasis level 1	RBR, HBR and HBR2	2		4.2	dB
$V_{(TX\_PRE\_RATIO\_2)}$	Pre-emphasis level 2	RBR, HBR and HBR2	5		7.2	dB
$\Delta V_{PRE(L1L0)}$	Pre-emphasis delta	Measured in compliance with latest PHY CTS	2			dBdB
$\Delta V_{PRE(L2L1)}$			1.6			

(1) Does not support Level 3 Swing or Pre-emphasis

6.10 Switching Characteristics, TMDS

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
d_R	Data rate		250		6000	Mbps
t_{TPLH}	Propagation delay time (low to high)	see Figure 7 2	250		600	ps
t_{PHL}	Propagation delay time (high to low)	Figure 7 2	250		800	ps
$t_{T(DATA)}$	Transition time (rise and fall time); measured at 20% and 80%. SDA_CTL = L, OE = H, All Data Rates Note: Data lane control by I2C only: See Slew Rate Control	Reg0Ah[1:0] = 11 (default)		60		ps
$t_{T(CLOCK)}$		Reg0Ah[1:0] = 10		80		ps
		Reg0Ah[1:0] = 01		95		ps
		Reg0Ah[1:0] = 00		110		ps
		TERM = H; Reg0Bh[7:6] = 11		125		ps
		Reg0Bh[7:6] = 10		155		ps
		TERM = L; Reg0Bh[7:6] = 00		185		ps
		TERM = NC; Reg0Bh[7:6] = 01		215		ps
t_{TX_INTRA}	Intra-pair output skew See Figure 6	Default setting for internal intra-pair skew adjust, TERM = Z; SDA_CTL/PRE = L; 1.48 Gbps, 2.97 Gbps, 6 Gbps Data Lines, 148 MHz, 297 MHz Clock			24	ps
t_{TX_INTER}	Inter-pair output skew See Figure 6	Default setting for internal inter-pair skew adjust, TERM = Z; SDA_CTL/PRE = L; 1.48 Gbps, 2.97 Gbps, 6 Gbps Data Lines, 148 MHz, 297 MHz Clock			100	ps
$t_{JITD1(1.4b)}$	Total output data jitter HDMI1.4b	D_R = 2.97 Gbps, SDA_CTL/PRE = L, A0/EQ1 = H, A1/EQ2 = H ; See Figure 7 4 at TTP3			0.2	Tbit
$t_{JITD1(2.0)}$	Total output data jitter HDMI2.0 In Redriver Mode only ISI will be compensated for.	3.4 Gbps < R_{bit} ≤ 3.712 Gps TERM = Z; SDA_CTL/PRE = L; OE = H			0.4	Tbit
		3.712 Gbps < R_{bit} < 5.94 Gbps TERM = Z; SDA_CTL/PRE = L; OE = H			-0.0332R_{bit} 2 +0.2312 R_{bit} + 0.1998	Tbit
		5.94Gbps ≤ R_{bit} ≤ 6 Gbps TERM = Z; SDA_CTL/PRE = L; OE = H			0.6	Tbit
$t_{JITC1(1.4b)}$	Total output clock jitter	CLK = 25 MHz, 74.25 MHz, 75 MHz,150 MHz, 297 MHz			0.25	Tbit
$t_{JITC1(2.0)}$	Total output clock jitter	D_R = 6 Gbps: CLK = 150 MHz			0.3	Tbit

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.11 Switching Characteristics, HPD

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$t_{PD(HPD)}$	Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge	see Figure Figure 13; not valid during switching time		40	120	ns
$t_{T(HPD)}$	HPD logical disconnected timeout	see Figure 14	2			ms

(1) The Typical rating is simulated at 3.3 V V_{CC} and 1.1 V V_{DD} and at 27°C temperature unless otherwise noted
(2) The Maximum rating is simulated at 3.6 V V_{CC} and 1.27 V V_{DD} and at 85°C temperature unless otherwise noted

6.12 Switching Characteristics, DDC and I²C

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of both SDA and SCL signals	V_{CC} = 3.3 V; See Figure 17			300	ns
t_f	Fall time of both SDA and SCL signals	See Figure 17			300	ns
t_{HIGH}	Pulse duration , SCL high	See Figure 16	0.6			µs
t_{LOW}	Pulse duration , SCL low	See Figure 16	1.3			µs
t_{SU1}	Setup time, SDA to SCL	See Figure 16	100			ns
$t_{ST,\ ST}$A	Setup time, SCL to start condition	See Figure 16	0.6			µs
$t_{HD,STA}$	Hold time, start condition to SCL	See Figure 15	0.6			µs
$t_{HD,DAT}$	Data Hold Time		0			ns
$t_{VD,DAT}$	Data valid time		0.9			µs
$t_{VD,ACK}$	Data valid acknowledge time		0.9			µs
$t_{ST,STO}$	Setup time, SCL to stop condition	See Figure 15	0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition	See Figure 15	1.3			µs
t_{PLH1}	Propagation delay time, low-to-high-level output	Source to Sink:100 kbps pattern; $C_{b(Sink)}$ = 400 pF (1); see Figure 17		360		ns
t_{PHL1}	Propagation delay time, high-to-low-level outpu			230		ns
tPLH2	Propagation delay time, low-to-high-level output	Sink to Source: 100 kbps pattern; $C_{b(Source)}$ = 100 pF (1); see Figure 18		250		ns
tPHL2	Propagation delay time, high-to-low-level output			200		ns

(1) C_b = total capacitance of one bus line in pF.

6.13 Typical Characteristics

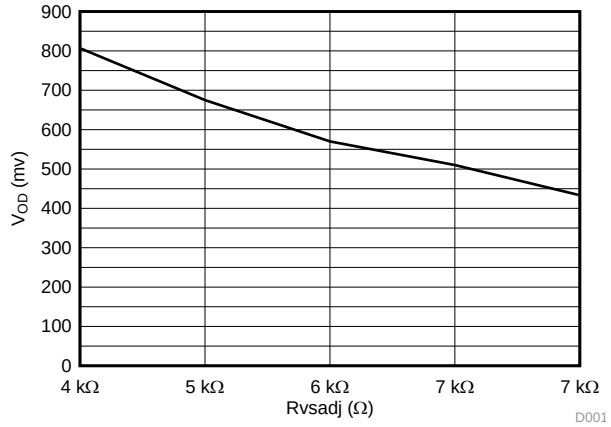


Figure 1. V_{OD} Swing vs VASDJ Resistor Value

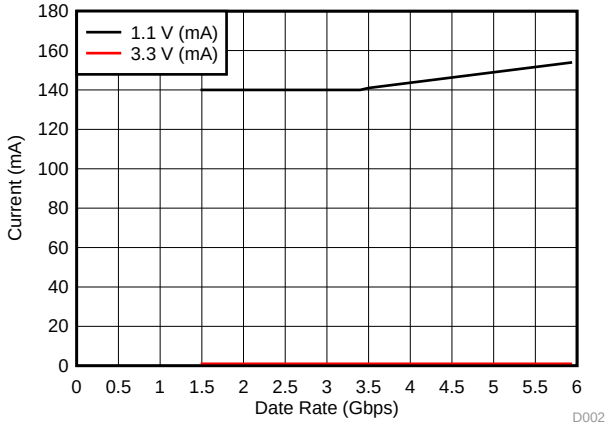


Figure 2. HDMI Current vs Data Rate

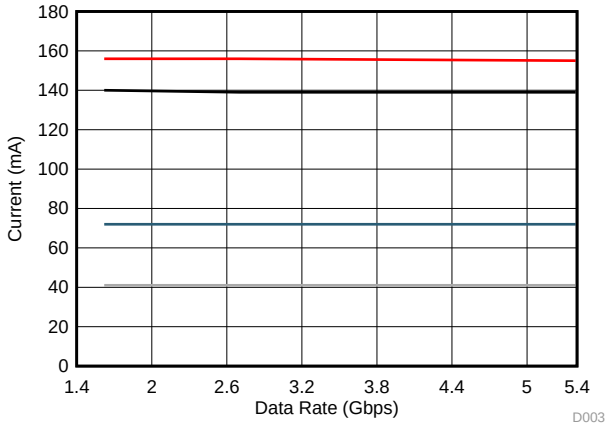


Figure 3. DisplayPort Current vs Data Rate

7 Parameter Measurement Information

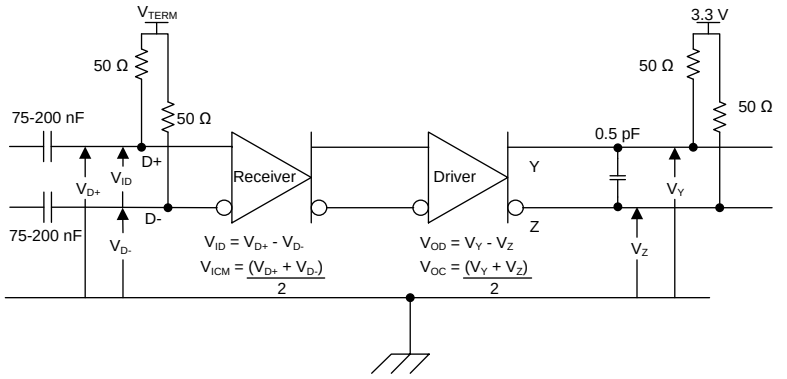


Figure 4. TMDS Main Link Test Circuit

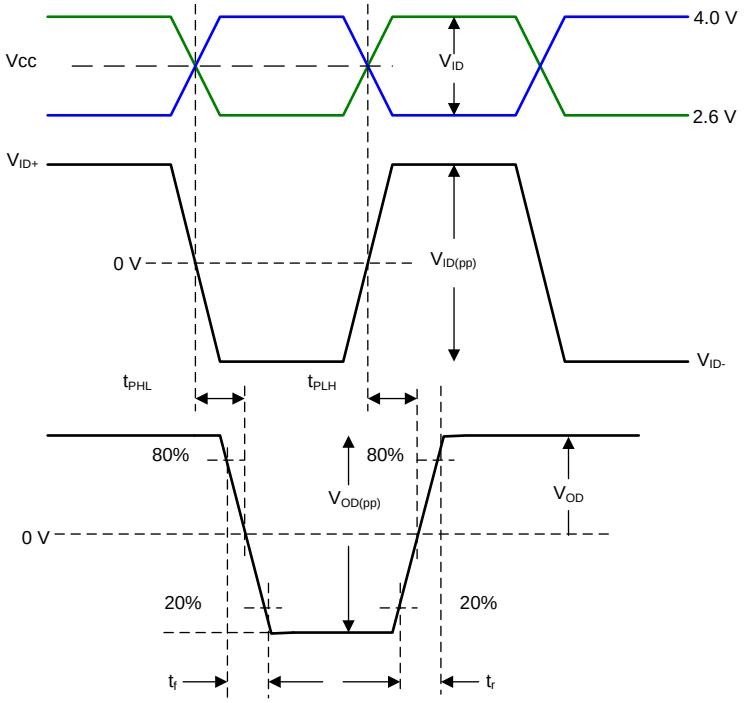


Figure 5. Input or Output Timing Measurements

Parameter Measurement Information (continued)

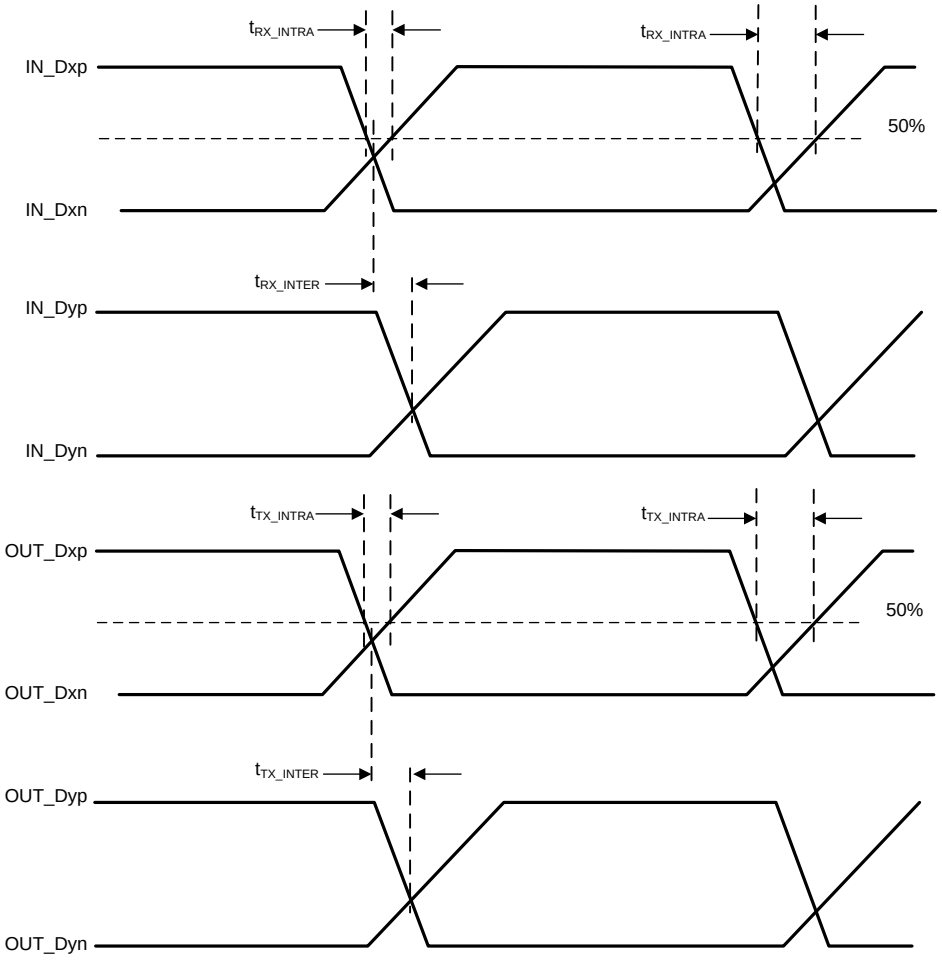


Figure 6. TMDS Output Skew Measurements

Figure 7. HDMI/DVI TMDS Output Common Mode Measurement

Parameter Measurement Information (continued)

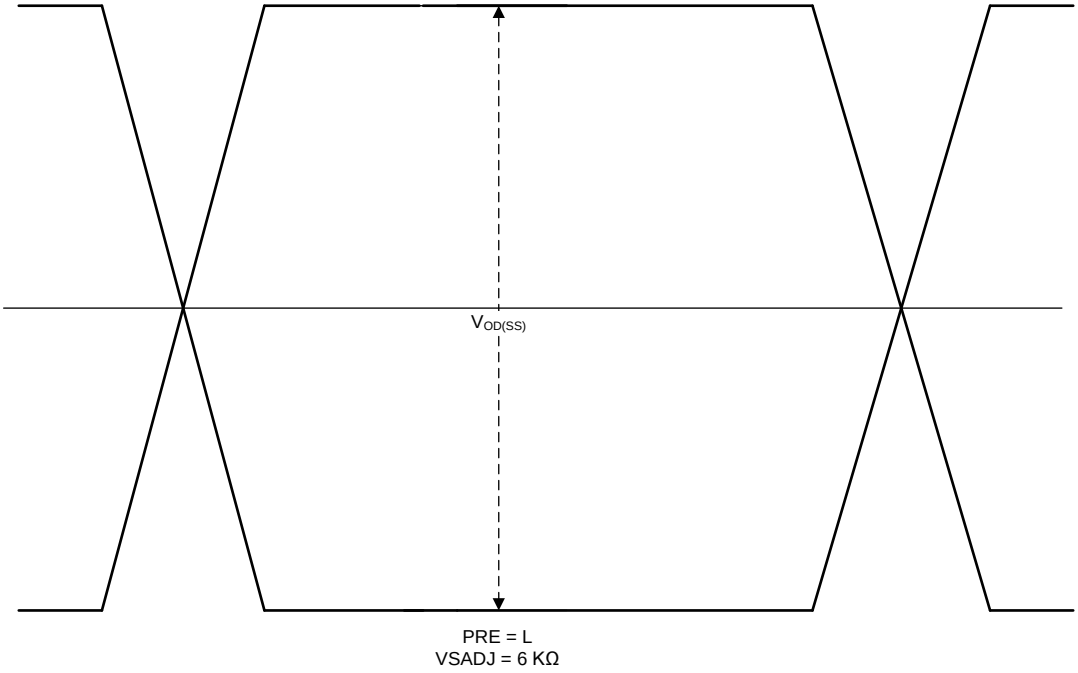


Figure 8. Output Differential Waveform

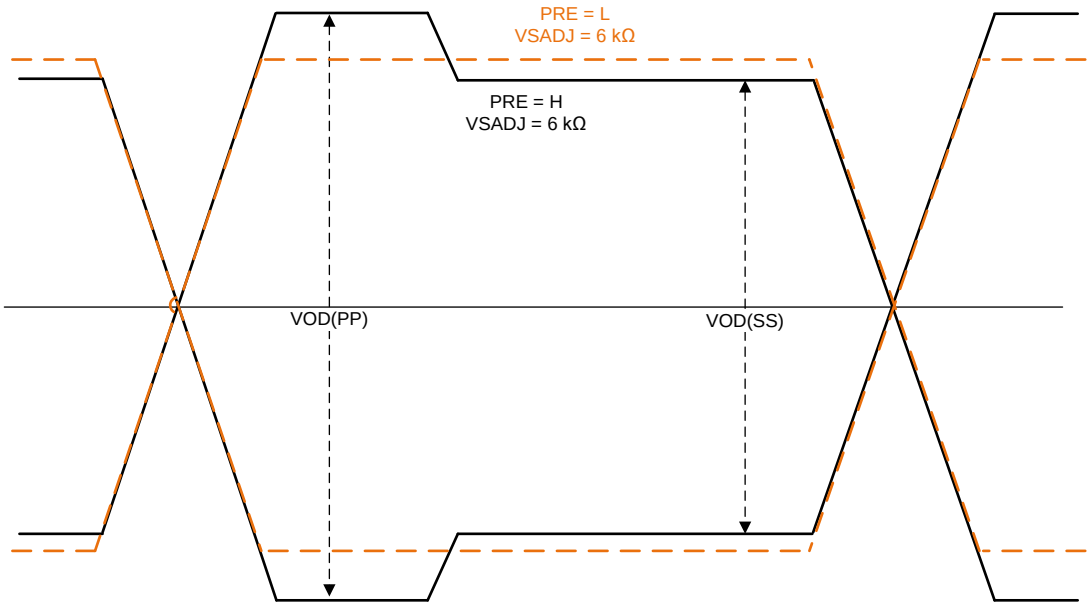
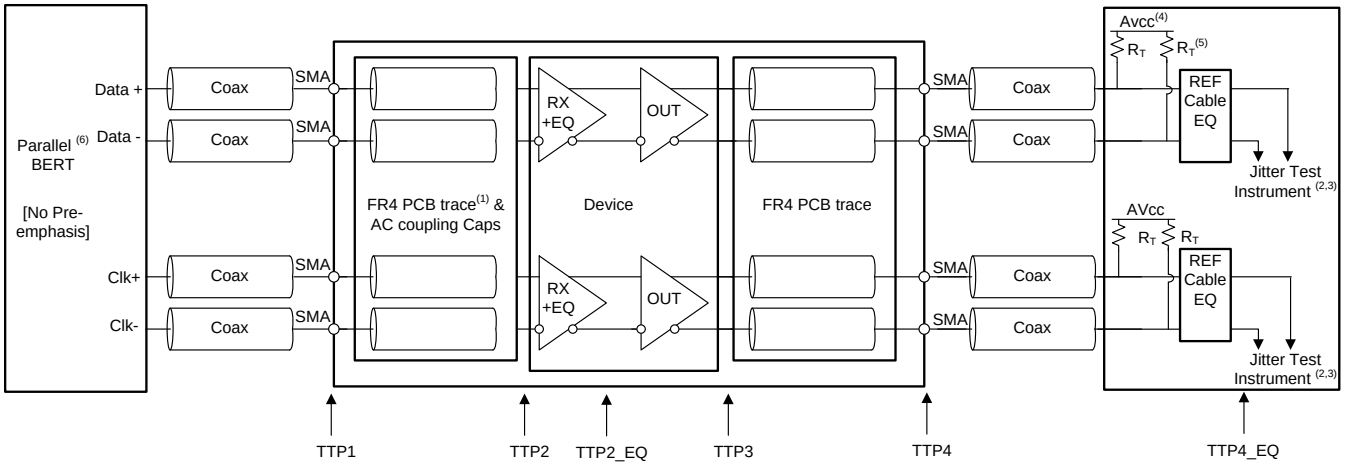


Figure 9. Output Differential Waveform with De-empahsis

Parameter Measurement Information (continued)



(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling cap, connector and another 1-8" of FR4. Trace width – 4 mils. 100 Ω differential impedance.

(2) All Jitter is measured at a BER of 10^9

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP

(4) AVCC = 3.3 V

(5) R_T = 50 Ω

(6) The input signal from parallel Bert does not have any pre-emphasis. Refer to recommended operating conditions.

Figure 10. HDMI Output Jitter Measurement

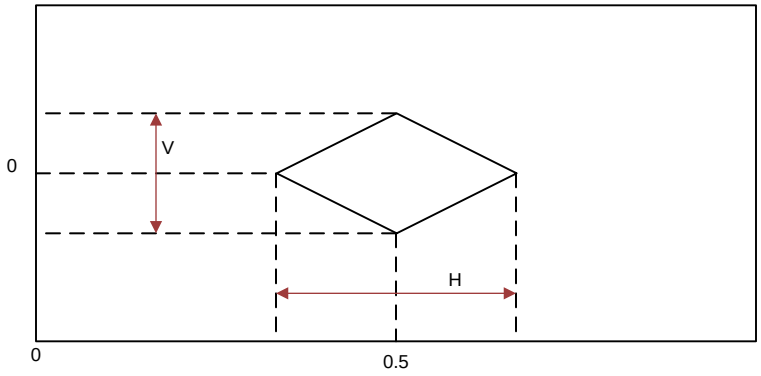


Figure 11. Output Eye Mask at TTP4_EQ for HDMI 2.0

TMDS Data Rate (Gbps)	H (Tbit)	V (mV)
3.4 < DR < 3.712	0.6	335
3.712 < DR < 5.94	$-0.0332Rbit^2 + 0.2312\ R_{bit} + 0.1998$	$-19.66Rbit^2 + 106.74R_{bit} + 209.58$
5.94 ≤ DR ≤ 6.0	0.4	150

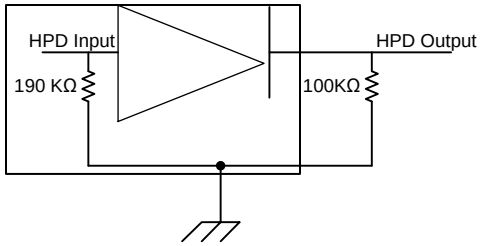


Figure 12. HPD Test Circuit

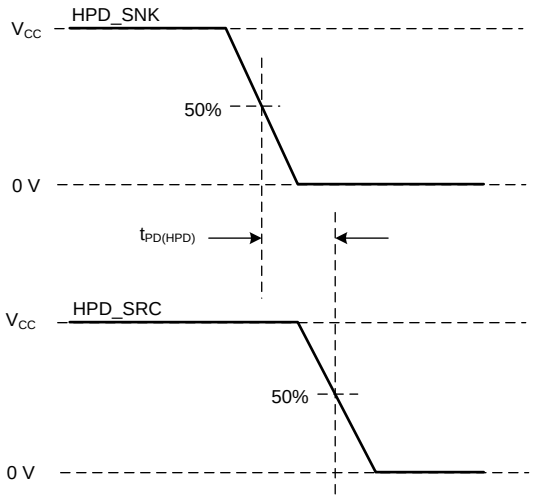


Figure 13. HPD Timing Diagram No. 1

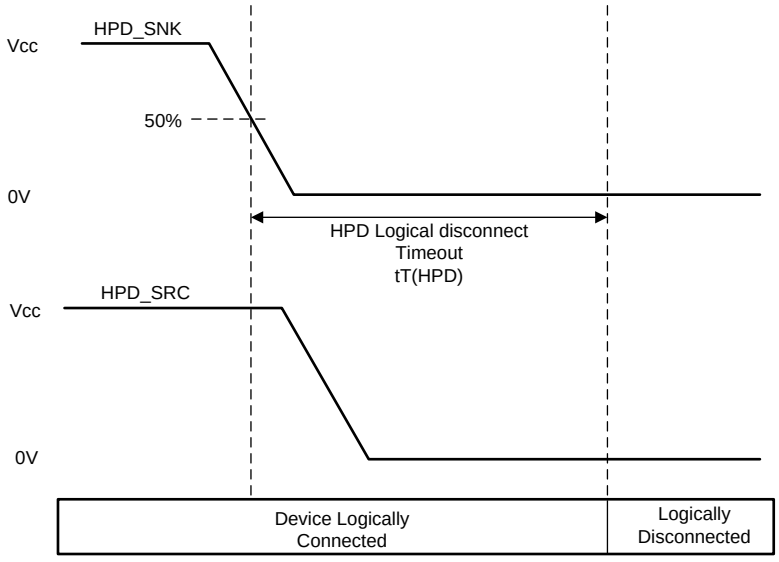


Figure 14. HPD Logic Disconnect Timeout

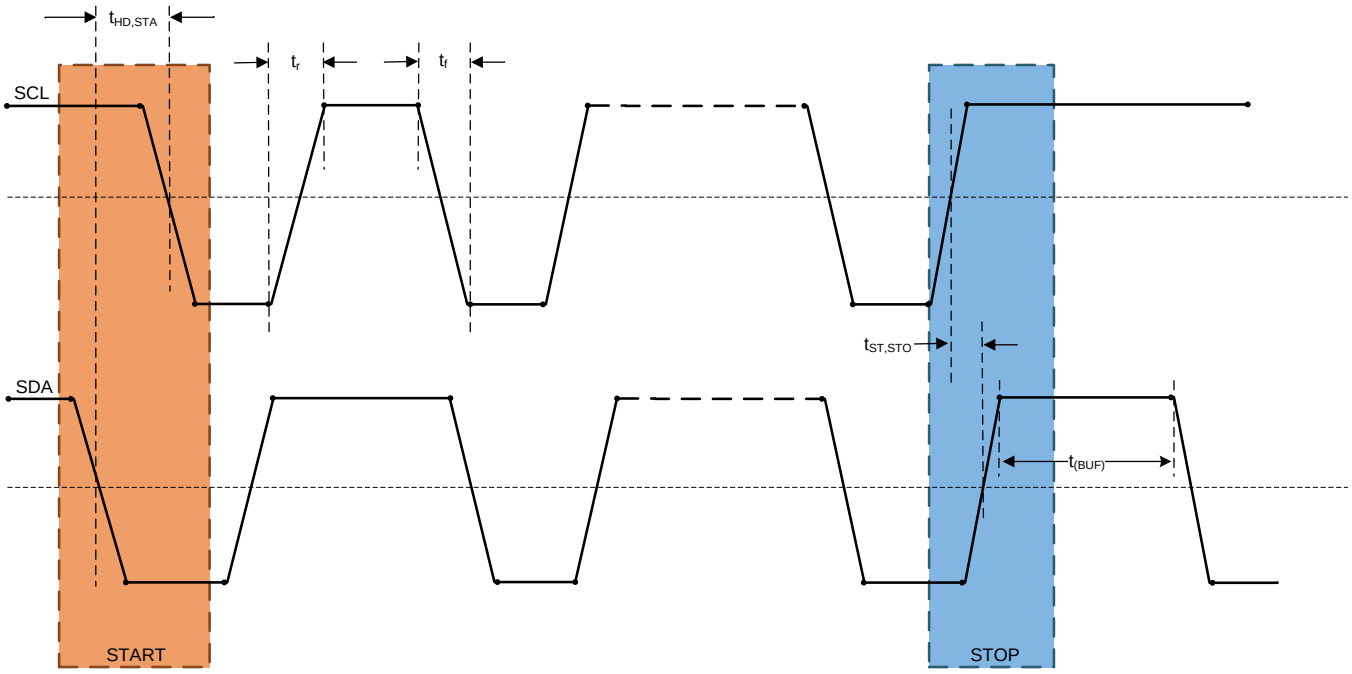


Figure 15. Start and Stop Condition Timing

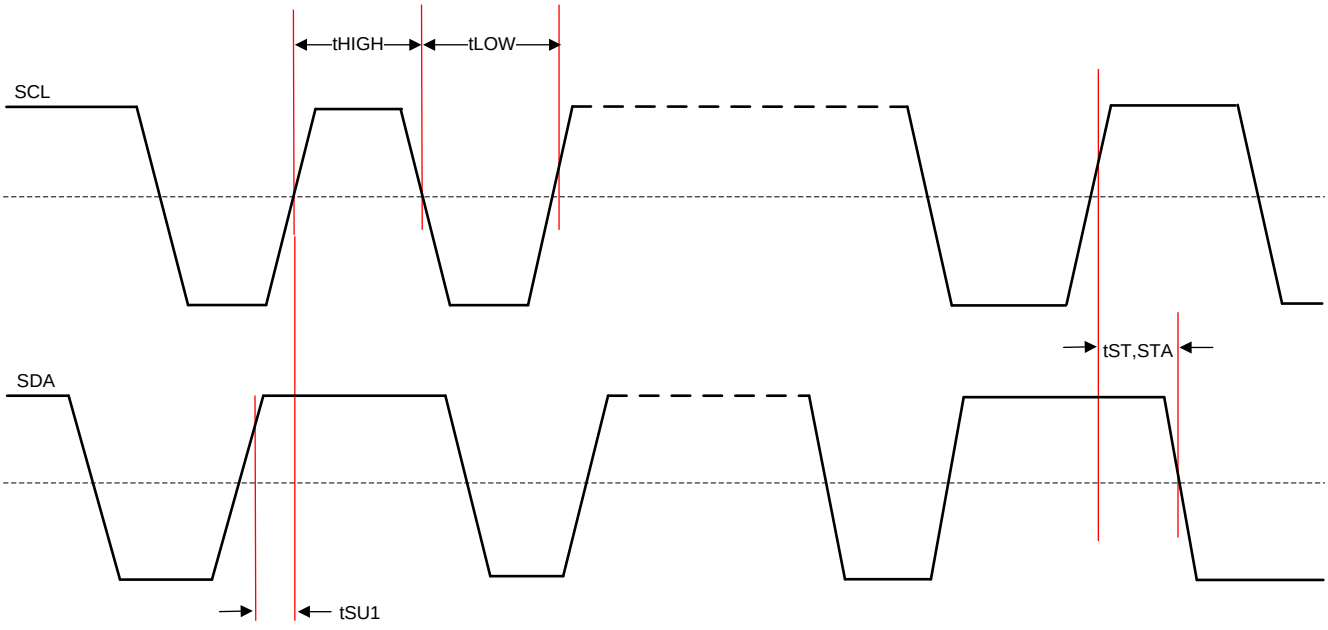


Figure 16. SCL and SDA Timing

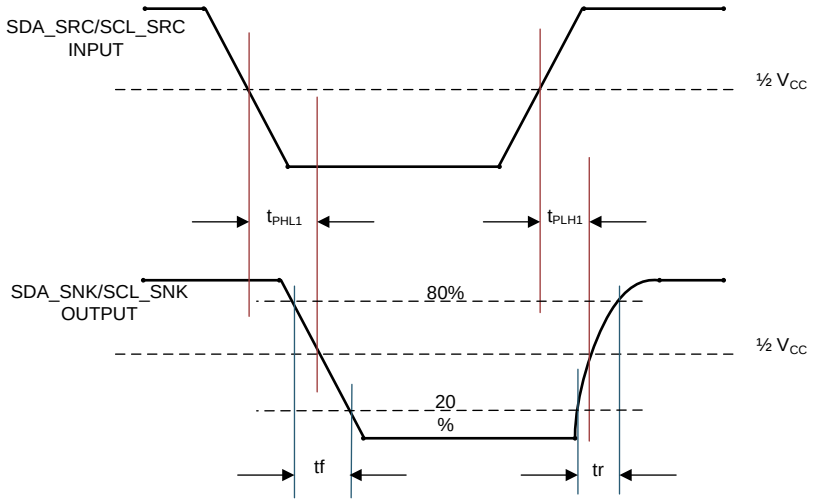


Figure 17. DDC Propagation Delay – Source to Sink

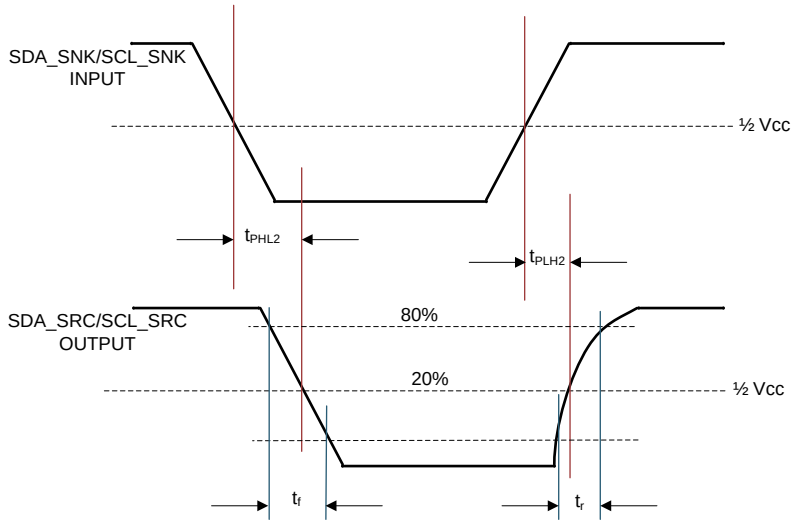


Figure 18. DDC Propagation Delay – Sink to Source

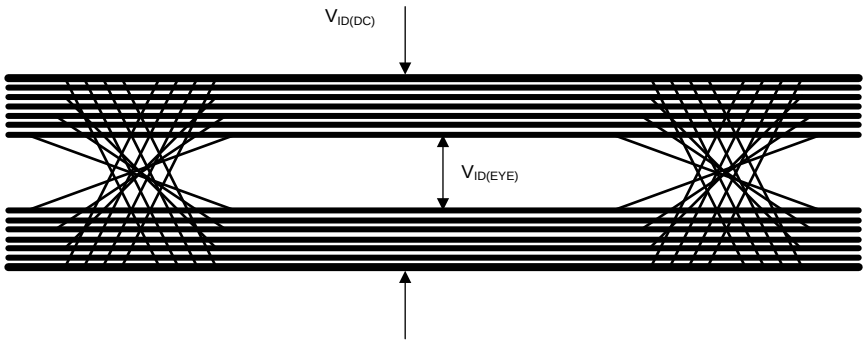


Figure 19. $V_{ID(DC)}$ and $V_{ID(EYE)}$

8 Detailed Description

8.1 Overview

The TDP158 is an AC coupled digital video interface (DVI) or high-definition multimedia interface (HDMI) signal input to Transition Minimized Differential Signal (TMDS) level shifting Redriver. The TDP158 supports four TMDS channels, Hot Plug Detect, and a Digital Display Control (DDC) interfaces. The TDP158 supports signaling rates up to 6 Gbps to allow for the highest resolutions of 4k2k60p 24 bits per pixel and up to WUXGA 16-bit color depth or 1080p with higher refresh rates. For passing compliance and reducing system level design issues several features have been included such as TMDS output amplitude adjust using an external resistor on the VSADJ pin, source termination selection, pre-emphasis and output slew rate control. Device operation and configuration can be programmed by pin strapping or I^2C. Four TDP158s can be used on one I^2C bus when I2C_EN is high with device address set by A0/A1.

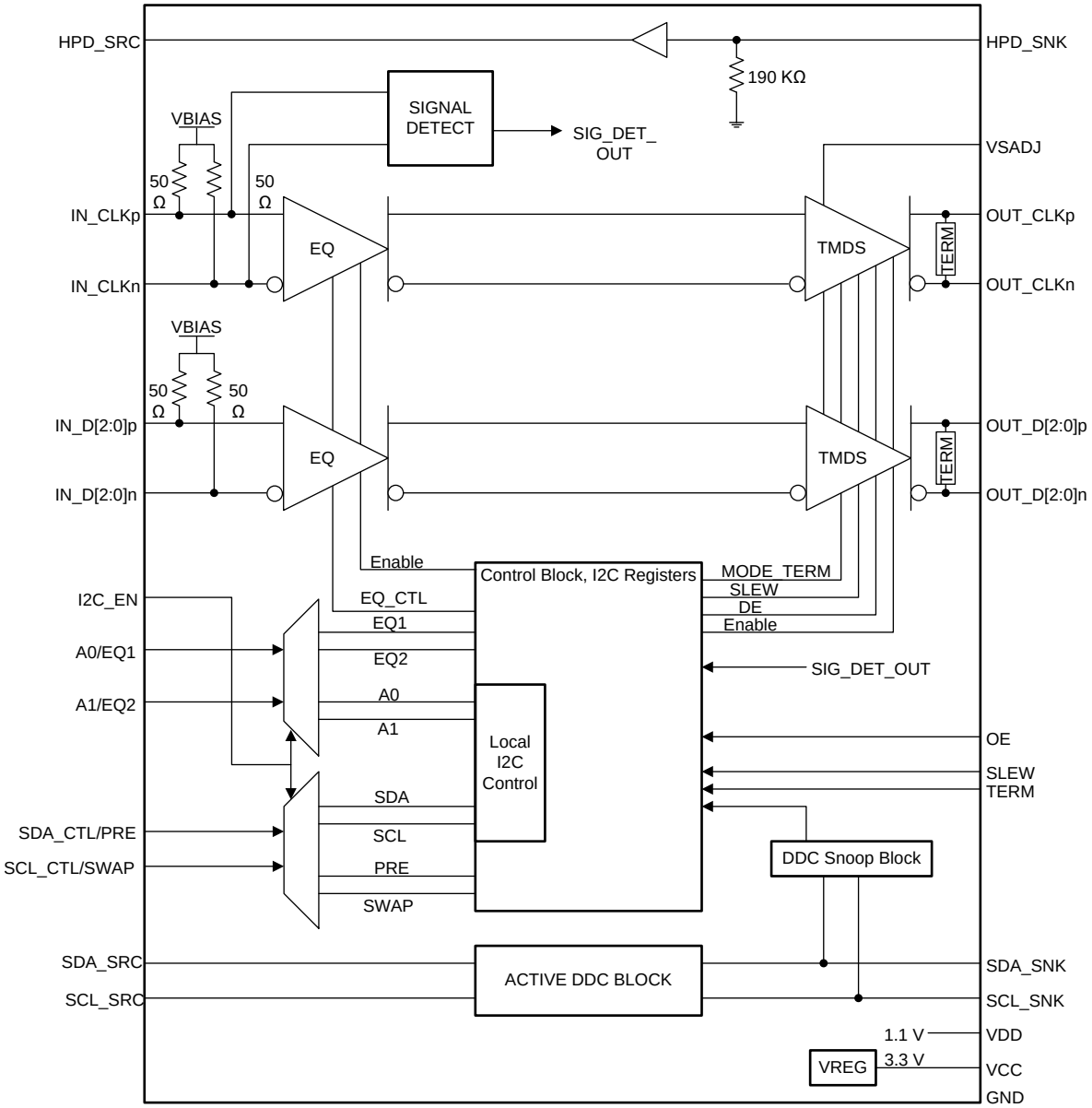
To reduce active power the TDP158 supports dual power supply rails of 1.1 V on VDD and 3.3 V on VCC. There are several methods of power management such as going into power down mode using three methods:

1. HPD is low
2. Writing a 1 to register 09h[3]
3. de-asserting OE.

De-asserting OE clears the I^2C registers, thus once re-asserted, the device must be reprogrammed if I^2C was used for device setup. Upon return to normal active operation from re-asserted, OE or re-asserted HPD, and the TDP158 requires the source to write a 1 to the TMDS_CLOCK_RATIO_STATUS register in order for the TDP158 to resume 75 Ω to 150 Ω source termination. If during the source to sink read, this bit is already set as a one, the TDP158 automatically sets this bit to 1. The SIG_EN register enables the signal detect circuit that provides an automatic power-management feature during normal operation. When no valid signal is present on the clock input, the device enters Standby mode. DDC link supports the HDMI 2.0b SCDC communication, 100 Kbps data rate default and 400 kbps adjustable by software.

TDP158 supports fixed EQ gain control to compensate for different lengths of input cables or board traces. The EQ gain can be software adjusted by I^2C control or pin strapping EQ1 and EQ2 pins. Customers can use the TERM to change to one of three source termination impedances for better output performance when working in HDMI1.4b or HDMI2.0b. When the TMDS_CLOCK_RATIO_STATUS bit is set to 1, the TDP158 automatically switches in 75 Ω to 150 Ω source termination. To assist in ease of implementation, the TDP158 supports lanes swapping, see *Lane Control*. Two temperature gradient versions of the device available extended commercial temperature range 0ºC to 85ºC (TDP158) and industrial temperature range from –40ºC to 85ºC (TDP158I).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reset Implementation

When OE is low, Control signal inputs are ignored; the HDMI inputs and outputs are high impedance. It is critical to transition the OE from a low level to high after the V_{CC} supply has reached the minimum recommended operating voltage. This is achieved by a control signal to the OE input, or by an external capacitor connected between OE and GND. To insure the TDP158 is properly reset, the OE pin must be de-asserted for at least 100 µs before being asserted. When OE is re-asserted the TDP158 must be reprogrammed if it was programmed by I^2C and not pin strapping. When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for TDP158; consider approximately 0.1 µF capacitor as a reasonable first estimate for the size of the external capacitor. Both OE implementations are shown in Figure 20 and Figure 21.

Feature Description (continued)

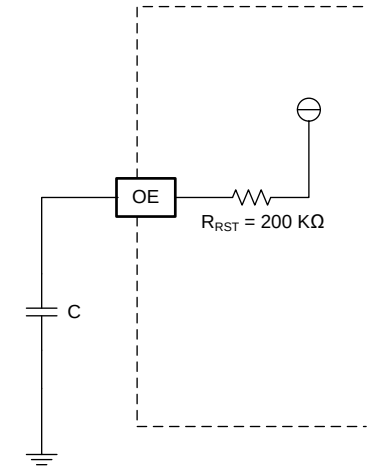


Figure 20. External Capacitor Controlled OE

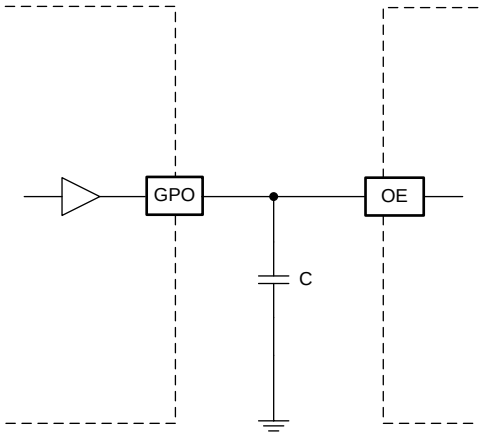


Figure 21. OE Input from Active controller

8.3.2 Operation Timing

TDP158 starts to operate after the OE signal is properly set after power up timing complete. See Figure 22 and Table 1. OE must be held low until V_{DD} and V_{CC} become stable if the rail sequence is in Figure 22 is a concern.

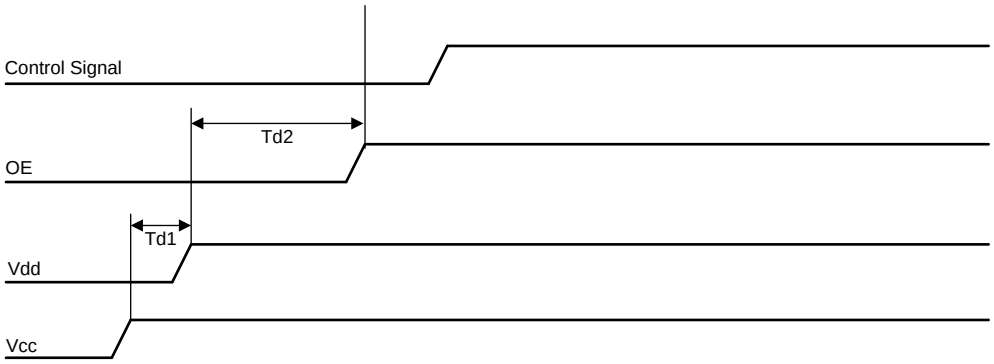


Figure 22. Power up Timing for TDP158

Feature Description (continued)

Table 1. Power Up and Operation Timing Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{d1}	V_{CC} stable before Vdd	0		200	µs
t_{d1}	V_{DD} and V_{CC} stable before OE de-assertion	100			µs
$V_{DD(ramp)}$	V_{DD} supply ramp up requirements	0.2		100	ms
$V_{CC(ramp)}$	V_{CC} supply ramp up requirements	0.2		100	ms

8.3.3 Lane Control

The TDP158 has various lane control features. By default the high speed lanes are globally controlled. Pin strapping can globally control features like receiver equalization, V_{OD} swing and Pre-emphasis. I^2C programming performs the same global programming using default configurations. Through I2C a method to control receive equalization, transmitter swing (V_{OD}) and Pre-emphasis on each individual lane. Setting reg09h[5] = 1 puts the device into independent lane configuration mode.

Reg31h[7:3] controls the clock lane, reg32h[7:3] controls lane D0, reg33h[7:3] controls lane D1 and reg34h[7:3] controls lane D2 while Reg4E and Reg4F control the individual lane EQ control.

NOTE

If the swap function is enabled and individual lane control has been implemented it is recommended to reprogram the lanes to make sure they match the expected results. Register are mapped to the pin name convention.

8.3.4 Swap

TDP158 incorporates a swap function which can swap the lanes, see Figure 23. The EQ, Pre-emphasis, termination, and slew setup will follow the new mapping. This function can be used with the SCL_CTL/SWAP pin 13 when I2C_EN pin 8 is low or can be implemented using control the register 0x09h bit 7 and is only valid for HDMI Mode.

Table 2. TBD

Normal Operation	SWAP = L or CSR 0x09h bit 7 is 1'b1
IN_D2 → OUT_D2	IN_CLK → OUT_CLK
IN_D1 → OUT_D1	IN_D0 → OUT_D0
IN_D0 → OUT_D0	IN_D1 → OUT_D1
IN_CLK → OUT_CLK	IN_CLK → OUT_CLK

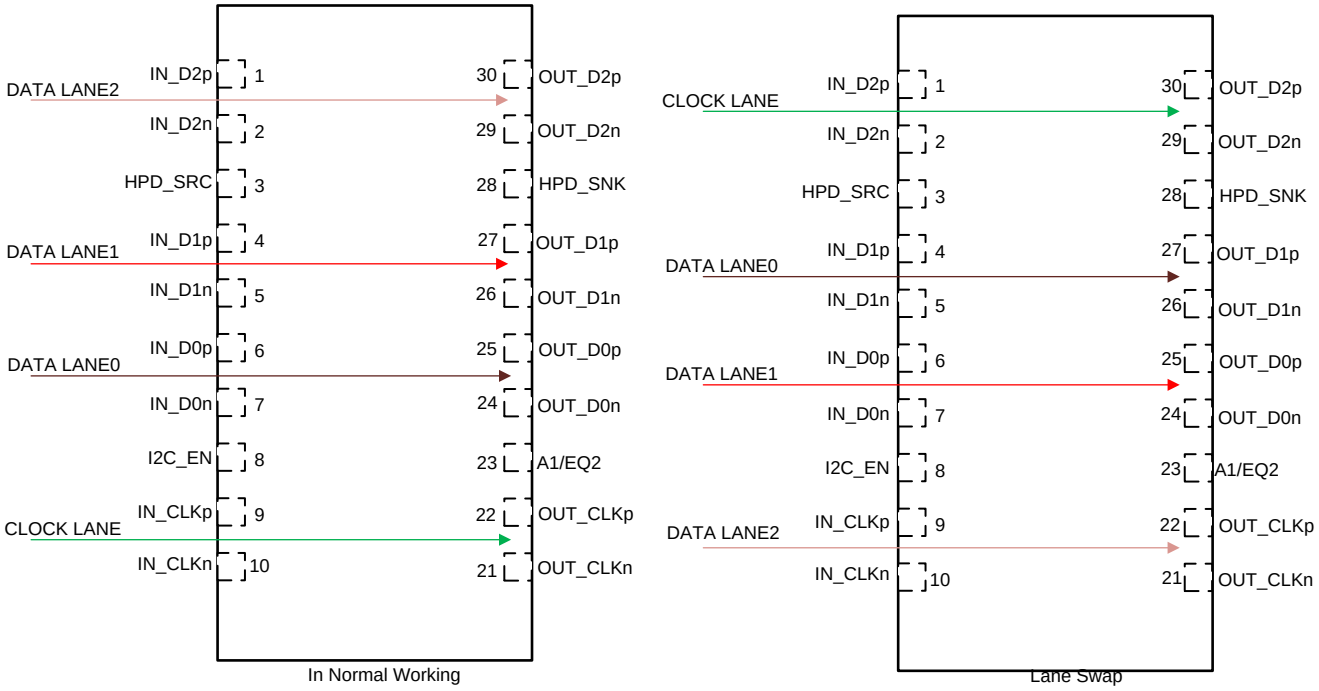


Figure 23. TDP158 Swap Function

8.3.5 Main Link Inputs

Standard Dual Mode DisplayPort terminations are integrated on all inputs with expected AC coupling capacitors on board prior to input pins. External terminations are not required. Each input data channel contains an equalizer to compensate for cable or board losses. The voltage at the input pins must be limited under the absolute maximum ratings.

8.3.6 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter/loss from the bandwidth-limited board traces or cables. TDP158 supports fixed receiver equalizer by setting the A0/EQ1 and A1/EQ2 pins or through I^2C. Table 3 shows the pin strap settings and EQ values.

Table 3. Receiver EQ Programming and Values

		Global	Independent Lane Control			
RX EQ (dB)	Pin Control (1)	I2C Control	I2C Control (2)			
	{EQ2,EQ1}	P0_Reg0D[6:3]	D2 P0_Reg4E[3:0]	D1 P0_Reg4E[7:4]	D3 P0_Reg4F[3:0]	CLK(2)(3) P0_Reg4F[7:4]
2	2'b00	4'b0000	4'b0000	4'b0000	4'b0000	4'b0000
3	2'b0Z	4'b0001	4'b0001	4'b0001	4'b0001	4'b0001
4		4'b0010	4'b0010	4'b0010	4'b0010	4'b0010
5	2'b01	4'b0011	4'b0011	4'b0011	4'b0011	4'b0011
6.5	2'bZ0	4'b0100	4'b0100	4'b0100	4'b0100	4'b0100
7.5		4'b0101	4'b0101	4'b0101	4'b0101	4'b0101
8.5	2'bZZ	4'b0110	4'b0110	4'b0110	4'b0110	4'b0110
9		4'b0111	4'b0111	4'b0111	4'b0111	4'b0111
10	2'bZ1	4'b1000	4'b1000	4'b1000	4'b1000	4'b1000
11	2'b10	4'b1001	4'b1001	4'b1001	4'b1001	4'b1001

(1) For Pin Control 0 = GND, 1 = VCC, Z = Floating (No Connect)
(2) Individual Lane control is based upon the pin names with no swap
(3) The CLK EQ in HDMI mode is controlled by register P0_Reg0D[2:1]

Table 3. Receiver EQ Programming and Values (continued)

RX EQ (dB)	Pin Control (1)	Global	Independent Lane Control			
	I2C Control	I2C Control (2)				
	{EQ2,EQ1}	P0_Reg0D[6:3]	D2 P0_Reg4E[3:0]	D1 P0_Reg4E[7:4]	D3 P0_Reg4F[3:0]	CLK(2)(3) P0_Reg4F[7:4]
12		4'b1010	4'b1010	4'b1010	4'b1010	4'b1010
13		4'b1011	4'b1011	4'b1011	4'b1011	4'b1011
14		4'b1100	4'b1100	4'b1100	4'b1100	4'b1100
14.5	2'b1Z	4'b1101	4'b1101	4'b1101	4'b1101	4'b1101
15		4'b1110	4'b1110	4'b1110	4'b1110	4'b1110
15.5	2'b11	4'b1111	4'b1111	4'b1111	4'b1111	4'b1111

8.3.7 Input Signal Detect Block

When SIG_EN is enabled through I^2C the receiver looks for a valid HDMI clock signal input and is fully functional when a valid signal is detected. If no valid HDMI clock signal is detected, the device enters standby mode waiting for a valid signal at the clock input. All of the TMDS outputs and IN_D[0:2] are in high-Z status. HDMI signal detect circuit is default enabled. If there is a loss of signal reg20h[5] can be read to determine if the TDP158 has not detected a valid signal or not.

8.3.8 Transmitter Impedance Control

HDMI2.0 standard requires a source termination impedance in the 75Ω to 150Ω range for data rates > 3.4Gbps. HDMI1.4b requires no source termination but has a provision for using 150 Ω to 300 Ω for higher data rates. The TDP158 has three termination levels that are selectable using pin 16 when programming through pin strapping or when using I^2C programming through reg0Bh[4:3]. When the TMDS_CLOCK_RATIO_STATUS bit, reg0Bh[1] = 1 theTDP158 automatically turns on the 75 Ω to 150 Ω source termination otherwise the termination must be selected. See Table 4.

Table 4. Source Termination Control Table

Pin 16	Reg0Bh[4:3]	Source Termination
TERM = L	00	150 Ω ~ 300 Ω
TERM = NC	01	None
	10	Automatic set based upon TMDS_CLOCK_RATIO_STATUS bit
TERM = H	11	75 Ω ~ 150 Ω

NOTE

If the TMDS_CLOCK_RATIO_STATUS bit = 1, the TDP158 automatically switches in 75 Ω ~ 150 Ω termination.

8.3.9 TMDS Outputs

A 1% precision resistor, 6 kΩ, connected from VSADJ pin to ground is recommended to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor.

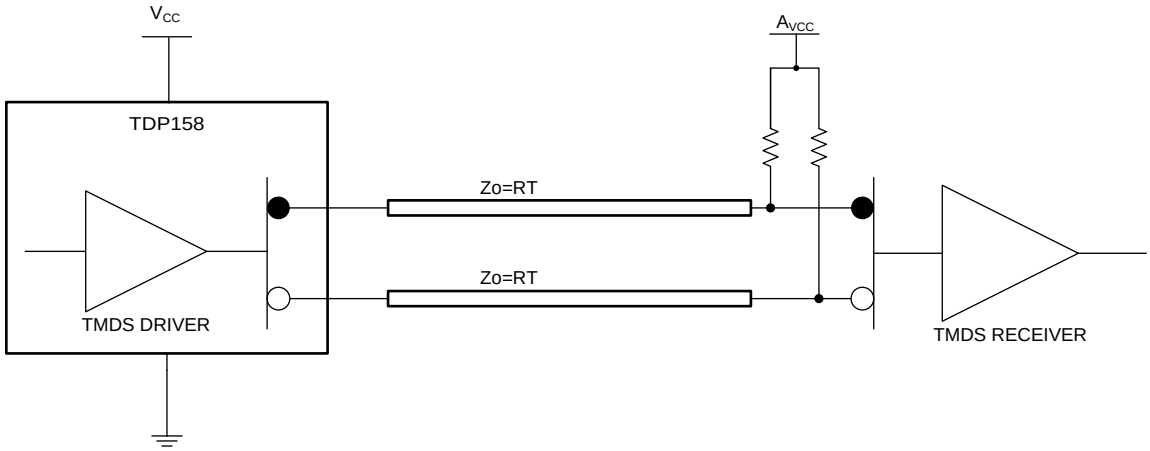


Figure 24. TMDS Driver and Termination Circuit

Referring to Figure 24, if V_{CC} (TDP158 supply) and A_{VCC} (sink termination supply) are both powered, the TMDS output signals are high impedance when OE = low. Both supplies being active is the normal operating condition. A total of approximately 33-mW of power is consumed by the terminations independent of the OE logical selection. When AVCC is powered on, normal operation (OE controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the $I_{O(off)}$, output leakage current, specification ensures the leakage current is limited 45-μA or less. The clock and data lanes V_{OD} can be changed through I^2C reg0Ch[7:2], VSWING_DATA and VSWING_CLK.

8.3.10 Slew Rate Control

The TDP158 has the ability to slow down the TMDS output edge rates. As the clock signal tends to be a primary source of EMI the edge rates have been slowed down. There are two ways of changing the slew rate, Pin strapping for clock lane and I^2C for both clock and data lanes. See Table 5 and Table 6.

Table 5. TMDS_CLK Output Slew Rate Control

Pin 34	Reg0Bh[7:6]	General	Typical Value (ps)
L	00	Slowest	215
NC	01 (Default)	Mid-range 1	185
	10	Mid-range 2	155
H	11	Fastest	125

Table 6. TMDS_D0, D1, D2 Output Slew Rate Control

No Pin Control	Reg0Ah[1:0]	General	Typical Value (ps)
NA	00	Slowest	110
NA	01	Mid-range 1	95
NA	10	Mid-range 2	80
NA	00 (Default)	Fastest	60

8.3.11 Pre-emphasis

The TDP158 provides Pre-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP158 outputs and a TMDS receiver. Pre-emphasis is not implemented on the clock lane unless the TDP158 is in DP Mode and at which time it becomes a data lane. The default value for Pre-emphasis is 0 dB. There are two methods to implement pre-emphasis, pin strapping or through I^2C programming. When using pin strapping the SDA_CTL/PRE pin controls global pre-emphasis values of 0 dB or 3.5 dB. Through I^2C, reg0Ch[1:0] pre-emphasis values are 0 dB, 3.5 dB and 6 dB. The 6 dB value has different meanings when device is normal operational mode, reg09h[5] = 0, or when the TDP158 has been put into DP-Mode, reg09h[5] = 1. In normal operation supporting HDMI when selecting 6 dB pre-emphasis the output will be more on the order of 3 dB pre-emphasis with a 3 dB de-emphasis, see Figure 25. For DP-Mode selecting 6 dB pre-emphasis the output will be more on the order of 3 dB pre-emphasis with a 3 dB de-emphasis, see Figure 26. Table 7 shows $V_{OD(SS)}$ typical values based upon VSADJ setting configured by 6 kΩ VSADJ resistor for both HDMI mode and DP mode. $V_{OD(PP)}$ value will not go above 1 V.

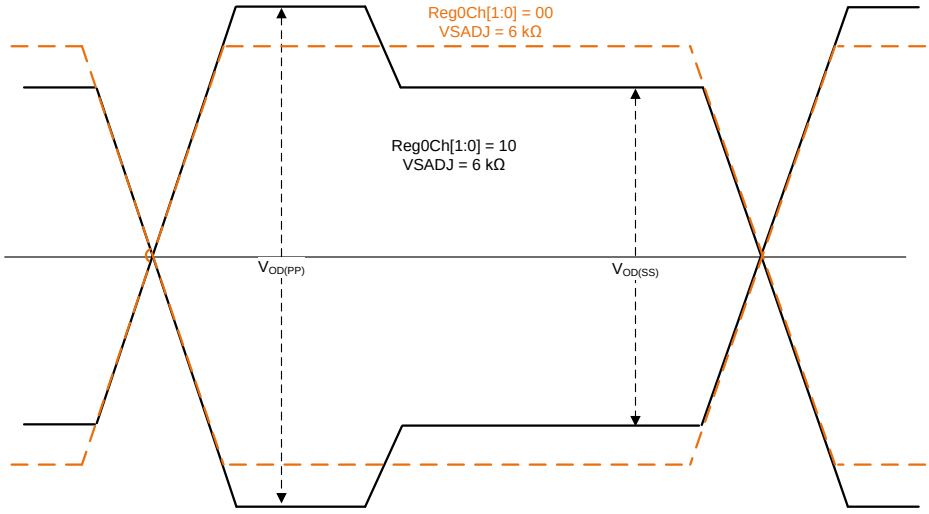


Figure 25. 3.5 dB Pre-emphasis in Normal Operation

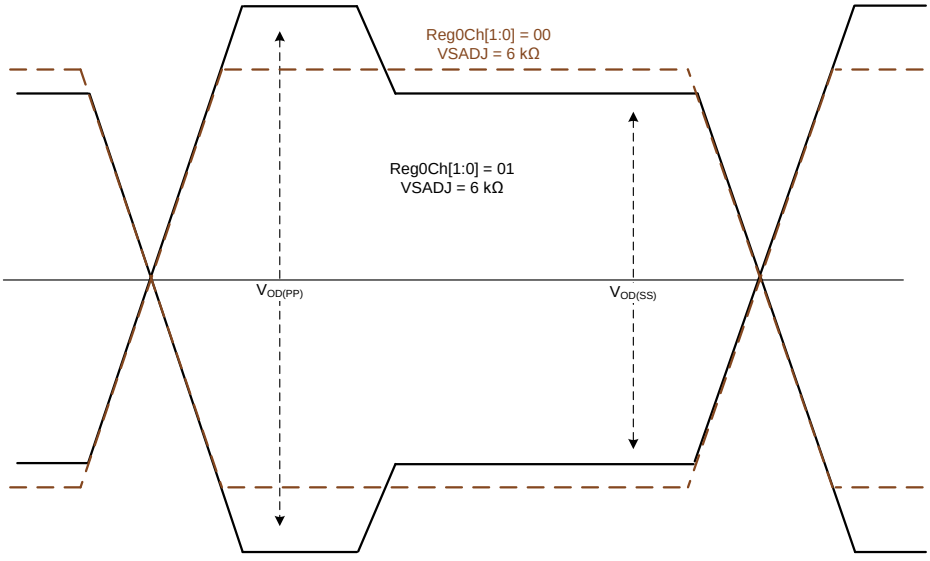


Figure 26. 6 dB Pre-emphasis in DP-Mode

Table 7. Swing and Pre-emphasis Programming Based Upon 6 kΩ VSADJ Resistor

	Global Control			Independent Lane Control		
Mode	**Reg09h[6] Lane CTL**	**Reg09[5] Mode CTL**	**P0_Reg0C[7:0]**	**Reg09h[6] Lane CTL**	**Reg09[5] Mode CTL**	**P0_Reg0C[7:0]**
HDMI	0	0	8'h00	1	0	8'h00
DP SWG0, PRE0	0	1	8'h80	1	1	8'h80
DP SWG0, PRE1	0	1	8'hC1	1	1	8'hC1
DP SWG0, PRE2	0	1	8'h42	1	1	8'h42
DP SWG1, PRE0	0	1	8'hC0	1	1	8'hA0
DP SWG1, PRE1	0	1	8'hF1	1	1	8'h21
DP SWG1, PRE2	0	1	8'h52	1	1	8'h62
DP SWG2, PRE0	0	1	8'h20	1	1	8'h00
DP SWG2, PRE1	0	1	8'h51	1	1	8'h61

8.3.12 DP-Mode Description

The TDP158 has the ability to perform as a DisplayPort redriver under the right conditions. The TDP158 is put into this mode by setting reg09h[5] to 1. The device is now programmable through I^2C only. As the transmitter is a DC coupled transmitter supporting TMDS some external circuits are required to level shift the signal to an AC coupled DisplayPort signal, see Figure 49. Note that the AUX lines bypass the TDP158. To set the device up correctly during link training the TDP158 must be programmed using I^2C. When this bit is set, the TDP158 does the following:

- Ignore SWAP function
- Ignore SIG_EN function
- Enable all four lanes and set to support 5.4 Gbps data rate
- Sets V_{OD} swing to the lowest level based on a 6 kΩ VSADJ resistor value
- Sets Pre-emphasis to 0 dB
- Defaults to global lane control
- Can be set to independent lane control by setting P0_Reg09[6] to a 1. This should be done after implementing DP Mode. Individual Lane control starts on P0_Reg30 through P0_Reg34 and also P0_Reg4E and 4F

In order for the system implementer to configure the TDP158 output to the properly requested levels during link training, the following registers are used.

- Reg0Ch[7:5] is a global V_{OD} swing control for all four lanes, see Table 7
- Reg0Ch[1:0] is a global Pre-emphasis control for all four lanes, see Table 7. This register works with Reg30h[7:6]
- Reg0D[6:3] is a global EQ control for all four lanes
- Reg30h[7:6] is to let the TDP158 know what the data rate is. This is used for the delay component for Pre-emphasis signal.
- Reg30h[5:2] is used to turn on or off individual lanes

Power down states while in DP-Mode are implemented the same as if in normal operation. See the *Electrical Characteristics, TMDS Differential Output* for the outputs based upon the VSADJ 6 kΩ VSADJ resistor.

8.4 Device Functional Modes

8.4.1 DDC Training for HDMI2.0 Data Rate Monitor

As part of discovery the source reads the sink E-EDID information to understand the sink's capabilities. Part of this read is HDMI Forum Vendor Specific Data Block (HF-VSDB) MAX_TMDS_Character_Rate byte to determine the data rate supported. Depending upon the value the source will write to slave address 0xA8 offset 0x20 bit1, TMDS_CLOCK_RATIO_STATUS. The TDP158 snoops the DDC link to determine the TMDS clock ratio status and thus sets its own TMDS_CLOCK_RATIO_STATUS bit accordingly. If a '1' is written by the source the TMDS clock is 1/40 of TMDS bit period. If a '0' is written, then the TMDS clock is 1/10 of TMDS bit period.

Device Functional Modes (continued)

The TDP158 will always default to 1/10 of TMDS bit period unless a '1' is written to address 0xA8 offset 0x20 bit 1 or during a read by the source this bit is set. This helps determine source termination when automatic source termination select is enabled. Otherwise this bit has no other impact on the TDP158. When HPD_SNK is de-asserted this bit is reset to default values of 0 if this feature is enabled. If the source does not write this bit to the sink or during the read the bit is not set the TDP158 will not set the output termination to 75 Ω to 150 Ω in support of HDMI2.0. If the TDP158 has entered a power down state using HDP_SNK = low or OE = low this bit is cleared and will be set on a read or write where this bit is set. When DDC_TRAIN_SETDISABLE is 1'b0 the TMDS_CLOCK_RATIO_STATUS bit will reflect the value of the DDC snoop. When DDC_TRAIN_SETDISABLE is 1'b1 the TMDS_CLOCK_RATIO_STATUS bit is set by I^2C and DDC snoop is ignored and thus automatic TERM control is ignored and must be manually set. To go back to snoop and automatic TERM control the DDC_TRAIN_SETDISABLE bit has to be cleared and TERM set back to automatic control.

8.4.2 DDC Functional Description

The TDP158 solves sink/source level issues by implementing a master/salve control mode for the DDC bus. When the TDP158 detects the start condition on the DDC bus from the SDA_SRC/SCL_SRC it transfers the data or clock signal to the SDA_SNK/SCL_SNK with little propagation delay. When SDA_SNK detects the feedback from the downstream device the TDP158 pulls up or pull down the SDA_SRC bus and deliver the signal to the source.

The DDC link defaults to 100kbps but can be set to various values including 400 kbps by setting the correct value to address 22h through the I^2C interface. The HPD goes to high impedance when VCC is under low power conditions, < 1.5 V.

NOTE

The TDP158 uses clock stretching for DDC transactions. As there are sources and sinks that do not perform this function correctly a system may not work correctly as DDC transactions are incorrectly transmitted/received. To overcome this, a snoop configuration can be implemented where the SDA/SCL from the source is connected directly to the SDA/SCL pins. The TDP158 needs the SDA_SNK and SCL_SNK pins connected to the sink DDC pins so that the TMDS_CLOCK_RATIO_STATUS bit can be automatically set otherwise it will have to be set through I^2C. For best noise immunity, the SDA_SRC and SCL_SRC pins should be connected to GND. Care must be taken when this configuration is being implemented as the voltage level for DDC between the source and sink may be different, 3.3 V vs 5 V.

8.5 Register Maps

The TDP158 local I^2C interface is enabled when I^2C_EN is high. The SCL_CTL and SDA_CTL terminals are used for I^2C clock and data respectively. The TDP158 I2C interface conforms to the two-wire serial interface defined by the I^2C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400 kbps. The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for TDP158 decides by the combination of A0/EQ1 and A1/EQ2. Table 8 clarifies the TDP158 target address.

Table 8. TDP158 I2C Device Address Description

A1/A0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
00	1	0	1	1	1	1	0	0/1	BC/BD
01	1	0	1	1	1	0	1	0/1	BA/BB
10	1	0	1	1	1	0	0	0/1	B8/B9
11	1	0	1	1	0	1	1	0/1	B6/B7

The local I^2C is 5-V tolerant, and no additional circuitry required. Local I^2C buses run at 400 kHz supporting fast-mode I^2C operation.

The following procedure is followed to write to the TDP158 I^{2}C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TDP158 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TDP158 acknowledges the address cycle.
3. The master presents the sub-address (I^{2}C register within TDP158) to be written, consisting of one byte of data, MSB-first.
4. The TDP158 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^{2}C register.
6. 6. The TDP158 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TDP158.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the TDP158 I^{2}C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TDP158 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TDP158 acknowledges the address cycle.
3. The TDP158 transmit the contents of the memory registers MSB-first starting at register 00h.
4. The TDP158 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^{2}C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TDP158 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

NOTE

Upon reset, the TDP158 sub-address will always be set to 0x00. When no sub-address is included in a read operation, the TDP158 sub-address will increment from previous acknowledged read or write data byte. If it is required to read from a sub-address that is different from the TDP158 internal sub-address, a write operation with only a sub-address specified is needed before performing the read operation.

Refer to *Local I^{2}C Control BIT Access TAG Convention* for TDP158 local I^{2}C register descriptions. Reads from reserved fields or addresses not specified return zeros. If they are written to and then read they will read back what was written but will not impact the device features or performance.

8.5.1 Local I^{2}C Control BIT Access TAG Convention

Reads from reserved fields shall return zero, and writes to read-only reserved registers shall be ignored. Writes to reserved register which are marked with ‘W’ will produce unexpected behavior. All addresses not defined by this specification shall be considered reserved. Reads from these addresses shall return zero and writes shall be ignored

8.5.2 BIT Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are described in Table 9.

Table 9. Field Access Tags

Access Tag	Name	DESCRIPTION
R	Read	The field shall be read by software
W	Write	The field shall be written by software
S	Set	The field shall be set by a write of one. Writes of Zero to the field have no effect
C	Clear	The field shall be cleared by a write of one. Writes of Zero to the field have no effect
U	Update	Hardware may autonomously update this field
NA	No Access	Not accessible or not applicable

8.5.3 CSR BIT FIELD DEFINITIONS, DEVICE_ID (address = 00h~07h)

Figure 27. DEVICE_ID

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. DEVICE_ID Field Descriptions

Bit	Field	Type	Reset	Description
7:0		R	TBD	These fields return a string of ASCII characters “TDP158” followed by one space characters TDP158: Address 0x00 – 0x07 = {- 0x54”T”, 0x44”D”, 0x50”P”, 0x31”1”, 0x35”5”, 0x38”8, 0x20, 0x20

8.5.4 CSR BIT FIELD DEFINITIONS, REV_ID (address = 08h)

Figure 28. REV_ID Field Descriptions

7	6	5	4	3	2	1	0
REV_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REV_ID

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	TBD	This field identifies the device revision. 0000001 – TDP158 Revision

8.5.5 CSR BIT FIELD DEFINITIONS – MISC CONTROL 09h (address = 09h)

Figure 29. MISC CONTROL 09h Field Descriptions

7	6	5	4	3	2	1	0
LANE_SWAP	Lane Control	DP-Mode	SIG_EN	PD_EN	HPD_AUTO_PWRDWN_DISABLE	I2C_DR_CTL	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. MISC CONTROL 09h

Bit	Field	Type	Reset	Description
7	LANE_SWAP	R/W	1’b0	This field Swaps the input lanes as per Figure 23 and Swap and valid when in HDMI Mode only. 0 --- Disable (default) No Lane Swap 1 --- Enable: Swaps both Input and Output Lanes
6	Lane Control	R/W	1’b0	See Lane Control 0 – Global (Default) 1 – Independent Note: In default mode reg0C and reg0D control all lanes. When set to 1 each lane can be individually controlled for Swing, EQ, Pre-emphasis.
5	DP-Mode	R/W	1’b0	See DP-Mode Description 0 – Normal DP158 Operation (Default) 1 – All lanes behave as data lanes and full control through I2C only

Table 12. MISC CONTROL 09h (continued)

Bit	Field	Type	Reset	Description
4	SIG_EN	R/W	1'b1	This field enable the clock lane activity detect circuitry. See *Input Signal Detect Block* 0 – Disable Clock detector circuit closed and receiver always works in normal operation. 1 – Enable (default) , Clock detector circuit will make receiver automatic enter the standby state when no valid data detect.
3	PD_EN	R/W	1'b0	0 – Normal working (default) 1 – Forced Power down by I2C, Lowest Power state
2	HPD_AUTO_PWRDWN_DISABL	R/W	1'b0	0 – Automatically enters power down mode based on HPD_SNK (default) 1 – Will not automatically enter power down mode
1:0	I2C_DR_CTL	R/W	2'b10	I2C data rate supported for configuring device. 00 – 5Kbps 01 – 10Kbps 10 – 100Kbps(Default) 11 – 400Kbps

8.5.6 CSR BIT FIELD DEFINITIONS – MISC CONTROL 0Ah (address = 0Ah)

Figure 30. MISC CONTROL 0Ah Field Descriptions

7	6	5	4	3	2	1	0
Reserved	HPDSNK_GATE_EN	Reserved				SLEW_CTL_DATA	
R	R/W	R				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. MISC CONTROL 0Ah

Bit	Field	Type	Reset	Description
7	Reserved	R	1'b0	Reserved
6	HPDSNK_GATE_EN	R/W	1'b0	The field set the HPD_SNK signal pass through to HPD_SRC or not and HPD_SRC whether held in the de-asserted state. 0 – HPD_SNK passed through to the HPD_SRC (default) 1 – HPD_SNK will not pass through to the HPD_SRC.
5:2	Reserved	R	1'b0	Reserved
1:0	SLEW_CTL_DATA	R/W	1'b0	See *Slew Rate Control* 00 – Slowest ~ 110 01 – Mid-Range 1 ~ 95 10 – Mid-Range 2 ~B 80 ps 11 – Fastest (Default) ~ 60 ps Values are typical

8.5.7 CSR BIT FIELD DEFINITIONS – MISC CONTROL 0Bh (address = 0Bh)

Figure 31. MISC CONTROL 0Bh Field Descriptions

7	6	5	4	3	2	1	0
SLEW_CTL_CLK		Reserved	TERM		DDC_DR_SEL	TMDS_CLOCK_RATIO_STATUS	DDC_TRAIN_SETDISABLE
R/W		R	R/W		R/W	R/W/U	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. MISC CONTROL 0Bh

Bit	Field	Type	Reset	Description
7:6	SLEW_CTL_CLK	R/W	2'b01	See *Slew Rate Control* 00 – Slowest ~ 215 ps 01 – Mid-Range 1 (Default) ~ 185 ps 10 – Mid-Range 2 ~ 155 ps 11 – Fastest ~ 125 ps Values are typical
5	Reserved	R	1'b0	Reserved
4:3	TERM	R/W	2'b10	Controls termination for HDMI TX. See *Transmitter Impedance Control* 00 – 150 to 300 Ω 01 – No termination 10 – Follows TMDS_CLOCK_RATIO_STATUS bit (default). When = 1 termination value is 75 to 150 Ω: When = 0 No termination 11 – 75 to 150 Ω: Note: When TMDS_CLOCK_RATIO_STATUS bit reg0Bh[1] = 1 this register will automatically be set to 11 for 75 to 150 Ω but can be overwritten using this address
2	DDC_DR_SEL	R/W	1'b0	Defines the DDC output speed for DDC bridge 0 = 100kbps (default) 1 = 400kbps
1	TMDS_CLOCK_RATIO_STATUS	R/W/U	1'b0	This field is updated from snoop of I2C write to slave address 0xA8 offset 0x20 bit 1 that occurred on the SDA_SRC/SCL_SRC interface. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b1 or read as a 1'b1, then this field will be set to a 1'b1. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b0, then this field will be set to a 1'b0. This field is reset to default value whenever HPD_SNK is de-asserted for greater than 2ms. The main function of this bit is to automatically set the proper TX termination when value = 1. 0 – HDMI1.4b (default) 1 – HDMI2.0 Note 1. When DDC_TRAIN_SETDISABLE is 1'b0 this bit will reflect the value of the DDC snoop. Note 2. When DDC_TRAIN_SETDISABLE is 1'b1 this bit is set by I2C and DDC snoop is ignored. If this bit was set to 1 during snoop prior to the DDC_TRAIN_SETDISABLE being set to 1 it will be cleared to 0.
0	DDC_TRAIN_SETDISABLE	R/W	1'b0	This field indicate the DDC training block function status. 0 – DDC training enable (default) 1 – DDC training disable –DDC snoop disabled Note 1. When DDC_TRAIN_SETDISABLE is 1'b0 the TMDS_CLOCK_RATIO_STUATU bit will reflect the value of the DDC snoop. Note 2. When DDC_TRAIN_SETDISABLE is 1'b1 this bit is set by I2C and DDC snoop is ignored and thus automatic TERM control is ignored and must be manually set and TMDS_CLOCK_RATIO_STATUS bit will be cleared. Note 3. To go back to snoop and automatic TERM control this bit has to be cleared and TERM set back to automatic control.

8.5.8 CSR BIT FIELD DEFINITIONS – MISC CONTROL 0Ch (address = 0Ch)

Figure 32. MISC CONTROL 0Ch Field Descriptions

7	6	5	4	3	2	1	0
VSWING_DATA			VSWING_CLK			HDMI_TWPST1[1:0]	
R/W			R/W			R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. MISC CONTROL 0Ch

Bit	Field	Type	Reset	Description
7:5	VSWING_DATA	R/W	3'b000	Data Output Swing Control 000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%
4:2	VSWING_CLK	R/W	3'b000	Clock Output Swing Control: Default is set by Vsadj resistor value and the value of reg0Dh[0]. 000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%
1:0	HDMI_TWPST1[1:0]	R/W	2'b00	HDMI Pre-emphasis 00 – No Pre-emphasis (default) 01 – 3.5 dB 10 – 6 dB 11 – Reserved NOTE: See Pre-emphasis Section for 6 dB explanation during normal operation supporting HDMI.

8.5.9 CSR BIT FIELD DIFINITIONS, Equalization Control Register (address = 0Dh)

Figure 33. Equalization Control Register

7	6	5	4	3	2	1	0
Reserved	Data Lane Fixed EQ Values				Clock EQ Values		DIS_HDMI2_SWG
R	R/W				R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Equalization Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	1'b0	Reserved
6:3	Data Lane Fixed EQ Values	R/W	4'b0000	(Section *Receiver Equalizer* and Table 3 for values) 0000 – 0 dB (default)
2:1	Clock EQ Values	R/W	2'b00	00 – 0dB (default) 01 – 1.5dB 10 – 3dB 11 – 4.5dB
0	DIS_HDMI2_SWG	R/W	1'b0	Disables halving the clock output swing when entering HDMI2.0 mode from TMDS_CLOCK_RATIO_STATUS. 0 – Disables TMDS_CLOCK_RATIO_STATUS control of the clock VOD so output swing is at full swing (default) 1 – Clock VOD is half of set values when TMDS_CLOCK_RATIO_STATUS states in HDMI2.0 mode

8.5.10 CSR BIT FIELD DEFINITIONS, POWER MODE STATUS (address = 20h)

Figure 34. POWER MODE STATUS

7	6	5	4	3	2	1	0
Power Down Status Bit	Standby Status Bit	Loss of Signal Status Bit – LOS	Reserved				
R/U	R/U	R/U	R				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. POWER MODE STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7	Power Down Status Bit	R/U	1'b0	0 – Normal Operation 1 – Device in Power Down Mode.
6	Standby Status Bit	R/U	1'b0	0 – Normal Operation 1 – Device in Standby Mode
5	Loss of Signal Status Bit – LOS	R/U	1'b0	0 – Clock present 1 – No Clock present
4:0	Reserved	R	5'b00000	Reserved

8.5.11 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 30h)

See Section 8.3.10 and 8.3.3 Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 35. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Data Rate Select		Clock Lane	Lane D0	Lane D1	Lane D2	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Data Rate Select	R/W	2'b00	00 – 5.4 Gbps (default) 01 – 2.7 Gbps 10 – 1.62 Gbps 11 - Reserved
5	Clock Lane	R/W	1'b1	0 – Disabled 1 – Enabled (default)
4	Lane D0	R/W	1'b1	0 – Disabled 1 – Enabled (default)
3	Lane D1	R/W	1'b1	0 – Disabled 1 – Enabled (default)
2	Lane D2	R/W	1'b1	0 – Disabled 1 – Enabled (default)
1:0	Reserved	R	2'b00	Reserved

8.5.12 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 31h)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 36. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for CLK Lane			Pre-emphasis Adjust for CLK Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for CLK Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for CLK Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5 dB Pre-emphasis. 10 – 6 dB Pre-emphasis 11 – Reserved Note 1. reg09h[6] = 1 otherwise all lanes are global control. Note 2. If in HDMI mode writes will be ignored and reg09h[7] SWAP = 0. No pre-emphasis on clock.
2:0	Reserved	R/W	3'b000	Reserved

8.5.13 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 32h)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 37. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D0 Lane			Pre-emphasis Adjust for D0 Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D0 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 11 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for D0 Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5 dB Pre-emphasis. 10 – 6 dB Pre-emphasis 11 – Reserved Note: reg09h[6] = 1 otherwise all lanes are global control.
2:0	Reserved	R/W	3'b000	Reserved

8.5.14 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 33h)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 38. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D1 Lane			Pre-emphasis Adjust for D1 Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D1 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 11 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for D1 Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5 dB Pre-emphasis. 10 – 6 dB Pre-emphasis 11 – Reserved Note: reg09h[6] = 1 otherwise all lanes are global control.
2:0	Reserved	R/W	3'b000	Reserved

8.5.15 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 34h)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 39. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
VOD Swing Adjust for D2 Lane			Pre-emphasis Adjust for D2 Lane		Reserved		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOD Swing Adjust for D2 Lane	R/W	3'b000	000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 11 – Decrease by 7% Note: reg09h[6] = 1 otherwise all lanes are global control.
4:3	Pre-emphasis Adjust for D2 Lane	R/W	2'b00	00 – No Pre-emphasis (default) 01 – 3.5 dB Pre-emphasis. 10 – 6 dB Pre-emphasis 11 – Reserved Note 1. reg09h[6] = 1 otherwise all lanes are global control. Note 2. If in HDMI mode writes will be ignored and reg09h[7] SWAP = 1. No pre-emphasis on clock.
2:0	Reserved	R/W	3'b000	Reserved

8.5.16 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 35h)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 40. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	‘h00	Reserved

8.5.17 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Dh)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 41. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	‘h00	Reserved

8.5.18 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Eh)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 42. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
Data Lane 1 Fixed EQ Values				Data Lane 2 Fixed EQ Values			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Data Lane 1 Fixed EQ Values	R/W	4’b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0 dB (default)
3:0	Data Lane 2 Fixed EQ Values	R/W	4’b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0 dB (default)

8.5.19 CSR BIT FIELD DIFINITIONS, DP-Mode and INDIVIDUAL LANE CONTROL (address = 4Fh)

See Section *DP-Mode Description* and *Lane Control* Note: DP-Mode is valid only when DP-Mode Register P0_Reg09[5] is set to one

Figure 43. DP-Mode and INDIVIDUAL LANE CONTROL

7	6	5	4	3	2	1	0
CLK Lane Fixed EQ Values				Data Lane 0 Fixed EQ Values			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. DP-Mode and INDIVIDUAL LANE CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CLK Lane Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0 dB (default)
3:0	Data Lane 0 Fixed EQ Values	R/W	4'b0000	Section 8.3.6 and Table 8 2 for values 0000 – 0 dB (default)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TDP158 was defined to work in mainly in source applications such as Blu-Ray DVD player, Desktop, Notebook or AVR. When in a sink application there are several system level architectures that must be considered. The following sections provide design consideration for various types of applications.

9.2 Typical Application

Figure 44 provides a schematic representation of what is considered a standard implementation.

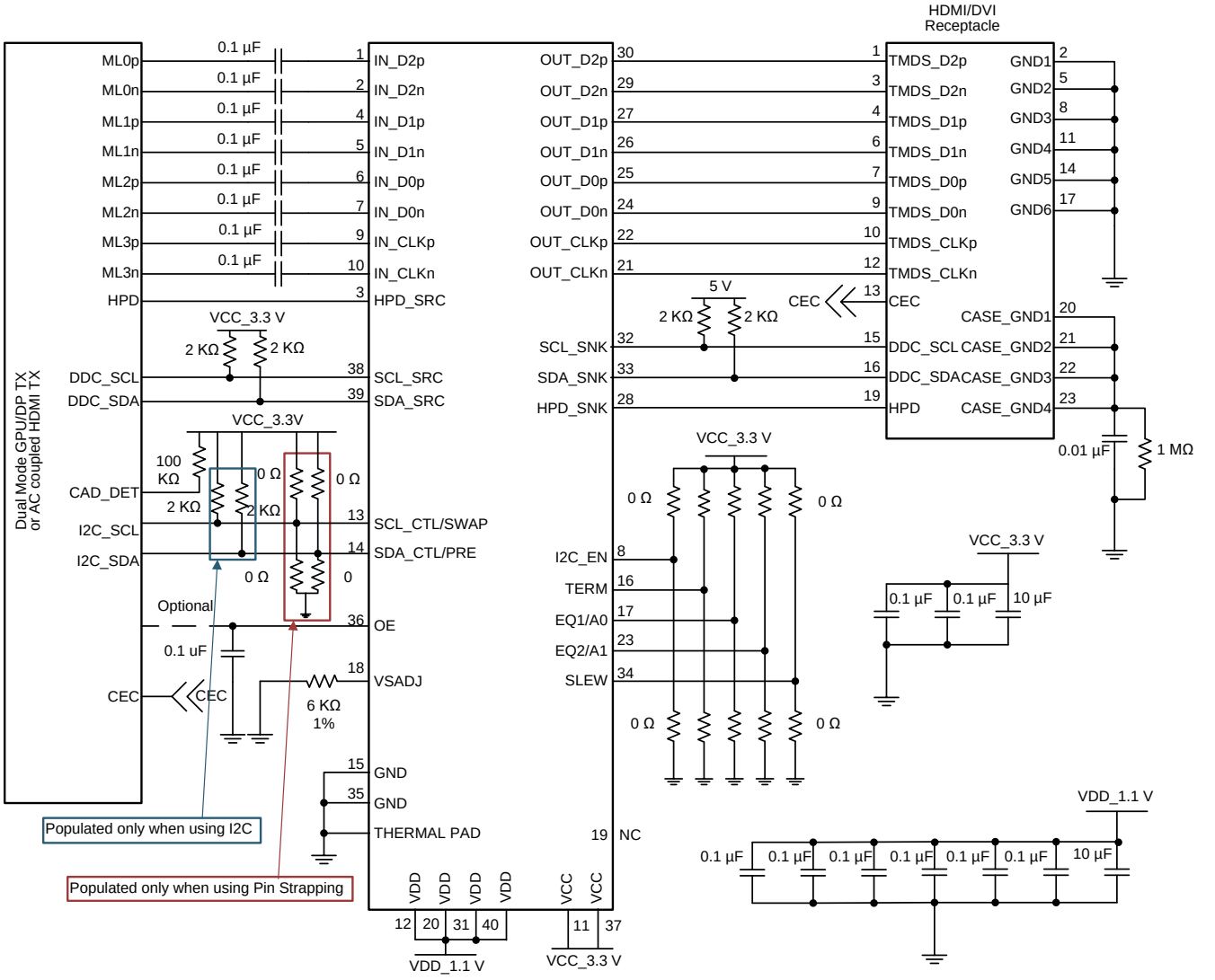


Figure 44. TDP158 in Source Side Application

Typical Application (continued)

9.2.1 Design Requirements

The TDP158 can be designed into many different applications. In all the applications there are certain requirements for the system to work properly. Two voltage rails are required in order to support lowest power consumption possible. OE pin must have a 0.1-µF capacitor to ground. This pin can be driven by a processor but the pin needs to change states after voltage rails have stabilized. The best way to configure the device is by using I2C but pin strapping is also provided as I^2C is not available in all cases. As sources may have many different naming conventions it is necessary to confirm that the link between the source and the TDP158 are correctly mapped. A Swap function is provide for the input pins incase signaling if reversed between source and device. The control pin values below are based upon driving pins with a microcontroller, otherwise, the shown pull up/down configuration meet device levels. Table below provides information on expected values in order to perform properly.

For this design, use the parameters shown in Table 27.

Table 27. Design Parameters

Design Parameter	Value
V_{CC}	3.3 V
V_{DD}	1.1 V
Main Link Input Voltage	V_{ID} = 0.15 to 1.4 Vpp
Control Pin Max Voltage for Low	Connect to GND
Control Pin Voltage Range Mid	Connect to GND
Control Pin Min Voltage for High	Connect to V_{CC}
$R_{(VSADJ)}$ Resistor	6 kΩ 1%

9.2.2 Detailed Design Procedure

9.2.2.1 Source Side

The TDP158 is a signal conditioning device that provides several forms of signal conditioning in order to support compliance for HDMI or DVI at a source connector. These forms of signal conditioning are accomplished using receive equalization, retiming, and output driver configurability. The transmitter will drive 1”- 2” of board trace and connector when compliance is required at the connector.

To design in the TDP158 the following need to be understood for a source side application:

- Determine the loss profile between the GPU/chipset and the HDMI/DVI connector.
- Based upon this loss profile and signal swing determine optimal location for the TDP158, in order to pass source electrical compliance. Usually within 1”- 2” of the connector.
- Use the typical application Figure 44 for information on control pin resistors.
- The TDP158 has a receiver equalizer but can also be configured using EQ1 and EQ2 control pins.
- Set the V_{OD}, Pre-emphasis, termination, and edge rate levels appropriately to support compliance by using the appropriate VSADJ resistor value and setting SDA_CTL/PRE, TERM and SLEW control pins.
- The thermal pad must be connected to ground.
- See schematics in Figure 44 on recommended decouple caps from V_{CC} pins to Ground.

9.2.2.2 DDC Pull Up Resistors

This section is for information only and subject to change depending upon system implementation. The pull-up resistor value is determined by two requirements:

1. The maximum sink current of the I^2C buffer:

   The maximum sink current is 3 mA or slightly higher for an I^2C driver supporting standard-mode I^2C operation.

$$R_{UP(min)} = \frac{V_{CC}}{I_{sink}} \tag{1}$$

2. The maximum transition time on the bus:

   The maximum transition time, T, of an I^2C bus is set by an RC time constant, where R is the pull-up resistor value, and C is the total load capacitance. The parameter, k, can be calculated from Equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 28 summarizes the possible values of k under different threshold combinations.

$$T = k \times RC \tag{2}$$

$$V(t) = V_{DD} \times (1 - e^{\frac{-t}{RC}}) \tag{3}$$

Table 28. Value k upon Different Input Threshold Voltages

V_{th}-|V_{th+}	0.7 V_{CC}	0.65 V_{CC}	0.6 V_{CC}	0.55 V_{CC}	0.5 V_{CC}	0.45 V_{CC}	0.4 V_{CC}	0.35 V_{CC}	0.3 V_{CC}
0.1 V_{CC}	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15 V_{CC}	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2 V_{CC}	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25 V_{CC}	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3 V_{CC}	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	

From Equation 1, Rup(min) = 5.5 V/3 mA = 1.83 kΩ to operate the bus under a 5-V pull-up voltage and provide less than 3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, Rup(min) can be as low as 1.375 kΩ.

If DDC working at standard mode of 100 Kbps, the maximum transition time T is fixed, 1 μs, and using the k values from Table 28, the recommended maximum total resistance of the pull-up resistors on an I^2C bus can be calculated for different system setups. If DDC working in fast mode of 400 Kbps, the transition time should be set at 300 ns according to I^2C specification.

To support the maximum load capacitance specified in the HDMI spec, $C_{(cable)}$(max) = 700 pF, $C_{(source)}$ = 50 pF, C_I = 50 pF, R(max) can be calculated as shown in Table 29.

Table 29. Pull-Up Resistor Upon Different Threshold Voltages and 800-pF Loads

V_{th}-|V_{th+}	0.7 V_{CC}	0.65 V_{CC}	0.6 V_{CC}	0.55 V_{CC}	0.5 V_{CC}	0.45 V_{CC}	0.4 V_{CC}	0.35 V_{CC}	0.3 V_{CC}	UNIT
0.1 V_{CC}	1.14	1.32	1.54	1.8	2.13	2.54	3.08	3.84	4.97	KΩ
0.15 V_{CC}	1.2	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	KΩ
0.2 V_{CC}	1.27	1.51	1.8	2.17	2.66	3.34	4.35	6.02	9.36	KΩ
0.25 V_{CC}	1.36	1.64	1.99	2.45	3.08	4.03	5.6	8.74	18.12	KΩ
0.3 V_{CC}	1.48	1.8	2.23	2.83	3.72	5.18	8.11	16.87	------	KΩ

To accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

9.2.3 Application Curves

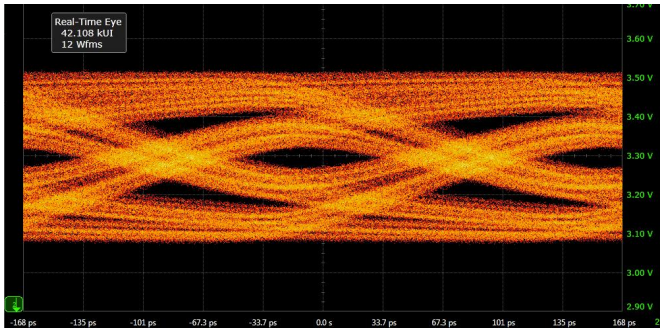


Figure 45. High Loss Input Eye -20” 4 mil Trace at TDP158 Pin

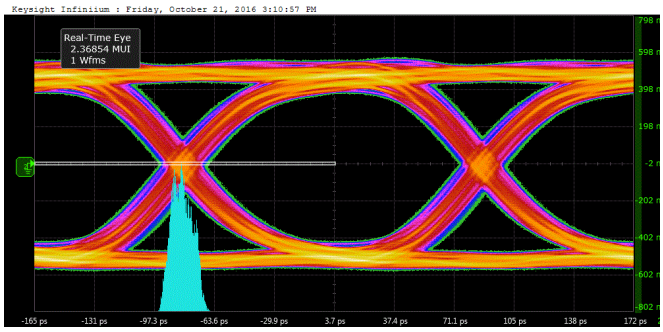


Figure 46. Output Eye from High Loss Input Eye at TDP158 Pin

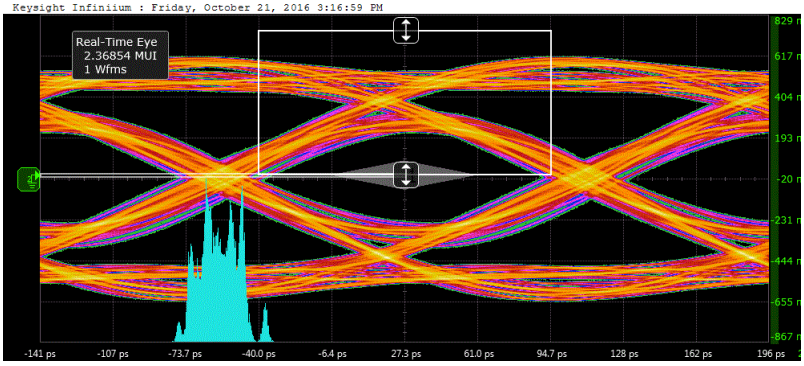


Figure 47. HDMI2 Compliance Eye from High Loss Input Eye

9.2.4 Application with DDC Snoop

9.2.4.1 Source Side HDMI Application

In source side applications the TDP158 takes an AC coupled HDMI signal and provides signal conditioning and level shifting to support TMDS signaling. Figure 48 provides an example of a DDC snoop version. Notes in both schematics provide important system design considerations. To help reduce overall EMI in a system the VCC and VDD decoupling caps need to be as close to the pins as possible. The drawings shown one set but multiple sets may be needed for each pin. In noisy systems a 4.7-pF capacitor may be added to the decoupling capacitors.

Control pins can be tied directly to VCC, GND or left floating. Drawings show 0-Ω resistors as this provides flexibility. In noisy systems a 0.1-µF capacitor to GND may reduce glitches on these pins and are not shown in the drawings. If an application requires completely bypassing the DDC source and sink pins on the TDP158 then connect them to GND as the SCL/SDA_SRC are shown in Figure 48. If this is done the TX termination must be controlled by the TERM pin or through I^2C.

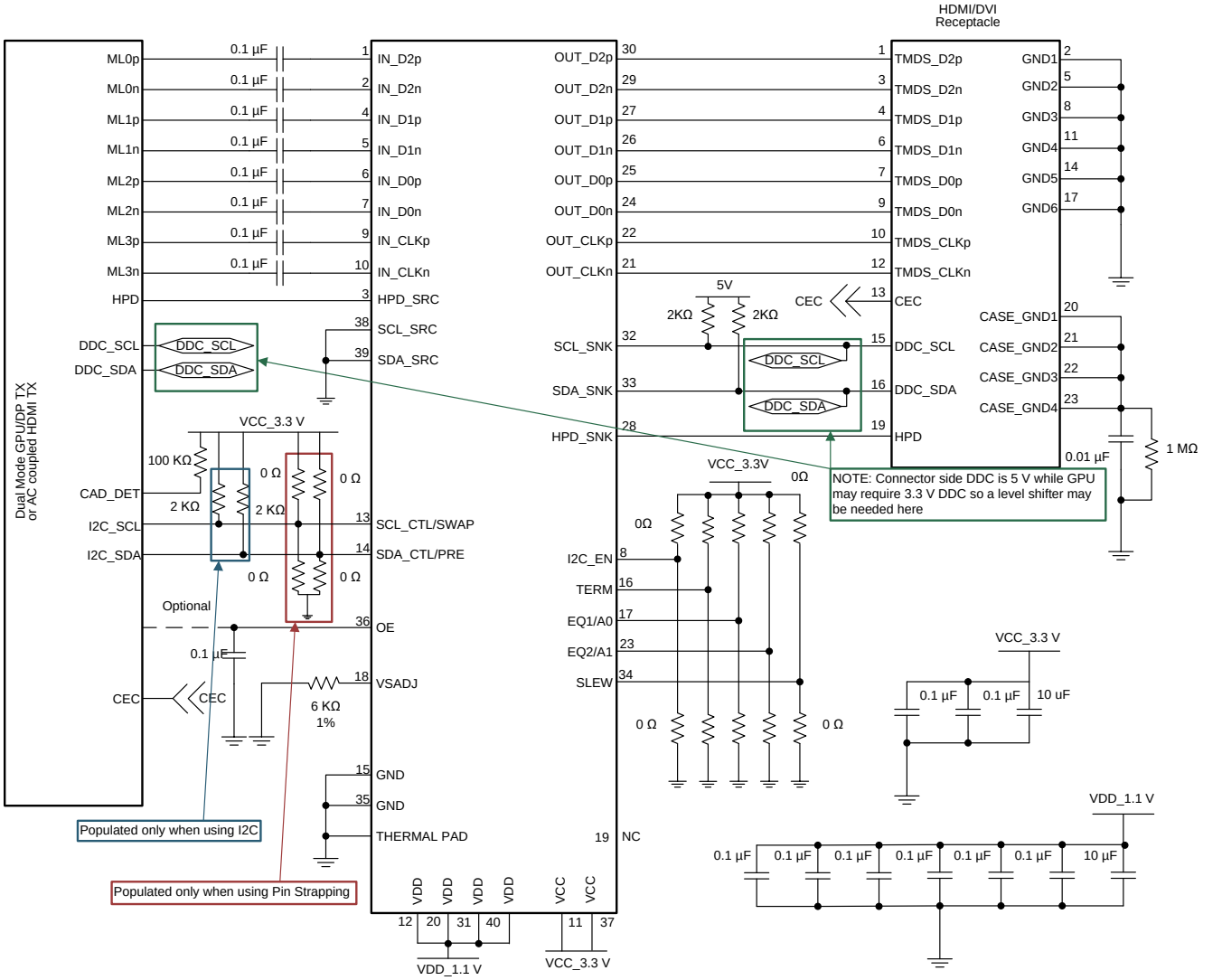


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Figure 48. TDP158 Source Side Application with DDC Snoop

9.2.5 9.1.2 Source Side HDMI/DP Application Using DP-Mode

The TDP158 has a special mode that will allow the device to support either HDMI or DP applications. The device is put into this mode by setting reg09h[5] to 1. The device will self-configure with the following settings and become I^2C programmable only. The TDP158 does not support automatic Link Training for DisplayPort. AUX channel bypasses device.

- All four lanes are turned on and configured for 5.4 Gbps data rate.
- Sets V_{OD} Swing to ~ 410 mV (This value is based upon a VSADJ value of 6 kΩ).
- Reg0Ch[7:5] is used to control VOD swing for all lanes.
- Reg0Ch[1:0] is used to control Pre-emphasis for all lanes.
- Reg30h[7:2] is used to turn on or off individual lanes as well as informing the TDP158 what the data rate is. This is used for the delay component for Pre-emphasis signal.

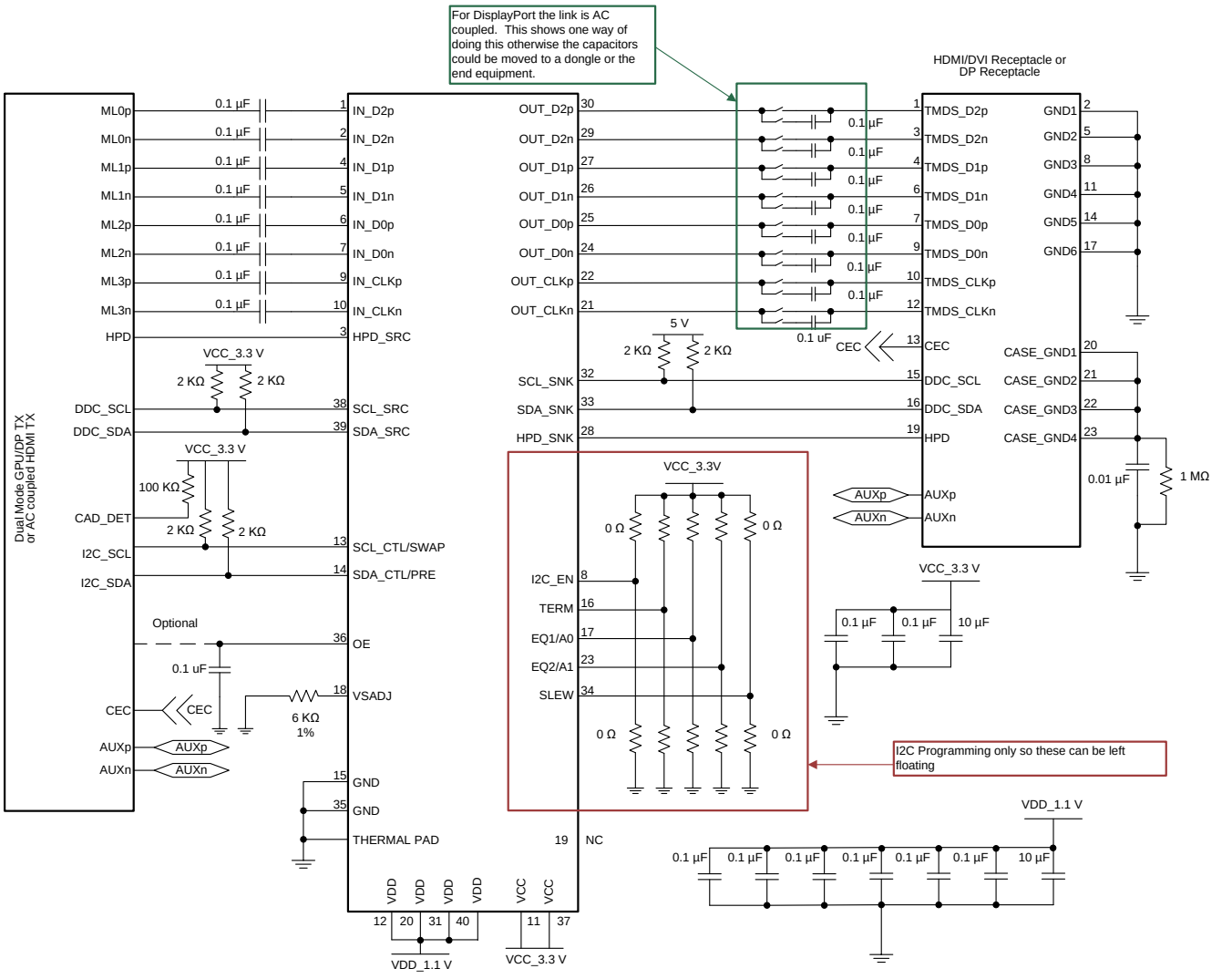


Figure 49. TDP158 in Dual Role Source Side Application

10 Power Supply Recommendations

10.1 Power Management

To minimize the power consumption of customer application, TDP158 used the dual power supply. V_{CC} is 3.3 V with 10% range to support the I/O voltage. The V_{DD} is 1.1 V with ~ 5% range to supply the internal digital control circuit. TDP158 operates in 3 different working states.

- Power down Mode:
  - OE = Low puts the device into its lowest power state by shutting down all function blocks.
    - When OE is re-asserted the transitions from L→H creates a reset and if the device is programmed through I^2C it must be reprogrammed.
  - Writing a 1 to register 09h[3].
  - OE = High, HPD_SNK = Low for > 2ms
- Standby Mode:
  - HPD_SNK = High but no valid clock signal detect on clock lane.
- Normal operation:
  - When HPD assert, the device output will enable based on the signal detector circuit result.
  - HPD_SRC = HPD_SNK in all conditions. The HPD channel operational when V_{CC} over 3 V.

NOTE

When the TDP158 is put into a power down state the I^2C registers are cleared. This is important as the TMDS_CLOCK_RATIO_STATUS bit will be cleared. If cleared and HDMI2.0 resolutions are to be supported the TDP158 expects the source to write a 1 to this bit location. If the read has the bit set, the TDP158 will set this bit; otherwise, the source termination must be set manually.

10.2 Standby Power

The TDP158/I implement a two stage standby power process.

Stage 1: If there is no signal on the Clock line, the max I_{VCC} ~ 5 ma and max I_{VDD} ~ 6 ma.

Stage 2: If a signal is on the clock line like noise or a clock signal, the TDP158 investigates for 3 µs to 5 µs at which time, it determines if a is clock present.

- If a clock is detected the TDP158 will go into normal operation.
- If it is determined that no clock is present the TDP158 will re-enter stage 1.

In stage 2; max I_{VCC} ~ 5 ma and max I_{VDD} ~ 27 ma.

Table 30. Power Modes

INPUTS				STATUS					
OE	HPD_SNK	Reg09[2]	IN_CLK	HPD_SRC	IN_Dx	SDA/SCL_CTL	OUT_Dx OUT_CLK	DDC	Mode
L	X	X	X	H	High-Z	Disable	High-Z	Disabled	Power Down Mode
H	X	1	X	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation
H	X	1	No Valid TMDS Clock	HPD_SNK	D0-D2 Disabled IN_CLK Active	Active	High-Z	Active	Standby Mode (Squelch waiting)
H	X	1	Valid TMDS Clock	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation
H	H	0	No Valid TMDS Clock	HPD_SNK	D0-D2 Disabled IN_CLK Active	Active	High-Z	Active	Standby Mode (Squelch waiting)
H	H	0	Valid TMDS Clock	HPD_SNK	RX Active	Active	TX Active	Active	Normal operation

11 Layout

11.1 Layout Guidelines

For the TDP158 On a high-K board – It is required to solder the PowerPAD™ onto the thermal land to ground. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board the TDP158 can operate over the full temperature range by soldering the PowerPAD onto the thermal land. On a low-K board, for the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\theta JA}$ = 100.84°C/W allowing 545 mW power dissipation at 70°C ambient temperature. A general PCB design guide for PowerPAD packages is provided in the document SLMA002 . TI recommends using at a minimum a four layer stack up to accomplish a low-EMI PCB design. TI recommends six layers as the TDP158 is a two voltage rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias. (and the introduction of their inductances) and allows for clean interconnects from the HDMI connectors to the Redriver inputs and outputs. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed single layer establishes controlled impedance for transmission link interconnects and provides an excellent low –inductance path for the return current flow.
- Placing a power plane next to the ground plane creates and additional high-frequency bypass capacitance.
- Routing slower seed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be place closer together, thus increasing the high frequency bypass capacitance significantly.

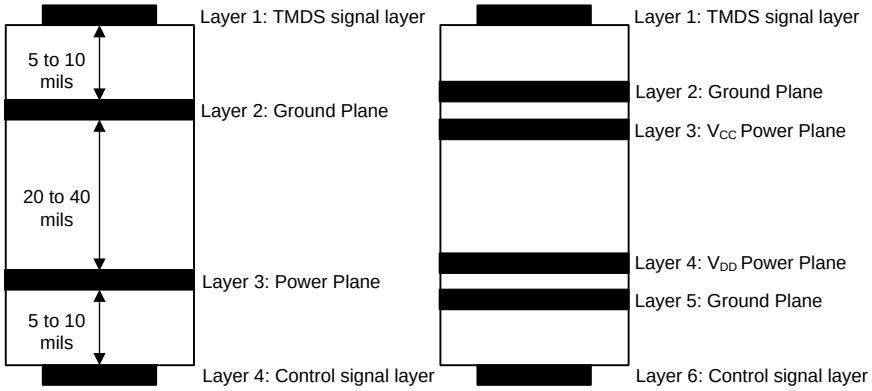
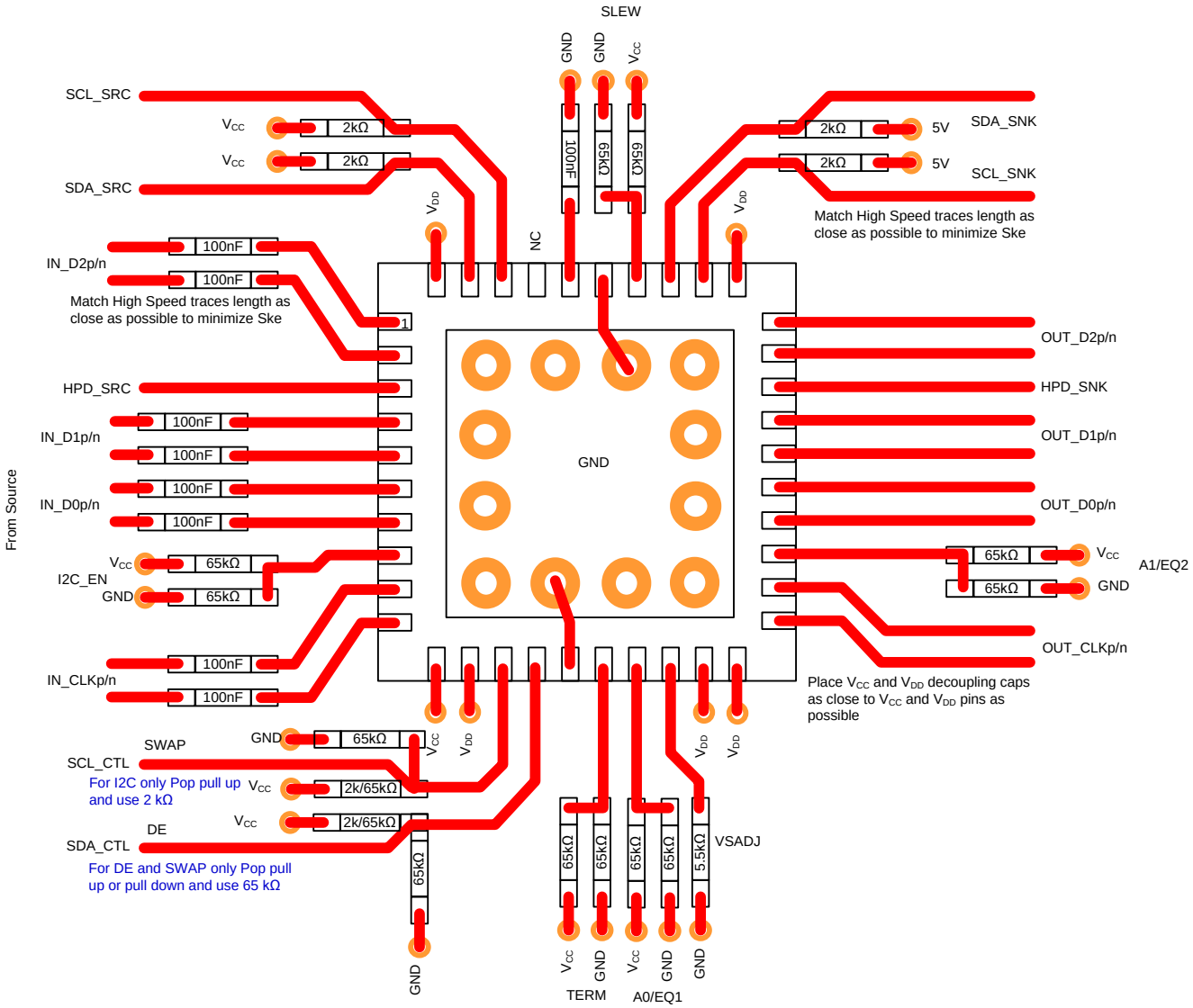


Figure 50. Recommended 4 – or 6 – Layer PCB Stack

11.2 Layout Example



The differential input lanes and differential output lanes should be separated as close to the TDP158 as feasible in order to minimize crosstalk. Adding a ground flood plain between each differential lane further reduces crosstalk and thus improves signal integrity at high speed data rates.

Figure 51. Example Layout for Source Side Application

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002
- [HDMI] High-definition Multimedia Interface Specification Version 1.4b October,2011 HDMI] High-definition Multimedia Interface Specification Version 2.0 September 4,2013
- [HDMI] High-definition Multimedia Interface CTS Version 1.4b October, 2011
- [HDMI] High-definition Multimedia Interface CTS Version 2.0o June 2016
- [I2C] The I2C-Bus specification version 2.1 January 2000

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 31. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TDP158	Click here	Click here	Click here	Click here	Click here
TDP158I	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
Blu-ray is a trademark of Blu-ray Disc Accociation.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDP158RSBR	PREVIEW	WQFN	RSB	40	3000	TBD	Call TI	Call TI	0 to 85		
TDP158RSBT	PREVIEW	WQFN	RSB	40	250	TBD	Call TI	Call TI	0 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

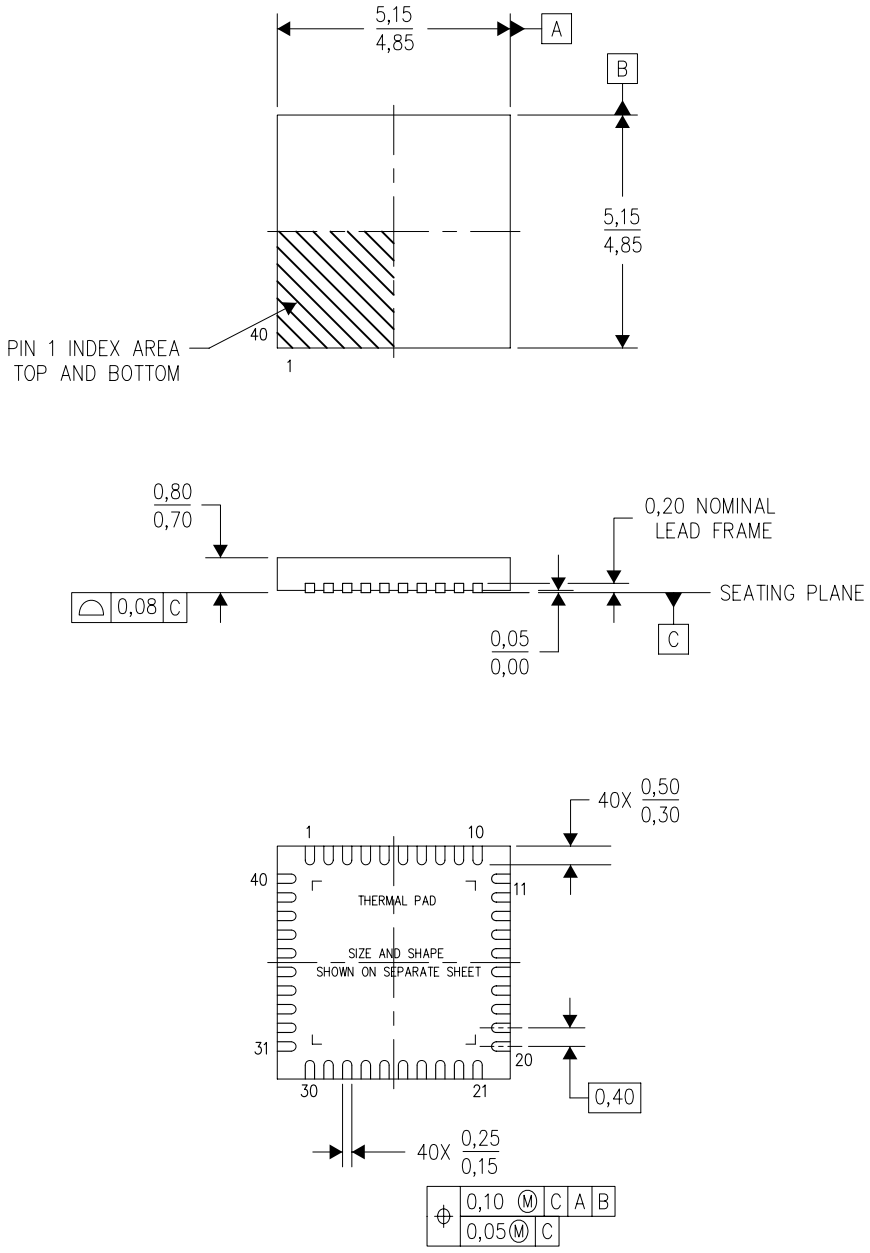
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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