Digital Input Class-D Speaker Amplifier with Audio Processing and mono headphone amplifier

Check for Samples: TAS2505

1 INTRODUCTION

1.1 Features

- **Digital Input Mono Speaker Amp**
- **Supports 8-kHz to 96-kHz Sample Rates**
- **Mono Class-D BTL Speaker Driver (2 W Into 4 Ω or 1.7 W Into 8 Ω)**
- **Mono Headphone Driver**
- **Two Single-Ended Inputs With Output Mixing and Level Control**
- **Embedded Power-on-Reset**
- **Integrated LDO**
- **Programmable Digital Audio Processing Blocks for Bass Boost, Treble, EQ With up to Six Biquads for Playback**
- **Integrated PLL Used for Programmable Digital Audio Processing Blocks**
- **I^{2}S, Left-Justified, Right-Justified, DSP, and TDM Audio Interfaces**
- **I^{2}C Control and SPI control with auto-increment**
- **Full Power-Down Control**
- **Power Supplies:**
  - **Analog: 1.5 V–1.95 V**
  - **Digital Core: 1.65 V–1.95 V**
  - **Digital I/O: 1.1 V–3.6 V**
  - **Class-D: 2.7 V–5.5 V (SPKVDD ≥ AVDD)**
- **24-Pin QFN Package (4mm × 4mm)**

1.2 Applications

- **Portable Audio Devices**
- **White goods**
- **Portable Navigation Devices**

1.3 Description

The TAS2505 is a low power digital input speaker amp with support for 24-bit digital I2S data mono playback.

In addition to driving a speaker amp upto 4-Ω, the device also features a mono headphone driver and a programmable digital-signal processing block. The digital audio data format is programmable to work with popular audio standard protocols (I^{2}S, left/right-justified) in master, slave, DSP and TDM modes. The programmable digital-signal processing block can support Bass boost, treble, or EQ functions. An on-chip PLL provides the high-speed clock needed by the digital signal-processing block. The volume level can be controlled by register control. The audio functions are controlled using the I^{2}C™ serial bus or SPI bus. The device includes an on-board LDO that runs off the speaker power supply to handle all internal device analog and digital power needs. The included POR as power-on-resetcircuit reliably resets the device into its default state so no external reset is required at normal usage; however, the device does have a reset pin for more complex system initialization needs. The device also includes two analog inputs for mixing and muxing in both speaker and headphone analog paths.

I^{2}C is a trademark of NXP B.V. Corporation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

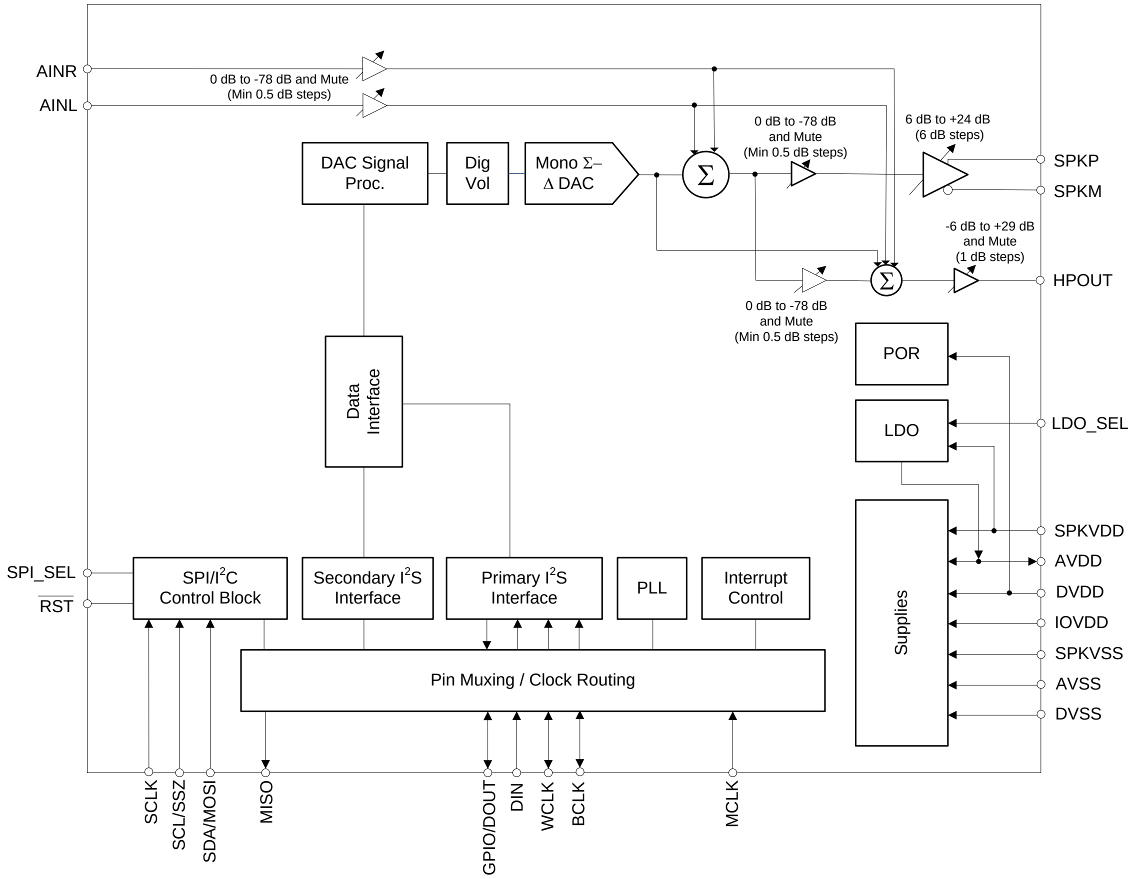

Figure 1-1. Simplified Block Diagram

NOTE

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2 PACKAGE AND SIGNAL DESCRIPTIONS

2.1 Package/Ordering Information

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TAS2505	QFN-24	RGE	–40°C to 85°C	TAS2505IRGET	Tape and reel, 250
				TAS2505IRGER	Tape and reel, 3000

2.2 Device Information

RGE PACKAGE
(TOP VIEW)

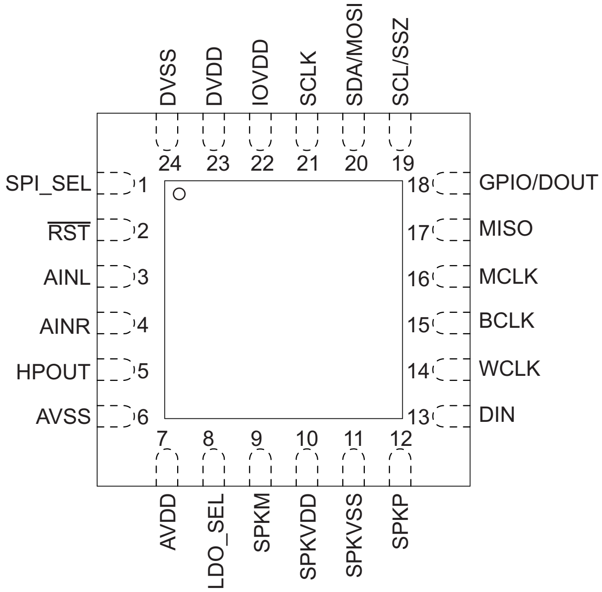


Table 2-1. RGE PIN FUNCTIONS

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
SPI_SEL	1	I	Selects between SPI and I2C digital interface modes; (1 = SPI mode) (0 = I2C mode)
$\overline{\text{RST}}$	2	I	Reset for logic, state machines, and digital filters; asserted LOW.
AINL	3	I	Analog single-ended line left input
AINR	4	I	Analog single-ended line right input
HPOUT	5	O	Headphone and Lineout Driver Output
AVSS	6	GND	Analog Ground, 0V
AVDD	7	PWR	Analog Core Supply Voltage, 1.5V - 1.95V, tied internally to the LDO output
LDO_SEL	8	I	Select Pin for LDO; ties to either SPKVDD or SPKVSS
SPKM	9	O	Class-D speaker driver inverting output
SPKVDD	10	PWR	Class-D speaker driver power supply
SPKVSS	11	PWR	Class-D speaker driver power supply ground supply
SPKP	12	O	Class-D speaker driver non-inverting output
DIN	13	I	Audio Serial Data Bus Input Data
WCLK	14	I/O	Audio Serial Data Bus Word Clock
BCLK	15	I/O	Audio Serial Data Bus Bit Clock
MCLK	16	I	Master CLK Input / Reference CLK for CLK Multiplier - PLL (On startup PLLCLK = CLKIN)
MISO	17	O	SPI Serial Data Output
GPIO/DOUT	18	I/O/Z	GPIO / Audio Serial Bus Output
SCL/SSZ	19	I	Either I2C Input Serial Clock or SPI Chip Select Signal depending on SPI_SEL state
SDA/MOSI	20	I	Either I2C Serial Data Input or SPI Serial Data Input depending on SPI_SEL state.
SCLK	21	I	Serial clock for SPI interface
IOVDD	22	PWR	I/O Power Supply, 1.1V - 3.6V
DVDD	23	PWR	Digital Power Supply, 1.65V - 1.95V
DVSS	24	GND	Digital Ground, 0V

(1) I = Input, O = Output, GND = Ground, PWR = Power, Z = High Impedance

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	**MAX**	
AVDD to AVSS		–0.3	2.2	V
DVDD to DVSS		–0.3	2.2	V
SPKVDD to SPKVSS		–0.3	6	V
IOVDD to IOVSS		–0.3	3.9	V
Digital input voltage		IOVSS – 0.3	IOVDD + 0.3	V
Analog input voltage		AVSS – 0.3	AVDD + 0.3	V
Operating temperature range		–40	85	°C
Storage temperature range		–55	150	°C
Junction temperature (T_J Max)			105	°C
QFN	Power dissipation(with thermal pad soldered to board)		(T_J Max – T_A) / θ_{JA}	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 THERMAL INFORMATION

THERMAL METRIC (1)		TAS2505	UNITS
		RGE (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	32.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30.0	
θ_{JB}	Junction-to-board thermal resistance	9.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

3.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AVDD (1)	Power-supply voltage range	Referenced to AVSS (2)	1.5	1.8	1.95	V
DVDD		Referenced to DVSS (2)	1.65	1.8	1.95	
SPKVDD (1)		Referenced to SPKVSS (2)	2.7		5.5	
IOVDD		Referenced to IOVSS (2)	1.1	1.8	3.6	
	Speaker impedance	Load applied across class-D output pins (BTL)	4			Ω
	Headphone impedance	AC-coupled to R_L	16			Ω
V_I	Analog audio full-scale input voltage	AVDD = 1.8 V, single-ended		0.5		V_{RMS}
	Line output load impedance (in half drive ability mode)	AC-coupled to R_L		10		kΩ
MCLK (3)	Master clock frequency	IOVDD = DVDD = 1.8V			50	MHz
SCL	SCL clock frequency				400	kHz

(1) To minimize battery-current leakage, the SPKVDD voltage level should not be below the AVDD voltage level.
(2) All grounds on board are tied together, so they should not differ in voltage by more than 0.2 V maximum for any combination of ground signals. By use of a wide trace or ground plane, ensure a low-impedance connection between AVSS and DVSS.
(3) The maximum input frequency should be 50 MHz for any digital pin used as a general-purpose clock.

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	–40		85	°C

3.4 Electrical Characteristics

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V, f_S (audio) = 48 kHz, CODEC_CLKIN = 256 × f_S, PLL = Off

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL OSCILLATOR—RC_CLK						
	Oscillator frequency			8.48		MHz
Audio DAC – Stereo Single-Ended Headphone Output						
	Device Setup	Load = 16Ω (single-ended), Input & Output CM = 0.9V, DOSR = 128, Device Setup MCLK = 256* fs, Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full-scale output voltage (0 dB)			0.5		Vrms
ICN	Idle channel noise	Measured as idle-channel noise, A-weighted (1) (2)		20.7		μVms
THD+N	Total harmonic distortion + noise	0-dBFS input, 1-kHz input signal		-78.2		dB
	Mute attenuation	Mute		103.7		dB
PSRR	Power-supply rejection ratio (3)	Ripple on AVDD (1.8 V) = 200 mV_{PP} at 1 kHz		47.2		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal		88.1		
	Gain error	0dB, 1kHz input full scale signal		±0.3		dB
P_O	Maximum output power	R_L = 32 Ω, THD+N ≤ –40 dB		11		mW
		R_L = 16 Ω, THD+N ≤ –40 dB		18		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

(3) DAC to headphone-out PSRR measurement is calculated as PSRR = 20 X log(ΔV_{HP} / ΔV_{AVDD}).

Electrical Characteristics *(continued)*

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V, f_S (audio) = 48 kHz, CODEC_CLKIN = 256 × f_S, PLL = Off

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio DAC – Stereo Single-Ended Headphone Output						
	Device Setup	Load = 16Ω (single-ended), Input & Output CM = 0.75V, DOSR = 128, Device Setup MCLK = 256* fs, Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full-scale output voltage (0 dB)			0.375		Vrms
ICN	Idle channel noise	Measured as idle-channel noise, A-weighted (1) (2)		18.1		μVms
THD+N	Total harmonic distortion + noise	0-dBFS input, 1-kHz input signal		-78.2		dB
	Mute attenuation	Mute		105.5		dB
PSRR	Power-supply rejection ratio (3)	Ripple on AVDD (1.8 V) = 200 mV_{PP} at 1 kHz		48.4		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal		86.8		
	Gain error	0dB, 1kHz input full scale signal		±0.3		dB
P_O	Maximum output power	R_L = 32 Ω, THD+N ≤ –40 dB		8		mW
		R_L = 16 Ω, THD+N ≤ –40 dB		16		
DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS						
See for DAC interpolation filter characteristics.						
DAC OUTPUT TO CLASS-D SPEAKER OUTPUT; LOAD = 4 Ω (DIFFERENTIAL)						
ICN	Idle channel noise	BTL measurement, class-D gain = 6 dB, Measured as idle-channel noise, A-weighted (1) (2)		37		μVms
	Output voltage	BTL measurement, class-D gain = 6 dB, -3dBFS input		1.4		Vrms
THD+N	Total harmonic distortion + noise	BTL measurement, DAC input = –6 dBFS, class-D gain = 6 dB		–73.9		dB
PSRR	Power-supply rejection ratio	BTL measurement, ripple on SPKVDD = 200 mV_{PP} at 1 kHz		55		dB
	Mute attenuation	Mute		103		dB
P_O	Maximum output power	SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 10%		1.1		W
		SPKVDD = 4.2 V, BTL measurement, CM = 0.9 V, class-D gain = 18 dB, THD = 10%		1.4		
		SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%		0.8		
		SPKVDD = 4.2 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%		1.1		
		SPKVDD = 5.5 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB			2	

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

(3) DAC to headphone-out PSRR measurement is calculated as PSRR = 20 X log(ΔV_{HP} / ΔV_{AVDD}).

Electrical Characteristics *(continued)*

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V, f_S (audio) = 48 kHz, CODEC_CLKIN = 256 × f_S, PLL = Off

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC OUTPUT TO CLASS-D SPEAKER OUTPUT; LOAD = 8 Ω (DIFFERENTIAL)						
ICN	Idle channel noise	BTL measurement, class-D gain = 6 dB, Measured as idle-channel noise, A-weighted (1) (2)		35.2		μVms
	Output voltage	BTL measurement, class-D gain = 6 dB, -3dBFS input		1.4		Vrms
THD+N	Total harmonic distortion + noise	BTL measurement, DAC input = –6 dBFS, class-D gain = 6 dB		–73.6		dB
P_O	Maximum output power	SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 10%		0.7		W
		SPKVDD = 4.2 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 10%		1		
		SPKVDD = 5.5 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 10%		1.7		
		SPKVDD = 3.6 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%		0.5		
		SPKVDD = 4.2 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%		0.8		
		SPKVDD = 5.5 V, BTL measurement, CM = 0.9V, class-D gain = 18 dB, THD = 1%		1.3		
ANALOG BYPASS TO HEADPHONE AMPLIFIER						
	Device Setup	AC-COUPLED LOAD = 16 Ω (SINGLE-ENDED), DRIVER GAIN = 0 dB, Input and output common-mode = 0.9 V, input signal frequency fi = 1kHz				
	Voltage Gain	Input common-mode = 0.9 V		1		V/V
	Gain Error	-1dBFS (446mVrms), 1-kHz input signal		±0.8		dB
ICN	Idle channel noise	Idle channel, IN1L and IN1R ac-shorted to ground, Measured as idle-channel noise, A-weighted (1) (2)		10.2		μVms
THD+N	Total harmonic distortion + noise	-1 dBFS (446mVrms), 1-kHz input signal		-80.4		dB

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics *(continued)*

At 25°C, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 3.6 V, DVDD = 1.8 V, f_S (audio) = 48 kHz, CODEC_CLKIN = 256 × f_S, PLL = Off

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO CLASS-D SPEAKER AMPLIFIER						
	Device Setup	BTL measurement, DRIVER GAIN = 6 dB, LOAD = 4 Ω (DIFFERENTIAL), 50 pF, input signal frequency fi = 1 KHz				
	Voltage Gain	Input common-mode = 0.9 V		4		V/V
	Gain Error	-1dBFS (446mVrms), 1-kHz input signal		±0.7		dB
ICN	Idle channel noise	Idle channel, IN1L and IN1R ac-shorted to ground, Measured as idle-channel noise, A-weighted(1) (2)		32.6		µVms
THD+N	Total harmonic distortion + noise	-1 dBFS (446mVrms), 1-kHz input signal		-73.7		dB
LOW DROPOUT REGULATOR (AVDD)						
	AVDD Output Voltage 1.8V	SPKVDD = 2.7V, Page 1, Reg 2, D5-D4 = 00, I_O = 50mA		1.79		V
		SPKVDD = 3.6V, Page 1, Reg 2, D5-D4 = 00, I_O = 50mA		1.79		V
		SPKVDD = 5.5V, Page 1, Reg 2, D5-D4 = 00, I_O = 50mA		1.79		V
	Output Voltage Accuracy	SPVDD = 2.7V		±2		%
	Load Regulation	SPVDD = 2.7V, 0A to 50mA		7		mV
	Line Regulation	Input Supply Range 2.7V to 5.5V		0.6		mV
	Decoupling Capacitor		1.0			uF
	Bias Current			55		uA
	Noise @0A Load	A-weighted, 20Hz to 20kHz bandwidth		166		uV
	Noise @50mA Load	A-weighted, 20Hz to 20kHz bandwidth		174		uV
SHUTDOWN POWER CONSUMPTION						
	Device Setup	Power down POR, /RST held low, AVDD = 1.8V, IOVDD = 1.8 V, SPKVDD = 4.2 V, DVDD = 1.8 V				
	I(AVDD)			1.32		µA
	I(DVDD)			0.04		µA
	I(IOVDD)			0.68		µA
	I(SPKVDD)			2.24		µA
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
V_{IH}	Logic level	I_{IH} = 5 µA, IOVDD ≥ 1.6 V	0.7 × IOVDD			V
		I_{IH} = 5 µA, IOVDD < 1.6 V	IOVDD			
V_{IL}		I_{IL} = 5 µA, IOVDD ≥ 1.6 V	–0.3		0.3 × IOVDD	V
		I_{IL} = 5 µA, IOVDD < 1.6 V			0	
V_{OH}		I_{OH} = 2 TTL loads	0.8 × IOVDD			V
V_{OL}		I_{OL} = 2 TTL loads			0.25	V
	Capacitive load			10		pF

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

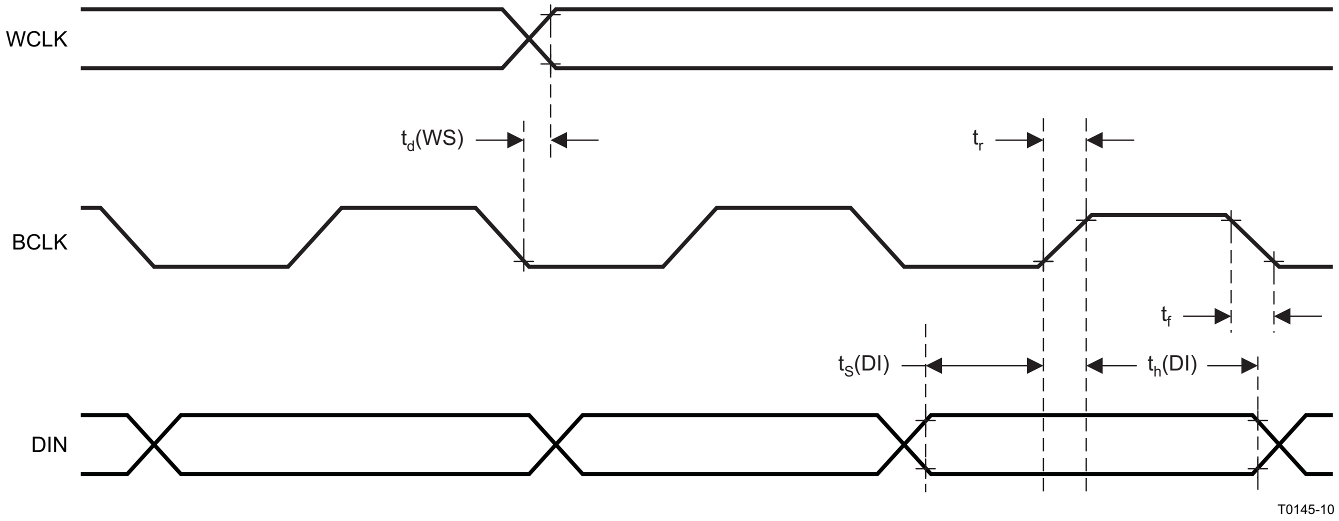
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

3.5 Timing Characteristics

3.5.1 I²S/LJF/RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V

Note: All timing specifications are measured at characterization but not tested at final test.



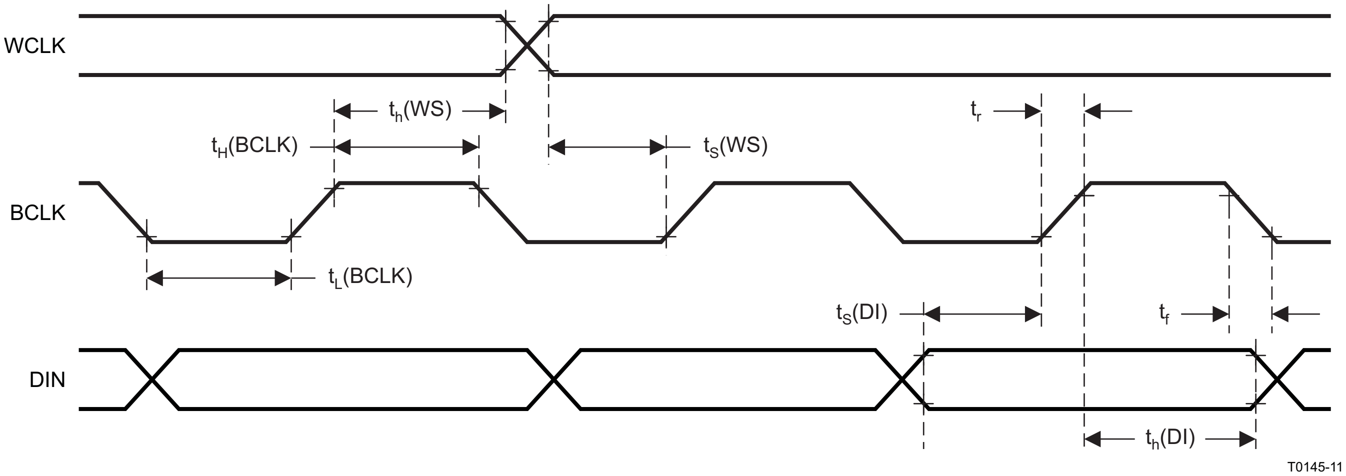
PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		45		45	ns
t_S(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		25		10	ns
t_f	Fall time		25		10	ns

Figure 3-1. I²S/LJF/RJF Timing in Master Mode

3.5.2 I^2S/LJF/RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V

Note: All timing specifications are measured at characterization but not tested at final test.



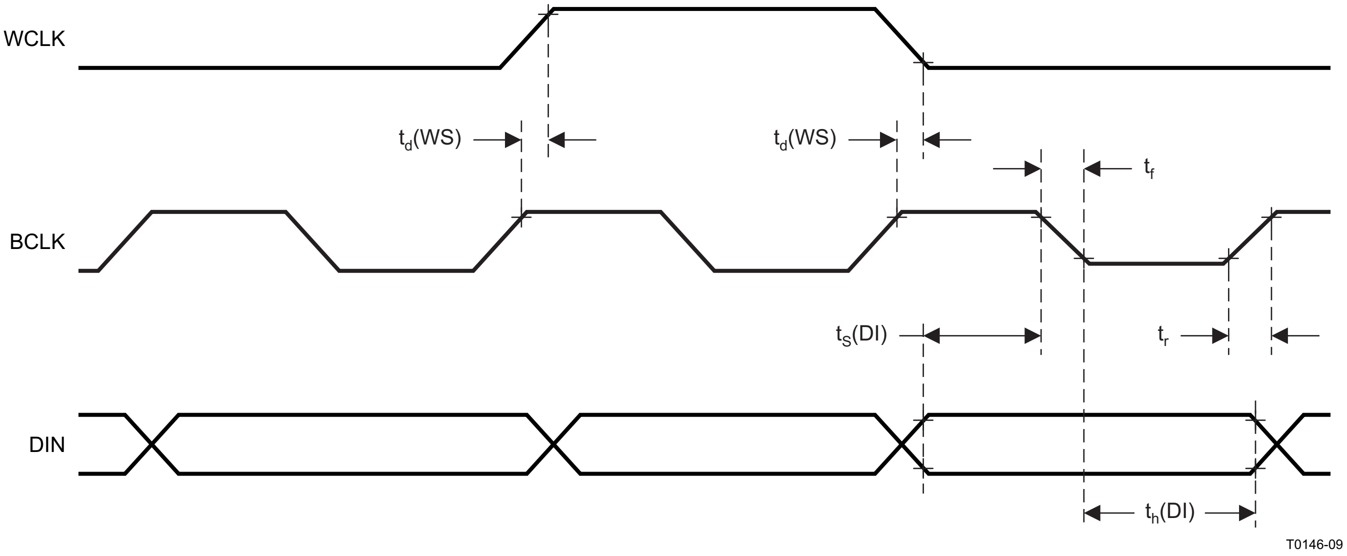
PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		6		ns
t_h(WS)	WCLK hold	8		6		ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

Figure 3-2. I^2S/LJF/RJF Timing in Slave Mode

3.5.3 DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V

Note: All timing specifications are measured at characterization but not tested at final test.



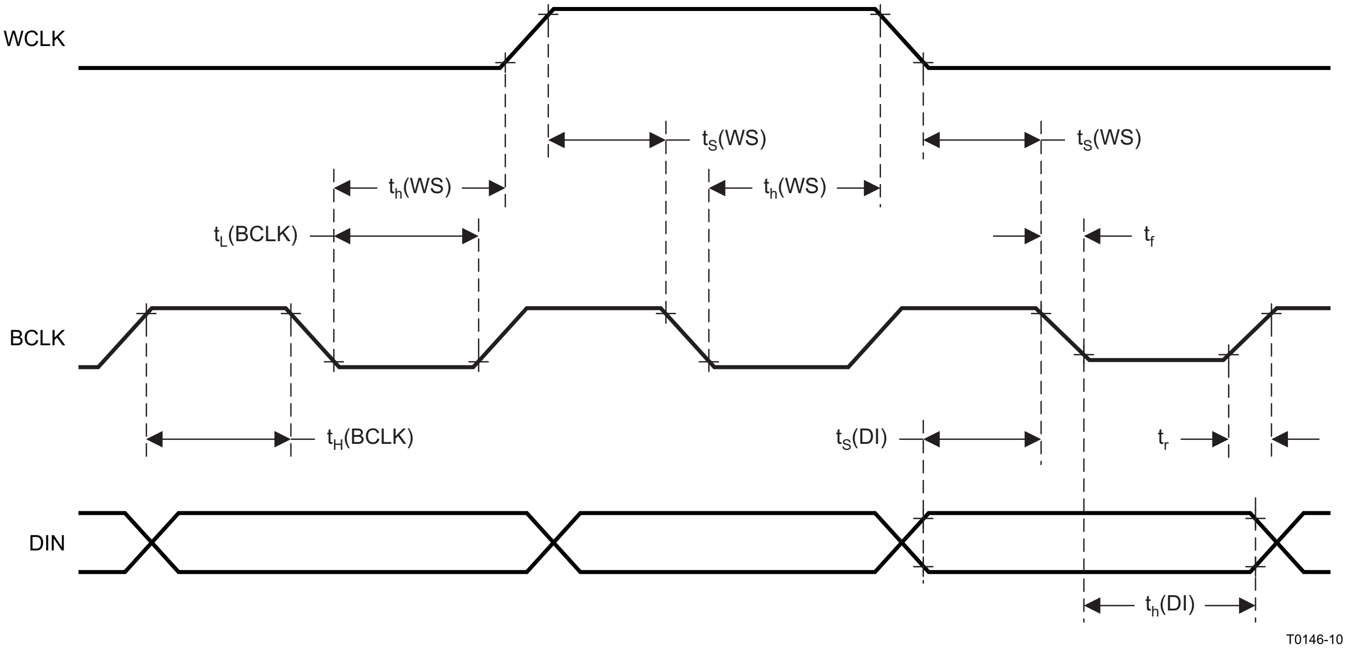
PARAMETER		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		45		45	ns
t_S(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		25		10	ns
t_f	Fall time		25		10	ns

Figure 3-3. DSP Timing in Master Mode

3.5.4 DSP Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V

Note: All timing specifications are measured at characterization but not tested at final test.



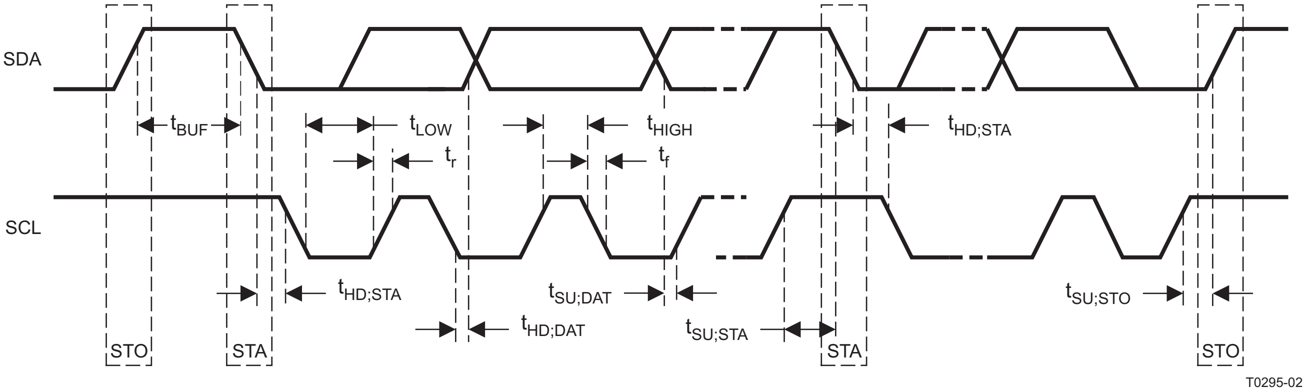
PARAMETER		IOVDD = 1.8V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		8		ns
t_h(WS)	WCLK hold	8		8		ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

Figure 3-4. DSP Timing in Slave Mode

3.5.5 I^2C Interface Timing

All specifications at 25°C, DVDD = 1.8 V

Note: All timing specifications are measured at characterization but not tested at final test.



PARAMETER		Standard-Mode			Fast-Mode			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency	0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			0.8			µs
t_{LOW}	LOW period of the SCL clock	4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock	4			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I^2C bus devices	0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data setup time	250			100			ns
t_r	SDA and SCL rise time			1000	20 + 0.1 C_b		300	ns
t_f	SDA and SCL fall time			300	20 + 0.1 C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			1.3			µs
C_b	Capacitive load for each bus line			400			400	pF

Figure 3-5. I^2C Interface Timing

3.5.6 SPI Interface Timing

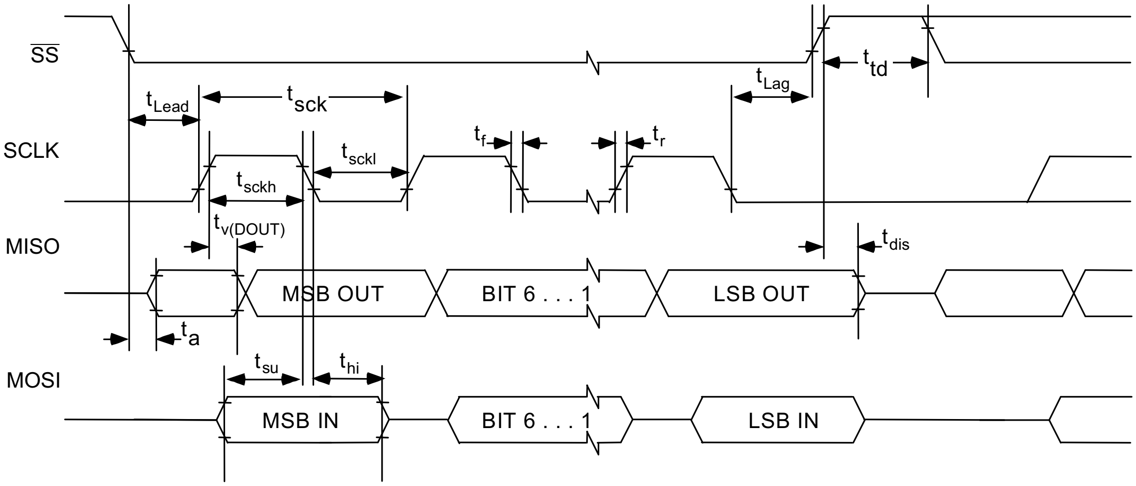


Figure 3-6. SPI Interface Timing Diagram

Timing Requirements

At 25°C, DVDD = 1.8V

Table 3-1. SPI Interface Timing

PARAMETER		TEST CONDITION	IOVDD=1.8V			IOVDD=3.3V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period (1)		100			50			ns
t_{sckh}	SCLK Pulse width High		50			25			ns
t_{sckl}	SCLK Pulse width Low		50			25			ns
t_{lead}	Enable Lead Time		30			20			ns
t_{lag}	Enable Lag Time		30			20			ns
t_d	Sequential Transfer Delay		40			20			ns
t_a	Slave DOUT access time				40			40	ns
t_{dis}	Slave DOUT disable time				40			40	ns
t_{su}	DIN data setup time		15			15			ns
t_{hi}	DIN data hold time		15			10			ns
$t_{v;DOUT}$	DOUT data valid time				25			18	ns
t_r	SCLK Rise Time				4			4	ns
t_f	SCLK Fall Time				4			4	ns

(1) These parameters are based on characterization and are not tested in production.

4 Typical Performance

4.1 Class D Speaker Driver Performance

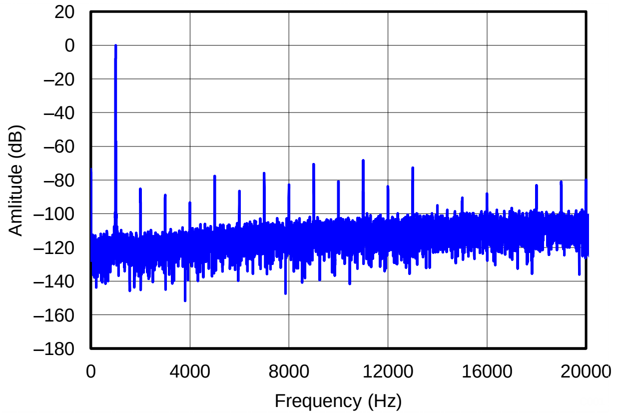


Figure 4-1. DAC To Speaker Amplitude at 0 dBFS vs Frequency (4 Ω Load)

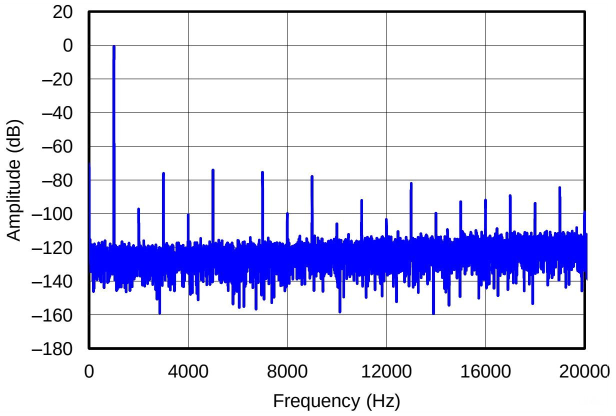


Figure 4-2. AINL To Speaker FFT Amplitude at 0 dBFS vs Frequency (4 Ω Load)

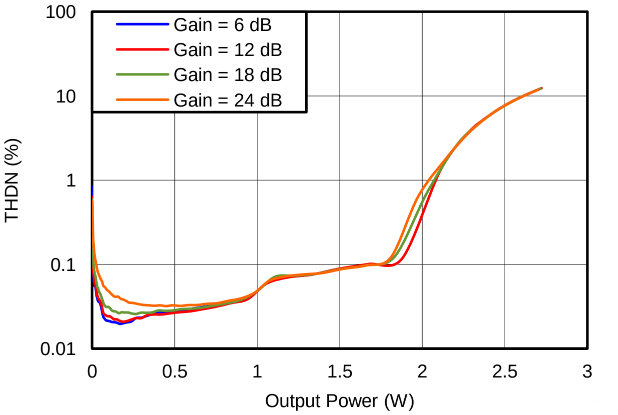


Figure 4-3. Total Harmonic Distortion + Noise vs 4 Ω Speaker Power (SPKVDD = 5.5 V)

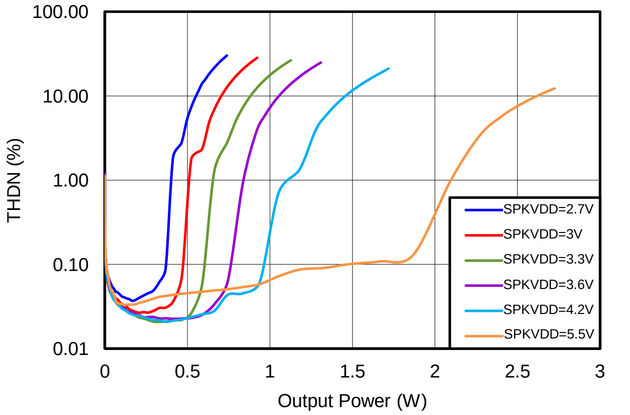


Figure 4-4. Total Harmonic Distortion + Noise + NOISE vs 4 Ω Speaker Power (Gain = 18 dB)

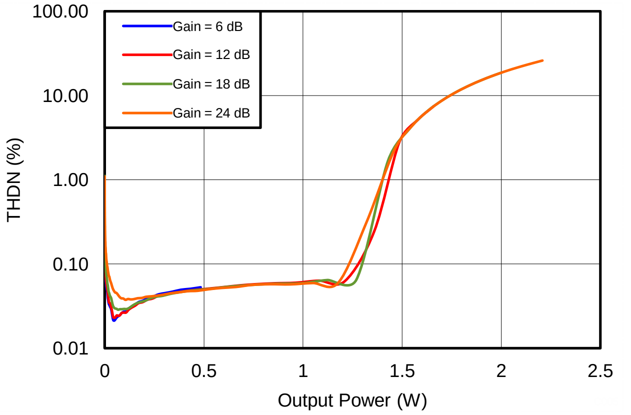


Figure 4-5. Total Harmonic Distortion + Noise + NOISE vs 8 Ω Speaker Power (SPKVDD = 5.5 V)

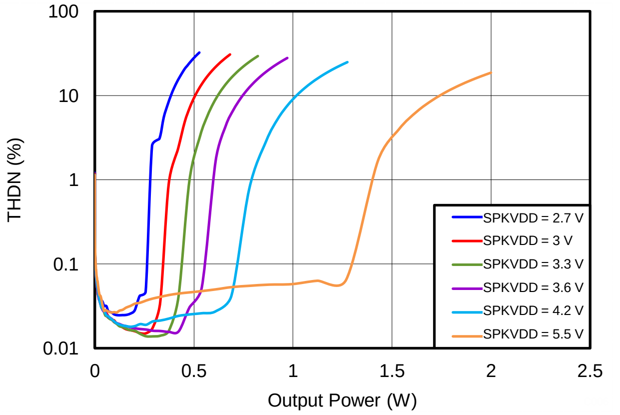


Figure 4-6. Total Harmonic Distortion + Noise + NOISE vs 8 Ω Speaker Power (Gain = 18 dB)

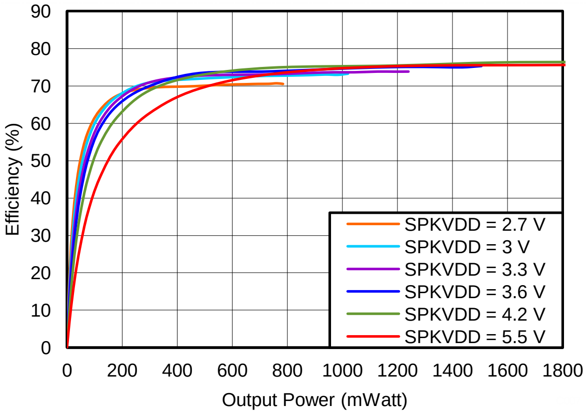


Figure 4-7. Total Power Consumption vs Output Power Consumption (Gain = 18 dB, Load = 4 Ω)

4.2 HP Driver Performance

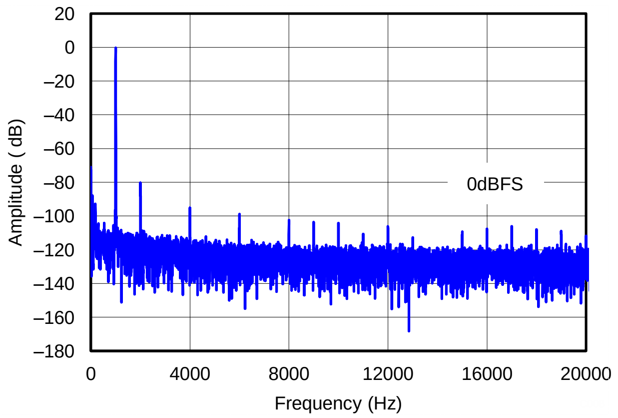


Figure 4-8. DAC TO HP FFT Amplitude at 0 dBFS vs Frequency (16 Ω Load)

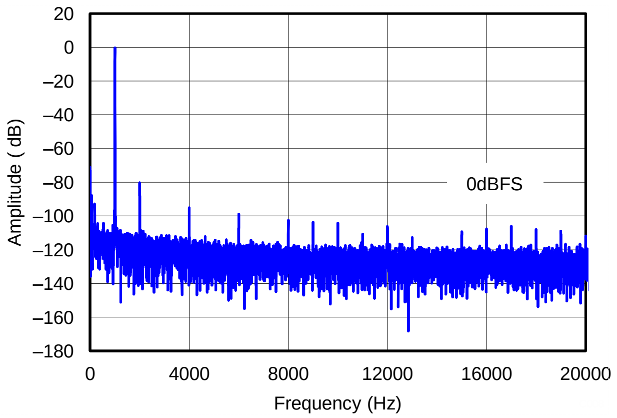


Figure 4-9. AINL TO HP FFT Amplitude at 0 dBFS vs Frequency (16 Ω Load)

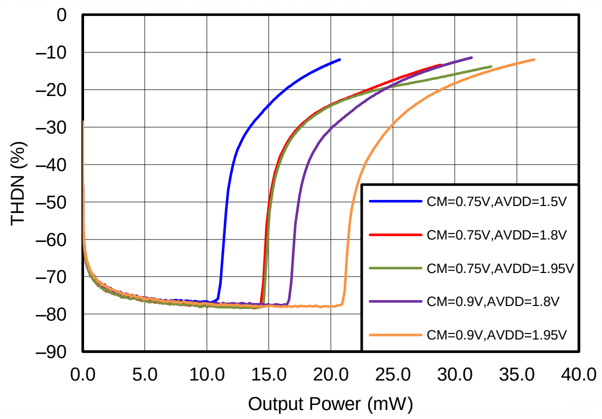


Figure 4-10. Total Harmonic Distortion + Noise vs HP Power (Gain = 9 dB)

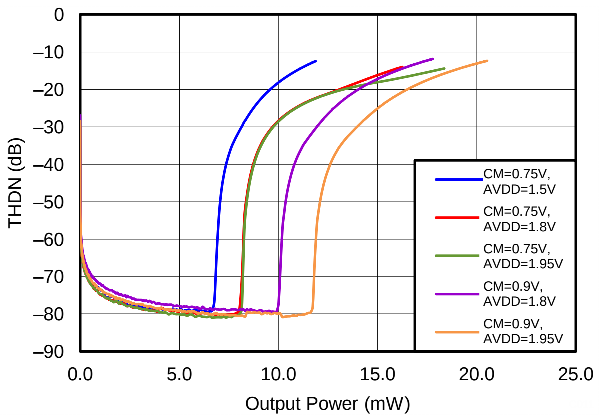


Figure 4-11. Total Harmonic Distortion + Noise vs HP Power (Gain = 32 dB)

5 Application Overview

The TAS2505 offers a wide range of configuration options. Figure 1-1 shows the simplified functional blocks of the device.

5.1 Typical Circuit Configuration

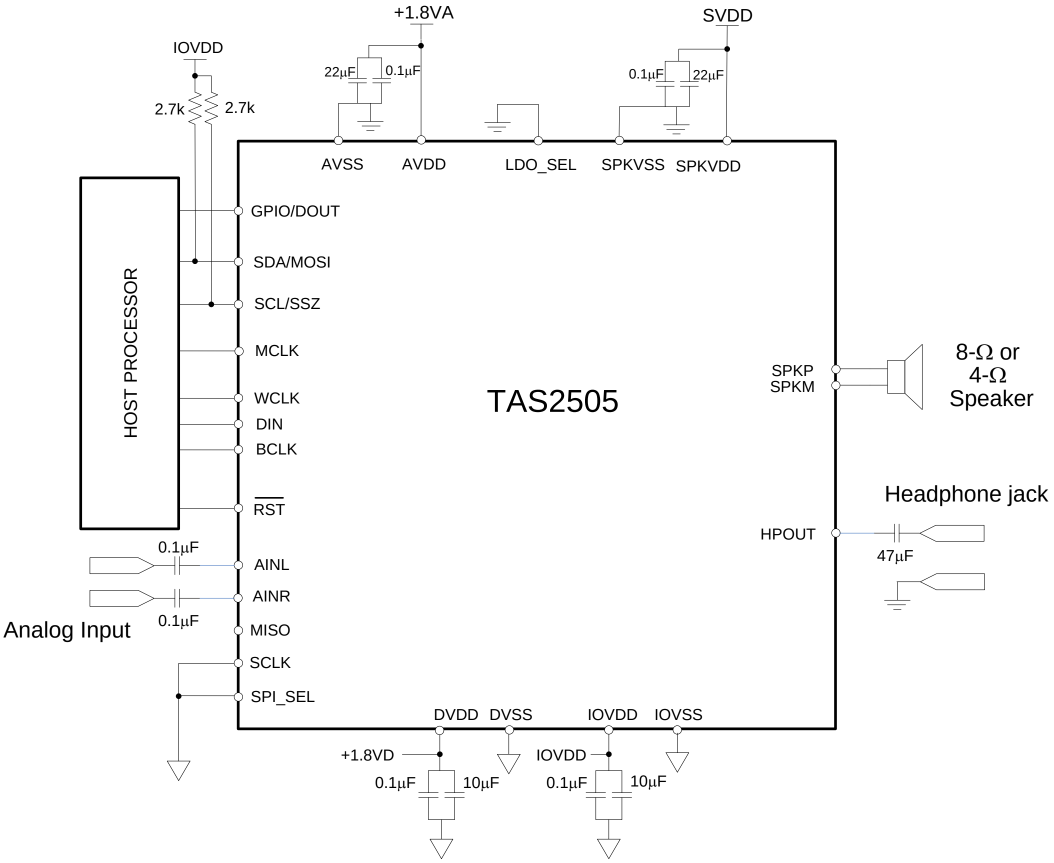


Figure 5-1. Typical Circuit Configuration

5.2 Circuit Configuration with Internal LDO

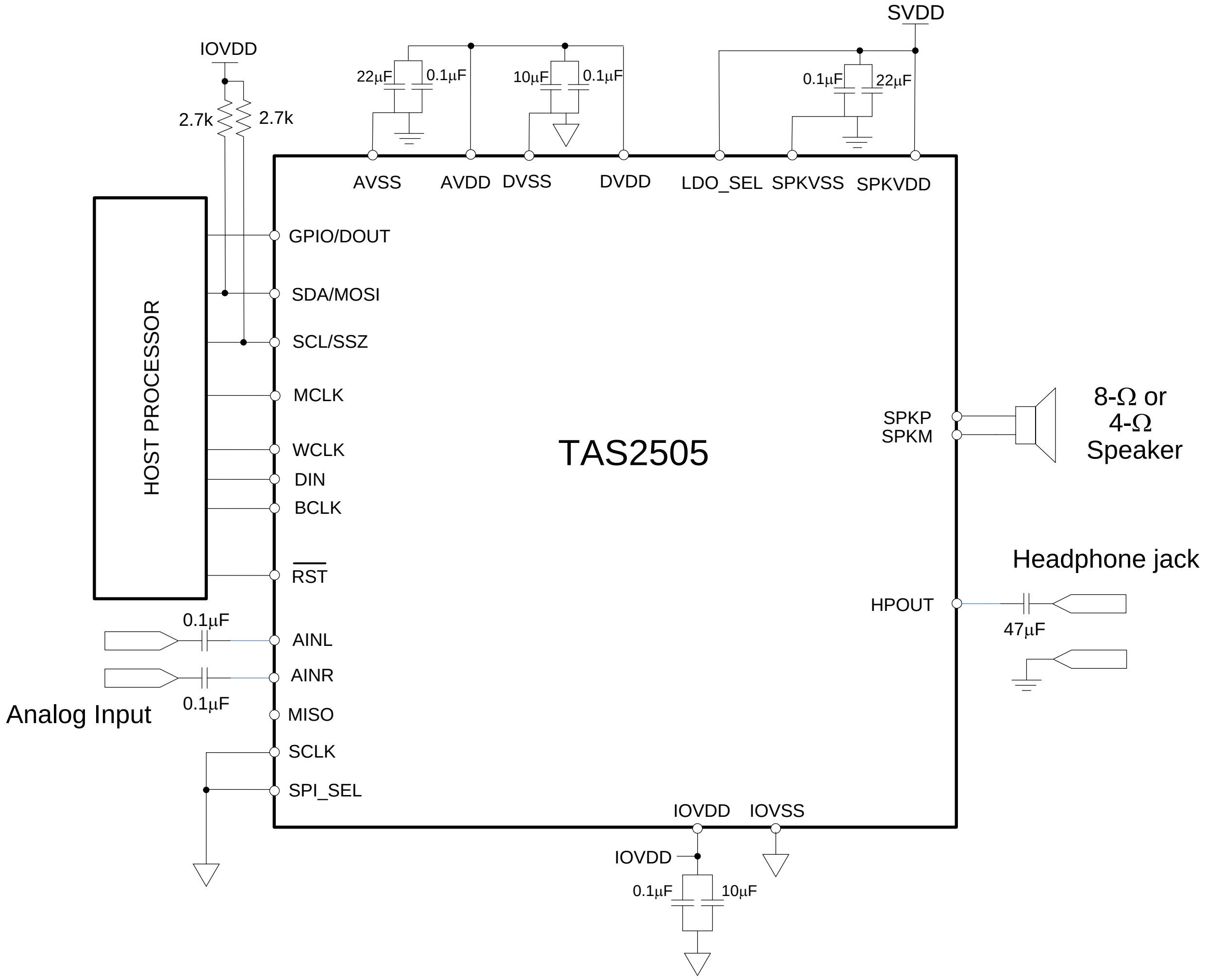


Figure 5-2. Application Schematics for LDO

5.3 Device Connections

5.3.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are $\overline{\text{RST}}$ LDO_SEL and the SPI_SEL pin, which are HW control pins. Depending on the state of SPI_SEL, the two control-bus pins SCL/SSZ and SDA/MOSI are configured for either I^{2}C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in Section 5.3.3.

5.3.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

5.3.3 *Multifunction Pins*

Table 5-1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Table 5-1. Multifunction Pin Assignments

		1	**2**	**3**	**4**	**5**	**6**	**7**
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN**	**GPIO /DOUT**	**SCLK**	**MISO**
A	PLL Input	S(1)	S(2)		E		S(3)	
B	Codec Clock Input	S(1),D(4)	S(2)				S(3)	
C	I^2S BCLK input		S(2),D					
D	I^2S BCLK output		E(5)					
E	I^2S WCLK input			E, D				
F	I^2S WCLK output			E				
G	I^2S DIN				E, D			
I	General Purpose Output I					E		
I	General Purpose Output II							E
J	General Purpose Input I				E			
J	General Purpose Input II					E		
J	General Purpose Input III						E	
K	INT1 output					E		E
L	INT2 output					E		E
M	Secondary I^2S BCLK input					E	E	
N	Secondary I^2S WCLK input					E	E	
O	Secondary I^2S DIN					E	E	
P	Secondary I^2S BCLK OUT					E		E
Q	Secondary I^2S WCLK OUT					E		E
R	Secondary I^2S DOUT							E
S	Aux Clock Output					E		E

(1) S(1): The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.
(2) S(2): The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.
(3) S(3): The GPIO/DOUT pin can drive the PLL and Codec Clock inputs **simultaneously**.
(4) D: Default Function
(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/DOUT has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

5.4 Audio Analog I/O

The TAS2505 features a mono audio DAC. It supports a wide range of analog interfaces to support different headsets such as 16-Ω to 200-Ω impedance and analog line outputs. TheTAS2505 can drive a speaker upto 4-Ω impedance.

5.5 Analog Signals

The TAS2505 analog signals consist of:

- Analog inputs AINR and AINL, which can be used to pass-through or mix analog signals to output stages
- Analog outputs class-D speaker driver and headphone/lineout driver providing output capability for the DAC, AINR, AINL, or a mix of the three

5.5.1 Analog Inputs AINL and AINR

AINL (pin 3 or C2) and AINR (pin 4 or B2) are inputs to Mixer P and Mixer M along with the DAC output. Also AINL and AINR can be configured inputs to HP driver. Page1 / register 12 provides control signals for determining the signals routed through Mixer P, Mixer M and HP driver. Input of Mixer P can be attenuated by Page1 / register 24, input of Mixer M can be attenuated by Page1 / register 25 and input of HP driver can be attenuated by Page1 / register 22. Also AINL and AINR can be configured to a monaural differential input with use Mixer P and Mixer M by Page1 / register 12 setting.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6 Audio DAC and Audio Analog Outputs

The mono audio DAC consists of a digital audio processing block, a digital interpolation filter, a digital delta-sigma modulator, and an analog reconstruction filter. The high oversampling ratio (normally DOSR is between 32 and 128) exhibits good dynamic range by ensuring that the quantization noise generated within the delta-sigma modulator stays outside of the audio frequency band. Audio analog outputs include mono headphone and lineout and mono class-D speaker outputs. Because the TAS2505 contains a mono DAC, it inputs the mono data from the left channel, the right channel, or a mix of the left and right channels as [(L + R) ÷ 2], selected by page 0, register 63, bits D5–D4.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.1 DAC

The TAS2505 mono audio DAC supports data rates from 8 kHz to 192 kHz. The audio channel of the mono DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multibit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and observed in the signal images strongly suppressed within the audio band to beyond 20 kHz. To handle multiple input rates and optimize power dissipation and performance, the TAS2505 allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring page 0, register 13 and page 0 / register 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TAS2505 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the delta-sigma modulator. The interpolation filter can be chosen from three different types, depending on required frequency response, group delay, and sampling rate.

The DAC path of the TAS2505 features many options for signal conditioning and signal routing:

- Digital volume control with a range of -63.5 to +24dB
- Mute function

In addition to the standard set of DAC features the TAS2505 also offers the following special features:

- Digital auto mute
- Adaptive filter mode

5.6.1.1 DAC Processing Blocks — Overview

The TAS2505 implements signal-processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choices among these processing blocks allows the system designer to balance power conservation and signal-processing flexibility. Table 5-2 gives an overview of all available processing blocks of the DAC channel and their properties. The resource-class column gives an approximate indication of power consumption for the digital (DVDD) supply; however, based on the out-of-band noise spectrum, the analog power consumption of the drivers (AVDD) may differ.

The signal-processing blocks available are:

- First-order IIR
- Scalable number of biquad filters

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal-processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 5-2. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	First-Order IIR Available	Number of Biquads	Resource Class
PRB_P1	A	Mono	Yes	6	6
PRB_P2	A	Mono	No	3	4
PRB_P3	B	Mono	Yes	6	4

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.2 Digital Mixing and Routing

The TAS2505 has four digital mixing blocks. Each mixer can provide either mixing or multiplexing of the digital audio data. The first mixer/multiplexer can be used to select input data for the mono DAC from left channel, right channel, or (left channel + right channel) / 2 mixing. This digital routing can be configured by writing to page 0, register 63, bits D5–D4.

5.6.3 Analog Audio Routing

The TAS2505 has the capability to route the DAC output to either the headphone or the speaker output. If desirable, both output drivers can be operated at the same time while playing at different volume levels. The TAS2505 provides various digital routing capabilities, allowing digital mixing or even channel swapping in the digital domain. All analog outputs other than the selected ones can be powered down for optimal power consumption.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.4 5V LDO

The TAS2505 has a built-in LDO which can generate the analog supply (AVDD) also the digital supply (DVDD) from input voltage range of 2.7 V to 5.5 V with high PSRR. If combined power supply current is 50 mA or less, then this LDO can deliver power to both analog and digital power supplies. If the only speaker power supply is present and LDO Select pin is enabled, the LDO can power up without requiring other supplies. This LDO requires a minimum dropout voltage of 300 mV and can support load currents up to 50 mA. For stability reasons the LDO requires a minimum decoupling capacitor of 1 µF (±50%) on the analog supply (AVDD) pin and the digital supply (DVDD) pin. If use this LDO output voltage for the digital supply (DVDD) pin, the analog supply (AVDD) pin connected to the digital supply (DVDD) externally is required.

The LDO is by default powered down for low sleep mode currents and can be enabled driving the LDO_SELECT pin to SPKVDD (Speaker power supply). When the LDO is disabled the AVDD pin is tri-stated and the device AVDD needs to be powered using external supply. In that case the DVDD pin is also tri-stated and the device DVDD needs to be powered using external supply. The output voltage of this LDO can be adjusted to a few different values as given in the Table 5-3.

Table 5-3. AVDD LDO Settings

Page-1, Register 2, D(5:4)	LDO Output
00	1.8 V
01	1.6 V
10	1.7 V
00	1.5 V

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.5 POR

TAS2505 has a POR (Power On Reset) function. This function insures that all registers are automatically set to defaults when a proper power up sequence is executed.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.6 CLOCK Generation and PLL

The TAS2505 supports a wide range of options for generating clocks for the DAC sections as well as interface and other control blocks. The clocks for the DAC require a source reference clock. This clock can be provided on a variety of device pins, such as the MCLK, BCLK, or GPIO pins. The source reference clock for the codec can be chosen by programming the CODEC_CLKIN value on page 0, register 4, bits D1–D0. The CODEC_CLKIN can then be routed through highly-flexible clock dividers shown in to generate the various clocks required for the DAC and the Digital Effects section. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO, the TAS2505 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN, the TAS2505 provides several programmable clock dividers to help achieve a variety of sampling rates for the DAC and clocks for the Digital Effects sections.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.7 Digital Audio and Control Interface

5.6.7.1 Digital Audio Interface

Audio data is transferred between the host processor and the TAS2505 via the digital audio data serial interface, or audio bus. The audio bus on this device is flexible, including left- or right-justified data options, support for I^{2}S or PCM protocols, programmable data-length options, a TDM mode for multichannel operation, flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TAS2505 can be configured for left- or right-justified, I^{2}S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring page 0, register 27, bits D5–D4. In addition, the word clock and bit clock can be independently configured in either master or slave mode for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected DAC sampling frequencies.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.7.2 Control Interface

The TAS2505 control interface supports SPI or I2C communication protocols, with the protocol selectable using the SPI_SEL pin. For SPI, SPI_SEL should be tied high; for I2C, SPI_SEL should be tied low. It is not recommended to change the state of SPI_SEL during device operation.

5.6.7.2.1 I²C Control Mode

The TAS2505 supports the I²C control protocol, and will respond to the I²C address of 0011 000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

5.6.7.2.2 SPI Digital Interface

In the SPI control mode,the TAS2505 uses the pins SCL/SSZ=SSZ, SCLK=SCLK, MISO=MISO, SDA/MOSI=MOSI as a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TAS2505) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master.The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock(driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shif tregister.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.7.3 Power Supply

The TAS2505 integrates a large amount of digital and analog functionality, and each of these blocks can be powered separately to enable the system to select appropriate power supplies for desired performance and power consumption. The device has separate power domains for digital IO, digital core, analog core, analog input, headphone driver, and speaker drivers. If desired, all of the supplies (except for the supplies for speaker drivers, which can directly connect to the battery) can be connected together and be supplied from one source in the range of 1.65 to 1.95V. Individually, the IOVDD voltage can be supplied in the range of 1.1V to 3.6V. For improved power efficiency, the digital core power supply can range from 1.26V to 1.95V. The analog core supply can either be derived from the internal LDO accepting an SPKVDD voltage in the range of 2.7V to 5.5V, or the AVDD pin can directly be driven with a voltage in the range of 1.5V to 1.95V. The speaker driver voltages (SPKVDD) can range from 2.7V to 5.5V.

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

5.6.7.4 Device Special Functions

- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the *TAS2505 Application Reference Guide* (SLAU472).

6 Register Map

6.1 Register Map Summary

Table 6-1. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2 - 3	0x00	0x02 - 0x03	Reserved Registers
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P and R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9 - 10	0x00	0x09 - 0x0A	Reserved Registers
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15 - 24	0x00	0x0F - 0x18	Reserved Registers
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Reserved Register
0	35 - 36	0x00	0x23 - 0x24	Reserved Registers
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Registers
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Reserved Register
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Reserved Register
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Registers
0	52	0x00	0x34	GPIO/DOUT Control Register
0	53	0x00	0x35	DOUT Function Control Register
0	54	0x00	0x36	DIN Function Control Register
0	55	0x00	0x37	MISO Function Control Register
0	56	0x00	0x38	SCLK/DMDIN2 Function Control Register

Table 6-1. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Instruction Set
0	61 - 62	0x00	0x3D -0x3E	Reserved Registers
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	DAC Channel Digital Volume Control Register
0	66 - 80	0x00	0x42 - 0x50	Reserved Registers
0	81	0x00	0x51	Dig_Mic Control Register
0	82 - 127	0x00	0x52 - 0x7F	Reserved Registers
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	REF, POR and LDO BGAP Control Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1
1	4 - 7	0x01	0x04 - 0x07	Reserved Registers
1	8	0x01	0x08	DAC PGA Control Register
1	9	0x01	0x09	Output Drivers, AINL, AINR, Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	HP Over Current Protection Configuration Register
1	12	0x01	0x0C	HP Routing Selection Register
1	13 - 15	0x01	0x0D - 0x0F	Reserved Registers
1	16	0x01	0x10	HP Driver Gain Setting Register
1	17 - 19	0x01	0x11 - 0x13	HPR Driver Gain Setting Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	HP Volume Control Register
1	23	0x01	0x17	Reserved Register
1	24	0x01	0x18	AINL Volume Control Register
1	25	0x01	0x19	AINR Volume Control Register
1	26 - 44	0x01	0x1A - 0x2C	Reserved Registers
1	45	0x01	0x2D	Speaker Amplifier Control 1
1	46	0x01	0x2E	Speaker Volume Control Register
1	47	0x01	0x2F	Reserved Register
1	48	0x01	0x30	Speaker Amplifier Volume Control 2
1	49 - 62	0x01	0x31 - 0x3E	Right MICPGA Positive Terminal Input Routing Configuration Register
1	64 - 121	0x01	0x40 - 0x79	Reserved Registers
1	122	0x01	0x7A	Reference Power Up Delay
1	123 - 127	0x01	0x7B - 0x7F	Reserved Registers
2 - 43	0 - 127	0x02 - 0x2B	0x00 - 0x7F	Reserved Registers
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2 - 7	0x2C	0x02 - 0x07	Reserved
44	8 - 127	0x2C	0x08 - 0x7F	DAC Coefficients Buffer-A C(0:29)
45 - 52	0	0x2D-0x34	0x00	Page Select Register
45 - 52	1 - 7	0x2D-0x34	0x01 - 0x07	Reserved.
45 - 52	8 - 127	0x2D-0x34	0x08 - 0x7F	DAC Coefficients Buffer-A C(30:255)
53 - 61	0 - 127	0x35 - 0x3D	0x00 - 0x7F	Reserved Registers

Table 6-1. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
62 - 70	0	0x3E-0x46	0x00	Page Select Register
62 - 70	1 - 7	0x3E-0x46	0x01 - 0x07	Reserved Registers
62 - 70	8 - 127	0x3E-0x46	0x08 - 0x7F	DAC Coefficients Buffer-B C(0:255)
71 - 255	0 - 127	0x47 - 0x7F	0x00 - 0x7F	Reserved Registers

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2013) to Revision A	Page
• Deleted P_O (Max Output power) SPKVDD = 5.5 V, THD = 10%	6
• Changed P_O (Max Output power) SPKVDD = 5.5 V value From: TYP = 2.1 W To: MAX = 2 W	6

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TAS2505IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TAS 2505	Samples
TAS2505IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TAS 2505	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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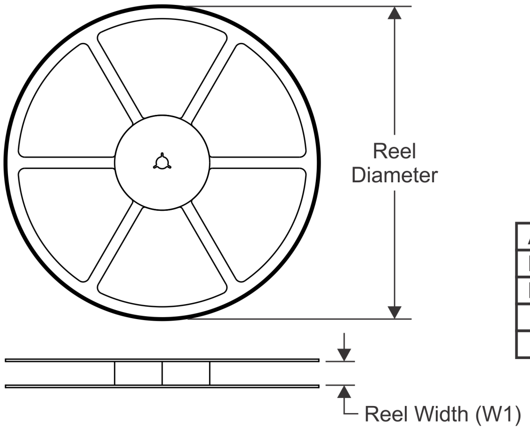
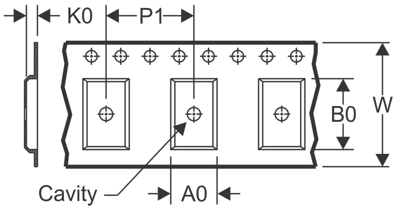
TAPE AND REEL INFORMATION

REEL DIMENSIONS

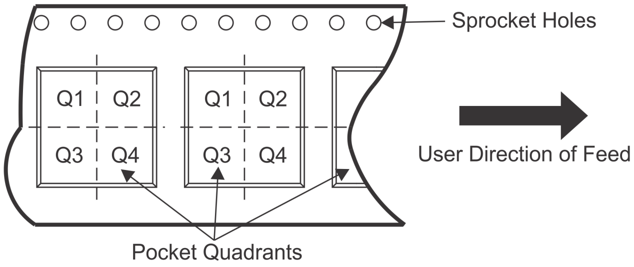


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

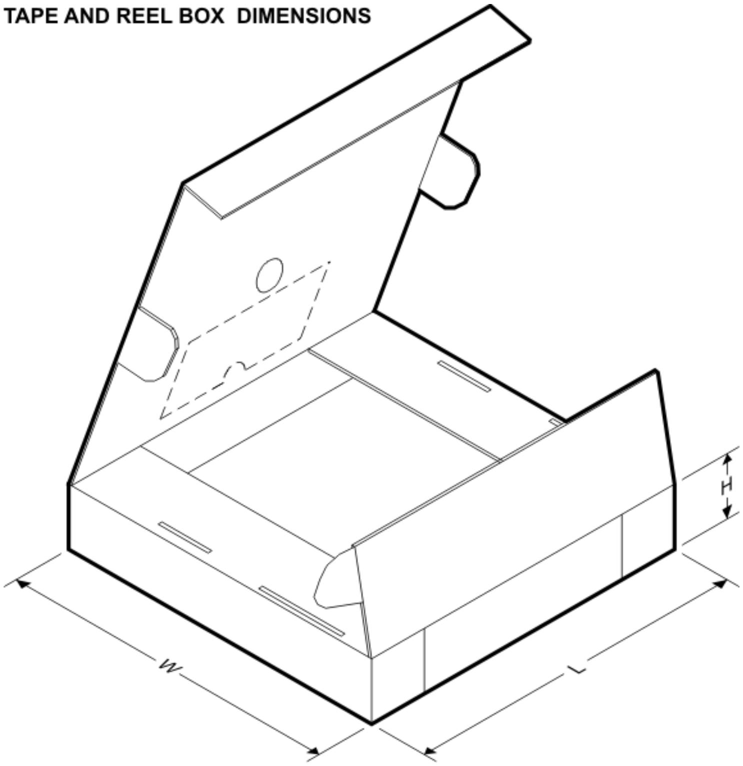
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2505IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

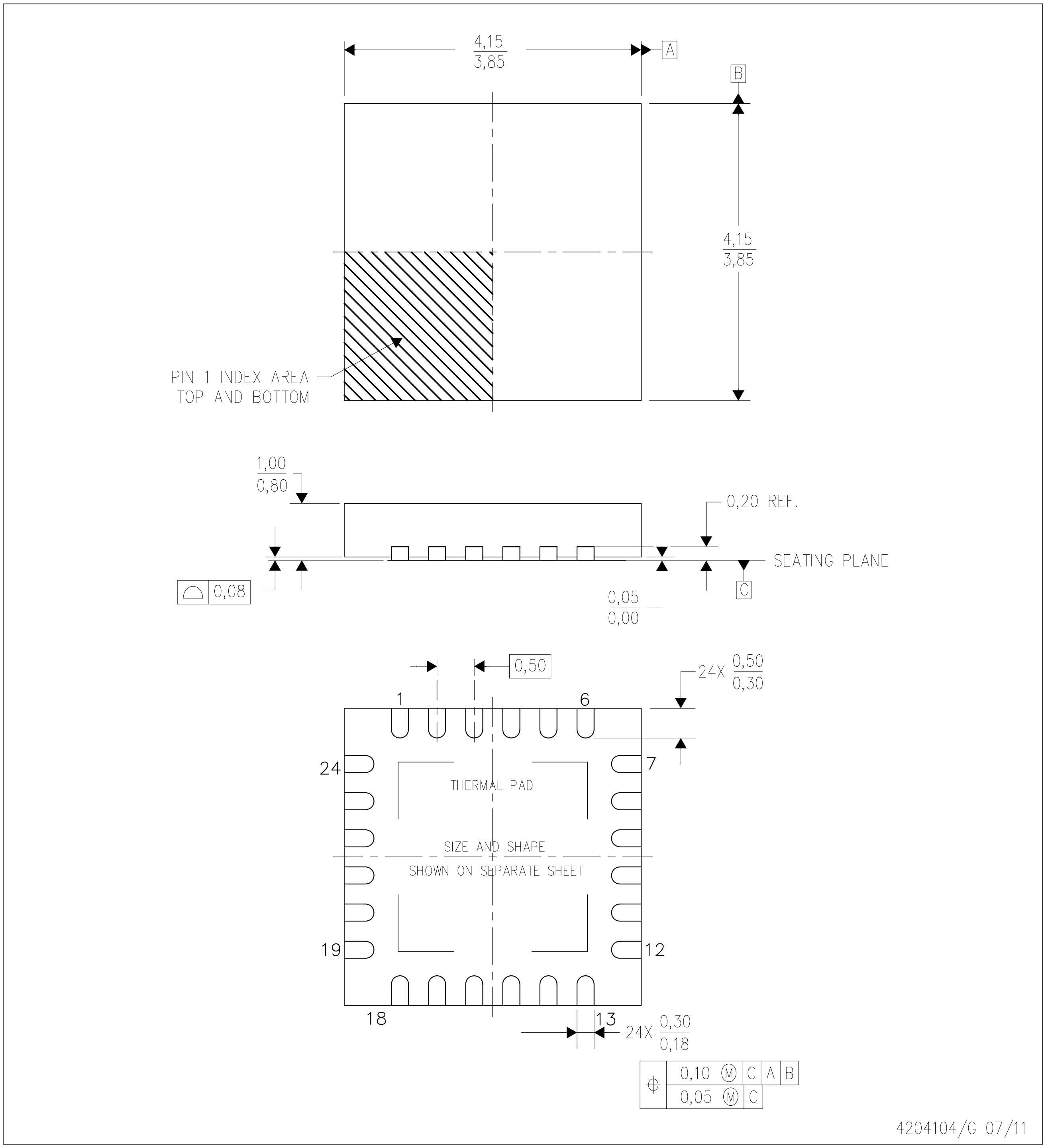
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2505IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

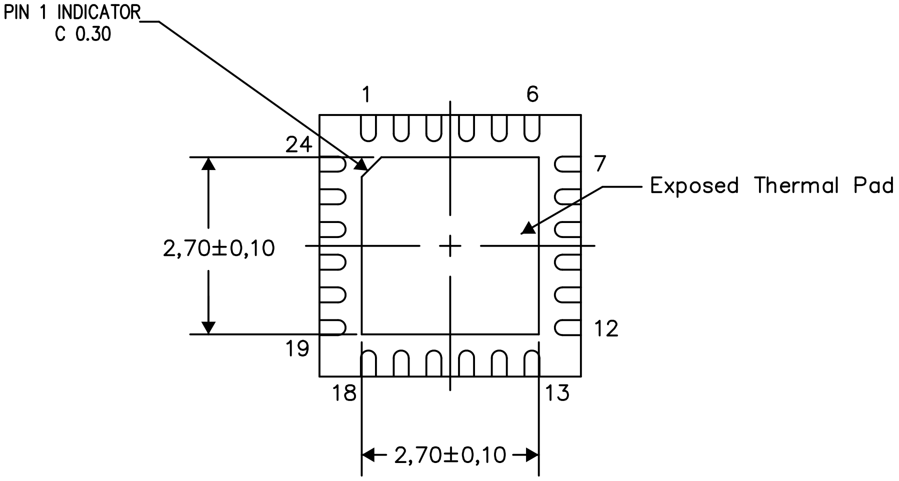
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



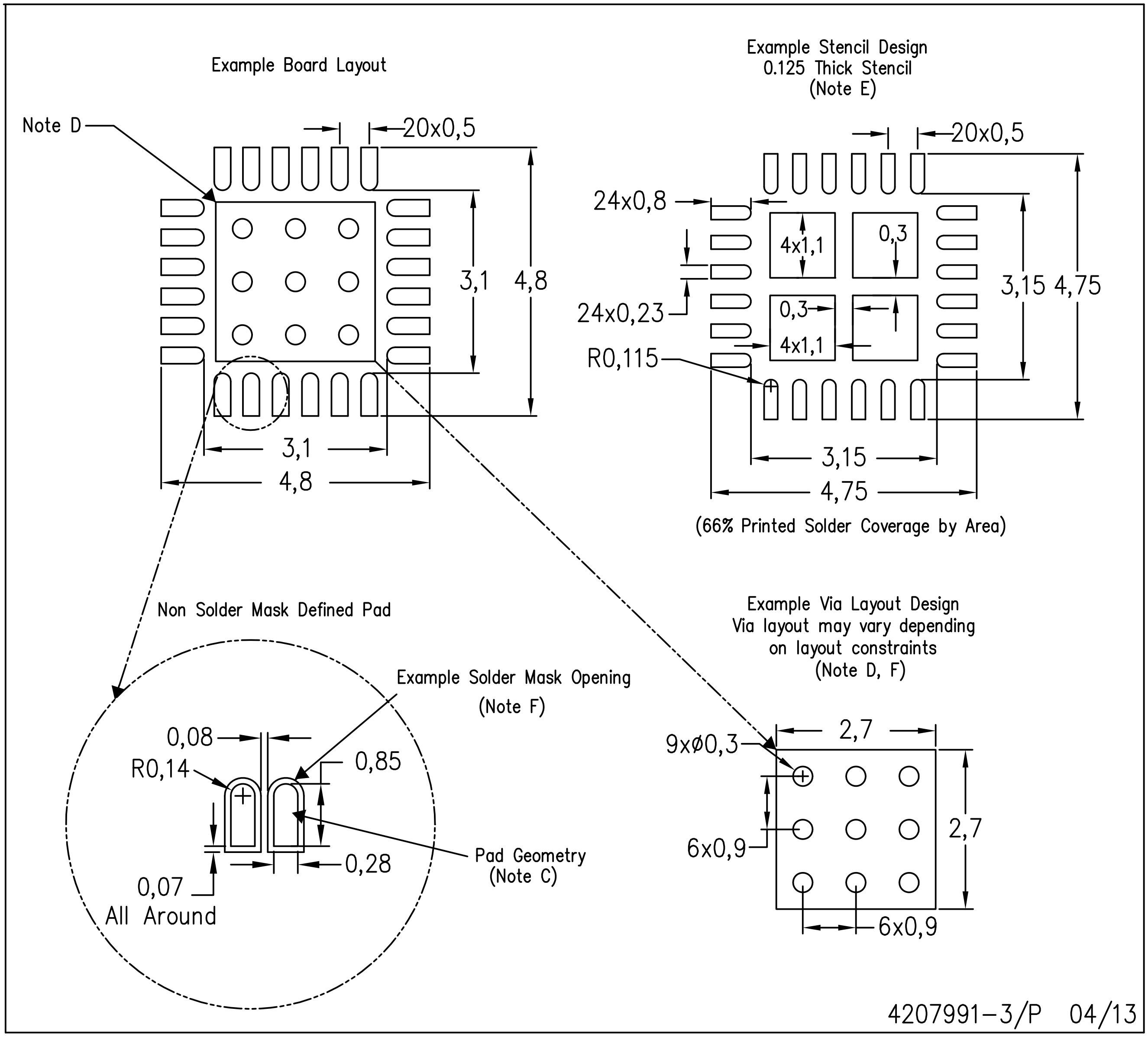
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/AD 04/13

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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