

# ESD7451, SZESD7451

## ESD Protection Diodes Micro-Packaged Diodes for ESD Protection

The ESD7451 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

### Features

- Ultra-Low Capacitance (0.35 pF Max)
- Low Clamping Voltage
- Stand-off Voltage: 3.3 V
- Low Leakage
- Response Time is < 1 ns
- Low Dynamic Resistance < 1  $\Omega$
- IEC61000-4-2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

### MAXIMUM RATINGS

| Rating  | Symbol          | Value                | Unit               |
|---|-----------------|----------------------|--------------------|
| IEC 61000-4-2 (ESD) Contact Air   |                 | $\pm 25$<br>$\pm 25$ | kV                 |
| Total Power Dissipation on FR-5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ | $P_D$           | 250                  | mW                 |
| Thermal Resistance, Junction-to-Ambient                                   | $R_{\theta JA}$ | 400                  | $^\circ\text{C/W}$ |
| Junction and Storage Temperature Range                                    | $T_J, T_{stg}$  | -55 to +150          | $^\circ\text{C}$   |
| Lead Solder Temperature - Maximum (10 Second Duration)                    | $T_L$           | 260                  | $^\circ\text{C}$   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

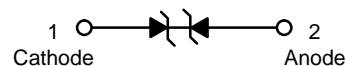
1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



ON Semiconductor®

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### MARKING DIAGRAM



XDFN2  
CASE 711AM



E = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

| Device         | Package         | Shipping†          |
|----------------|-----------------|--------------------|
| ESD7451N2T5G   | XDFN2 (Pb-Free) | 8000 / Tape & Reel |
| SZESD7451N2T5G | XDFN2 (Pb-Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

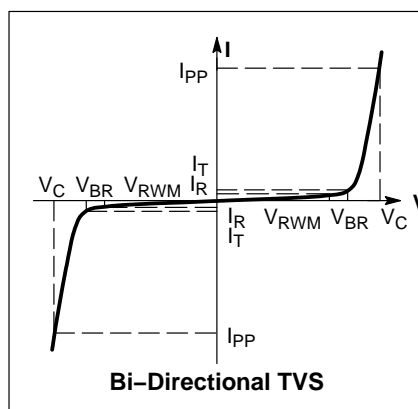
# ESD7451, SZESD7451

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Symbol    | Parameter                                   |
|-----------|---|
| $I_{PP}$  | Maximum Reverse Peak Pulse Current          |
| $V_C$     | Clamping Voltage @ $I_{PP}$                 |
| $V_{RWM}$ | Working Peak Reverse Voltage                |
| $I_R$     | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$  | Breakdown Voltage @ $I_T$                   |
| $I_T$     | Test Current                                |

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter                  | Symbol    | Conditions   | Min | Typ          | Max          | Unit     |
|----------------------------|-----------|--|-----|--------------|--------------|----------|
| Reverse Working Voltage    | $V_{RWM}$ |  |     |              | 3.3          | V        |
| Breakdown Voltage (Note 2) | $V_{BR}$  | $I_T = 1\text{ mA}$  |     | 6.0          |              | V        |
| Reverse Leakage Current    | $I_R$     | $V_{RWM} = 3.3\text{ V}$   |     | < 1.0        | 50           | nA       |
| Clamping Voltage (Note 3)  | $V_C$     | $I_{PP} = 1\text{ A}$  |     |              | 10           | V        |
| Clamping Voltage (Note 3)  | $V_C$     | $I_{PP} = 3\text{ A}$  |     |              | 13           | V        |
| ESD Clamping Voltage       | $V_C$     | Per IEC61000-4-2   |     |              |              |          |
| Junction Capacitance       | $C_J$     | $V_R = 0\text{ V}, f = 1\text{ MHz}$<br>$V_R = 0\text{ V}, f = 1\text{ GHz}$ |     | 0.25<br>0.22 | 0.35<br>0.35 | pF       |
| Dynamic Resistance         | $R_{DYN}$ | TLP Pulse  |     | 0.55         |              | $\Omega$ |

- Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
- Non-repetitive current pulse at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-5 waveform.

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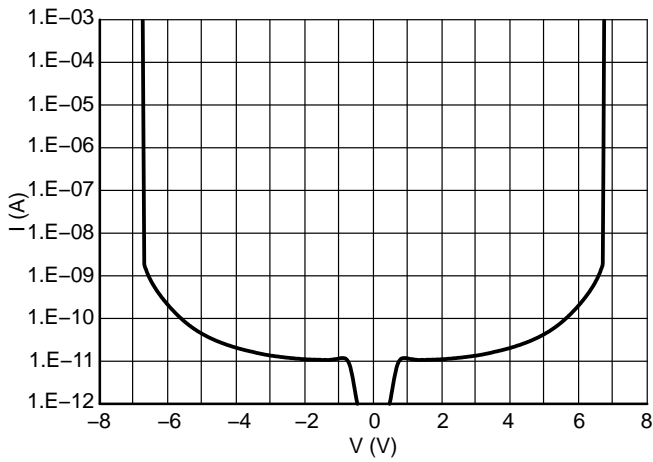


Figure 1. IV Characteristics

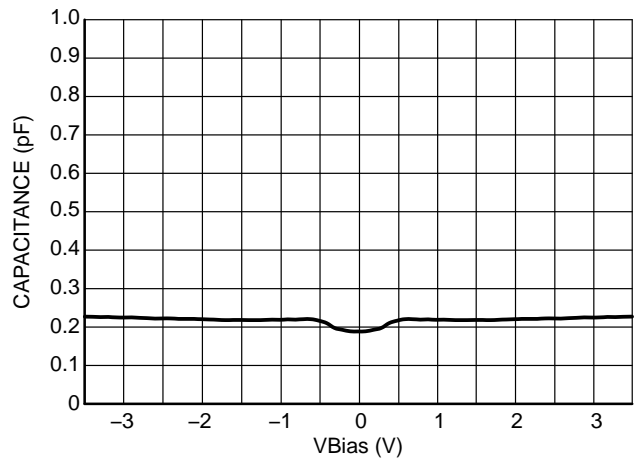


Figure 2. CV Characteristics

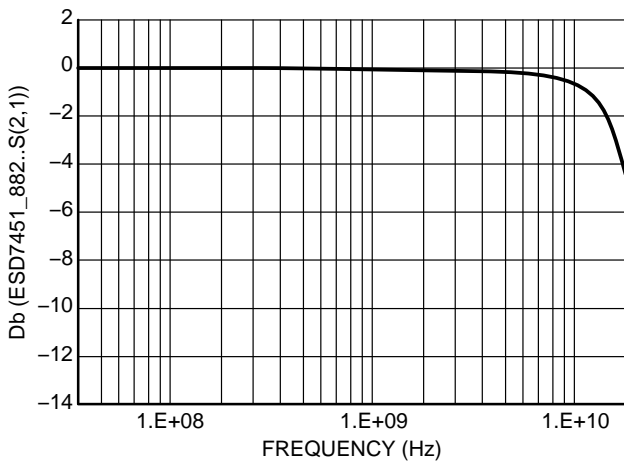


Figure 3. RF Insertion Loss

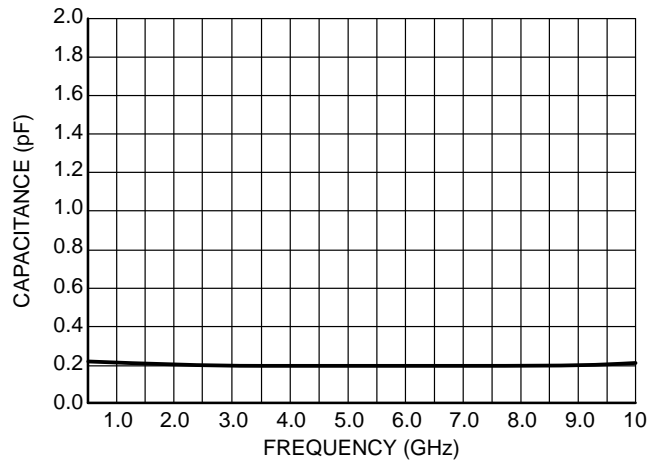


Figure 4. Capacitance over Frequency

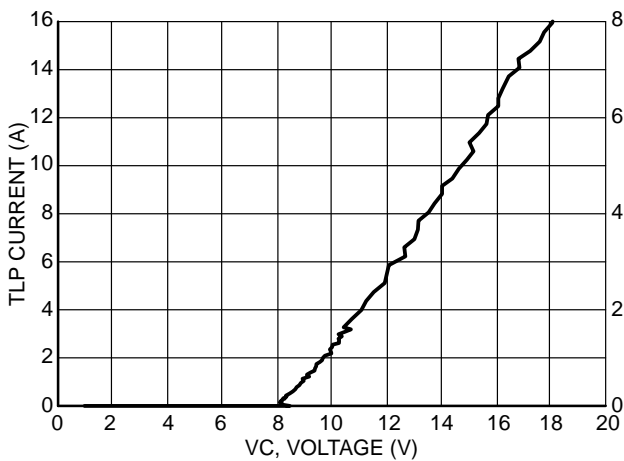


Figure 5. Positive TLP I-V Curve

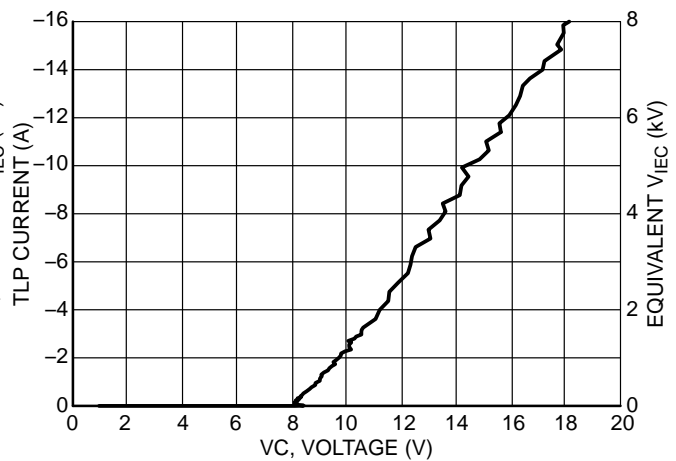


Figure 6. Negative TLP I-V Curve

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## IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1     | 2                 | 7.5                    | 4                    | 2                    |
| 2     | 4                 | 15                     | 8                    | 4                    |
| 3     | 6                 | 22.5                   | 12                   | 6                    |
| 4     | 8                 | 30                     | 16                   | 8                    |

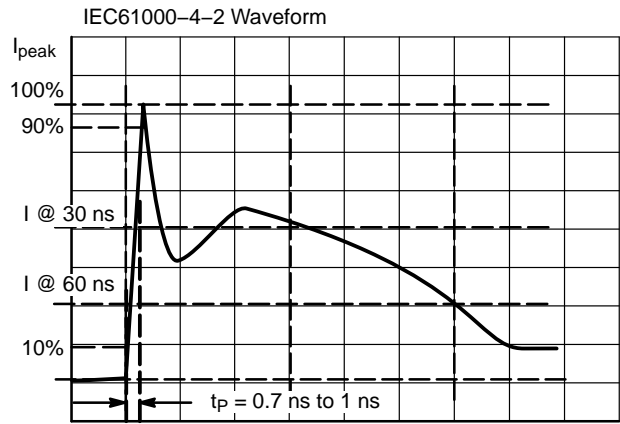


Figure 7. IEC61000-4-2 Spec

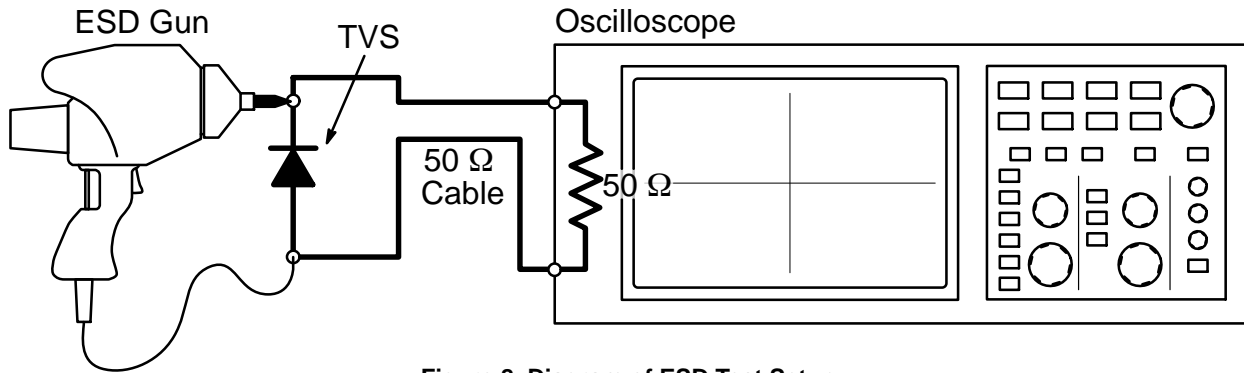


Figure 8. Diagram of ESD Test Setup

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

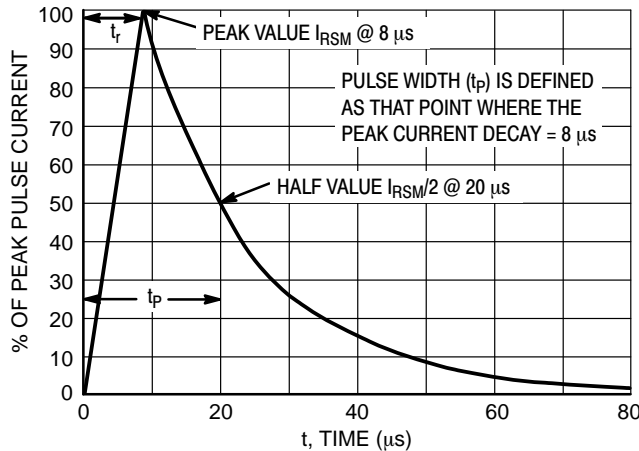
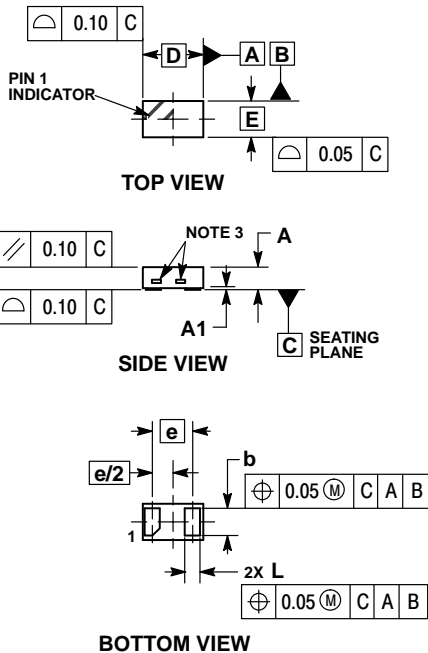


Figure 9. 8 X 20 μs Pulse Waveform

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## PACKAGE DIMENSIONS

XDFN2 1.0x0.6, 0.65P (SOD-882)  
CASE 711AM  
ISSUE O

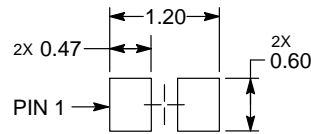


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 0.34     | 0.44 |
| A1          | ---      | 0.05 |
| b           | 0.43     | 0.53 |
| D           | 1.00 BSC |      |
| E           | 0.60 BSC |      |
| e           | 0.65 BSC |      |
| L           | 0.20     | 0.30 |

**RECOMMENDED  
SOLDER FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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