



# STW52NK25Z

## N-CHANNEL 250V - 0.033Ω - 52A TO-247 Zener-Protected SuperMESH™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STW52NK25Z	250 V	< 0.045 Ω	52 A	300 W

- TYPICAL R<sub>DS(on)</sub> = 0.033 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

### DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

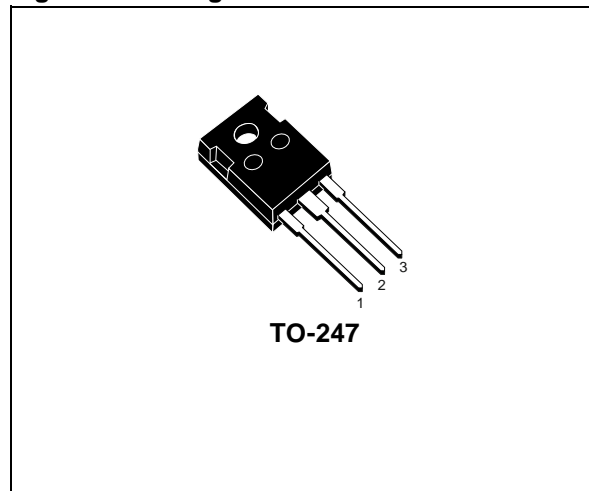
### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING DC CHOPPERS
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC

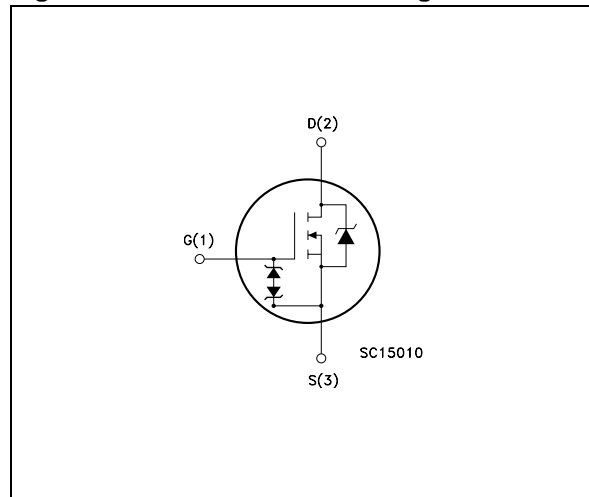
**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW52NK25Z	W52NK25Z	TO-247	TUBE

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	250	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	250	V
$V_{GS}$	Gate- source Voltage	$\pm 30$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	52	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	32.76	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	208	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating Factor	2.38	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
$T_j$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(●) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 52\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 4: Thermal Data**

Rthj-case	Thermal Resistance Junction-case Max	0.42	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
$T_I$	Maximum Lead Temperature For Soldering Purpose	300	°C

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	52	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	500	mJ

**Table 6: GATE-SOURCE ZENER DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{ mA}$ (Open Drain)	30			V

**PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES**

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	250			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 150 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 26 \text{ A}$		0.033	0.045	$\Omega$

**Table 8: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 26 \text{ A}$		25		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		4850 855 222		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 200 \text{ V}$		720		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 125V, I_D = 26 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (see Figure 17)		40 75 115 55		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 200 \text{ V}, I_D = 52 \text{ A},$ $V_{GS} = 10V$		160 32 87		nC nC nC

**Table 9: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				52 208	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 52 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 52 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 100 \text{ V}, T_j = 25^{\circ}C$ (see Figure 18)		285 0.285 2		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 52 \text{ A}, di/dt = 100A/\mu s$ $V_{DD} = 100 \text{ V}, T_j = 150^{\circ}C$ (see Figure 18)		336 0.37 2.2		ns $\mu C$ A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Figure 3: Safe Operating Area

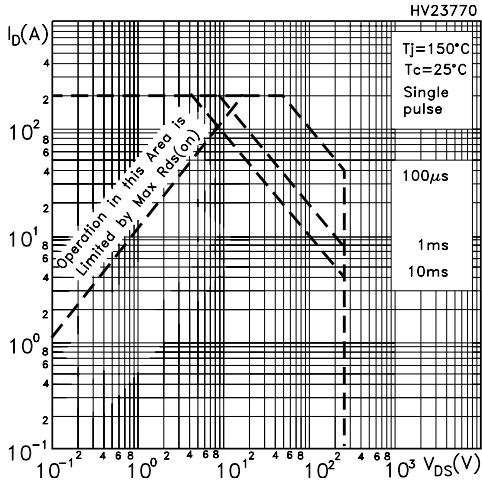


Figure 4: Output Characteristics

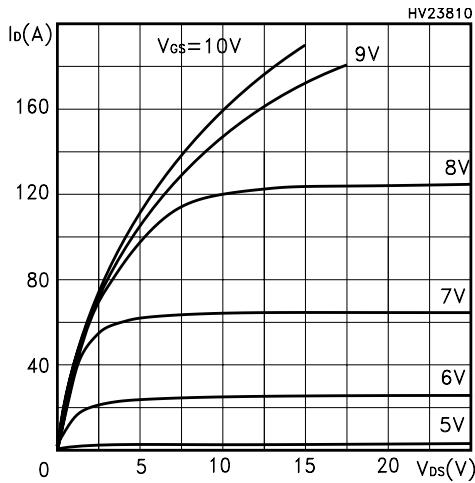


Figure 5: Transconductance

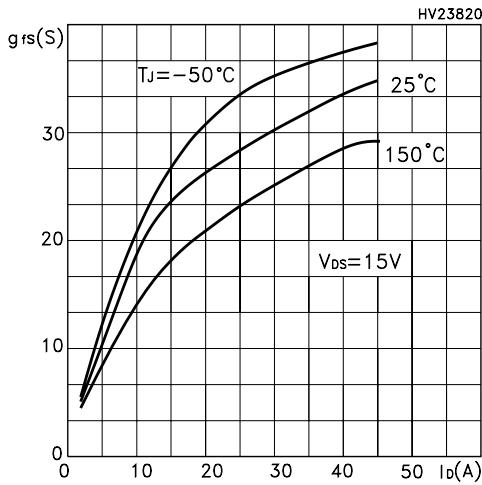


Figure 6: Thermal Impedance

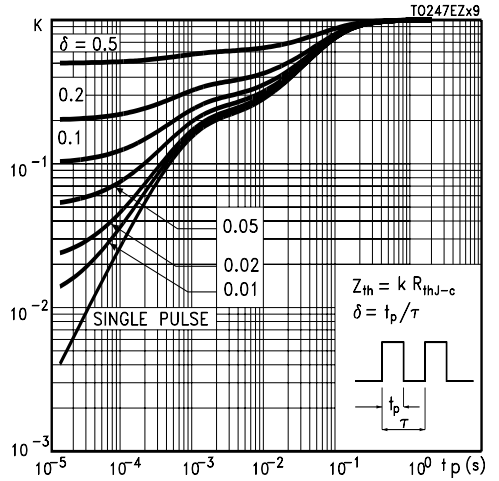


Figure 7: Transfer Characteristics

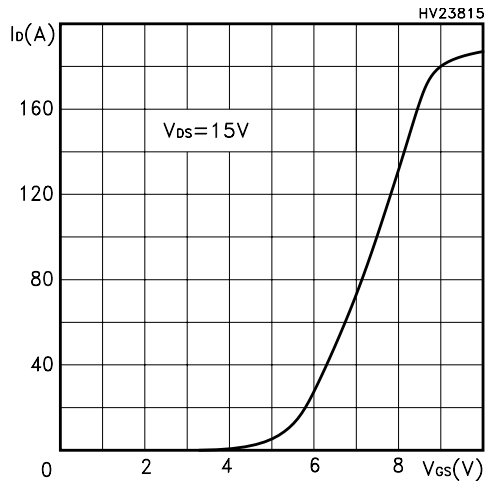


Figure 8: Static Drain-source On Resistance

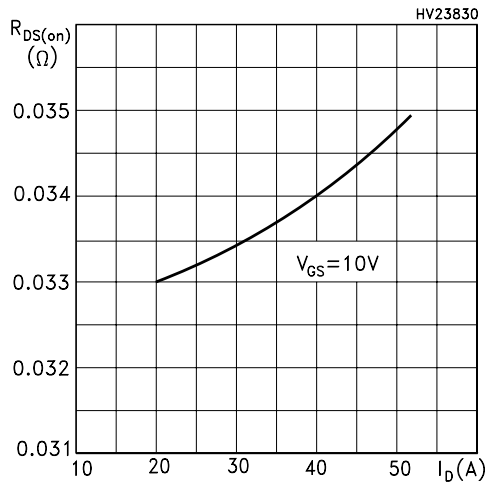


Figure 9: Gate Charge vs Gate-source Voltage

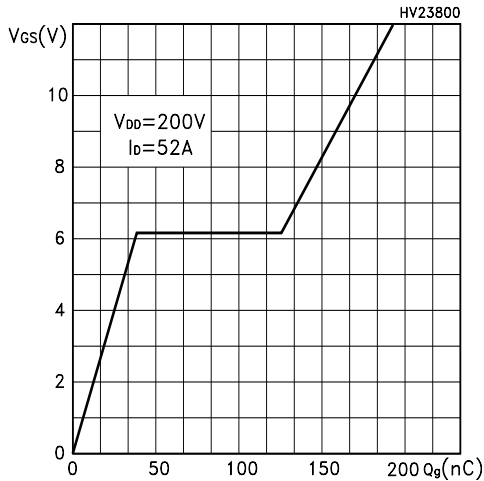


Figure 10: Normalized Gate Threshold Voltage vs Temperature

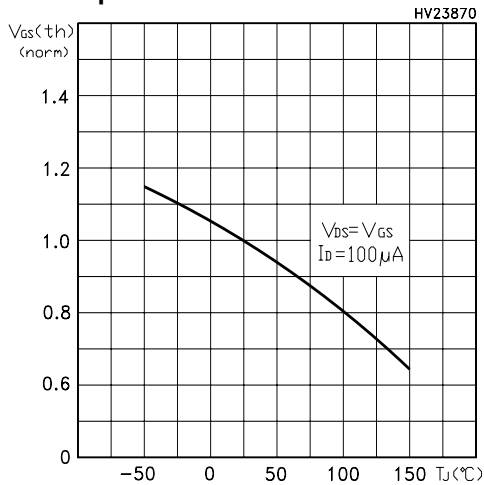


Figure 11: Source-Drain Diode Forward Characteristics

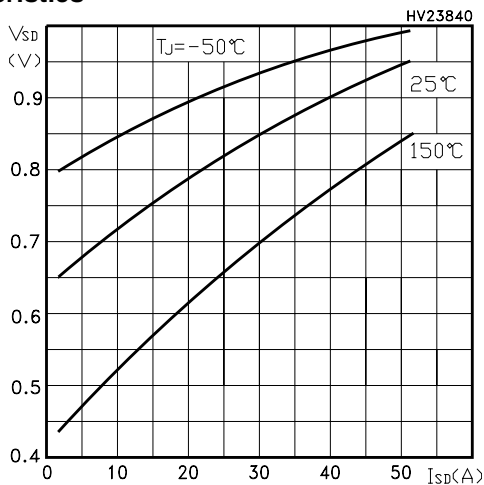


Figure 12: Capacitance Variations

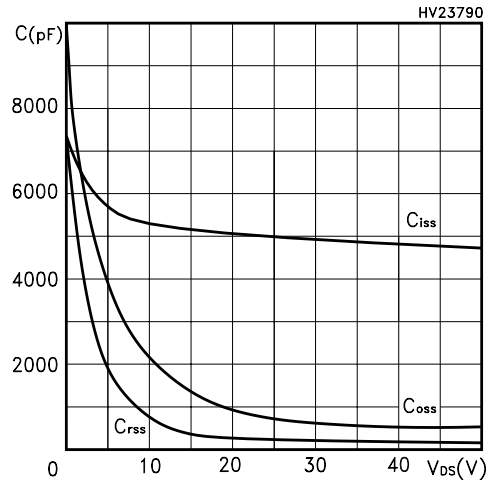


Figure 13: Normalized On Resistance vs Temperature

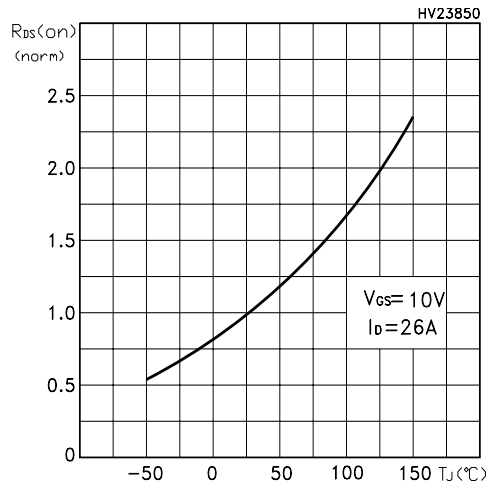


Figure 14: Normalized BVds vs Temperature

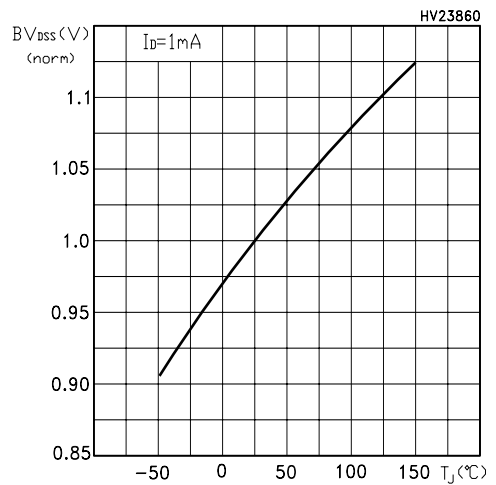


Figure 15: Avalanche Energy vs Starting Tj

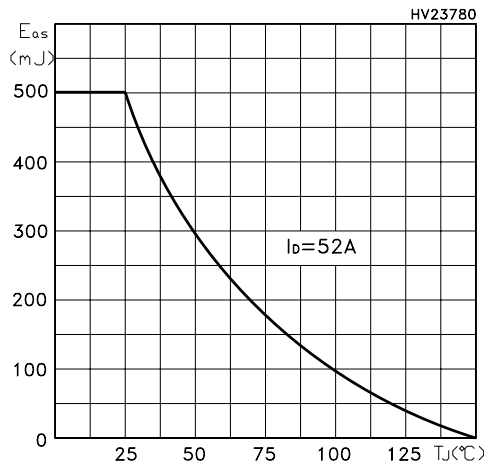


Figure 16: Unclamped Inductive Load Test Circuit

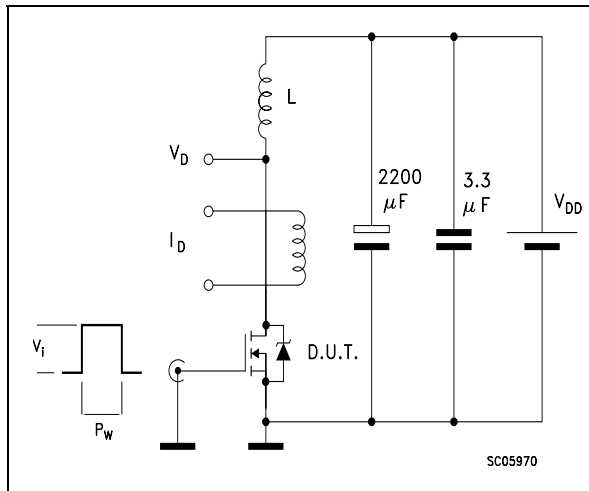


Figure 17: Switching Times Test Circuit For Resistive Load

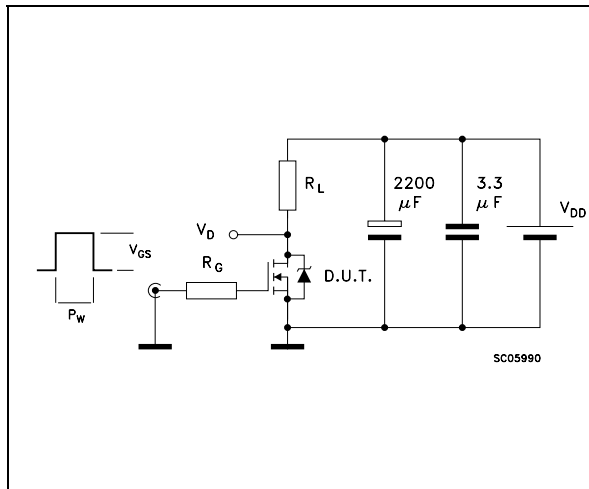


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

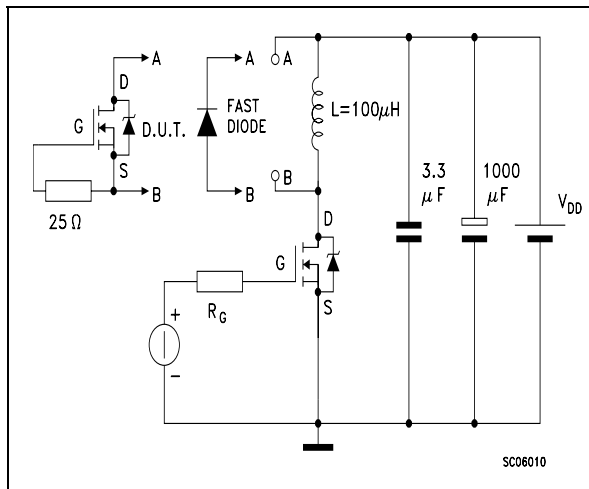


Figure 19: Unclamped Inductive Waferform

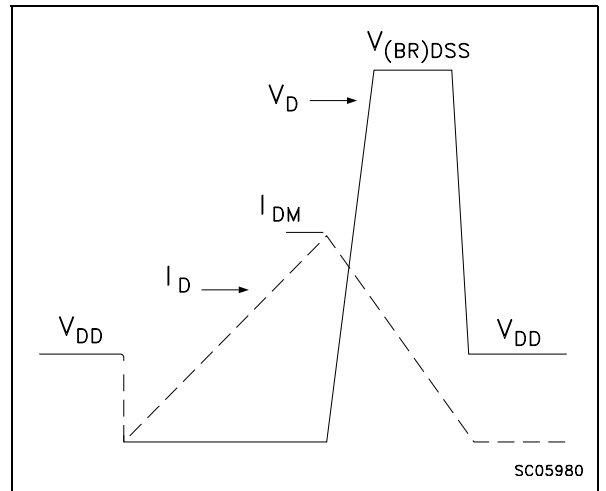
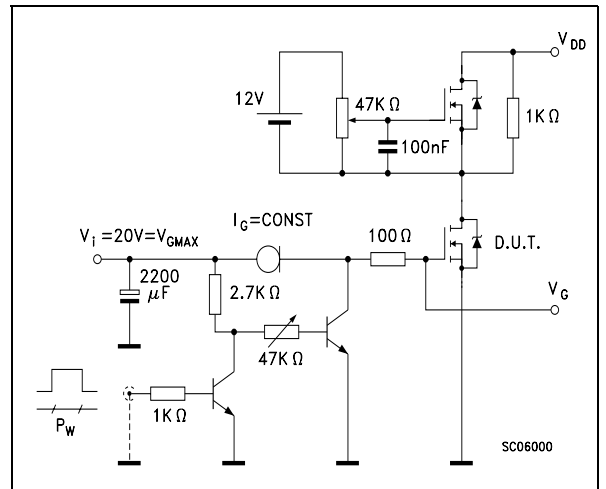
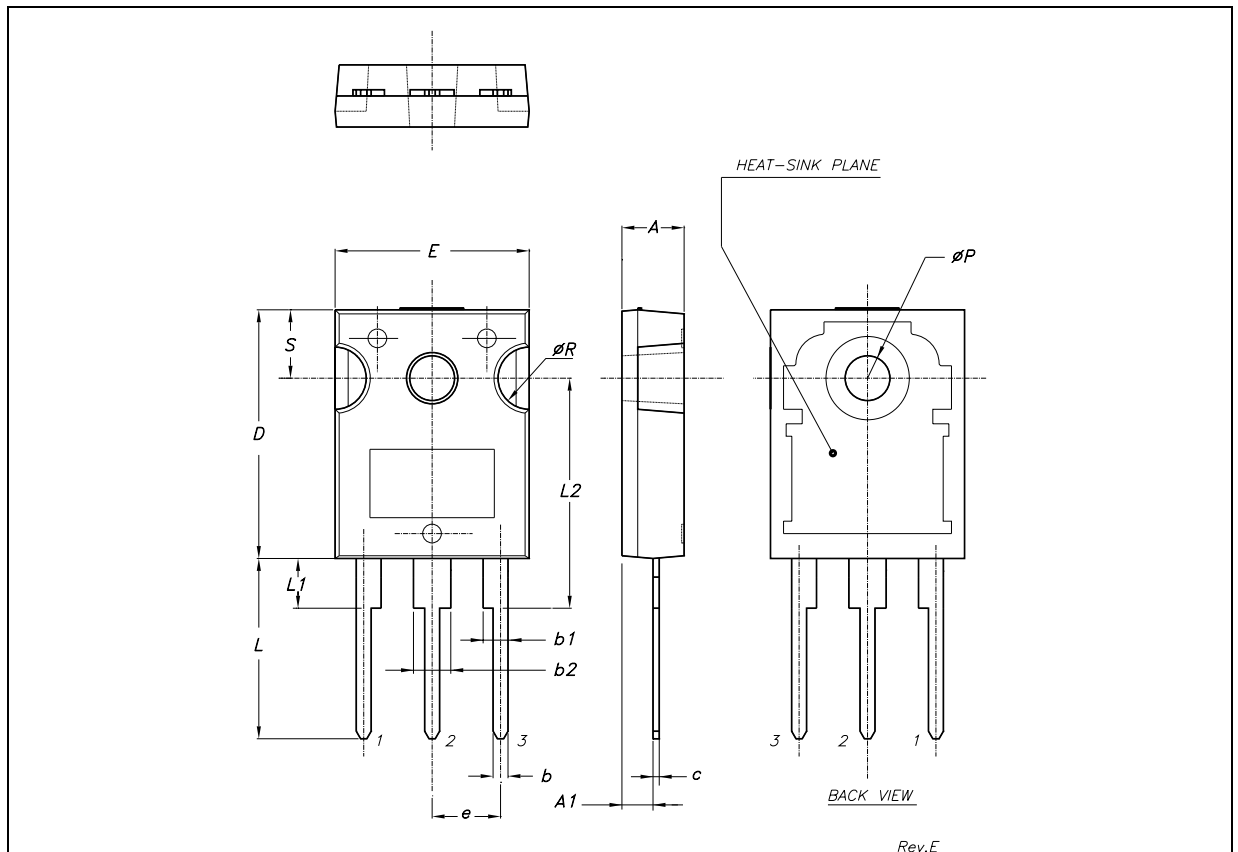


Figure 20: Gate Charge Test Circuit



## TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	





**Table 10: Revision History**

Date	Revision	Description of Changes
29-Oct-2004	1	First Release
22-Nov-2004	2	Final datasheet

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