STB36NM60N

Automotive-grade N-channel 600 V, 0.093 Ω, 29 A, MDmesh™ II Power MOSFET in a D²PAK package

Datasheet — production data

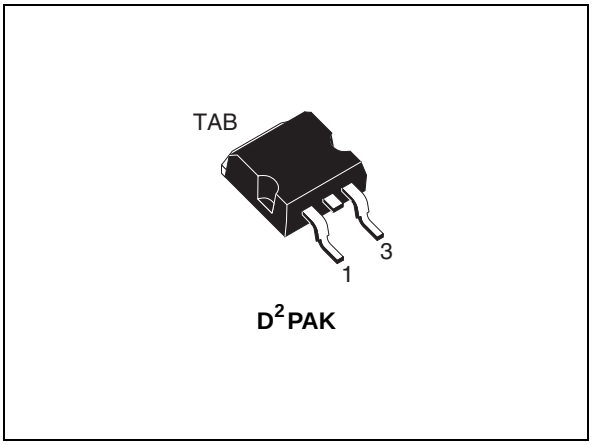
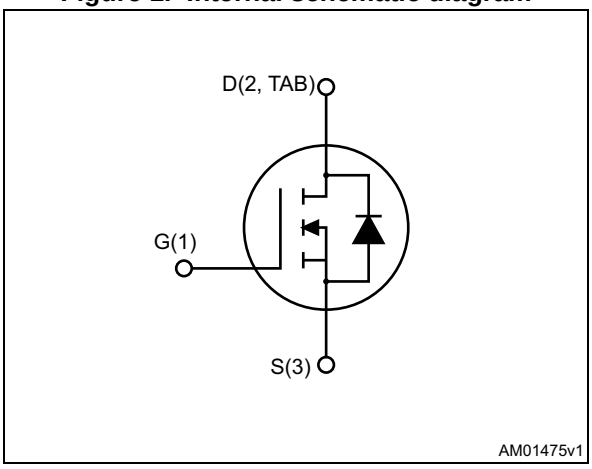


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB36NM60N	650 V	0.105 Ω	29 A	210 W

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB36NM60N	36NM60N	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	29	A
I_D	Drain current (continuous) at T_C = 100 °C	18	A
I_{DM} (1)	Drain current (pulsed)	116	A
P_{TOT}	Total dissipation at T_C = 25 °C	210	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max.)	10.5	A
E_{AS}	Single pulse avalanche energy (Starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.)	345	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating juncion temperature	150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 29$ A, di/dt $\leq$ 400 A/µs, V_{DS} peak $\leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.6	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	30	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			10	µA
		V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14.5 A		0.093	0.105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2722 173 1.75	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent Output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	458	-	pF
R_g	Gate input resistance	f =1MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	2.9	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 29 A, V_{GS} = 10 V *(see Figure 15)*	-	83.6 14 45	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 14.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*	-	17	-	ns
t_r	Rise time		-	34	-	ns
$t_{d(off)}$	Turn-off-delay time		-	106	-	ns
t_f	Fall time		-	67	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		29	A
I_{SDM} (1)	Source-drain current (pulsed)		-		116	A
V_{SD} (2)	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 19)*	-	408		ns
Q_{rr}	Reverse recovery charge		-	8		µC
I_{RRM}	Reverse recovery current		-	39		A
t_{rr}	Reverse recovery time	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD}= 60 V Tj = 150 °C *(see Figure 19)*	-	480		ns
Q_{rr}	Reverse recovery charge		-	10		µC
I_{RRM}	Reverse recovery current		-	42		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

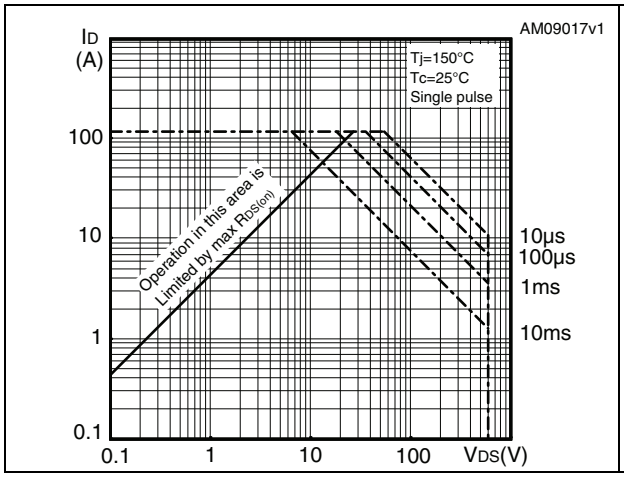


Figure 3. Thermal impedance

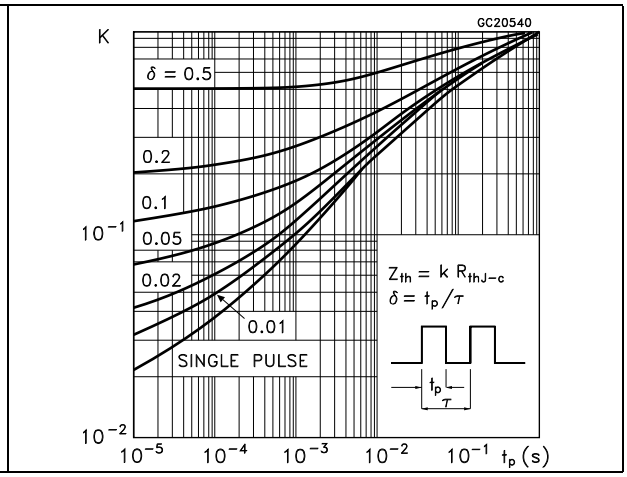


Figure 4. Output characteristics

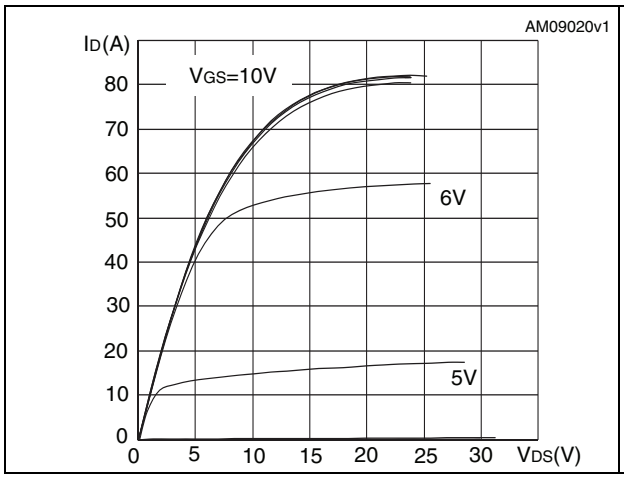


Figure 5. Transfer characteristics

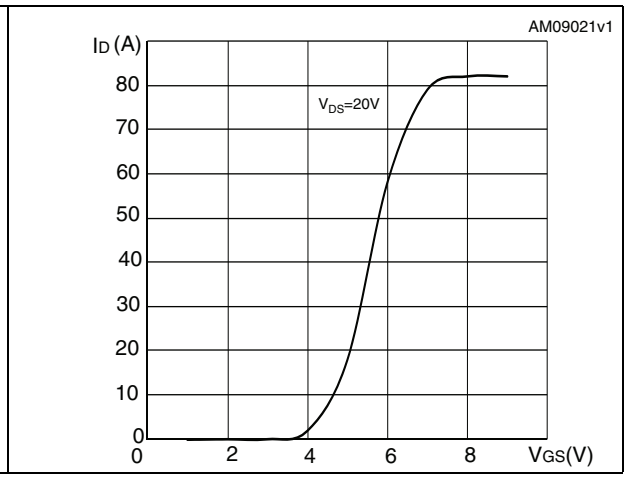


Figure 6. Gate charge vs gate-source voltage

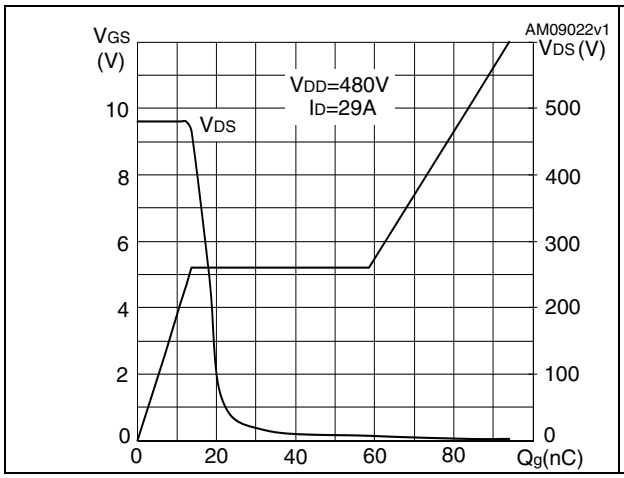


Figure 7. Static drain-source on-resistance

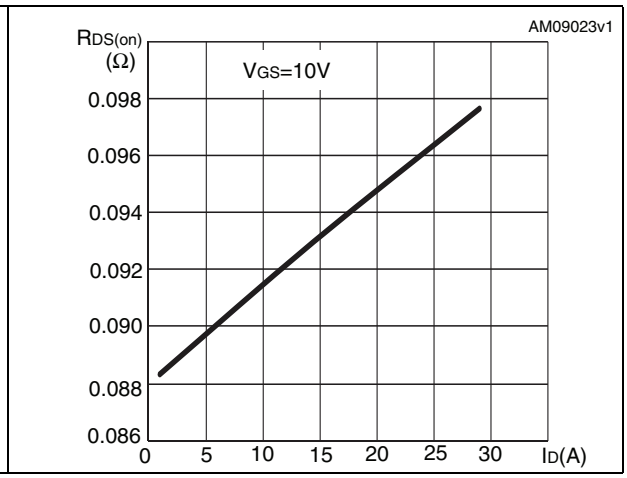


Figure 8. Capacitance variations

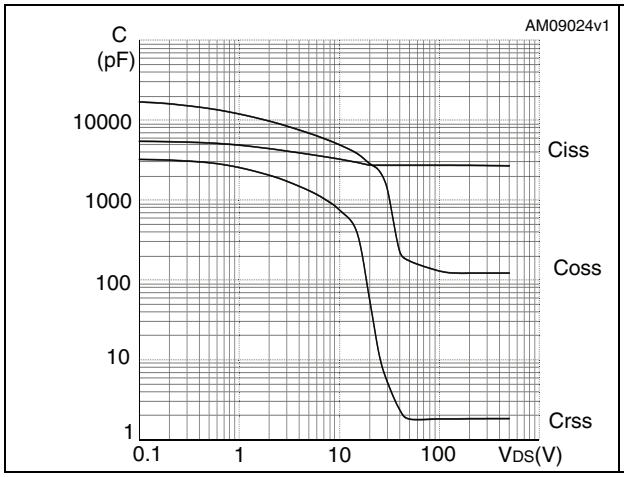


Figure 9. Output capacitance stored energy

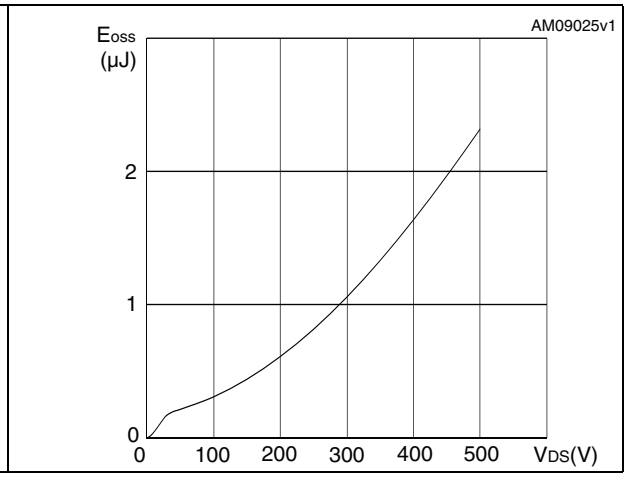


Figure 10. Normalized gate threshold voltage vs temperature

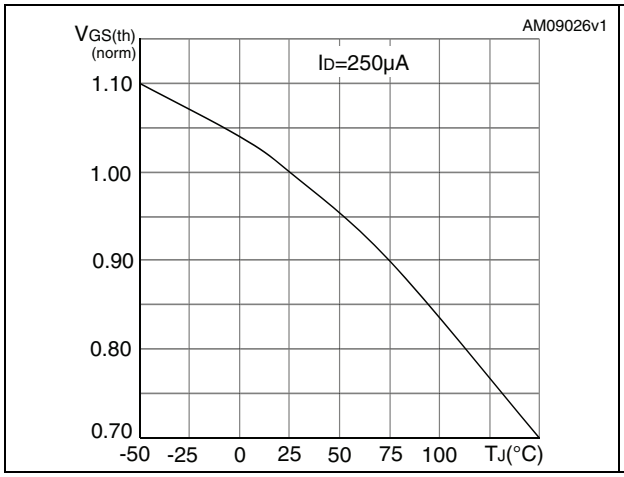


Figure 11. Normalized on-resistance vs temperature

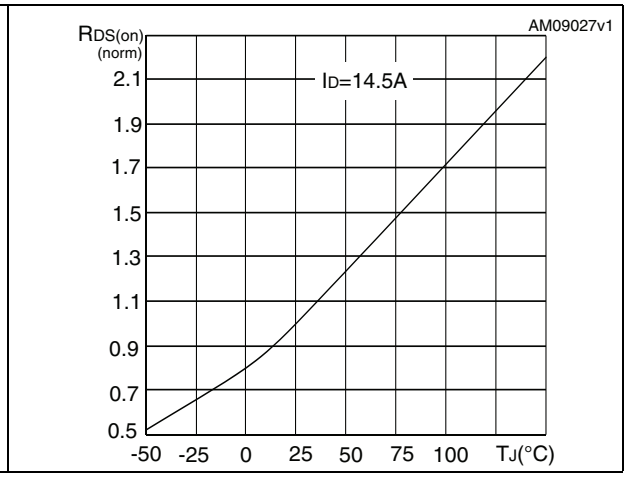


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

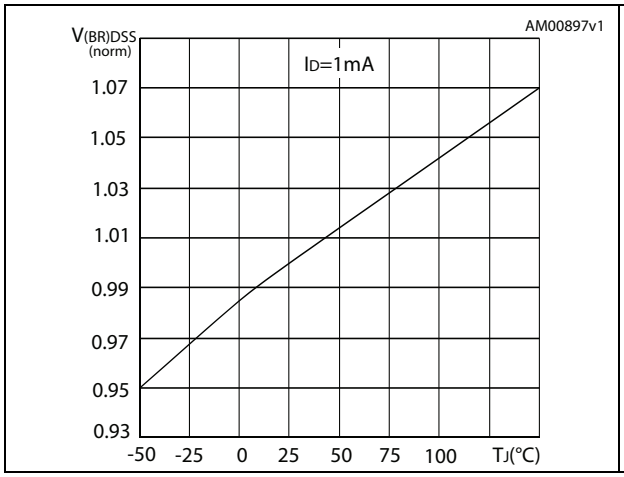
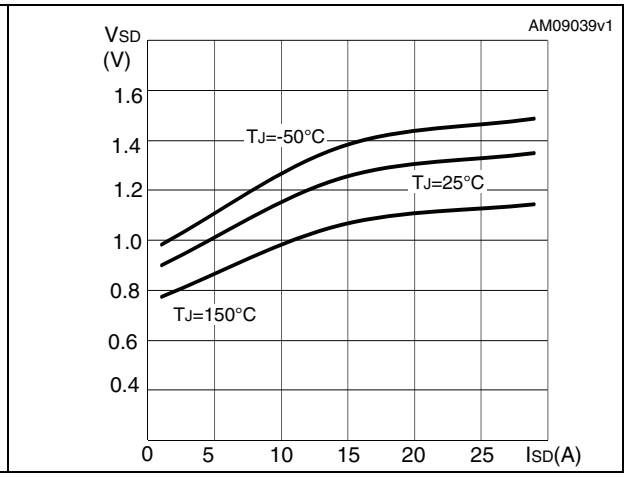


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

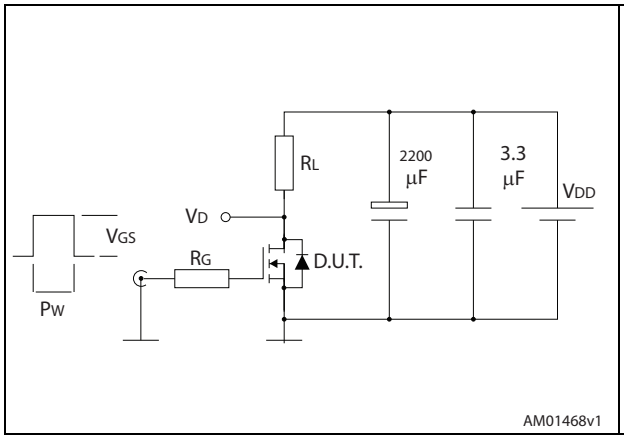


Figure 15. Gate charge test circuit

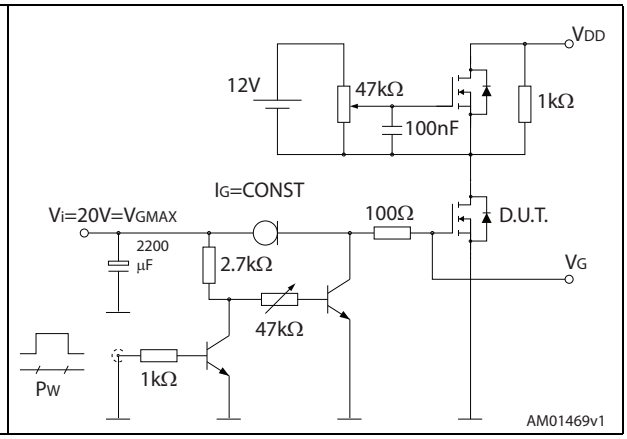


Figure 16. Test circuit for inductive load switching and diode recovery times

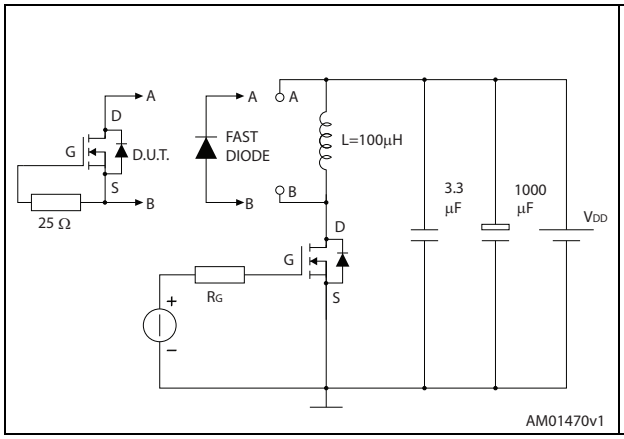


Figure 17. Unclamped inductive load test circuit

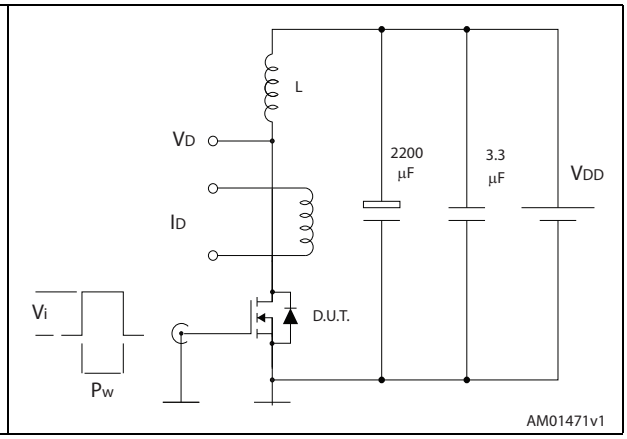


Figure 18. Unclamped inductive waveform

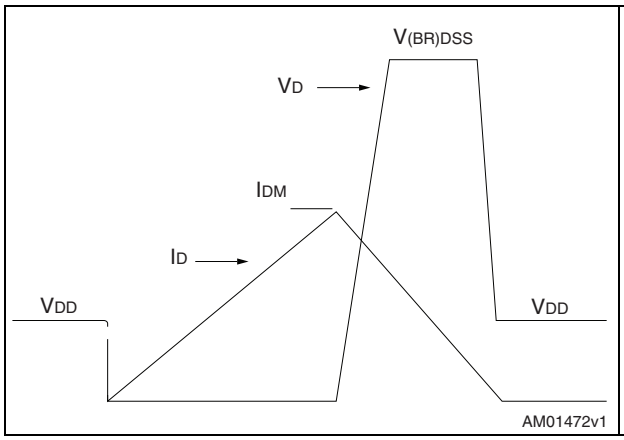
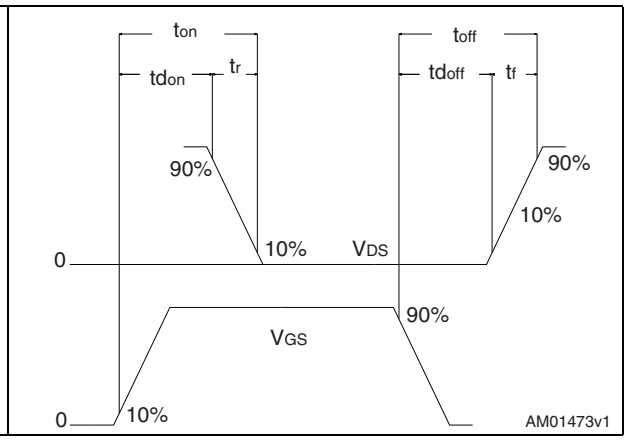


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. D²PAK (TO-263) type A package outline

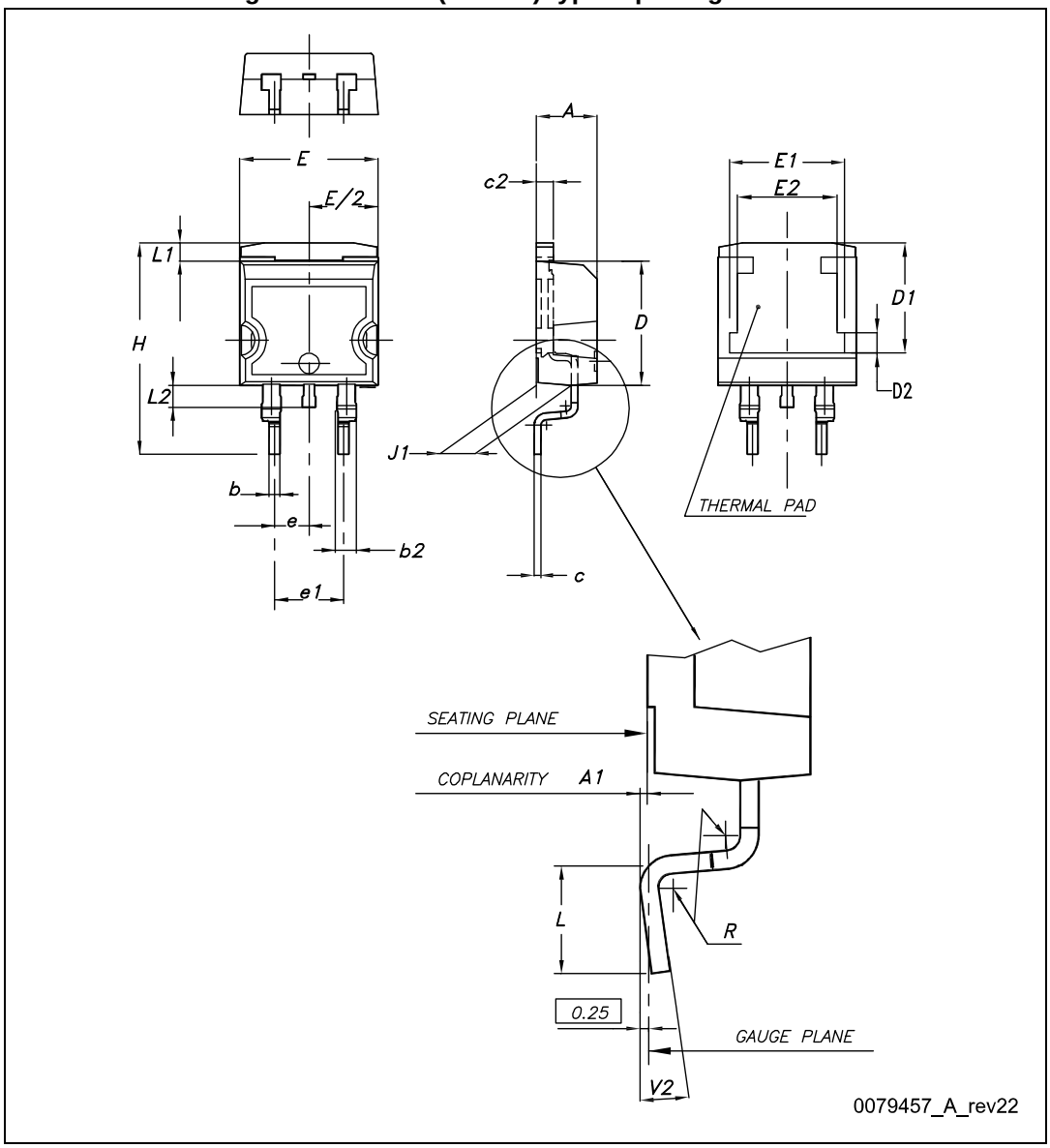
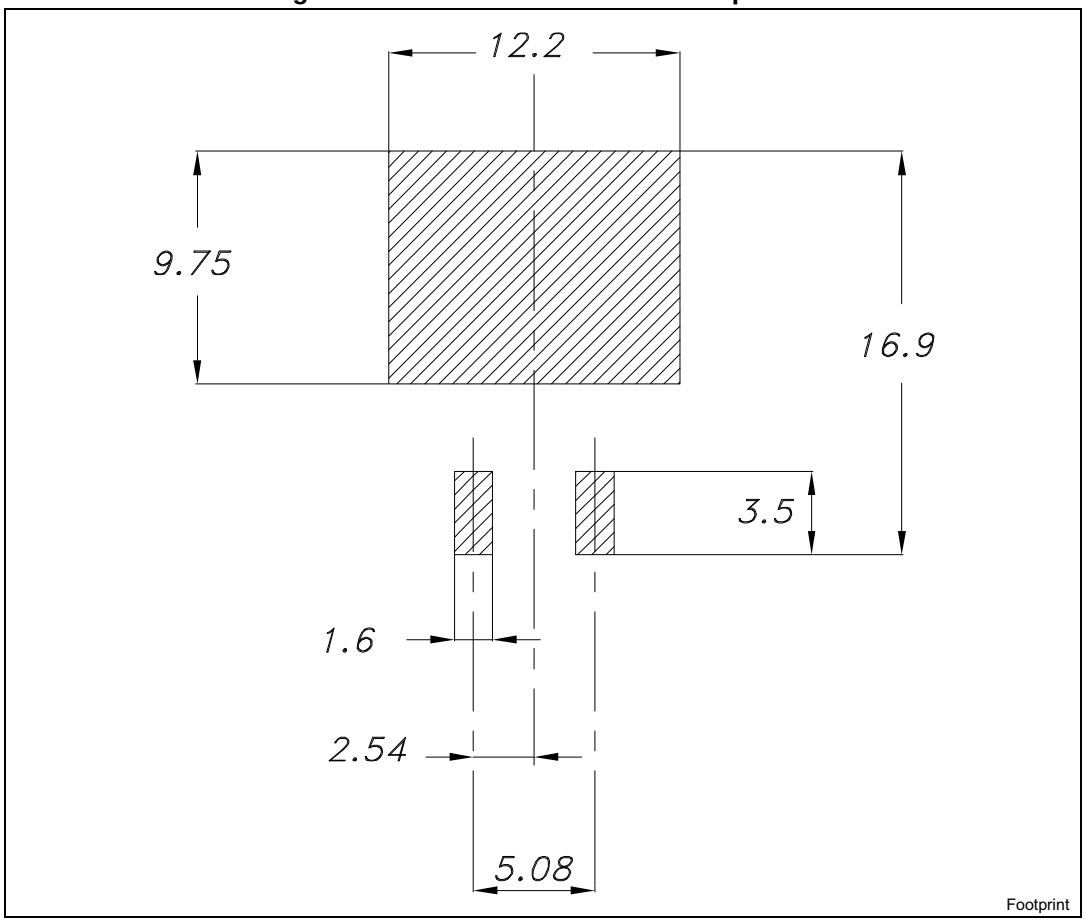


Table 8. D²PAK (TO-263) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D²PAK recommended footprint(a)



a. All dimension are in millimeters

5 Packing information

Figure 22. Tape

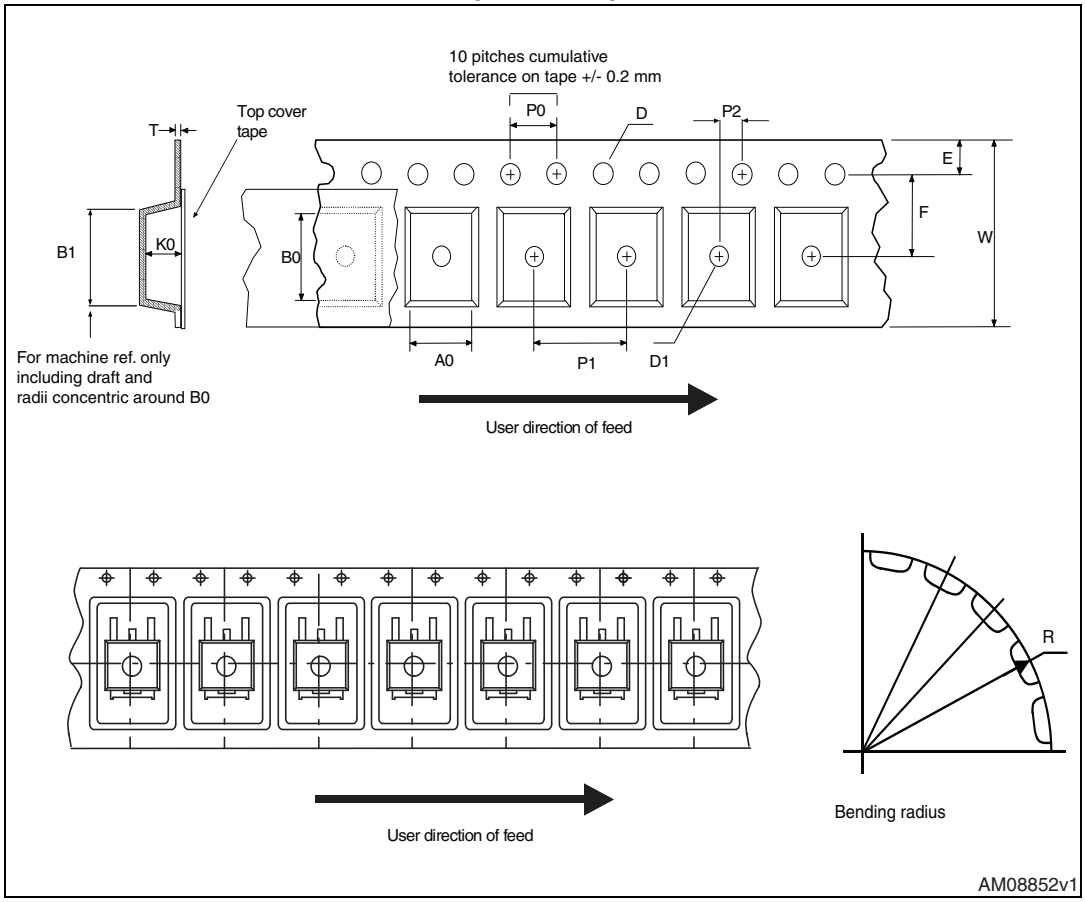


Figure 23. Reel

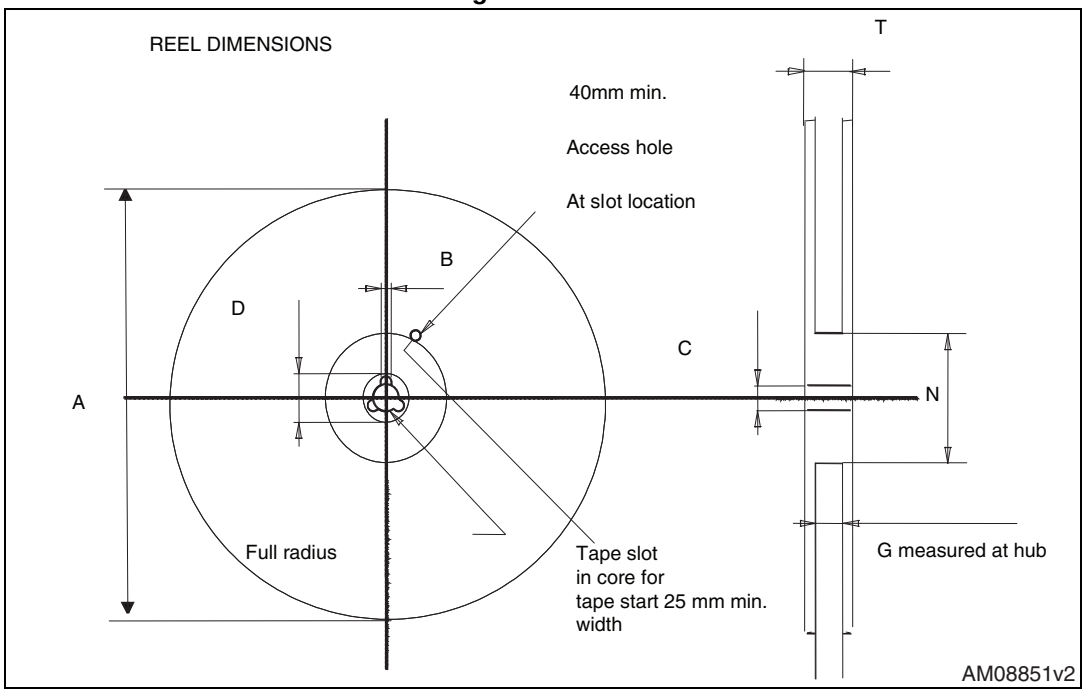


Table 9. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Nov-2009	1	First release.
22-Jun-2011	2	Document status promoted from preliminary data to datasheet.
10-May-2012	3	*Figure 6: Gate charge vs gate-source voltage* has been modified. Minor text changes.
19-Sep-2014	4	– Modified: title and features – Minor text changes
09-Jun-2015	5	– Updated title, internal schematic diagram and features in cover page. – Updated *Table 3: Thermal data* and *Figure 12: Normalized $V_{(BR)DSS}$ vs temperature*. – Updated *Section 4: Package information*. – Minor text changes.