



12 ns TRIPLE-CHANNEL HIGH VOLTAGE VIDEO AMPLIFIER

FEATURES

- Triple-channel video amplifier
- Supply voltage up to 115 V
- 80V Output dynamic range
- Perfect for PICTURE BOOST application requiring high video amplitude
- Pinning for easy PCB layout
- Supports DC coupling (optimum cost saving) and AC coupling applications.
- Built-in Voltage Gain: 20 (Typ.)
- Rise and Fall Times: 12 ns (Typ.)
- Bandwidth: 29 MHz (Typ.)
- Very low stand-by power consumption
- Perfectly matched with the STV921x preamplifiers

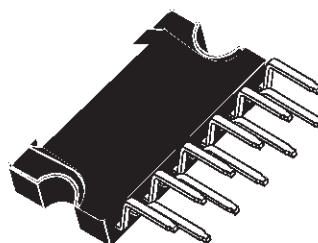
DESCRIPTION

The STV9553 is a triple-channel video amplifier designed in a 120V-high voltage technology and able to drive in DC-coupling mode the 3 cathodes of a CRT monitor.

The STV9553 supports PICTURE BOOST applications where video amplitude up to 50V or

above is required, ensuring a maximum quality of the still pictures or moving video.

Perfectly matched with the STV921x ST preamplifiers, it provides a highly performant and very cost effective video system.



CLIPWATT 11
(Plastic Package)

ORDER CODE: STV9553

PIN CONNECTIONS

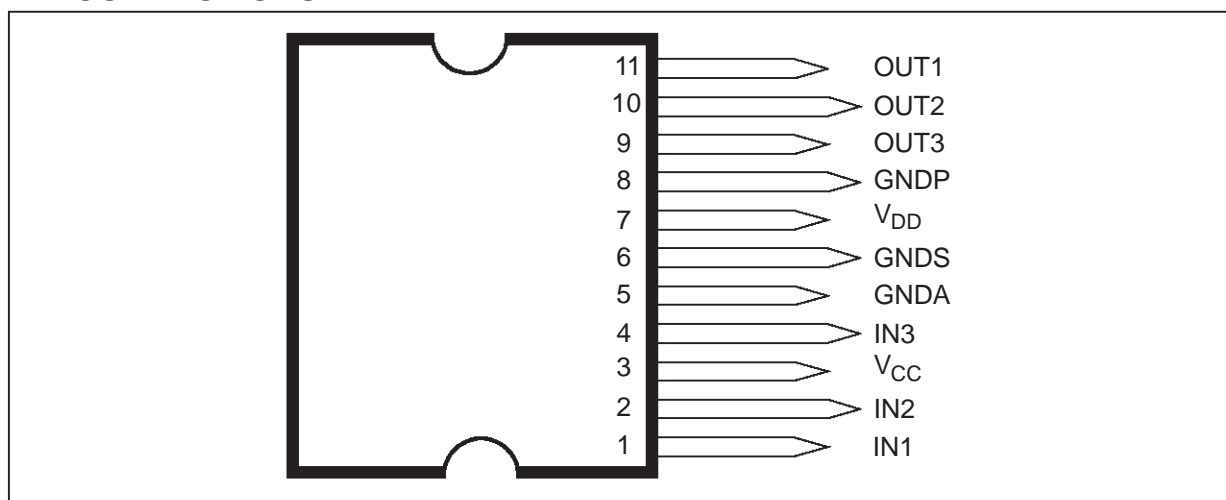
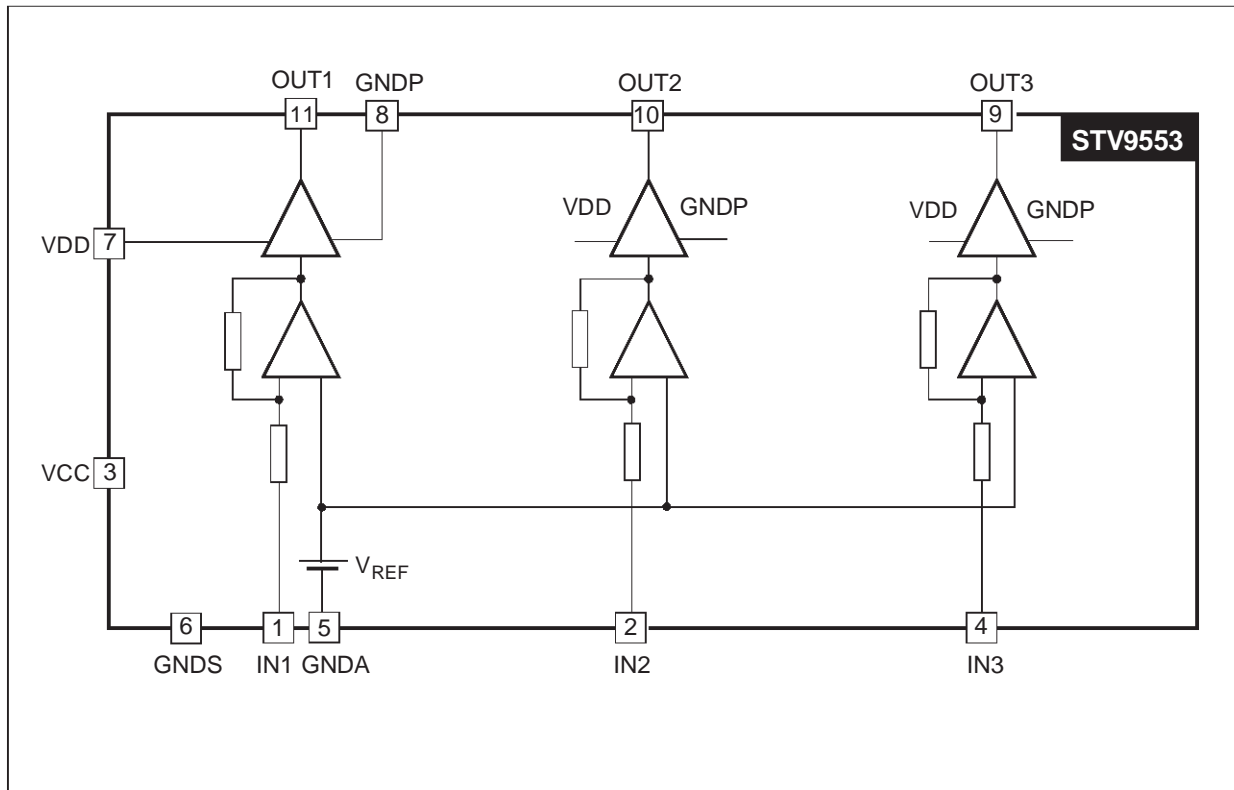


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1 BLOCK DIAGRAM



2 PIN DESCRIPTION

Pin	Name	Function
1	IN1	Video Input (channel 1)
2	IN2	Video Input (channel 2)
3	VCC	Low Supply Voltage
4	IN3	Video Input (channel 3)
5	GNDA	Ground Analog
6	GNDS	Ground Substrat
7	VDD	High Supply Voltage
8	GNDP	Ground Power
9	OUT3	Video output (channel 3)
10	OUT2	Video output (channel 2)
11	OUT1	Video output (channel 1)

3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	High supply voltage	120	V
V_{CC}	Low supply voltage	16.5	V
V_{ESD}	ESD susceptibility Human Body Model (100pF discharged through 1.5K Ω) EIAJ norm (200pF discharged through 0 Ω)	2	kV
		300	V
I_{OD}	Output source current (pulsed < 50 μ s)	80	mA
I_{OG}	Output sink current (pulsed < 50 μ s)	80	mA
$V_{IN Max}$	Maximum Input Voltage	$V_{CC} + 0.3$	V
$V_{IN Min}$	Minimum Input Voltage	- 0.5	V
T_J	Junction Temperature	150	$^{\circ}$ C
T_{STG}	Storage Temperature	-20 + 150	$^{\circ}$ C

4 THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction-Case Thermal Resistance (Max.)	3	$^{\circ}$ C/W
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance (Typ.)	35	$^{\circ}$ C/W

5 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
SUPPLY parameters ($V_{CC} = 12V$, $V_{DD} = 110V$, $T_{amb} = 25^\circ C$, unless otherwise specified)						
V_{DD}	High supply voltage		20	110	115	V
V_{CC}	Low supply voltage		10	12	15	V
I_{DD}	V_{DD} supply current	$V_{OUT} = 50V$		15		mA
I_{DDS}	V_{DD} stand-by supply current	V_{CC} : switched off (<1.5V) V_{OUT} : low (Note 1)		60		μA
I_{CC}	V_{CC} supply current	$V_{OUT} = 50V$		40		mA
STATIC parameters ($V_{CC} = 12V$, $V_{DD} = 110V$, $T_{amb} = 25^\circ C$)						
V_{OUT}	DC output voltage	$V_{IN} = 1.90 V$	77	80	83	V
dV_{OUT}/dV_{DD}	High voltage supply rejection	$V_{OUT} = 50V$		0.5		%
dV_{OUT}/dT	Output voltage drift versus temperature	$V_{OUT} = 80V$		15		mV/ $^\circ C$
$d\Delta V_{OUT}/dT$	Output voltage matching versus temperature (Note 2)	$V_{OUT} = 80V$		1		mV/ $^\circ C$
R_{IN}	Video input resistor	$V_{OUT} = 50V$		2		k Ω
V_{SATH}	Output saturation voltage to supply	$I_0 = -60mA$ (Note 3)		$V_{DD} - 6.5$		V
V_{SATL}	Output saturation voltage to GND	$I_0 = 60mA$ (Note 3)		11		V
G	Video Gain	$V_{OUT} = 50V$		20		
LE	Linearity Error	$17 V < V_{OUT} < V_{DD} - 15 V$		3	8	%
V_{REF}	Internal voltage reference			5.6		V

Note 1: The STV9553 goes into stand-by mode when V_{CC} is switched off (<1.5V).
In stand-by mode, V_{out} is set to low level.

Note 2: Matching measured between each channel.

Note 3: Pulsed current width < 50 μs

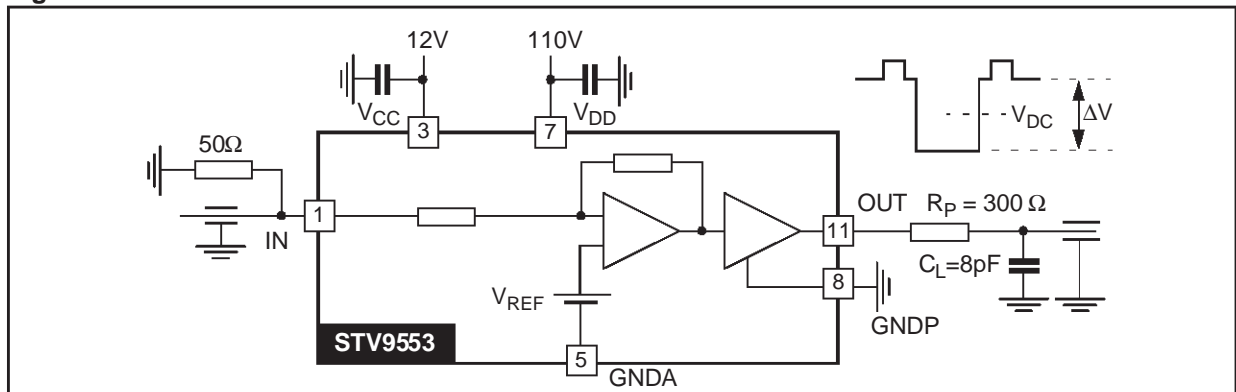
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
DYNAMIC parameters (see Figure 1)						
t_R	Rise time	$V_{DC}=50V, \Delta V=40V_{PP}$		10.8		ns
t_F	Fall time	$V_{DC}=50V, \Delta V=40V_{PP}$		12.8		ns
OS_R	Overshoot, white to black transition			5		%
OS_F	Overshoot, black to white transition			0		%
ΔG	Low frequency gain matching (Note 4)	$V_{DC} = 50V, f=1MHz$			5	%
BW	Bandwidth at -3dB	$V_{DC}=50V, \Delta V=20V_{PP}$		29		MHz
t_{SET}	2.5% Settling time	$V_{DC}=50V, \Delta V=40V_{PP}$		15		ns
CT_L	Low frequency crosstalk	$V_{DC}=50V, \Delta V=20V_{PP}$ $f = 1 MHz$		50		dB
CT_H	High frequency crosstalk	$V_{DC}=50V, \Delta V=20V_{PP}$ $f = 20MHz$		32		dB
DYNAMIC parameter in PICTURE BOOST condition (Note 5)						
t_{PB}	Rise/fall time	$V_{DC}=50V, \Delta V=60V_{PP}$		15		ns
OS_{PB}	Overshoot white to black or black to white transition	$V_{DC}=50V, \Delta V=60V_{PP}$		9		%

Note 4: Matching measured between each channel.

Note 5: PICTURE BOOST condition (video amplitude at 50V or above) is used in some applications when displaying still picture or moving video. In this condition the high level of contrast improves the pictures quality at the expense of the video performances (t_R , t_F and Overshoot) which are slightly deteriorated.

Figure 1. AC test circuit



6 THEORY OF OPERATION

6.1 General

The STV9553 is a three-channel video amplifier supplied by a low supply voltage: V_{CC} (typ. 12V) and a high supply voltage: V_{DD} (up to 115V).

The high values of V_{DD} supplying the amplifier output stage allow direct control of the CRT cathodes (DC coupling mode).

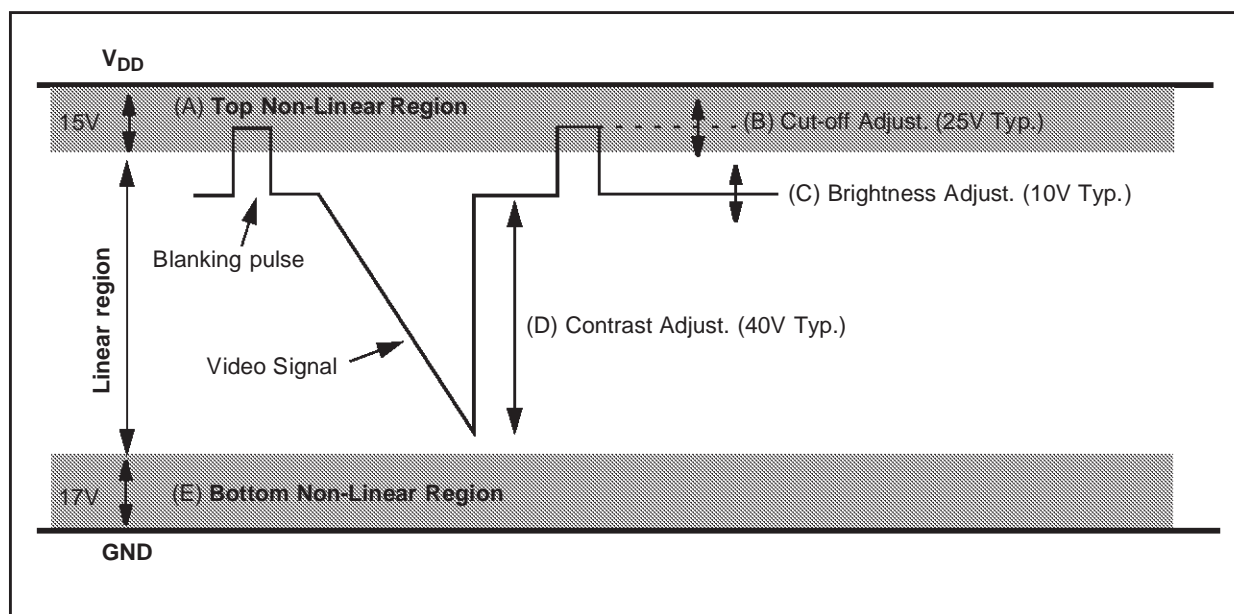
In DC coupling mode, the application schematic is very simple and only a few external components are needed to drive the cathodes. In particular, there is no need of the DC-restore circuitry which is used in classical AC coupling applications.

The output voltage range is wide enough (Figure 2) to provide simultaneously :

- Cut-off adjustment (typ. 25V)
- Video contrast (typ. up to 40V),
- Brightness (with the remaining voltage range).

In normal operation, the output video signal must remain inside the linear region whatever the cut-off, brightness and contrast adjustments are.

Figure 2. Output signal, level adjustments



6.2 Output voltage

A very simplified schematic of each STV9553 channel is shown in Figure 3.

The feedback network of each channel is integrated with a typical built-in voltage gain of $G=20$ ($40k/2k$).

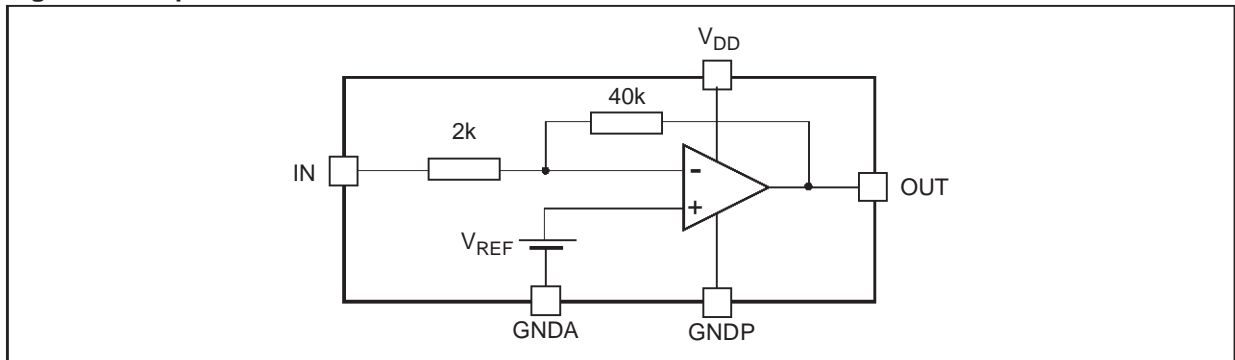
The output voltage V_{OUT} is given by the following formula:

$$V_{OUT} = (G+1) \times V_{REF} - (G \times V_{IN})$$

for $G = 20$ and $V_{REF} = 5.6V$, we have

$$V_{OUT} = 117.6 - 20 \times V_{IN}$$

Figure 3. Simplified schematic of one channel



7 POWER DISSIPATION

The total power dissipation is the sum of the static DC and the dynamic dissipation:

$$P_{TOT} = P_{STAT} + P_{DYN}$$

The static DC power dissipation is approximately:

$$P_{STAT} = V_{DD} \times I_{DD} + V_{CC} \times I_{CC}$$

The dynamic dissipation is, in the worst case (1 pixel On/ 1 pixel Off pattern):

$$P_{DYN} = 3 V_{DD} \times C_L \times V_{OUT(PP)} \times f \times K \text{ (see Note 6)}$$

where f is the video frequency and K the ratio between the active line and the total horizontal line duration.

Example:

$$\text{for } V_{DD} = 110V, V_{CC} = 12V,$$

$$I_{DD} = 15mA, I_{CC} = 40mA,$$

$$V_{OUT} = 40 V_{PP}, f = 25MHz,$$

$$C_L = 8pF \text{ and } K = 0.72.$$

We have:

$$P_{STAT} = 2.13W \text{ and } P_{DYN} = 1.90W$$

Therefore:

$$P_{TOT} = 4.03W.$$

Note 6: This worst thermal case must only be considered for T_{Jmax} calculation. Nevertheless, during the average life of the circuit, the conditions are closer to the white picture conditions.

8 TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD}=110V$, $V_{CC}=12V$, $C_L=8pF$, $R_P=300\Omega$, $\Delta V=40V_{PP}$, unless otherwise specified - see Figure 1

Figure 4. STV9553 pulse response

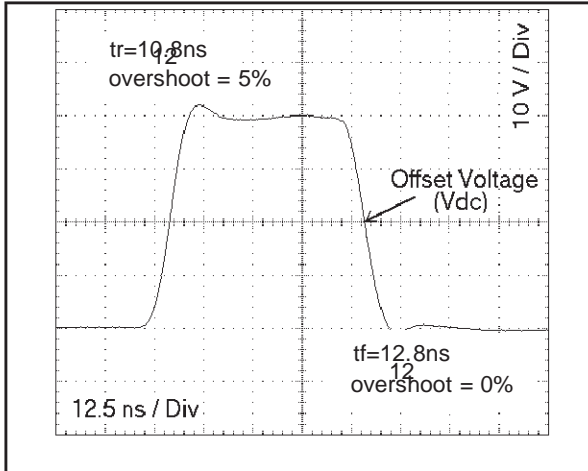


Figure 5. V_{OUT} versus V_{IN}

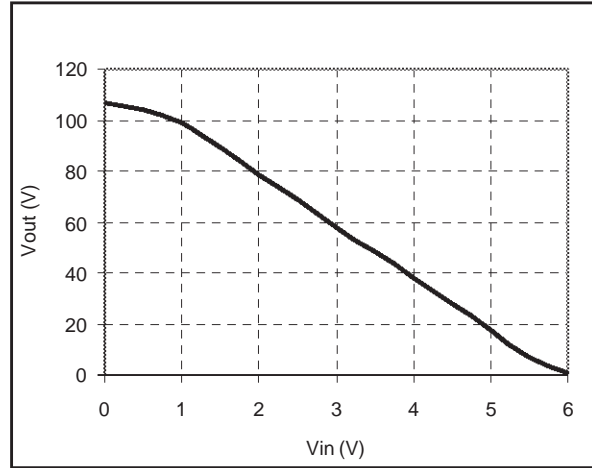


Figure 6. Power dissipation versus frequency

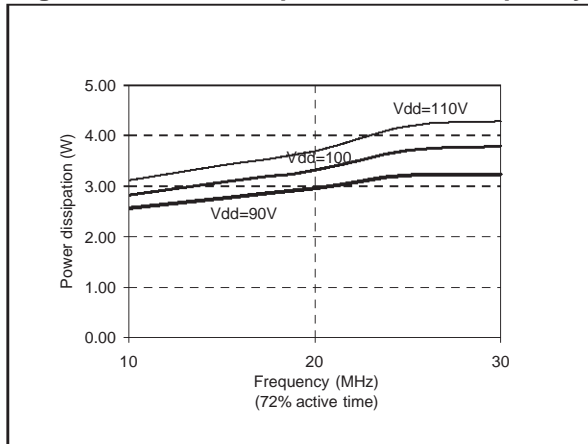


Figure 7. Speed versus temperature

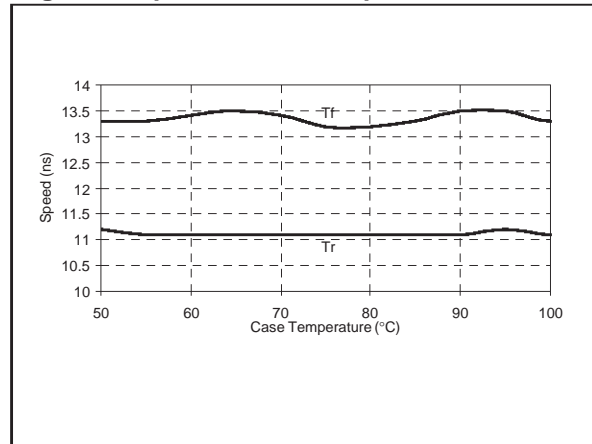


Figure 8. Speed versus offset

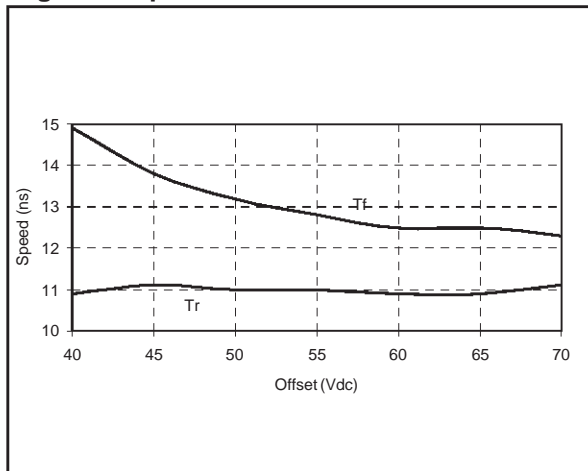
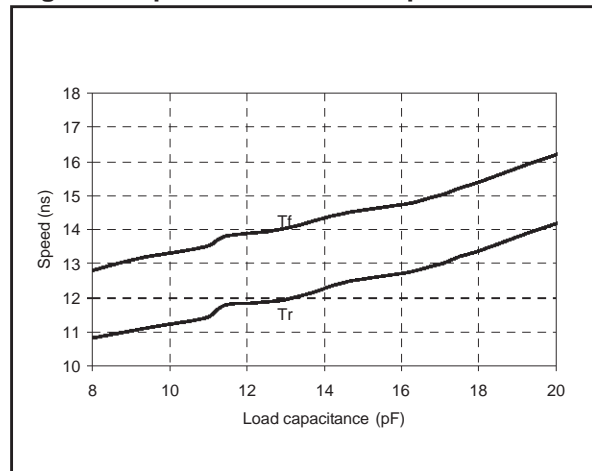


Figure 9. Speed versus load capacitance



9 INTERNAL SCHEMATICS

Figure 10. RGB inputs

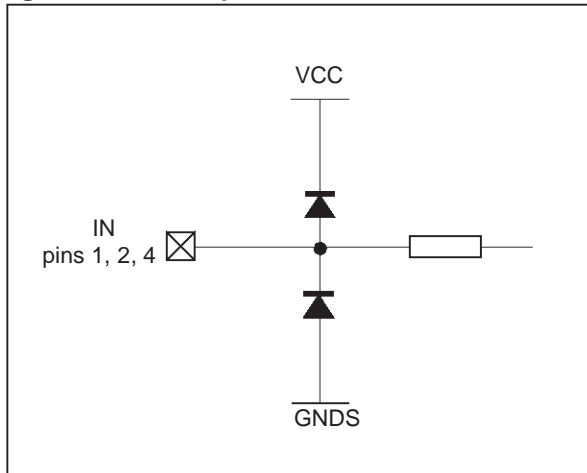


Figure 11. RGB outputs

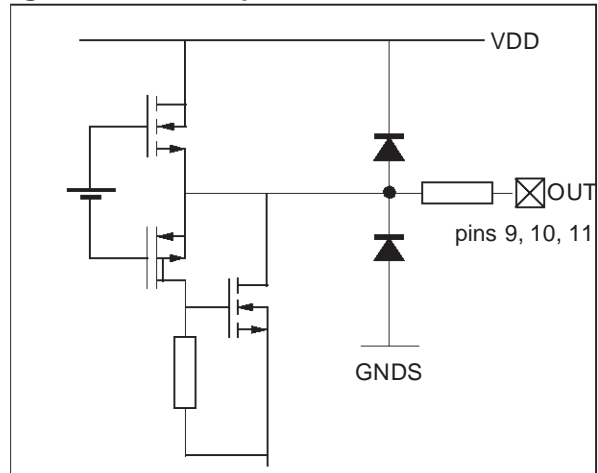


Figure 12. VDD

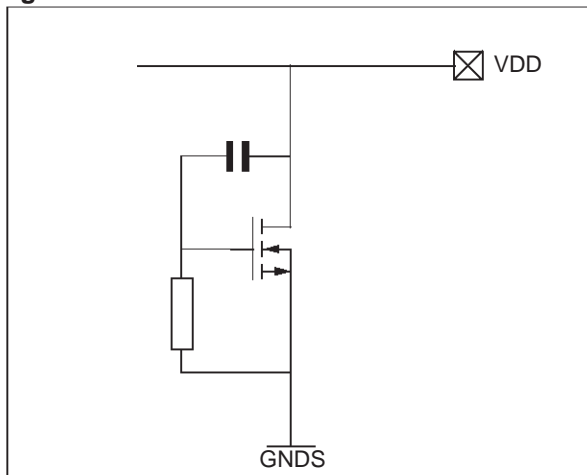


Figure 13. VCC

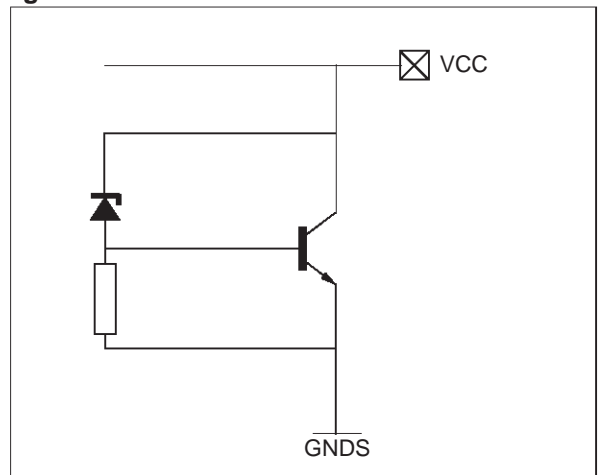


Figure 14. GNDP

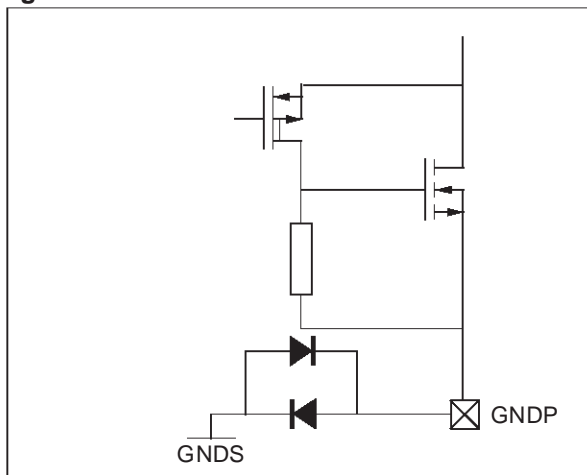
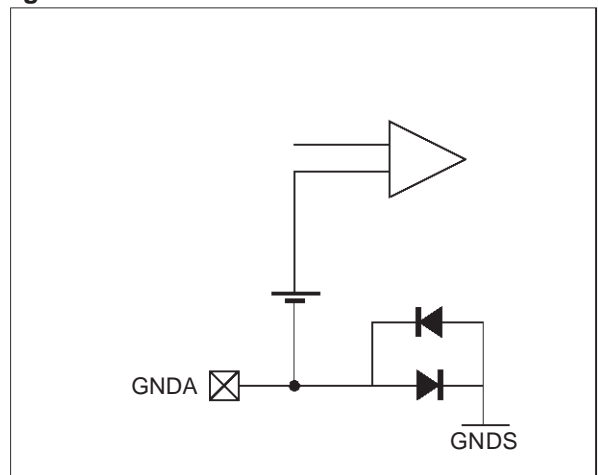


Figure 15. GNDA



10 APPLICATION HINTS

10.1 How to choose the high supply voltage value (V_{DD}) in DC coupling mode

The V_{DD} high supply voltage must be chosen carefully. It must be high enough to provide the necessary video adjustment but set to minimum value to avoid unnecessary power dissipation.

Example (see Figure 2):

The following example shows how the optimum V_{DD} voltage value is determined:

- Cut-off adjustment range (B) : 25V
- Max contrast (D) : 40V

Case 1:

10V Brightness (C) adjusted by the preamplifier :

$$V_{DD} = A + B + C + D + E$$

$$V_{DD} = 15V + 25V + 10V + 40V + 17V = 107V$$

Case 2:

10V Brightness (C) adjusted by the G1 anode:

$$V_{DD} = A + B + D + E$$

$$V_{DD} = 15V + 25V + 40V + 17V = 97V$$

10.2 Arcing Protection: schematics

As the amplifier outputs are connected to the CRT cathodes, special attention must be given to protect them against possible arcing inside the CRT.

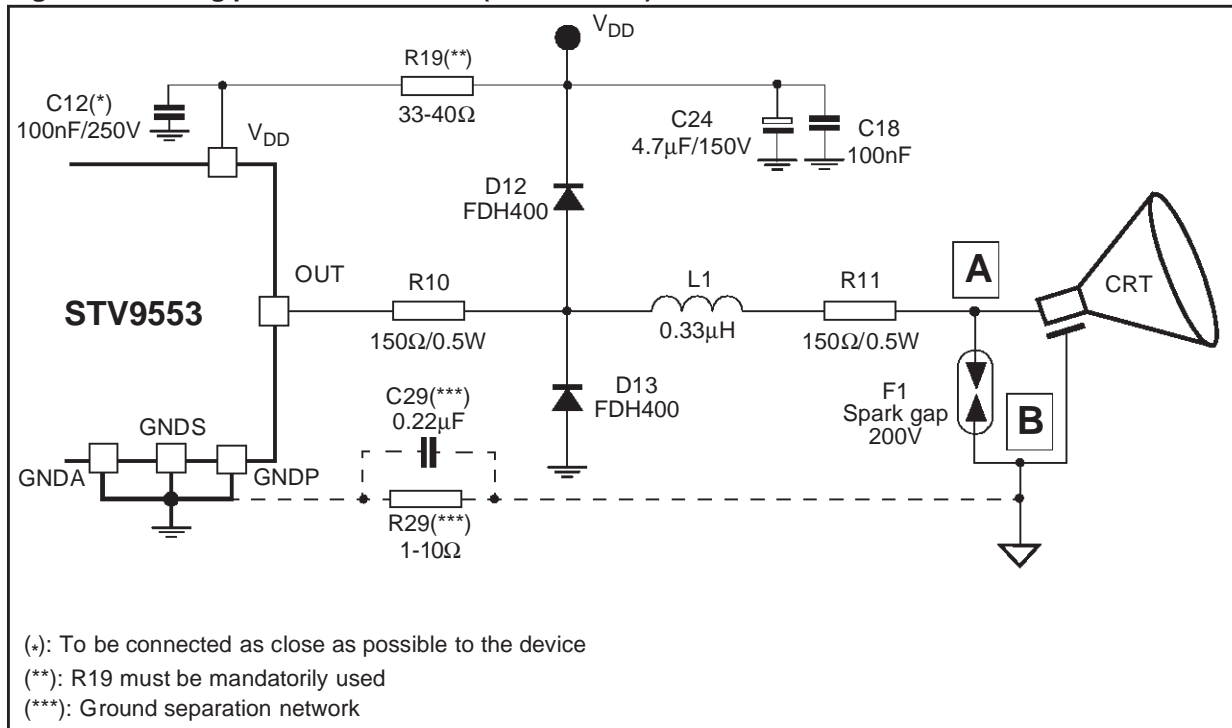
Protection must be considered when starting the design of the video CRT board. It should always be implemented before starting to adjust the dynamic video response of the system.

The arcing network that we recommend (see Figure 16) provides efficient protection without deteriorating the amplifier video performances.

The total resistance between the amplifier and the CRT cathode ($R_{10}+R_{11}$) protects the device against overvoltages. We recommend to use $R_{10}+R_{11} > 300 \Omega$.

Spark gaps are strongly recommended for arcing protection.

Figure 16. Arcing protection network (one channel)



10.3 Arcing protection: layout and decoupling

Several layout precautions have to be considered to get the optimum arcing protection:

Sparkgap grounding: when an arc occurs, the energy must flow through the CRT ground without reaching the amplifier. This is obtained by connecting the sparkgap grounding (point B) to the CRT ground (socket) via a wide/short trace. Conversely the point B must be connected to the amplifier ground via a longer/narrower trace.

Grounding separation: In order to set apart the amplifier ground and CRT ground, the R29/C29 network (Figure 16) can be used.

Amplifier grounding: The 3 grounds GNDS, GNDA and GNDP must be connected together as close as possible to the device.

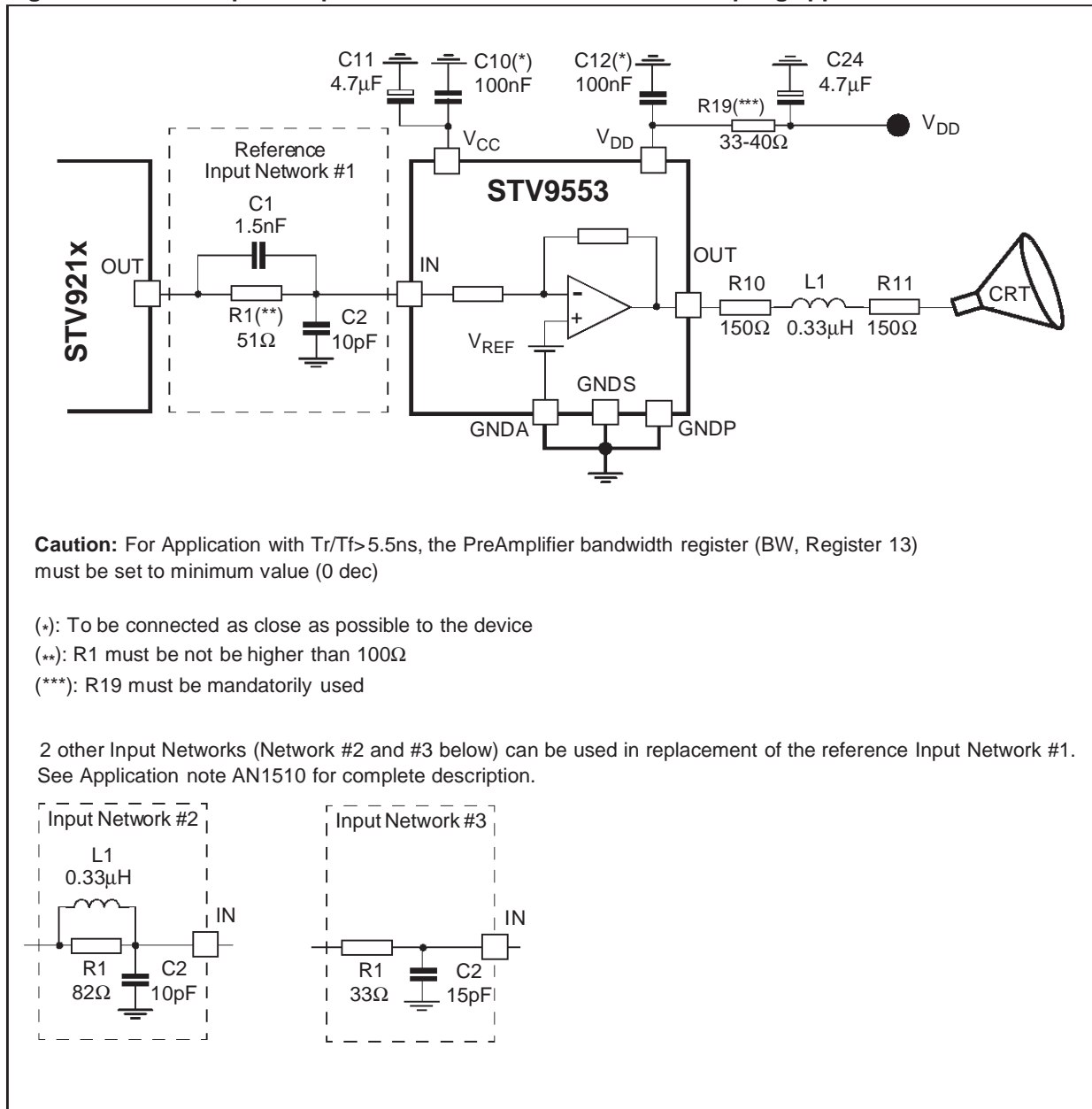
10.4 Video response optimization: schematics in DC-coupling mode

The dynamic video response is optimized by carefully designing the supply decoupling of the video board (see Section 10.7), the tracks (see Section 10.7), then by adjusting the input/output component network (see Section 10.5).

For dynamic measurements such as rise/fall time and bandwidth, a 8pF load is used (total load including the parasitic capacitance of the PC board and CRT Socket).

When used in kit with the STV921x preamplifier from ST, the preamplifier bandwidth register (BW, register 13) must be set to minimum (0 dec) for an application with $t_R/t_F > 5.5ns$.

Figure 17. Video response optimization for one channel - DC coupling application



10.5 Video response optimization: outputs networks

The output network (R10/L1/R11) is used to adjust the amplifier video performances. Once R10 and R11 resistors are set to protect the application against arcing ($R10 + R11 > 300\Omega$), it is possible to increase the bandwidth by increasing L1.

10.6 Video response optimization: inputs networks

The input network also plays an important role in the device dynamic behaviour. We recommend to use the reference input network #1, which is described in Figure 17, but 2 other networks (#2 and #3) can be used to better match the required performances and the video board layout. Refer to the application note referenced AN1510 for the complete description of these input networks.

10.7 Video response optimization: layout and decoupling

The decoupling of V_{CC} and V_{DD} through good quality HF capacitors (respectively C10 and C12) close to the device is necessary to improve the dynamic performance of the video signal.

Careful attention has to be given to the three output channels of the amplifier.

Capacitor: The parasitic capacitive load on the amplifier outputs must be as small as possible. Figure 9 from Section 8 clearly shows the deterioration of the t_R/t_F when the capacitive load increases. Reducing this capacitive load is achieved by moving away the output tracks from the other tracks (especially ground) and by using thin tracks ($< 0.5\text{mm}$), see Figure 17.

Cross talk: Output and input tracks must be set apart. The STV9553 pin-out allows the easy separation of input and output tracks on opposite sides of the amplifier (see Figure 21).

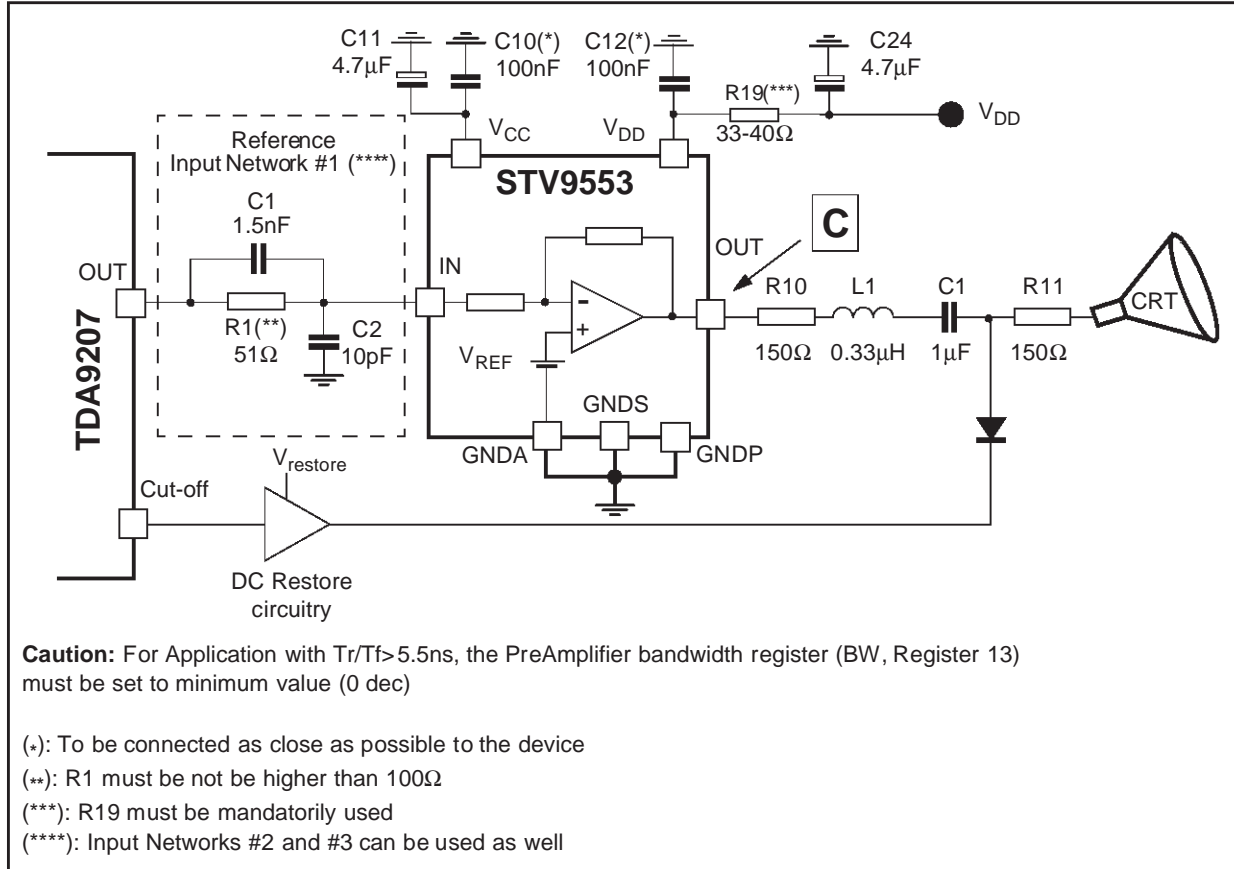
Length: Connection between amplifier output and cathode must be as short and direct as possible.

10.8 AC - Coupling mode

The STV9553 can be used in AC-Coupling mode in kit with the TDA9207/9212 preamplifier from ST. As for the DC-coupling mode, the STV9553 drives perfectly the video signal in PICTURE BOOST conditions.

A typical schematic is given on the Figure 18 below.

Figure 18. Video response optimization for one channel - AC coupling application



The advantage of such an architecture is to use smaller V_{DD} and therefore to have smaller power consumption. This is due to the fact that the STV9553 provides only the video signal and not the cut-off adjustment. The disadvantage is to have an application with more components (DC restore circuitry).

Note that it is mandatory to keep the output video signal (point C) inside the linear area of the amplifier (from 17V to $V_{DD} - 15V$).

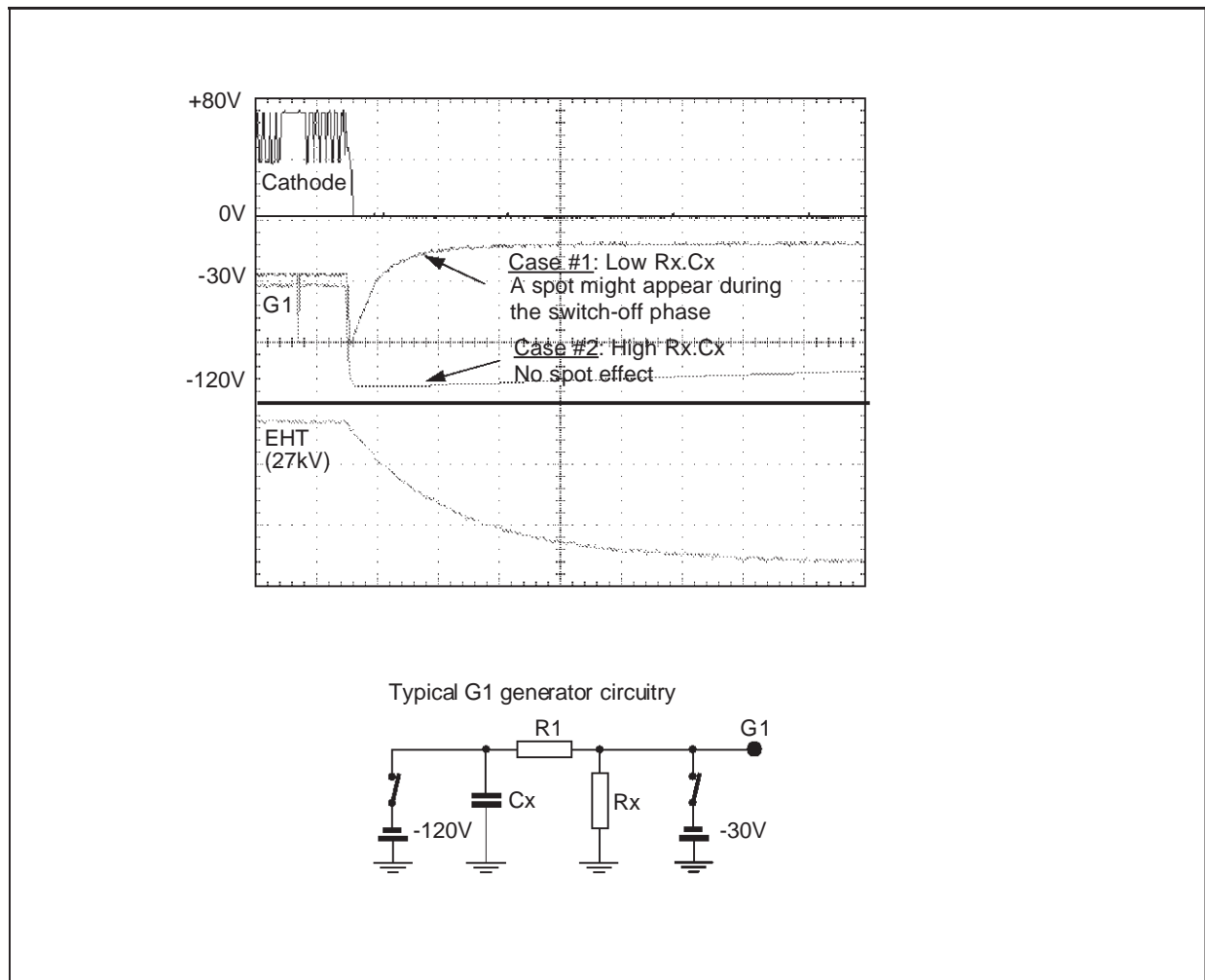
10.9 Stand-by mode, spot suppression

The usual way to set a monitor in stand-by mode is to switch-off the V_{CC} (12V).

The STV9553 has an extremely low power consumption ($I_{DD5} = 60\mu A$ when $V_{CC} < 1.5V$) in stand-by mode and the outputs are set to low level (white picture).

To avoid the display of a spot effect during the switch-off phase, it is necessary to adjust the G1 circuitry (Resistors R_x and C_x , see Figure 19) to pull the G1 voltage to low value during a sufficient time duration.

Figure 19. Stand-by mode, spot effect



10.10 Conclusion

Video response is always a compromise between several parameters. For example, the rise/fall time improvement leads to the overshoot deterioration.

The recommended way to optimize the video response is:

- 1 To set R10+R11 for arcing protection (min. 300 Ω)
2. To adjust R20 and R10+R11.
Increasing their value increases the t_R/t_F values and decrease the overshoot
3. To adjust L1
Increasing L1 speeds up the device but increases the overshoot.
4. To adjust the input network for the final dynamic tuning (e.g.: critical damping)

We recommend our customers to use the schematic shown on Figure 23 as a starting point for the video board and then to apply the optimization they need.

Figure 20. STV9553/9555/9556 + TDA9210/STV9211 + STV9936 S/P
DC-coupling demonstration board: Silk Screen and Trace

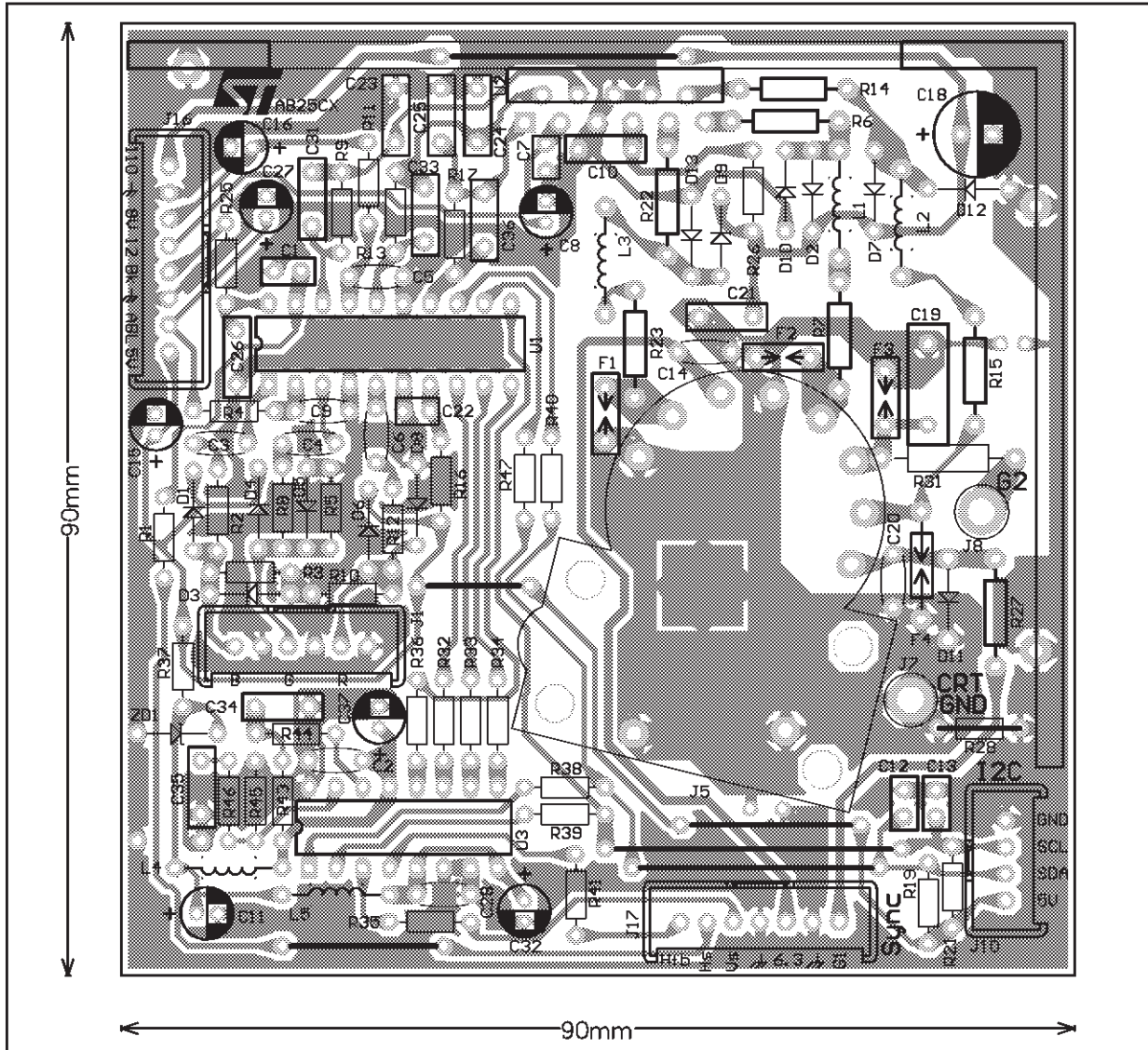


Figure 21. Outputs trace (from figure 19)

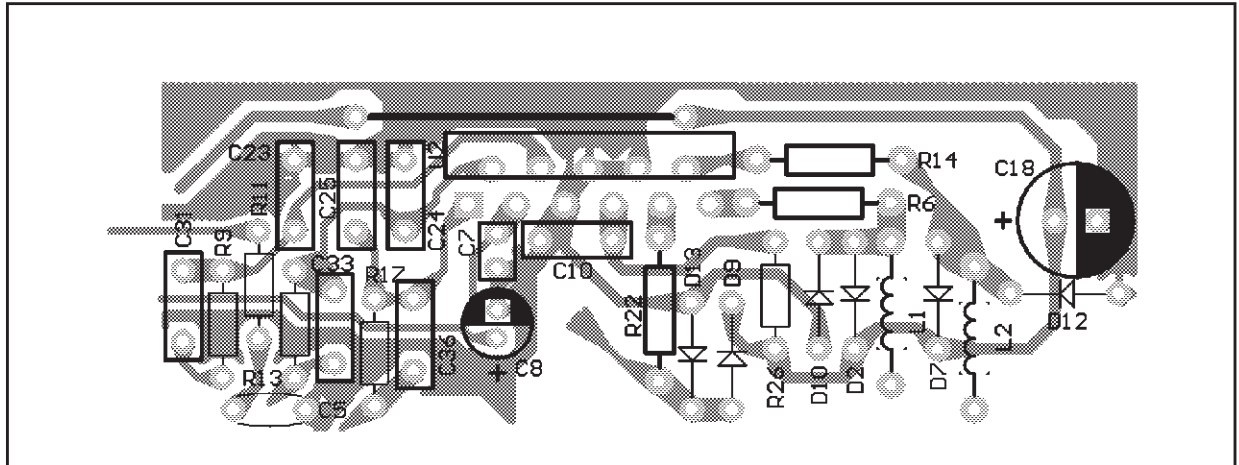


Figure 22. CRT socket trace (from figure 19)

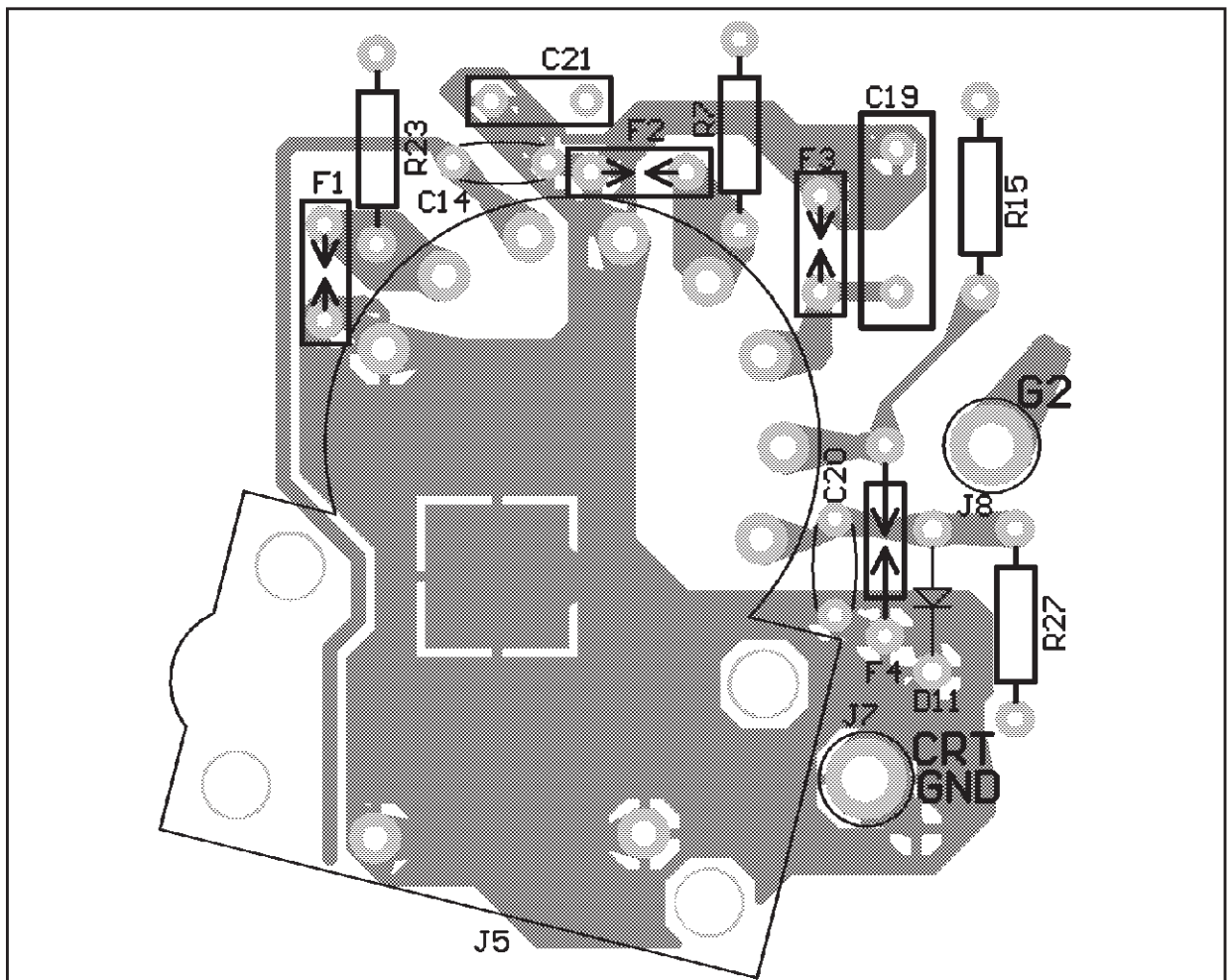
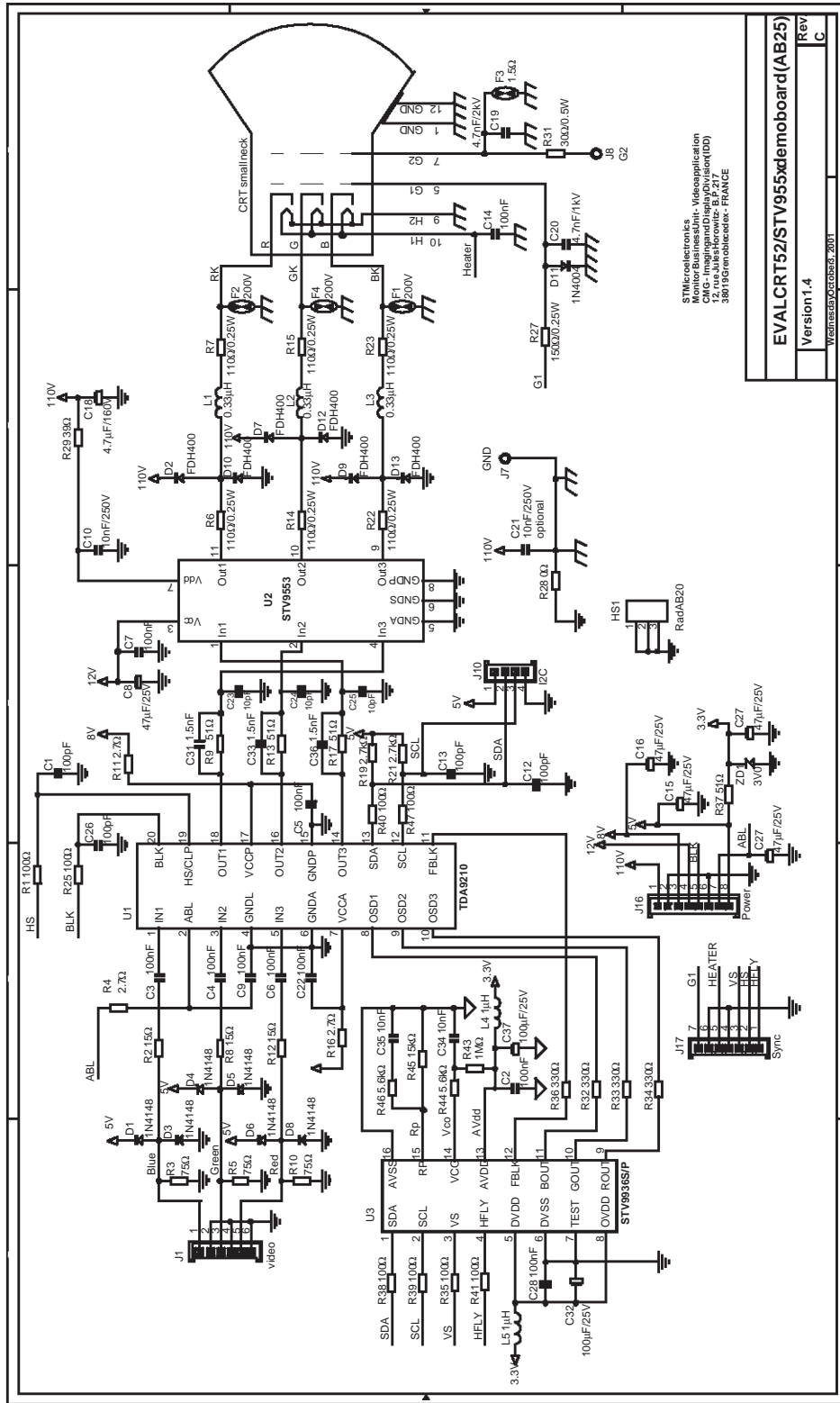
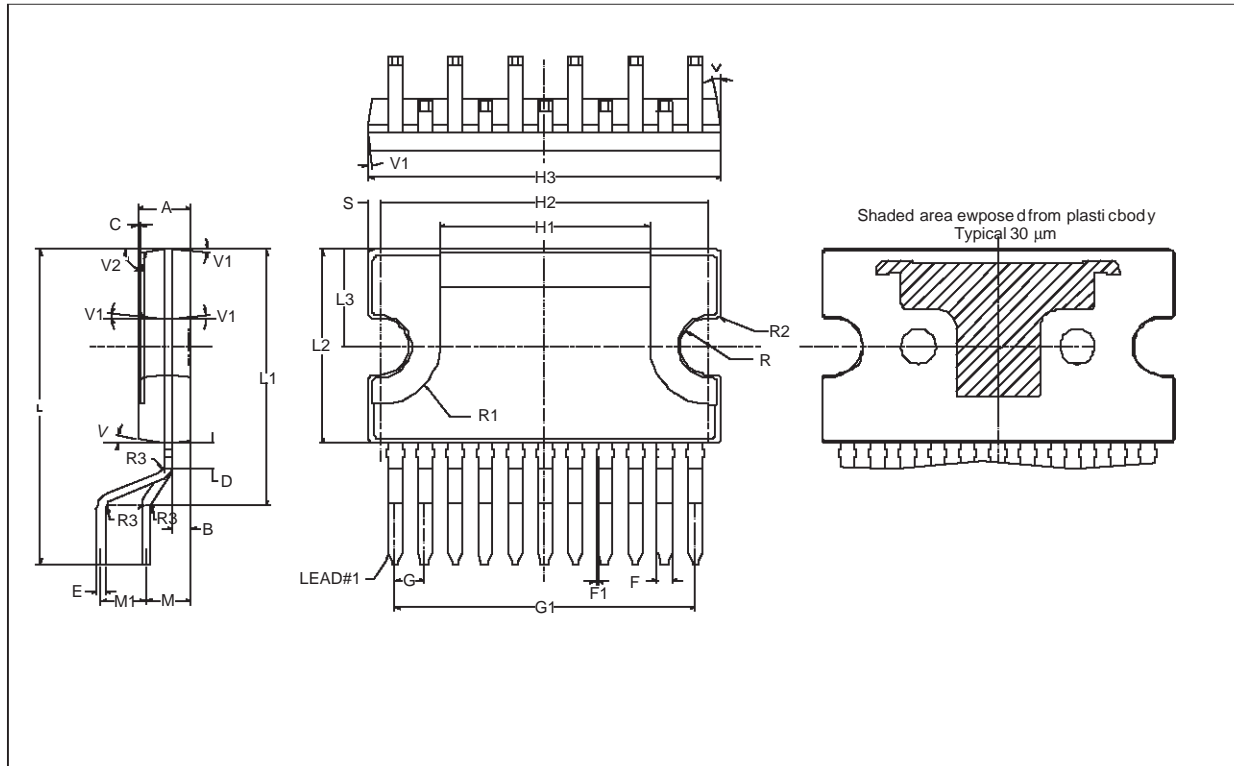


Figure 23. STV9553/55/56 + STV9936 + TDA9210/STV9211 DC-coupling demo - board schematic



11 PACKAGE MECHANICAL DATA

11 PIN - CLIPWATT



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.95	3	3.05	0.116	0.118	0.12
B	0.95	1	1.05	0.037	0.039	0.041
C	-	0.15	-	-	0.006	-
D	1.3	1.5	1.7	0.051	0.059	0.061
E	0.49	0.515	0.55	0.0019	0.02	0.021
F	0.78	0.8	0.86	0.03	0.031	0.034
F1	-	0.05	0.1	-	0.002	0.004 (6)
G	1.6	1.7	1.8	0.063	0.067	0.071
G1	16.9	17	17.1	0.665	0.669	0.673
H1	-	12	-	-	0.472	-
H2	18.55	18.6	18.65	0.73	0.732	0.734
H3	19.9	20	20.1	0.783	0.787	0.791 (5)
L	17.7	17.9	18.1	0.696	0.704	0.712
L1	14.35	14.55	14.65	0.564	0.572	0.576
L2	10.9	11	11.1	0.429	0.433	0.437(5)
L3	5.4	5.5	5.6	0.212	0.216	0.22
M	2.34	2.54	2.74	0.092	0.1	0.107
M1	2.34	2.54	2.74	0.092	0.1	0.107
R	1.45	-	-	0.057	-	-

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R1	3.2	3.3	3.4	0.126	0.13	0.134
R2	-	0.3	-	-	0.012	-
R3	-	0.5	-	-	0.019	-
S	0.65	0.7	0.75	0.025	0.027	0.029
V		10deg.			10deg.	
V1		5deg.			5deg.	
V2		75deg.			75deg.	

Note 5: "H3 and L2" do not include mold flash or protrusions
Mold flash or protrusions shall not exceed 0.15mm per side.

Note 6: No intrusions allowed inwards the leads

Critical dimensions:

Lead split (M1)

Total length (L)

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