STV300NH02L

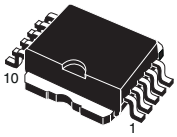
N-channel 24V - 0.8mΩ - 280A - PowerSO-10 STripFET™ Power MOSFET

PRELIMINARY DATA

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STV300NH02L	24V	0.001Ω	280A

- $R_{DS(on)}$*Q_g industry's benchmark
- Conduction losses reduced
- Low profile, very low parasitic inductance
- Switching losses reduced



PowerSO-10

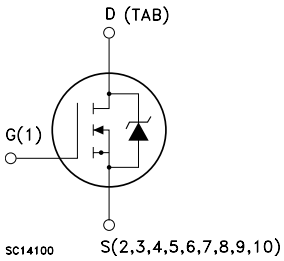
Description

This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for high current OR-ing application.

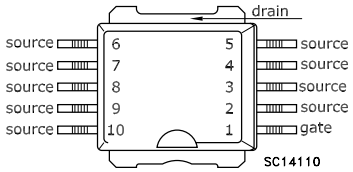
Applications

- Switching application
  - OR-ing
  - Specially designed and optimized for high efficiency DC/DC converters.

Internal schematic diagram



Connection diagram (top view)



Order code

Part number	Marking	Package	Packaging
STV300NH02L	V300NH02L	PowerSO-10	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	24	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	280	A
I_D (1)	Drain current (continuous) at T_C = 100°C	200	A
I_{DM} (2)	Drain current (pulsed)	1120	A
P_{TOT} (3)	Total dissipation at T_C = 25°C	300	W
	Derating factor	2	W/°C
E_{AS} (4)	Single pulse avalanche energy	2296	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

1. This value is limited by package
2. Pulse with limited by safe operating area
3. This value is rated according to Rthj-c
4. Starting Tj = 25°C, I_D = 60A, V_{DD} = 20V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.5	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	24			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, T_c=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{DS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	1	1.5	2	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 80A		0.8	1	mΩ
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 80A @100°C		1.1		mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 15V, f = 1 MHz, V_{GS} =0		7055 3251 307		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 12V, I_D= 120A, V_{GS}= 10V *(see Figure 2)*		109.4 30.2 26.4		nC nC nC
R_G	Gate input resistance	V_{DS} = 0V, f = 1 MHz, V_{GS} =0		4.4		Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 12V, I_D = 60A R_G= 4.7Ω, V_{GS}= 10V, *(see Figure 1)*		18 275		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 12V, I_D = 60A R_G= 4.7Ω, V_{GS}= 10V, *(see Figure 1)*		138 94.4		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				300 1200	A A
V_{SD} (1)	Forward on voltage	I_{SD} = 120A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120A,di/dt = 100A/µs V_{DD} = 20V, T_j = 25°C *(see Figure 6)*		63 85 2.7		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120A,di/dt = 100A/µs V_{DD} = 20V, T_j = 150°C *(see Figure 6)*		63.2 88 2.8		ns nC A

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 1. Switching times test circuit for resistive load

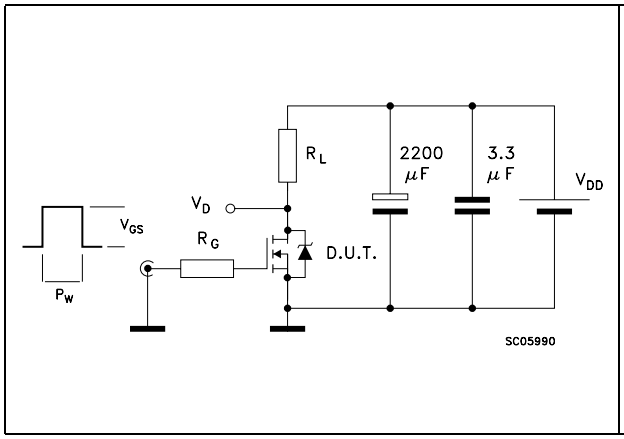


Figure 2. Gate charge test circuit

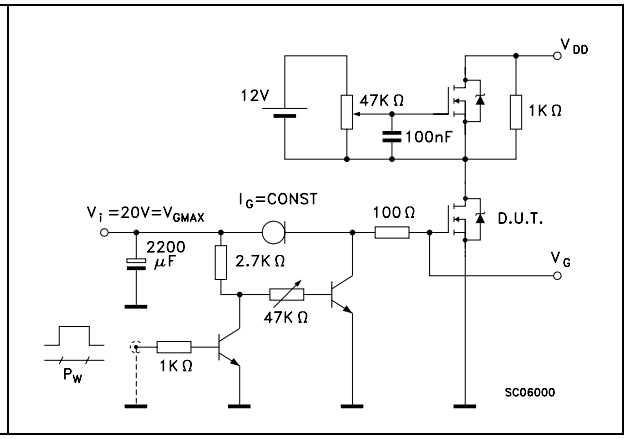


Figure 3. Test circuit for inductive load switching and diode recovery times

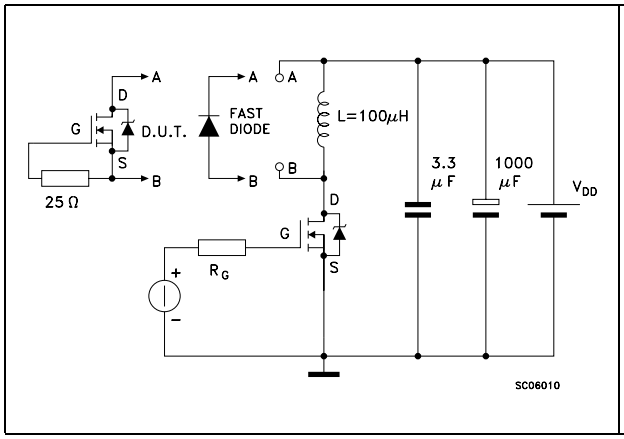


Figure 4. Unclamped inductive load test circuit

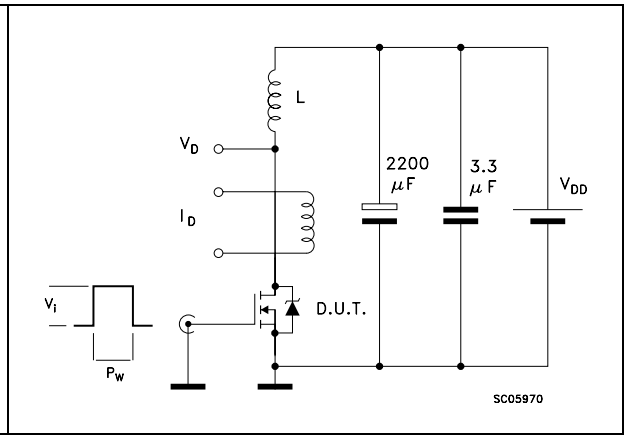


Figure 5. Unclamped inductive waveform

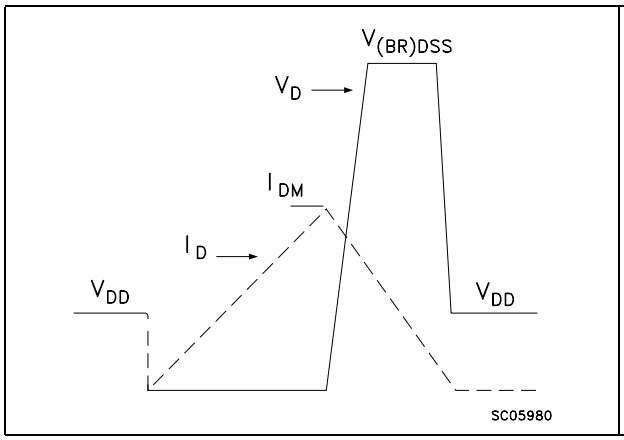
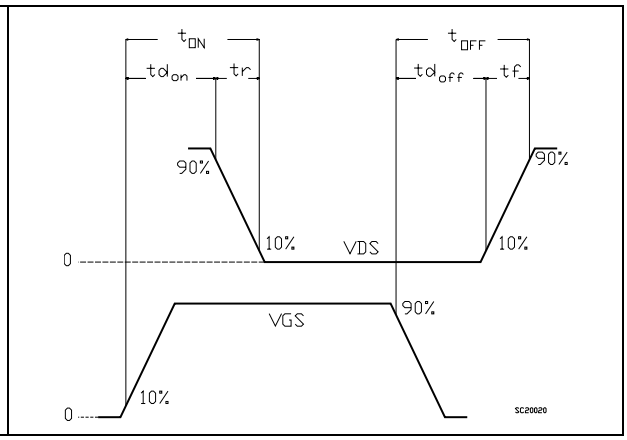


Figure 6. Switching time waveform

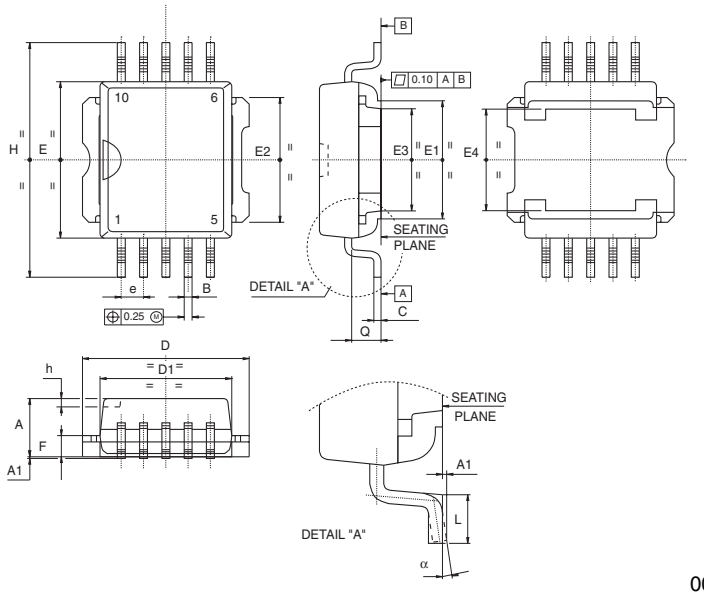


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



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5 Revision history

Table 7. Revision history

Date	Revision	Changes
08-Feb-2007	1	First release

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