

P-channel -30 V, 12 mΩ typ., -9 A, STripFET™ H6 Power MOSFET in an SO-8 package

Datasheet - production data

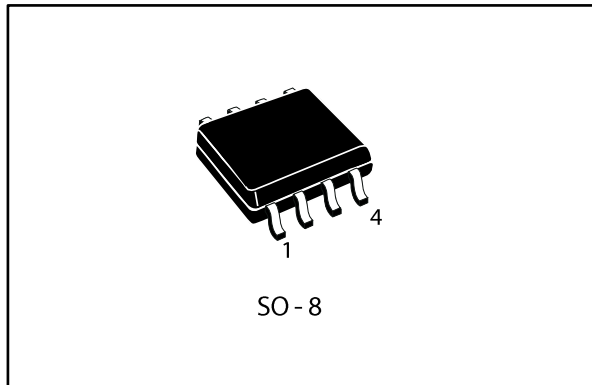


Figure 1: Internal schematic diagram

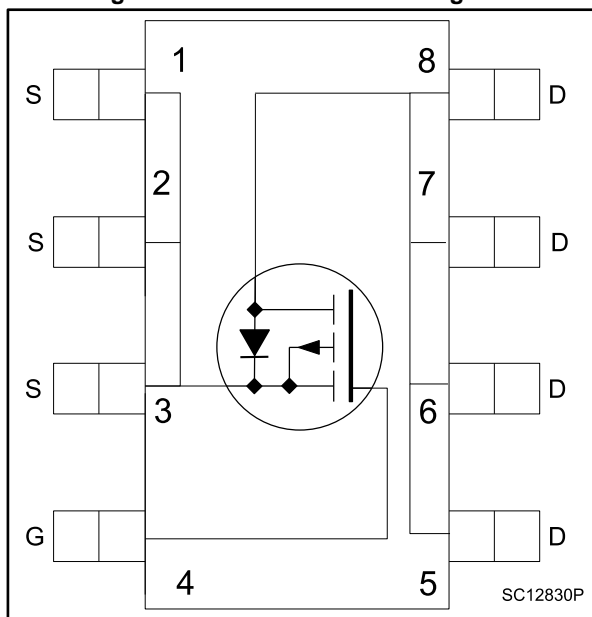


Table 1: Device summary

Order code	Marking	Packages	Packing
STS9P3LLH6	9K3L	SO-8	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STS9P3LLH6	-30 V	15 mΩ	-9 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{amb} = 25^\circ\text{C}$	-9	A
	Drain current (continuous) at $T_{amb} = 100^\circ\text{C}$	-5.6	
$I_{DM}^{(2)}$	Drain current (pulsed)	-36	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{amb} = 25^\circ\text{C}$	2.7	W
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾This value is rated according to $R_{thj-amb}$

⁽²⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	47	$^\circ\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10$ s

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -1\text{ mA}$	-30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = -30\text{ V}$			-1	μA
		$V_{DS} = -30\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			-10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			-100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1		-2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\text{ V}$, $I_D = -4.5\text{ A}$		12	15	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -4.5\text{ A}$		18	22.5	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2615	-	pF
C_{OSS}	Output capacitance		-	340	-	pF
C_{RSS}	Reverse transfer capacitance		-	235	-	pF
Q_g	Total gate charge	$V_{DD} = -15\text{ V}$, $I_D = -9\text{ A}$ $V_{GS} = -4.5\text{ V}$	-	24	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -15\text{ V}$, $I_D = -4.5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = -10\text{ V}$	-	13.2	-	ns
t_r	Rise time		-	93	-	ns
$t_{d(off)}$	Turn-off delay time		-	50	-	ns
t_f	Fall time		-	18	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = -4.5 \text{ A}$, $V_{GS} = 0$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -4.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = -24 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	20		ns
Q_{rr}	Reverse recovery charge		-	16		nC
I_{RRM}	Reverse recovery current		-	-1.6		A

Notes:

⁽¹⁾Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

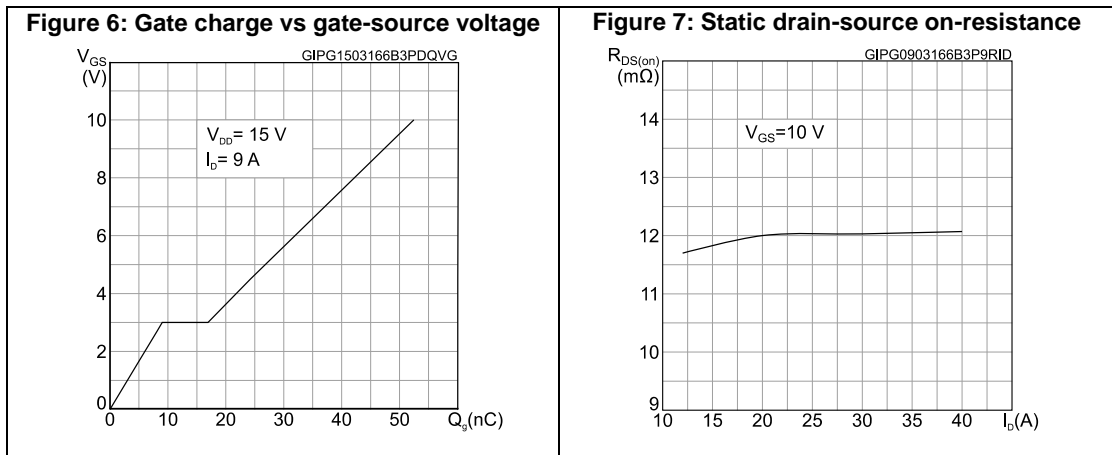
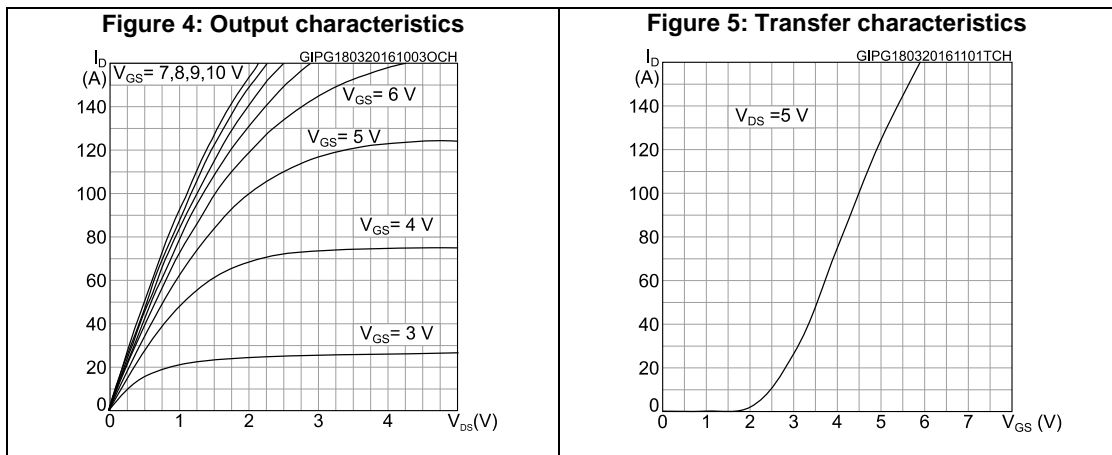
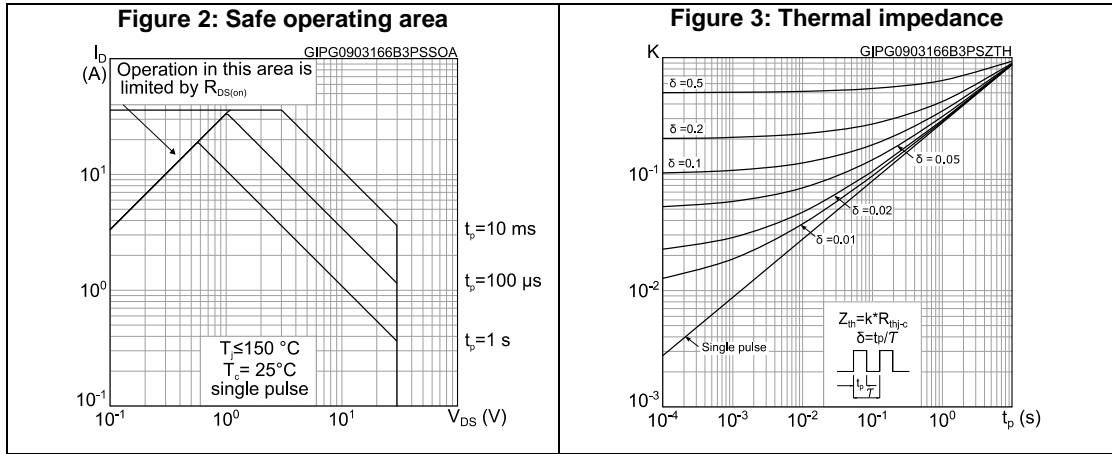


Figure 8: Capacitance variations

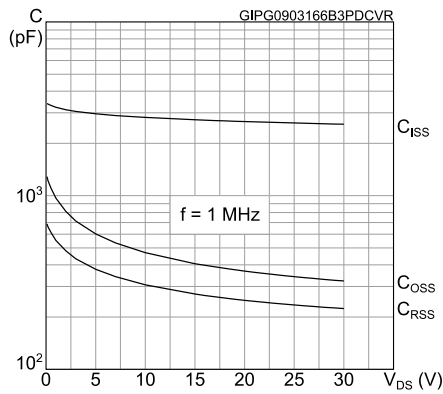


Figure 9: Normalized gate threshold voltage vs temperature

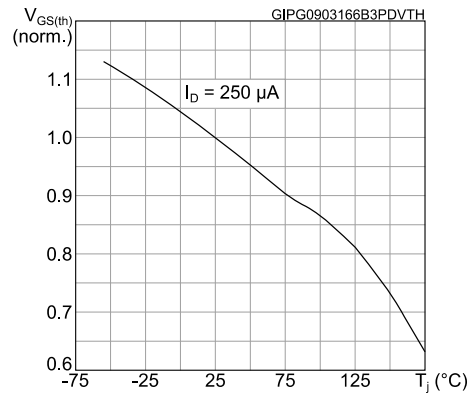


Figure 10: Normalized on-resistance vs temperature

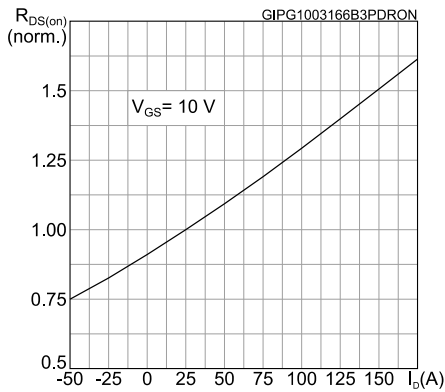


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

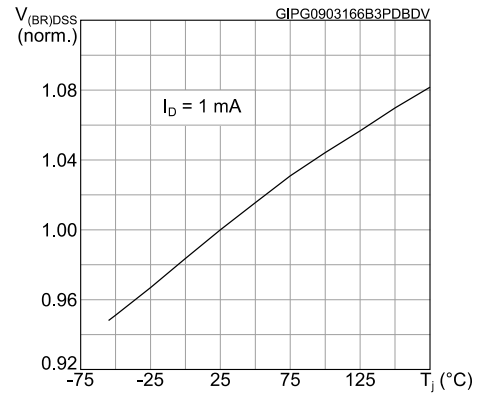
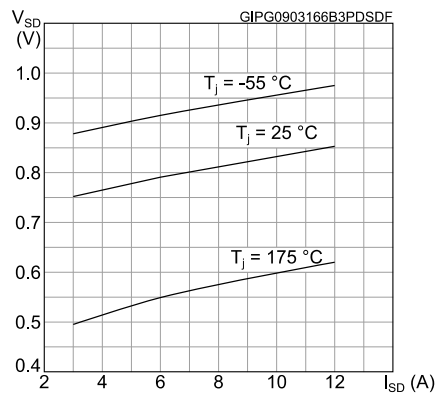


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

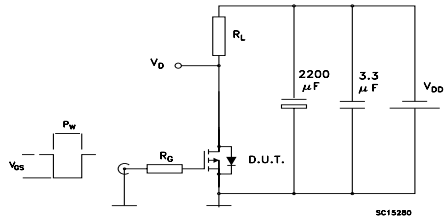


Figure 14: Gate charge test circuit

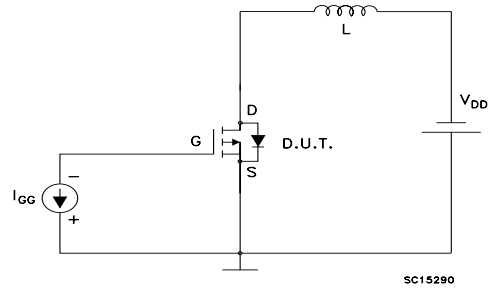
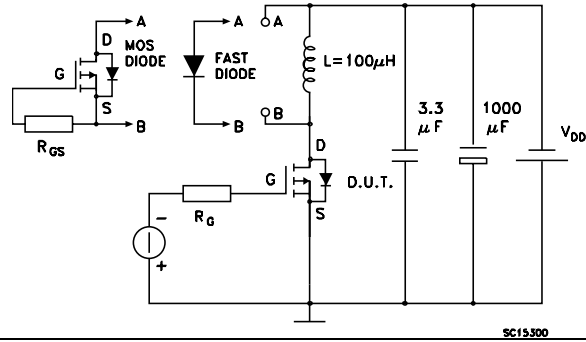


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SO-8 package information

Figure 16: SO-8 package outline

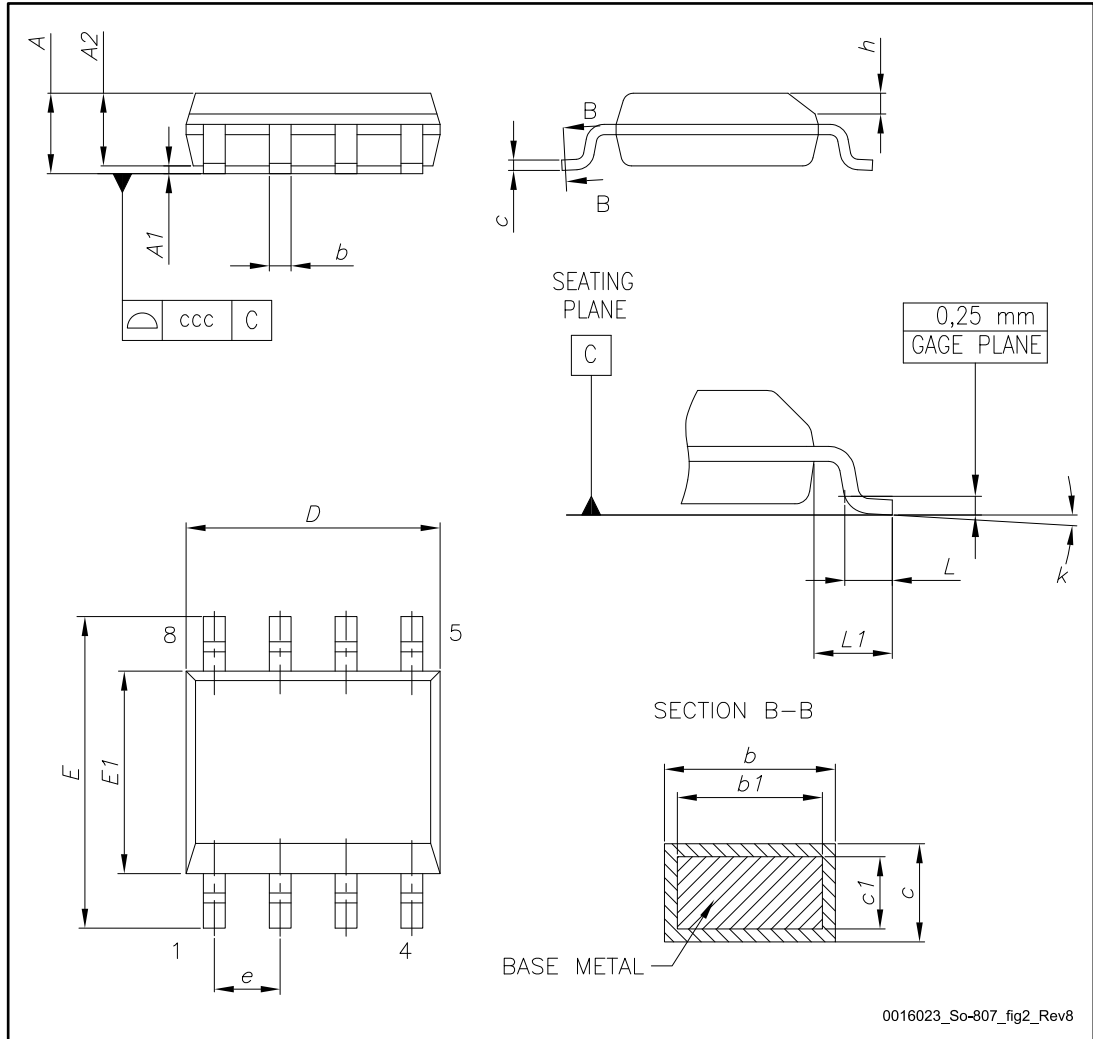
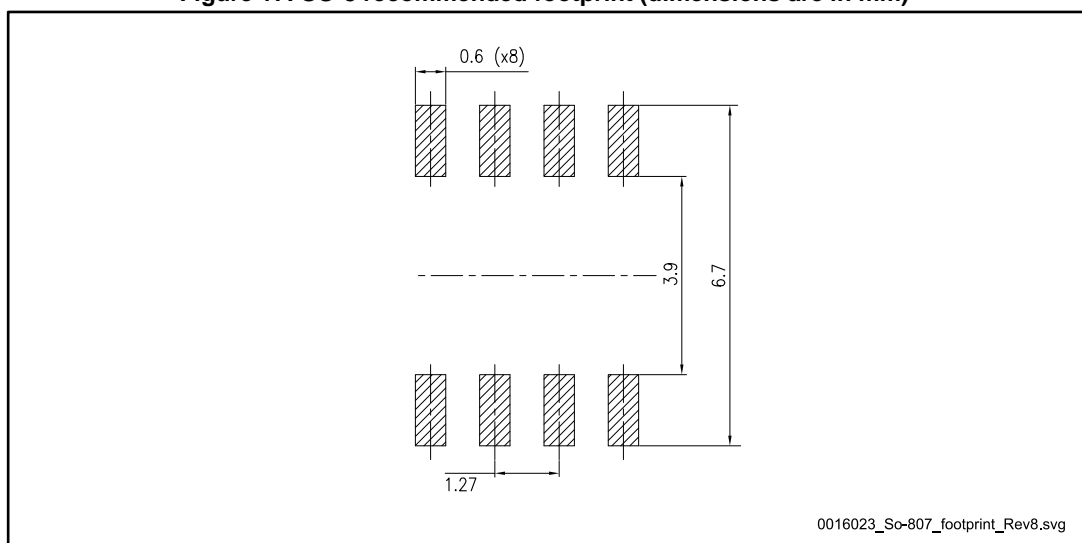


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17: SO-8 recommended footprint (dimensions are in mm)



4.2 SO-8 packing information

Figure 18: SO-8 tape and reel dimensions

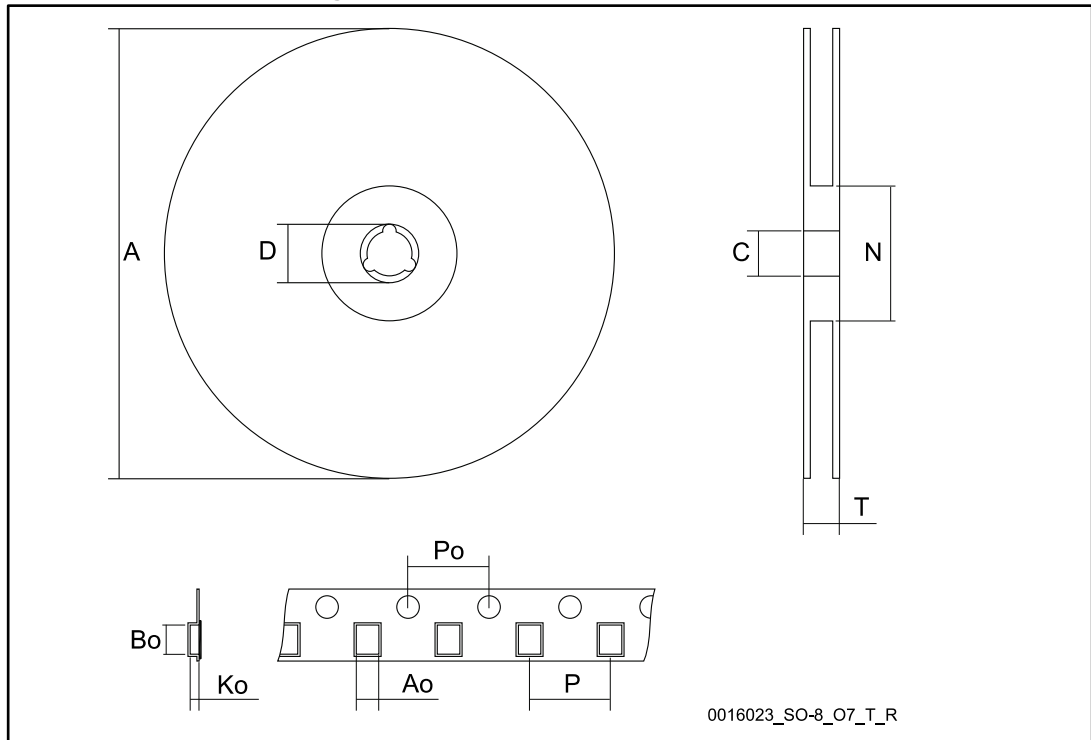


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
22-Jan-2014	1	Initial release.
15-Mar-2016	2	Modified: title and $R_{DS(on)}$ max value in cover page Modified: Table 4: "On/off states" , Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source drain diode" Minor text changes.

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