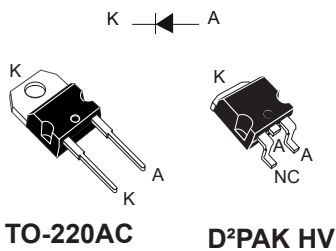


650 V, 10 A low V_F power Schottky silicon carbide diode



Features

- No or negligible reverse recovery
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- Operating T_j from -40 °C to 175 °C
- D²PAK HV creepage distance (anode to cathode) = 5.38 mm min.
- **ECOPACK2** compliant component

Applications

- DC/DC converter
- High frequency inverter
- Snubber
- Boost PFC function

Description

This 10 A, 650 V SiC diode is an ultra high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Housed in D²PAK HV, this diode is perfectly suited for a usage in PFC applications, in charging station, DC/DC, easing the compliance to IEC-60664-1.

Product label



Product status link

[STPSC10065](#)

Product summary

Symbol	Value
$I_{F(AV)}$	10 A
V_{RRM}	650 V
T_j (max.)	175 °C
V_F (typ.)	1.30 V

1 Characteristics

Table 1. Absolute ratings (limiting values at 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		650	V
$I_{F(RMS)}$	Forward rms current		22	A
$I_{F(AV)}$	Average forward current	$T_C = 150\text{ °C}$, DC current ⁽¹⁾	10	A
I_{FRM}	Repetitive peak forward current	$T_C = 150\text{ °C}$, $T_j = 175\text{ °C}$, $\delta = 0.1$	42	A
I_{FSM}	Surge non repetitive forward current	$t_p = 10\text{ ms}$ sinusoidal, $T_C = 25\text{ °C}$	48	A
		$t_p = 10\text{ ms}$ sinusoidal, $T_C = 125\text{ °C}$	39	
		$t_p = 10\text{ }\mu\text{s}$ square, $T_C = 25\text{ °C}$	210	
T_{stg}	Storage temperature range		-65 to +175	°C
T_j	Operating junction temperature		-40 to +175	°C

1. Value based on $R_{th(j-c)}$ max.

Table 2. Thermal parameters

Symbol	Parameter	Value		Unit
		Typ.	Max.	
$R_{th(j-c)}$	Junction to case	1.0	1.5	°C/W

For more information, please refer to the following application note:

- AN5088: Rectifiers thermal management, handling and mounting recommendations

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R ⁽¹⁾	Reverse leakage current	$T_j = 25\text{ °C}$	$V_R = V_{RRM}$	-	7	130	μA
		$T_j = 150\text{ °C}$		-	53	900	
V_F ⁽²⁾	Forward voltage drop	$T_j = 25\text{ °C}$	$I_F = 10\text{ A}$	-	1.30	1.45	V
		$T_j = 150\text{ °C}$		-	1.45	1.65	
		$T_j = 175\text{ °C}$		-	1.50		

1. Pulse test: $t_p = 5\text{ ms}$, $\delta < 2\%$

2. Pulse test: $t_p = 500\text{ }\mu\text{s}$, $\delta < 2\%$

To evaluate the conduction losses, use the following equation:

$$P = 0.97 \times I_{F(AV)} + 0.068 \times I_F^2 \text{ (RMS)}$$

For more information, please refer to the following application notes related to the power losses :

- AN604: Calculation of conduction losses in a power rectifier
- AN4021: Calculation of reverse losses on a power diode

Table 4. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Typ.	Unit
$Q_{Cj}^{(1)}$	Total capacitive charge	$V_R = 400 \text{ V}$	34	nC
C_j	Total capacitance	$V_R = 0 \text{ V}, T_c = 25 \text{ }^\circ\text{C}, F = 1 \text{ MHz}$	670	pF
		$V_R = 400 \text{ V}, T_c = 25 \text{ }^\circ\text{C}, F = 1 \text{ MHz}$	55	

1. Most accurate value for the capacitive charge: $Q_{Cj}(V_R) = \int_0^{V_R} C_j(V) dV$

1.1 Characteristics (curves)

Figure 1. Forward voltage drop versus forward current (typical values)

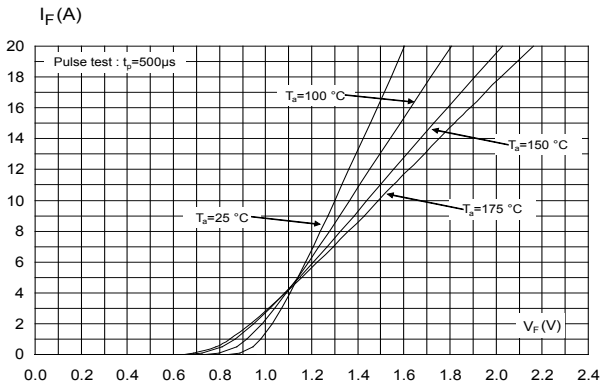


Figure 2. Reverse leakage current versus reverse voltage applied (typical values)

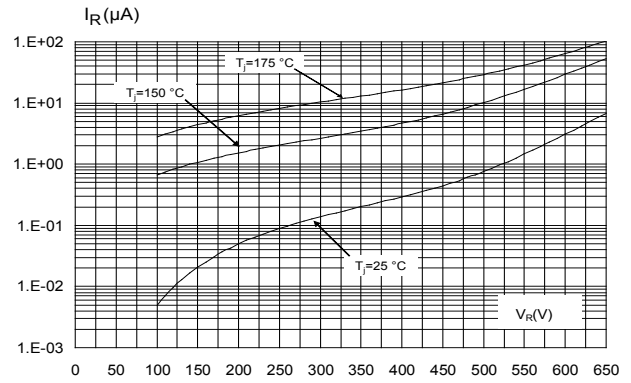


Figure 3. Peak forward current versus case temperature

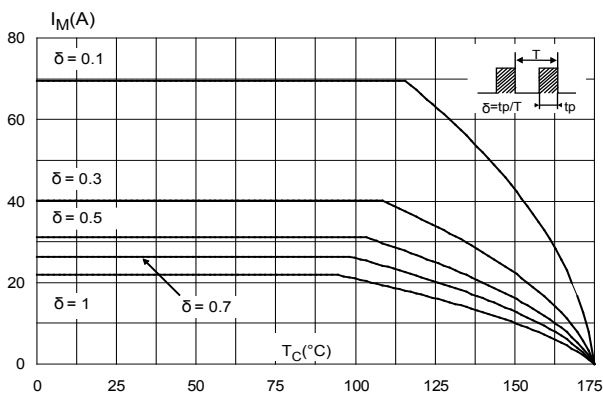


Figure 4. Junction capacitance versus reverse voltage applied (typical values)

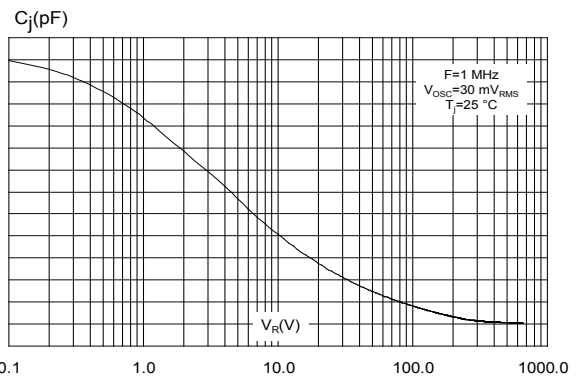


Figure 5. Relative variation of thermal impedance junction to case versus pulse duration

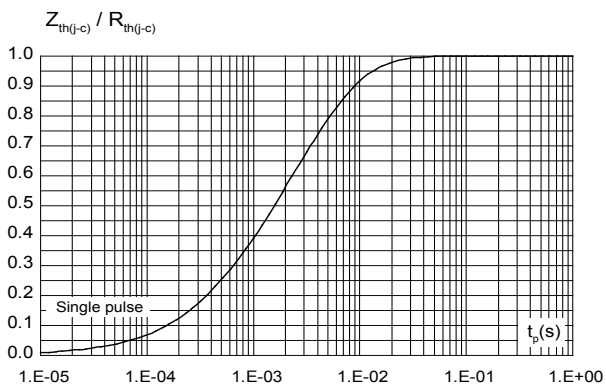


Figure 6. Non-repetitive peak surge forward current versus pulse duration (sinusoidal waveform)

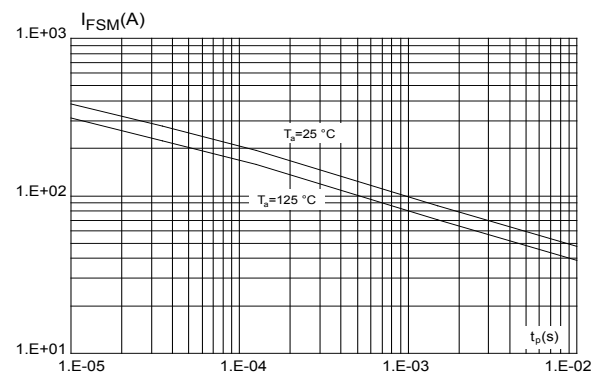


Figure 7. Total capacitive charges versus reverse voltage applied (typical values)

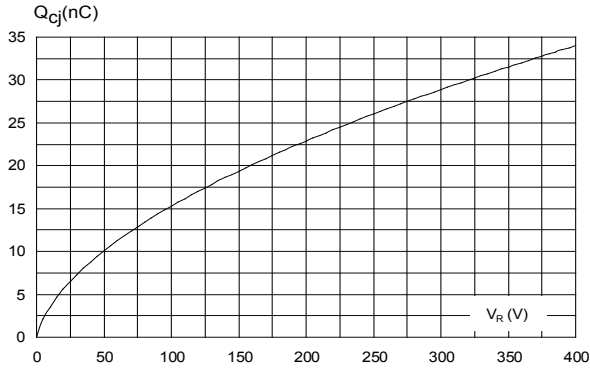
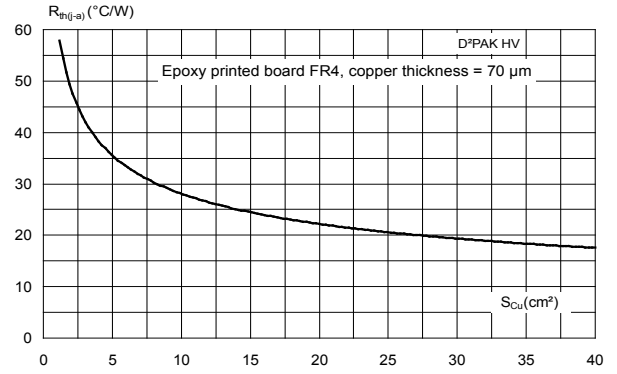


Figure 8. Thermal resistance junction to ambient versus copper surface under tab (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 TO-220AC package information

- Epoxy meets UL 94,V0
- Cooling method: by conduction (C)
- Recommended torque value: 0.55 N·m
- Maximum torque value: 0.70 N·m

Figure 9. TO-220AC package outline

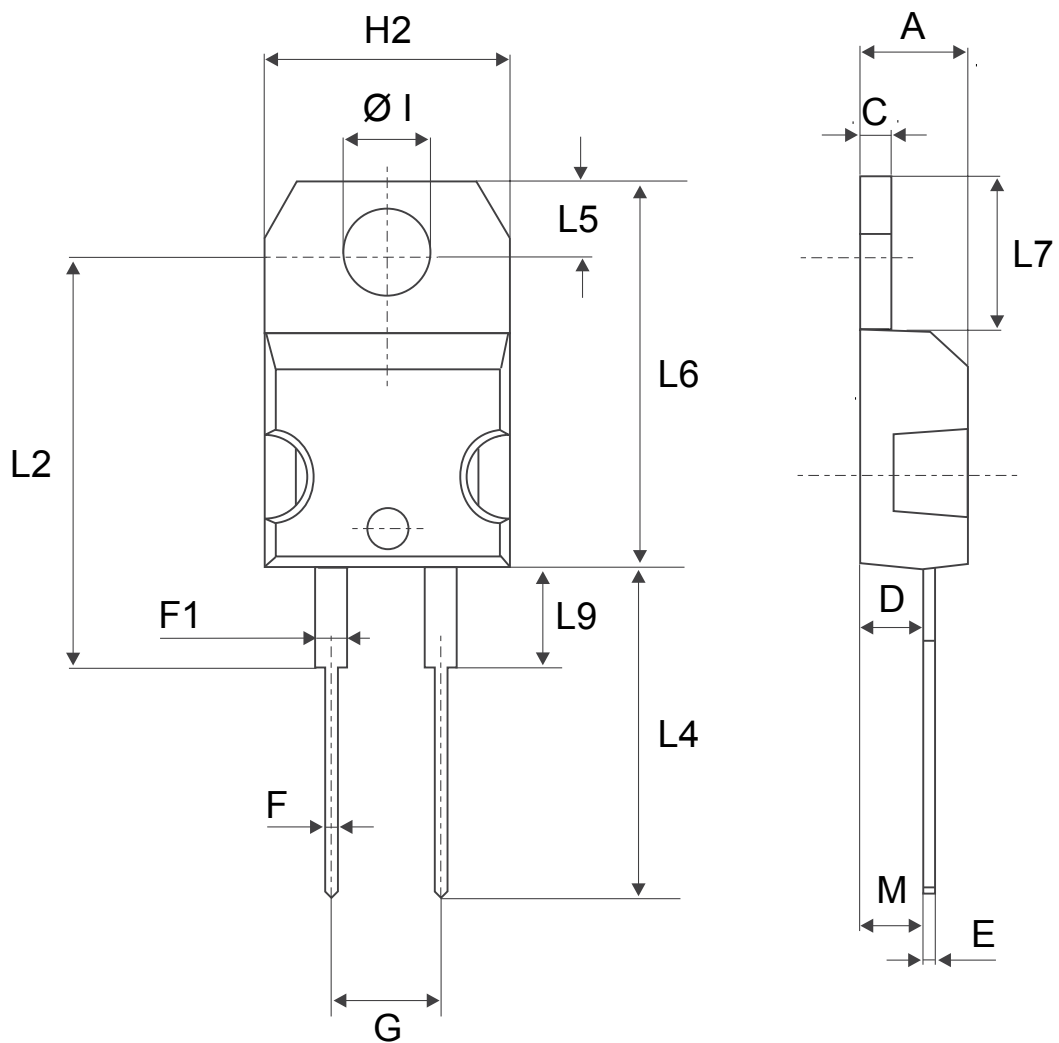


Table 5. TO-220AC package mechanical data

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
C	1.23	1.32	0.048	0.051
D	2.40	2.72	0.094	0.107
E	0.49	0.70	0.019	0.027
F	0.61	0.88	0.024	0.034
F1	1.14	1.70	0.044	0.066
G	4.95	5.15	0.194	0.202
H2	10.00	10.40	0.393	0.409
L2	16.40 typ.		0.645 typ.	
L4	13.00	14.00	0.511	0.551
L5	2.65	2.95	0.104	0.116
L6	15.25	15.75	0.600	0.620
L7	6.20	6.60	0.244	0.259
L9	3.50	3.93	0.137	0.154
M	2.6 typ.		0.102 typ.	
ØI	3.75	3.85	0.147	0.151

2.2 D²PAK high voltage package information

- Epoxy meets UL94, V0

Figure 10. D²PAK high voltage package outline

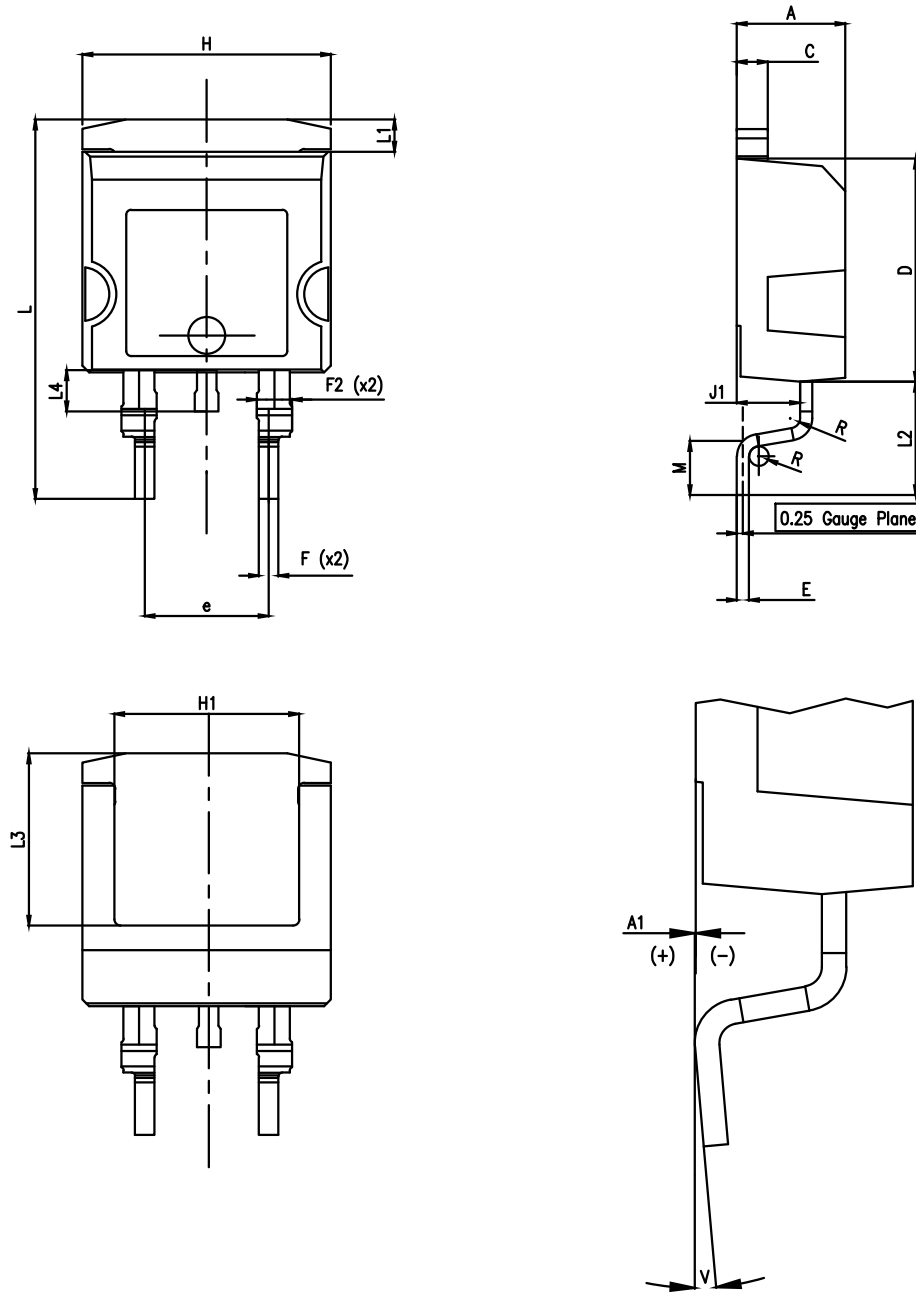
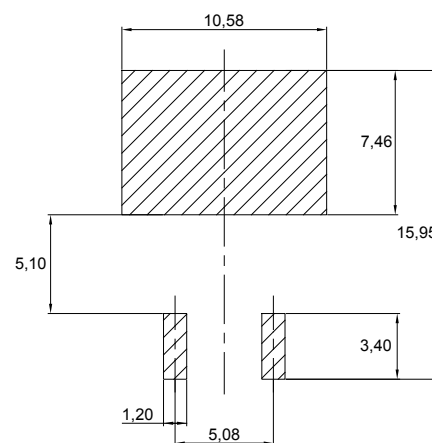


Table 6. D²PAK high voltage package mechanical data

Ref.	Dimensions		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03	-	0.20
C	1.17	-	1.37
D	8.95	-	9.35
e	4.98	-	5.18
E	0.50	-	0.90
F	0.78	- </td <td>0.85</td>	0.85
F2	1.14	-	1.70
H	10.00	-	10.40
H1	7.40	-	7.80
J1	2.49	-	2.69
L	15.30	-	15.80
L1	1.27	-	1.40
L2	4.93	-	5.23
L3	6.85	-	7.25
L4	1.5	-	1.7
M	2.6	-	2.9
R	0.20	-	0.60
V	0°	-	8°

Figure 11. D²PAK high voltage footprint in mm



Note: For package and tape orientation, reel and inner box dimensions and tape outline please check TN1173.

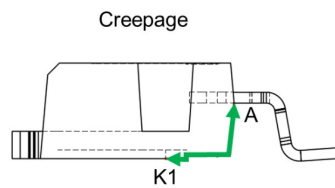
2.2.1 Creepage distance between anode and cathode

Table 7. Creepage distance between anode and cathode

Symbol	Parameter		Value	Unit
Cd _{A-K1}	Minimum creepage distance between A and K1 (with top coating)	D ² PAK HV	5.38	mm
Cd _{A-K2}	Minimum creepage distance between A and K2 (without top coating)		3.48	

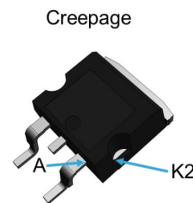
Note: D²PAK HV creepage distance (anode to cathode) = 5.38 mm min. (refer to IEC 60664-1)

Figure 12. Creepage with top coating



Minimum distance between A & K1 = 5.38 mm (with top coating)

Figure 13. Creepage without top coating



Minimum distance between A & K2 = 3.48 mm (without top coating)

3 Ordering information

Table 8. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STPSC10065D	PSC10065D	TO-220AC	1.86 g	50	Tube
STPSC10065G2-TR	PSC10065G2	D ² PAK HV	1.48 g	1000	Tape and reel

Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Jun-2017	1	First issue.
18-Jul-2017	2	Updated Table 3. Static electrical characteristics.
23-Mar-2021	3	Inserted STPOWER logo and product label "ST Sustainable". Added D ² PAK HV package information. Minor text changes.

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