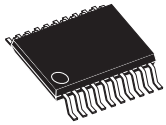
STPMC1

Programmable poly-phase energy calculator IC

Datasheet – production data

Features

- Supports 1-, 2- or 3-phase WYE and Delta services, from 2 to 4 wires
- Computes cumulative active and reactive wide-band and fundamental harmonic energies
- Computes active and reactive energies, RMS and momentary voltage and current values for each phase
- Supports Rogowski coil, current transformer, Shunt or Hall current sensors
- Exclusive ripple-free energy calculation algorithm
- Programmable pulsed output
- Stepper motor outputs
- Neutral current, temperature, and magnetic field monitoring
- OTP memory for configuration and calibration
- SPI interface
- Supports IEC 62052-11 / 62053-21 / 62053-23 standards
- Less than 0.1 % error over 1:1000 dynamic range



TSSOP20

Applications

- Power metering

Description

The STPMC1 device functions as an energy calculator and is an ASSP designed for effective energy measurement in power line systems utilizing Rogowski, current transformer, Shunt or Hall current sensors. Used in combination with one or more STPMSx ICs, it implements all the functions needed in a 1-, 2- or 3-phase energy meter. It can be coupled with a microprocessor for multi-function energy meters, or it can directly drive a stepper motor for a simple active energy meter. The calculator has five input data pins. The first three receive the voltage and current information of the phases. In fact, each data input processes two $\Delta\Sigma$ signals, multiplexed in time and generated by the STPMSx device. The fourth input receives multiplexed $\Delta\Sigma$ signals also, and can be used to sense the neutral current or another signal - temperature, for example. The fifth input data pin accepts non-multiplexed $\Delta\Sigma$ signals and it can be used for sensing the magnetic field information from a Hall sensor. Four internal hard-wired DSP (digital signal processing) units perform all the computations on the $\Delta\Sigma$ streams in real time by means of $\Delta\Sigma$ arithmetic blocks. This allows the achievement of very high computation precision with fast and efficient digital architecture. All the data recorded by the STPMC1 are accessible through an SPI port, which is also used to configure and calibrate the device. The configuration and calibration data can be saved in a 112-bit OTP block, or dynamically set in microprocessor-based meters.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STPMC1BTR	- 40 to 85 °C	TSSOP20 (tape and reel)	2500 parts per reel

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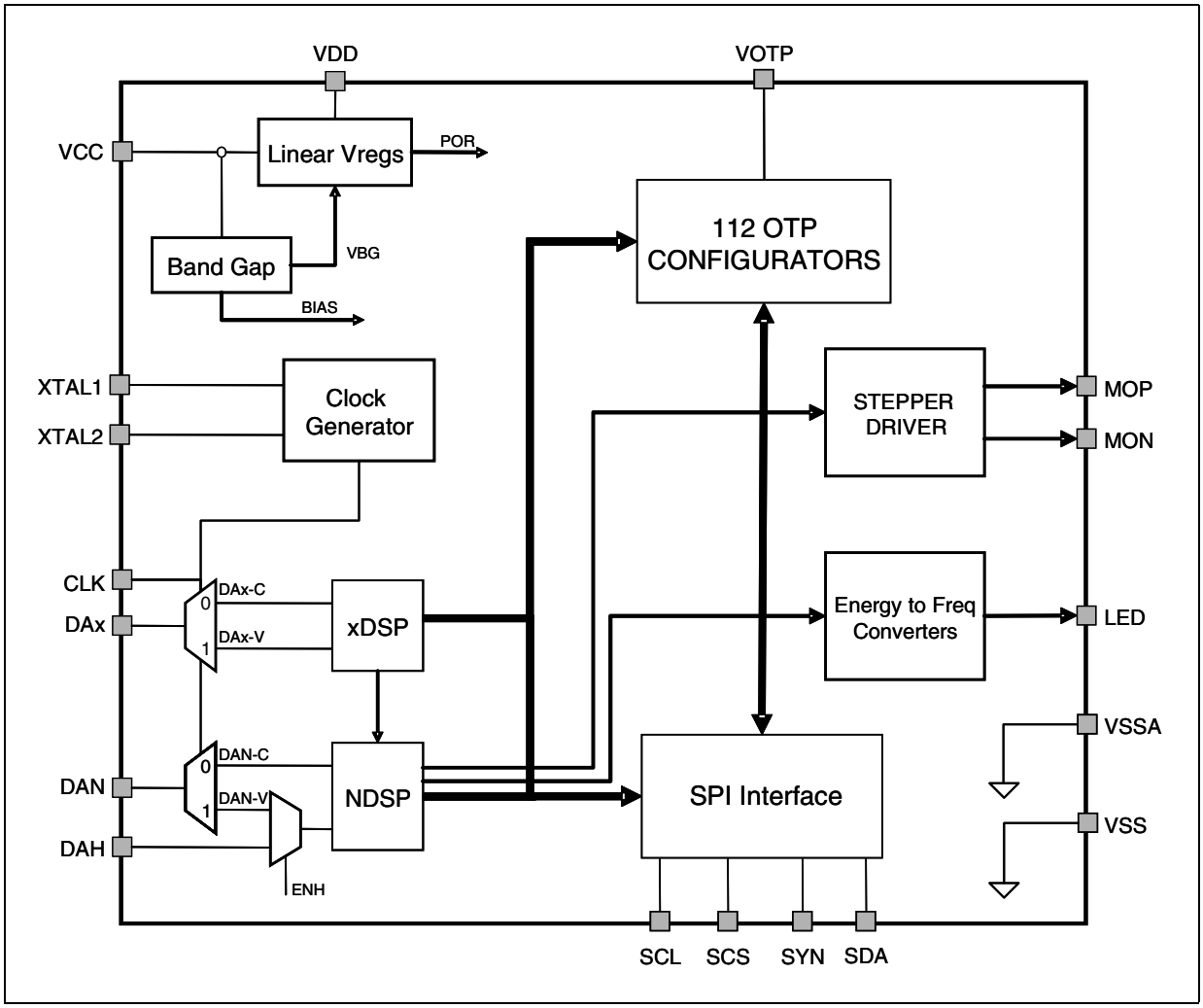
1 Functional block diagram

Figure 1. STPMC1 device block diagram



Note: DAx stands for DAR, DAS, DAT, and xDSP stands for RDSP, SDSP, TDSP.

2 Pin configuration

Figure 2. Pin connections (top view)

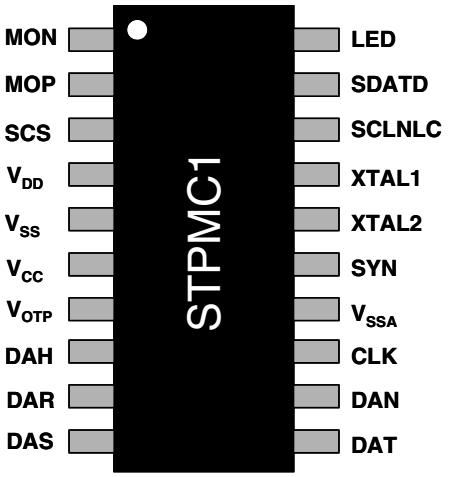


Table 2. Pin description

Pin n°	Symbol	Type (1)	Name and function
1	MON	D / P O	Programmable output pin, see *Table 5*
2	MOP	D / P O	Programmable output pin, see *Table 5*
3	SCS	D I	Digital input pin, see *Table 5*
4	V_{DD}	A O	1.8 V output of internal low drop regulator which supplies the digital core
5	V_{SS}	A GND	Ground level for pad-ring and power supply return
6	V_{CC}	P I	Supply voltage
7	V_{OTP}	P I	Supply voltage for OTP cells
8	DAH	D I	Input for non-multiplexed ΔΣ signals
9	DAR	D I	Input for multiplexed ΔΣ R-phase signals
10	DAS	D I	Input for multiplexed ΔΣ S-phase signals
11	DAT	D I	Input for multiplexed ΔΣ T-phase signals
12	DAN	D I	Input for multiplexed ΔΣ PTAT and neutral signal
13	CLK	D O	2 mA clock output for STPMSx devices
14	V_{SSA}	A GND	Ground level of core
15	SYN	D I/O	Programmable input/output pin, see *Table 5*
16	XTAL2	A	Crystal oscillator pin
17	XTAL1	A	Crystal oscillator pin
18	SCLNLC	D I/O	Programmable input/output pin, see *Table 5*
19	SDATD	D I/O	Programmable input/output pin, see *Table 5*
20	LED	D O	Programmable output pin, see *Table 5*

1. A: Analog, D: Digital, P: Power, I: Input, O: Output, GND: Ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	- 0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at all pins	-0.3 to V_{CC} + 0.3	V
V_{OTP}	Input voltage at OTP pin	- 0.3 to 25	V
ESD	Human body model (all pins)	± 3.5	kV
T_{OP}	Operating ambient temperature	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	114.5 (1)	°C/W

1. This value refers to single-layer PCB, JEDEC standard test board.

4 Functions

Table 5. Programmable pin functions

Programmable pin	Standalone mode (APL = 2 or 3)	Peripheral mode (APL = 0 or 1)
MON	Output for stepper node (MB) - charge pump	Watchdog reset
MOP	Output for stepper node (MA) - charge pump	*ZCR* signal
LED	3-phase energy pulsed output	Programmable energy pulsed output
SCLNLC	No load indicator	SPI interface
SDATD	Tamper indicator	
SYN-NP	Negative power indicator	
SCS	SPI data transmission enable	

5 Application

Figure 3. Application schematic in standalone operating mode

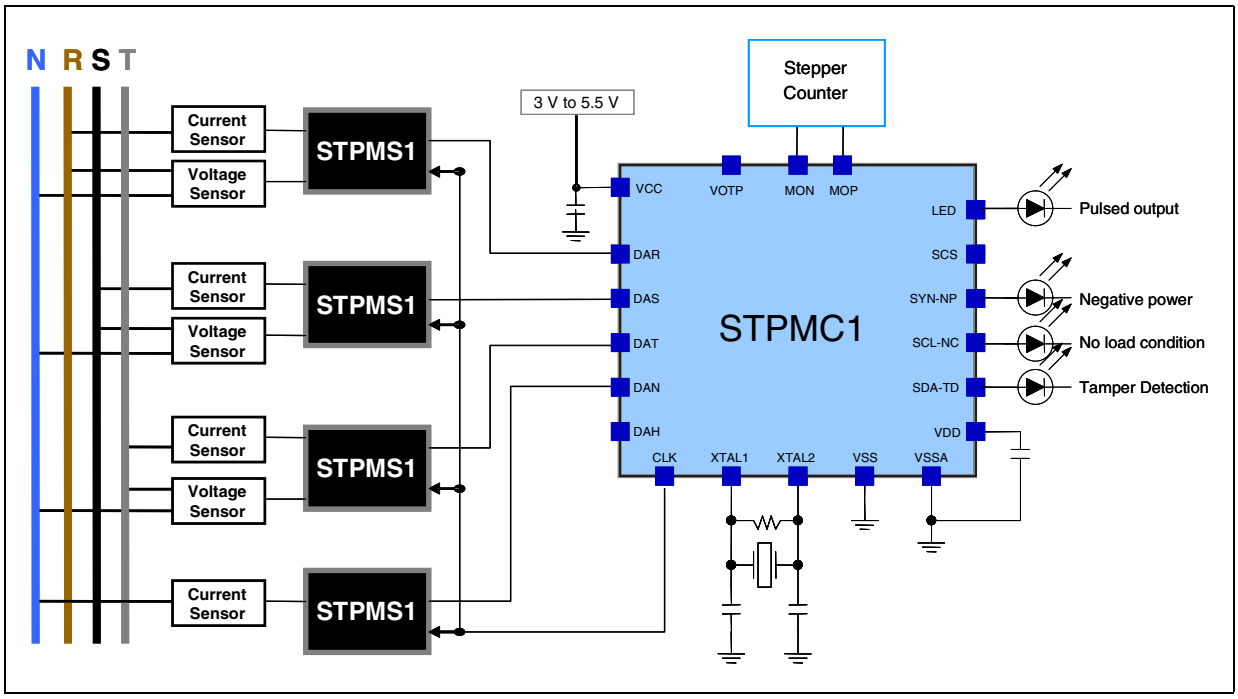


Figure 4. Application schematic using an MCU

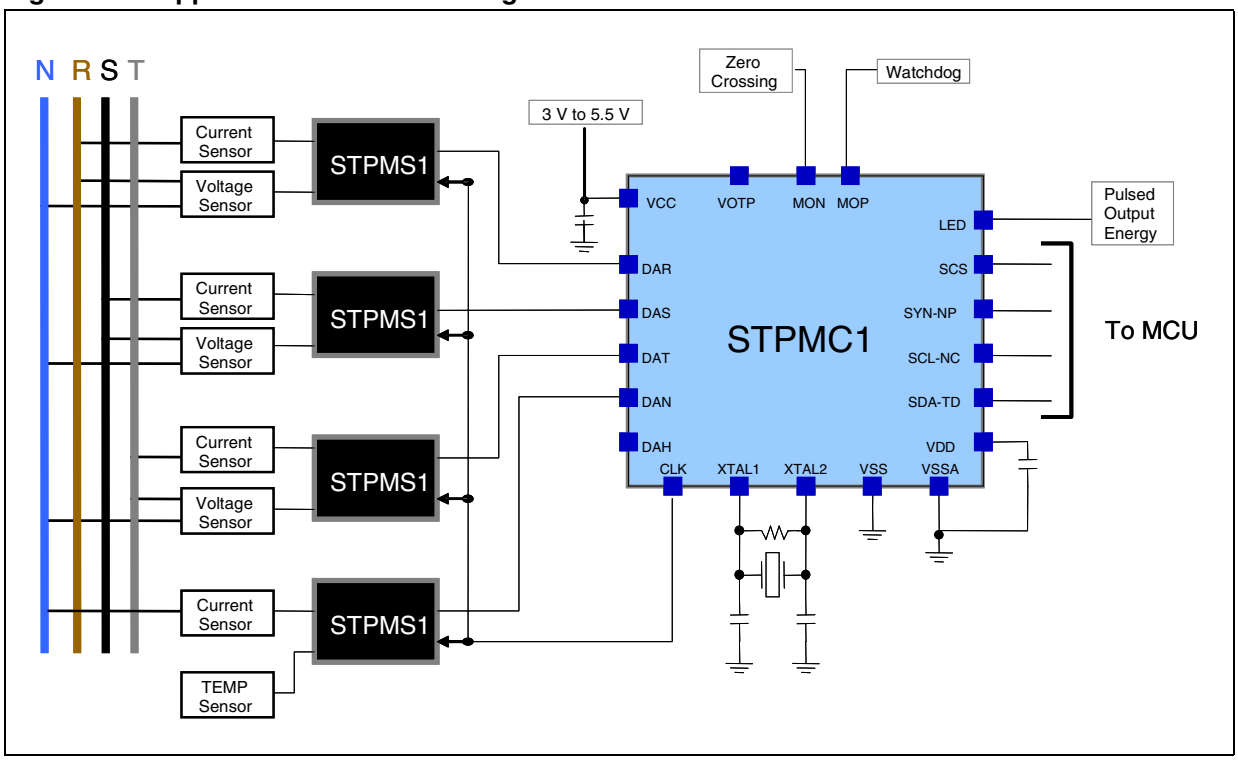


Table 6. Typical external components

Function	Component	Value	Tolerance	Unit
Reads or writes to a calculator device via SPI and performs computation	Microprocessor	---	---	---
Measurement reference clock	Crystal oscillator	4.194 8.192 4.915 9.830	± 30 ppm	MHz
Interface R-phase voltage, current	STPMSx	---	---	---
Interface S-phase voltage, current	STPMSx	---	---	---
Interface T-phase voltage, current	STPMSx	---	---	---
Interface PTAT, neutral current	STPMSx	---	---	---
Interface PTAT or hall	STPMSx	---	---	---
Low-end user interface	Stepper counter			

Note: The components listed above refer to a typical metering application. In any case, STPMC1 operation is not limited to the choice of these external components.

6 Electrical characteristics

(V_{CC} = 5 V, T_A= - 40 to + 85 °C, 100 nF across V_{CC} and V_{SS}; 1 µF across V_{DD} and V_{SSA}, unless otherwise specified).

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering	5		400	Hz
General Section						
V_{CC}	Operating supply voltage		3.17		5.5	V
I_{CC}	Supply current. Configuration registers cleared or device locked	f_{XTAL1} =4.194MHz; V_{CC}=3.2V; C_L=100nF; no loads	5	6	7	mA
ΔI_{CC}	Increase of supply current per configuration bit, during programming	f_{XTAL1} =4.194MHz; V_{CC}=3.2V		100		µA/bit
POR	Power on reset on V_{CC}	f_{XTAL1} =4.194MHz		2.5		V
V_{DD}	Digital supply voltage		1.70	1.80	1.90	V
V_{OTP}	OTP programming voltage		14		20	V
I_{OTP}	OTP programming current per bit	Single bit programming		5		mA
t_{OTP}	OTP programming time per bit	Single bit programming		500		µs
I_{LATCH}	Current injection latch-up immunity				300	mA
Digital I/O (DAH, DAR, DAS, DAT, DAN, CLK, SDA, SCS, SYN, LED)						
V_{IH}	Input high voltage	Other pins	0.75V_{CC}			V
V_{IL}	Input low voltage	Other pins			0.25V_{CC}	V
V_{OH}	Output high voltage	I_O=-2mA	V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O=+2mA			0.4	V
I_{UP}	Pull up current			15		µA
t_{TR}	Transition time	C_{LOAD}=50pF, V_{CC} =5V		10		ns
Power I/O (MOP, MON)						
V_{OH}	Output high voltage	I_O=-16mA	0.9V_{CC}			V
V_{OL}	Output low voltage	I_O=+16mA			0.1V_{CC}	V
t_{TR}	Transition time	C_{LOAD}=50pF, V_{CC} =5V		10		ns

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal oscillator						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{in}	Input current on XTAL2	V_{CC} =5.3V	-1		+1	µA
R_p	External resistor		1		4	MΩ
C_p	External capacitors			22		pF
f_{XTAL1}	Nominal output frequency		4.000	4.194	4.915	MHz
			8.000	8.192	9.830	
f_{MCLK}	Internal clock frequency	see *Table 10*	8.000	8.192	9.830	MHz
f_{CLK}	Output CLK pin frequency	HSA = 0		$f_{XTAL1}/4$		MHz
		HSA = 1		$f_{XTAL1}/2$		
SPI interface timing						
F_{SCLKr}	Data read speed	T_A= 25°C			32	MHz
F_{SCLKw}	Data write speed	T_A= 25°C			100	kHz
t_{DS}	Data setup time			20		ns
t_{DH}	Data hold time			0		ns
t_{ON}	Data driver on time			20		ns
t_{OFF}	Data driver off time			20		ns
t_{SYN}	SYN active width			$2/f_{XTAL1}$		s

Note: Typical value, not production tested.

7 Terminology

7.1 Measurement error

The error associated with the energy measured by the STPMC1 is defined as:

$$\text{Percentage Error} = \frac{\text{SPMC1(reading)} - \text{True Energy}}{\text{True Energy}}$$

7.2 Conventions

The lowest analog and digital power supply voltage is called V_{SS} which represents the system ground (GND). All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. “Sinking current” is the current flowing into the pin, and so it is positive. “Sourcing current” is the current flowing out of the pin, and so it is negative.

Signal timing specifications treated by a digital control part are relative to XTAL1. This signal is provided from the crystal oscillator or from an external source as specified in paragraph *9.4*.

Signal timing specifications of the SPI interface are relative to the SCLNLC. There is no direct relationship between the clock (SCLNLC) of the SPI interface and the clock of the DSP block (XTAL1).

A positive logic convention is used in all equations.

7.3 Notation

Table 8. Notation

Label	Description
u	Voltage
i	Current
u_X	Phase X voltage (X = R, S, T)
i_X	Phase X current (X = R, S, T)
i_N	Neutral current
U_X	Phase X RMS voltage (X = R, S, T)
I_X	Phase X RMS current (X = R, S, T)
P	Active energy full bandwidth
F	Active energy fundamental
Q	Reactive energy full bandwidth
R	Reactive energy fundamental
X_Y	X energy type per Y phase X = P, F, Q, R Y = R, S, T or Σ for 3-phase
PIN	Pin names are UPPERCASE
CFG	Configuration bit names are UNDERLINED
SIG	Internal signals and status bits are in *ITALICS*

8 Typical performance characteristics

Figure 5. Supply current vs. supply voltage, T_A = 25°C (f_{XTAL1} = 4.194 MHz, f_{XTAL1} = 8.192 MHz)

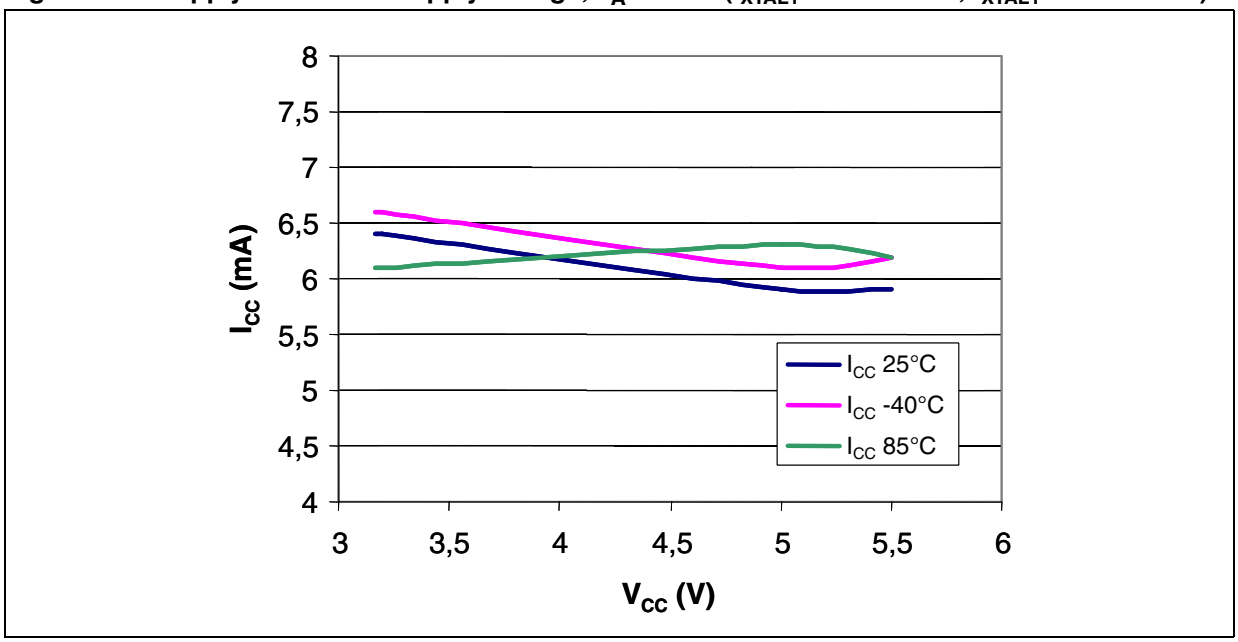


Figure 6. Digital voltage regulator: line - load regulation. (f_{XTAL1} = 0; 100 nF across V_{CC} and V_{SS}; 1 µF across V_{DD} and V_{SSA}; T_A = 25 °C)

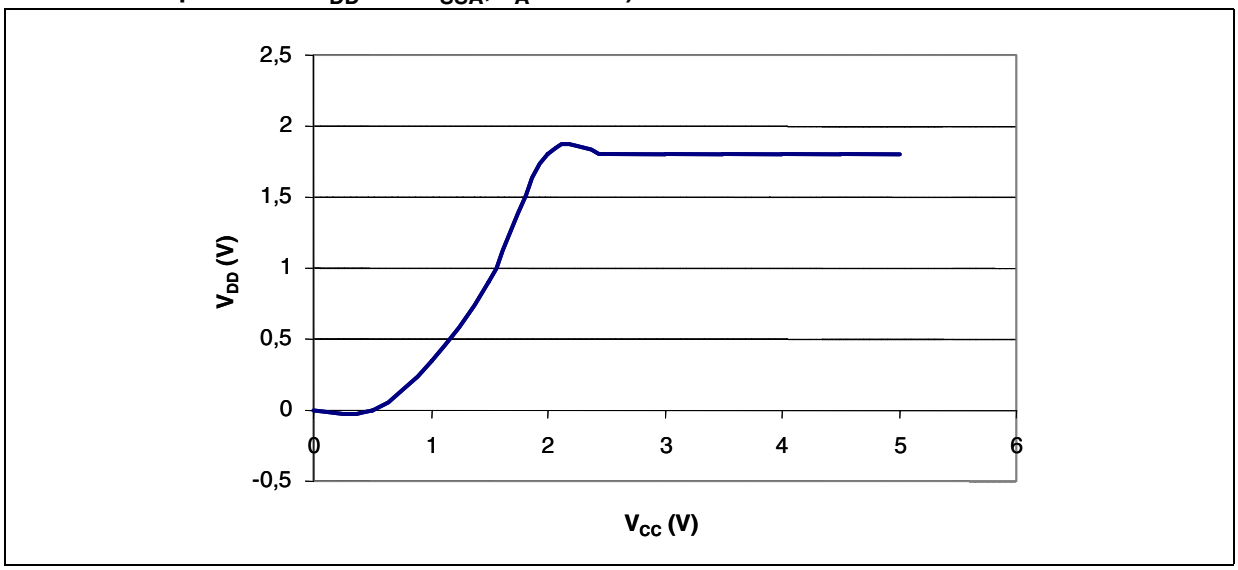
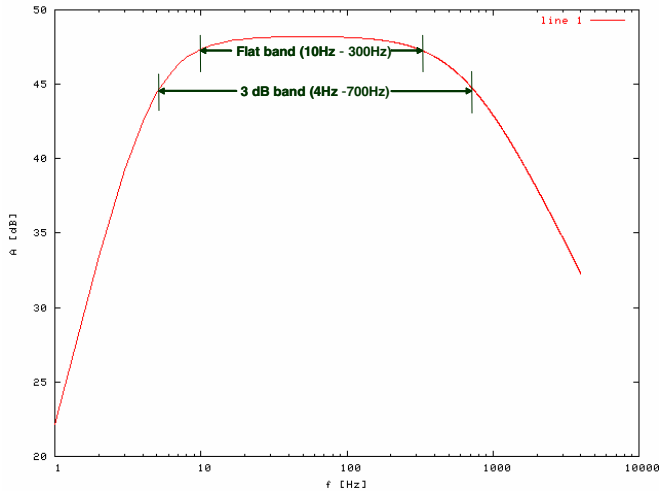


Figure 7. Gain response of decimator



9 Theory of operation

9.1 General operation

The STPMC1 (also called a calculator) is an ASSP designed for effective measurement in power line systems utilizing the Rogowski coil, current transformer, Shunt or Hall current sensors. This device, used with the STMicroelectronics STPMSx companion chip (an analog front-end device), can be implemented as standalone or as a peripheral in a microprocessor based 1-, 2- or 3-phase energy meter.

The calculator consists of three sections: analog, digital and OTP (see *Figure 1*):

- The analog section is composed of a band-gap voltage reference and a low-drop voltage regulator.
- The digital section consists of a system control, clock generator, three PDSP and a NDSP, a SPI interface.
- The 112-bit OTP block and the 16 system signals, used for testing, configuration and calibration purposes, are controlled through SPI by means of a dedicated command set.

The calculator has five input data pins, of which four are fed by signals generated by the STPMSx, see *Table 9*.

Three of them (DAR/DAS/DAT) are used to receive multiplexed signals of voltage and current, implementing energy measurement in 1-, 2- and 3-phase (3 and 4 wires) systems.

After being de-multiplexed, each phase input is sent to the correspondent DSP unit that processes voltage and current information and performs energy calculation, according to the settings of the configuration bits (see *Table 33*).

The DAN input, which also receives a multiplexed signal output from STPMSx device, is typically used to monitor neutral current for anti tampering functions in 1-, 2- and 3-phase (4 wires) systems. Normally the STPMSx monitors current and voltage but in case of neutral monitoring the voltage channel can be connected to a different type of sensor, for example a temperature sensor.

The fifth input data pin (DAH) accepts non-multiplexed $\Delta\Sigma$ signals. It can be used for EMI sensing through Hall sensors or for temperature sensing.

Table 9. Input channels from the STPMSx

Channel name	Property	Signal 1	Signal 2
DAR	Multiplexed	Voltage	Current
DAS	Multiplexed	Voltage	Current
DAT	Multiplexed	Voltage	Current
DAN	Multiplexed	Temperature	Current
DAH	Not multiplexed	EMI or temperature	

The companion chip (STPMSx) embeds 2 $\Delta\Sigma$ ADC converters and the necessary logic capable of providing the multiplexed $\Delta\Sigma$ streams.

See the STPMSx documentation for more details.

These four multiplexed signals are separated, by a digital de-multiplexer, back into eight ΔΣ signals, called streams. The signal coming from the voltage channel of the STPMSx is named with the suffix V, while the stream coming from the current channel is named with the suffix C. For example, the voltage stream of the S-phase is named DAS-V.

Then, each pair of phase the voltage and current stream coming from DAR, DAS and DAT is connected to a dual-channel RDSP, SDSP, TDSP unit (i.e. DAR-V and DAR-C are connected to RDSP).

Each phase voltage input stream is proportional to phase voltage u. Each phase current input stream is proportional to derivation of phase current di/dt, when it originates from Rogowski coil, or to phase current i, when it originates from Shunt or CT or Hall sensor. In this case a derivative is inserted into the voltage channel to get a stream proportional to du/dt. The sensors differ from each other for sensitivity, phase error and susceptibility to external EM fields.

Each of these DSP units performs the following:

- checks the integrity of the streams
- calibrates streams
- filters both streams with a dedicated decimation filter
- computes active and reactive energies, momentary and RMS values for voltage and current, period of power line voltage signal.

In each DSP there are calibrators capable of adjusting the readings ±12.5%.

The power computer does the final calculations of the value and direction of the power and checks for no-load condition.

Another dual DSP unit, called NDSP, processes the streams coming from DAN and DAH. In fact, using the ENH bit (see *Table 33*), the user can select either the voltage stream of the DAN pin (DAN-V) or the DAH stream as the input of the NDSP unit, while the current stream DAN-C is always processed as neutral current.

In its voltage channel, the NDSP unit uses a 2 s time multiplex to process two streams. During the first half of the interval the voltage input stream is processed (which can be DAN-V or DAH, according to the ENH bit), while during the second half a stream constituted by the sum of all four calibrated currents (i.e. DAR-C + DAS-C + DAT-C + DAN-C).

In its current channel the NDSP unit process the current stream of the neutral conductor as follows:

- checks the integrity of stream
- calibrates the stream
- filters the stream with a dedicated decimation filter
- computes momentary and RMS values of the stream
- if no errors have been detected in the phase timing, computes phase frequency, integrates the phase powers by means of 3-input integrators of energies and generates all pulse output signals.

When the DAH input stream is selected, it is checked to detect an external magnetic influence (EMI) to the meter.

The calculator, thanks to its flexibility, can work in all worldwide distribution network standards. By programming the SYS OTP bits, it is possible to implement the following systems:

- 3-phase, 4-wire RSTN, 4-system RSTN (tamper);
- 3-phase, 4-wire RSTN, 3-system RST;
- 3-phase, 3-wire RST_, 3-system RST_ (tamper);
- 3-phase, 3-wire RST_, 2-system R_T_ (Aron);
- 2-phase, 3-wire _STN, 2-system _ST_ (America);
- 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:coil);
- 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:shunt);
- 1-phase, 2-wire __TN, 1-system __T_.

The results of all DSP units are available as pulse frequency on pin LED, MOP and MON, which can also drive a stepper counter, and as states on the digital outputs of device or as data bits in data records, which can be read from the device by means of SPI interface from pins SDA, SNC, SCL and SYN. This system bus interface is also used during temporary or permanent programming OTP bits and system signals or to execute a remote reset request.

A logic block common to all DSP units performs other operations like:

- selecting the valid phase period result from which line frequency is computed in NDSP unit
- checking the equality of phase angles between all three phase voltages
- preparing current values for compensation of external intermediate phase magnetic influences
- checking the sum of currents
- computing intermediate phase voltages
- combining the 3-phase status bits
- performing a watchdog user function

After the device is fully tested, configured and calibrated, a dedicated bit of the OTP block, called TSTD, can be written permanently in order to prevent the change of any configuration bit.

9.2 Power supply

The supply pins for the analog part are V_{CC} and V_{SS}. The V_{CC} is the power input of the 1.8 V low drop regulator, band-gap reference and bias generators.

From the V_{CC} pin a linear regulator generates the +1.8 V voltage supply level (V_{DD}) which is used to power the OTP module and digital core. The V_{SS} pin represents the reference point for all the internal signals. 100 nF low ESR capacitors should be connected between V_{CC} and V_{SS}, and 1 µF between V_{DD} and V_{SSA}. All these capacitors must be placed very close to the device.

The STPMC1 contains a power on reset (POR) detection circuit. If the V_{CC} supply is less than 2.5 V then the STPMC1 goes into an inactive state, all the functions are blocked asserting a reset condition. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which gives a high degree of immunity from false triggering due to noisy supplies.
A bandgap voltage reference (VBG) of 1.23 V ±1% is used as a reference voltage level

source for the linear regulator. Also, this module produces several bias currents and voltages for all other analog modules and for the OTP module.

9.3 Resetting the STPMC1 (status bit *HLT*)

The STPMC1 has no reset pin. The device is automatically reset by the power-on-reset detection circuit (POR) when the V_{CC} crosses the 2.5 V value, but it can be reset also through the SPI interface through a dedicated remote reset request (RRR) command (see paragraph *9.21* for RRR details).

The reset through SPI is used during production testing or in an application with some on-board microprocessors when a malfunction of the device is detected.

Resetting the STPMC1 causes all the functional modules of STPMC1 to be cleared, including the OTP shadow latches (see paragraph *9.19* for an OTP shadow latch memory description). In case of reset through SPI the mode signals (see paragraph *9.20* for a description of the mode signals) are not cleared.

In cases of reset caused by the POR circuit all blocks of the digital part, except the SPI interface, are held in a reset state for 125 ms after the reset condition. When the reset is performed through SPI, no delayed turn-on is generated.

During the device reset, the status bit *HLT* is held high, meaning that data read from the device register are not valid.

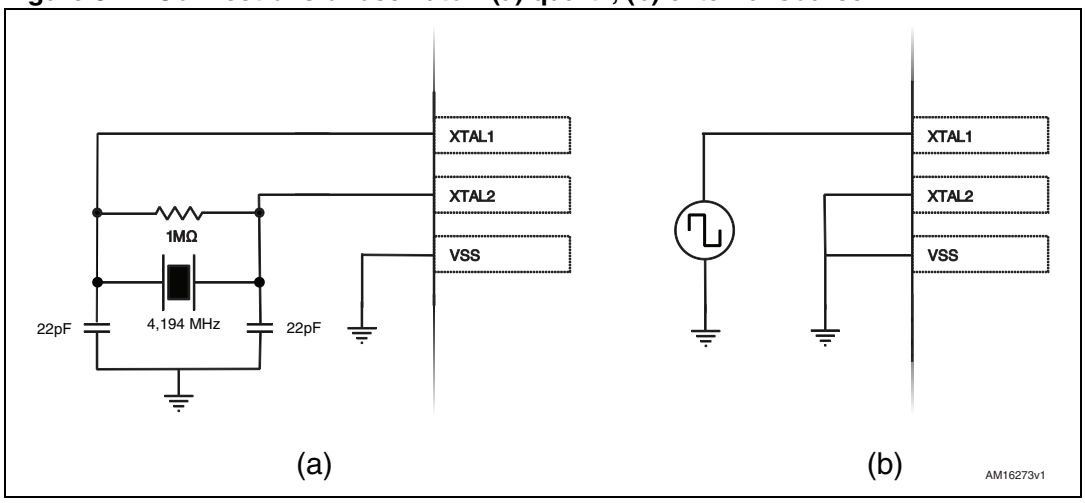
9.4 Clock generator (bits MDIV, FR1, HSA)

All the internal timing of the STPMC1 is based on the XTAL1 signal. This signal can be generated in two different ways:

- Quartz: the oscillator works with an external crystal.
- External clock: the clock is provided by an external source connected to XTAL1.

The suggested circuits are depicted in *Figure 8*.

Figure 8. Connections of oscillator: (a) quartz, (b) external source



The clock generator is responsible for two tasks.
The first is to retard the turn-on of some functional blocks after POR in order to help a smooth start of external power supply circuitry by keeping off all major loads. For this

reason, all blocks of the digital part, except the SPI interface, are held in a reset state for 125 ms after a power on reset (see *Section 9.3*).
The second task of the clock generator is to provide all necessary clocks for the digital part. In this task, a MDIV and FR1 programming bits are used to inform the device about the nominal frequency value from XTAL1 (f_{XTAL1}).
Four nominal frequencies are possible through proper setting of the MDIV and FR1 bits (see *Table 10*).

The internal master clock f_{MCLK} is derived from f_{XTAL1} as shown in *Table 10*.

Table 10. Frequency settings through MDIV and FR1 (1)

f_{XTAL1}	MDIV (1 bit)	FR1 (1 bit)	f_{MCLK}
4.194 MHz	0	0	8.389 MHz
4.915 MHz	0	1	9.830 MHz
8.192 MHz	1	0	8.192 MHz
9.830 MHz	1	1	9.830 MHz

1. 4 MHz and 8 MHz clock are also supported. MDIV and FR1 have to be set as for 4.194 MHz and 8.192 MHz respectively.

Through the HSA bit the frequency of the output pin CLK (f_{CLK}), which provides the clock for the STPMSx devices, can be derived as reported in *Table 11*.

Table 11. CLK pin frequency settings through HSA

HSA (1 bit)	f_{CLK} STPMC1
0	f_{XTAL1} / 4
1	f_{XTAL1} / 2

To properly work with STPMS2, the clock configurations in *Table 12* must be used. Moreover, with STPMS2 companion chip the PM bit must always be set.

Table 12. STPMC1 configuration for STPMS2

MDIV (1 bit)	HSA (1 bit)	f_{CLK}
0	0	f_{XTAL1} / 4
1	0	f_{XTAL1} / 4
0	1	f_{XTAL1} / 2

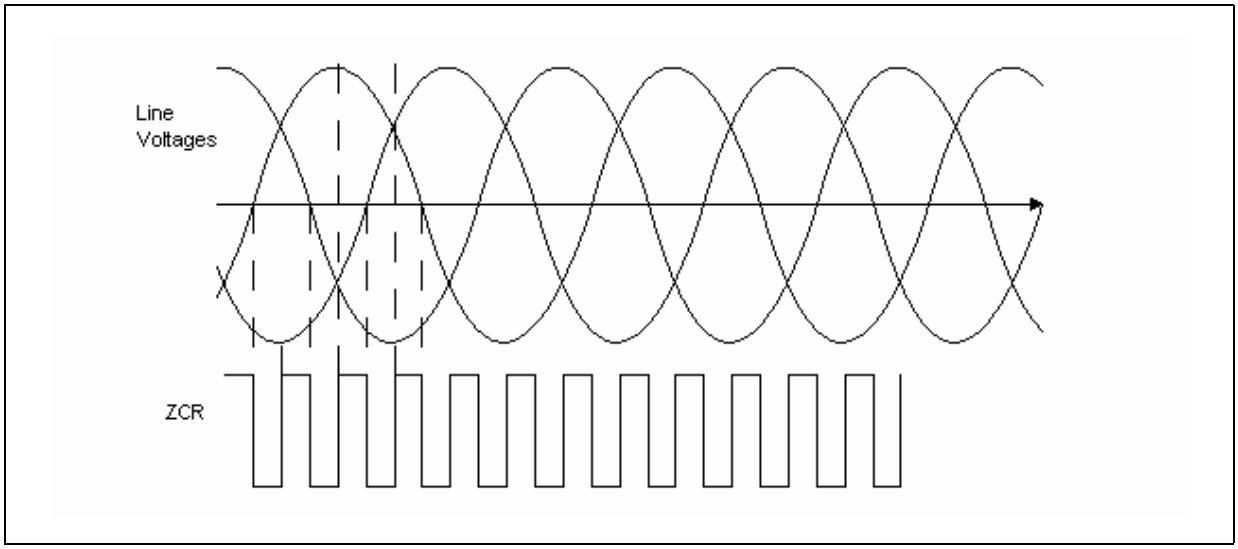
9.5 Zero crossing detection (signal *ZCR*)

The STPMC1 has a zero crossing detection circuit on the voltage channel that can be used to synchronize some utility equipment to zero crossing or max of line voltage events. This circuit produces the internal signal *ZCR* that has a falling edge every zero crossing of one of the line voltages and a rising edge every peak (positive or negative) of one of the line voltages.

The *ZCR* signal is a 3-phase voltage zero cross signal. It is the result of a XNOR of the *ZCR* of each phase. The *ZCR* of each of the three-phases is a 100 Hz signal, so a 3-phase *ZCR*

is 300 Hz signal. The *ZCR* signal is available on the MOP pin only when the STPMC1 works as a peripheral with the configuration bit APL=0.

Figure 9. *ZCR* signal



9.6 Period and line voltage measurement (status bits: *LIN*, *BFR*, *LOW*, *BFF*)

From voltage channels, a base frequency signal *LIN* is obtained, which is high when the line voltage is rising and it is low when the line voltage is falling, so that, *LIN* signal represents the sign of dv/dt. With further elaboration, the *ZCR* signal is also produced.

A period meter, which is counting up pulses of $f_{MCLK}/8$ reference signal, measures the period of voltage channel base frequency and checks if the voltage signal frequency is in the band going from $f_{MCLK}/(2^{18} - 2^3) \approx f_{MCLK}/2^{18}$ to $f_{MCLK}/2^{16}$.

This is done, phase by phase, by means of the signal *LIN*, which trailing edge is extracted and it is used to reset the period meter.

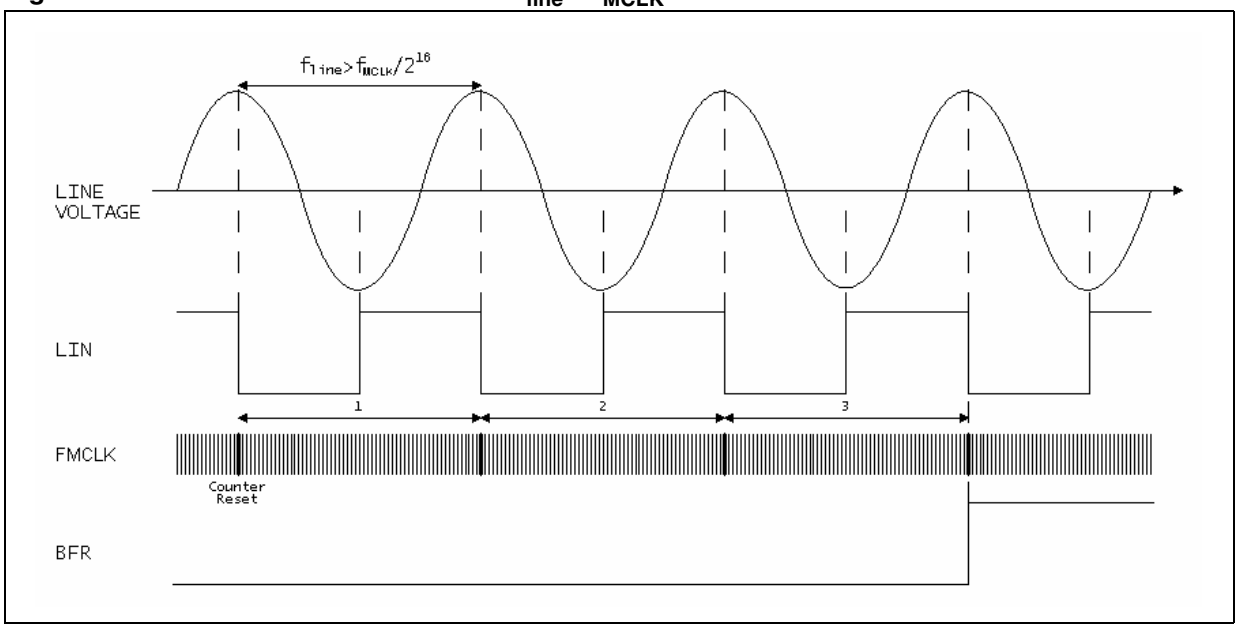
Table 13. Good frequency ranges for different clock source values

f_{XTAL}	f_{MCLK}	freq. min. = $f_{MCLK}/2^{18}$	freq. max. = $f_{MCLK}/2^{16}$
4.194 MHz	8.389 MHz	32.0 Hz	128.0 Hz
4.915 MHz	9.830 MHz	37.5 Hz	150.0 Hz
8.192 MHz	8.192 MHz	31.3 Hz	125.0 Hz
9.830 MHz	9.830 MHz	37.5 Hz	150.0 Hz

If the counted number of $f_{MCLK}/8$ pulses between two trailing edges of *LIN* is higher than the 2^{18} equivalent pulses or if the counting is never stopped (no more *LIN* trailing edge), the base frequency exceeds the lower limit and an error flag *BFR* is set. This error flag is part of the 8-bit status byte of each phase (see *Table 32*).

If the counted number of $f_{MCLK}/8$ pulses between two trailing edges of *LIN* is lower than the 2^{16} equivalent pulses, the base frequency exceeds the upper limit. In this case, such error must be repeated three times, in order to set the error flag *BFR*, as shown in *Figure 10*.

Figure 10. *LIN* and *BFR* behavior when $f_{line} > f_{MCLK}/2^{16}$



The in-band base frequency resets the flag *BFR*. If *BFR* is cleared, the measured period value is latched, otherwise a default value of period is used as a stable data to compute frequency needed to adapt the decimation filter and to perform frequency compensation of reactive energy and RMS current I_X in case of non Rogowski current sensor.

The *BFR* flag is also set if the register value of the RMS is too low. In this case also the status bit *LOW* is set.

The condition for setting *LOW* and consequently *BFR* of each phase is $U_X < U_{Xmax}/32$ ($U_{Xmax} = 2^{12}$) it means if the U_X register drops below 128 *LOW* and *BFR* are cleared when the register value goes above 256 ($U_X > U_{Xmax}/16$). *BFR*, then, gives also information about the presence of the line voltage.

When the *BFR* error is set, the computation of power is zero and the energy registers (active, reactive and fundamental) are blocked, unless single wire mode operation is entered (see *Section 9.7*).

When the MOP, MON and LED pins are configured to provide the pulsed energy information they are held low if *BFR* is set.

The 3-ph status bit *BFF* is the OR of each phase bit *BFR*.

9.7 Single wire operation mode: SWM (status bits: *NAH*, *BFR*, configuration bit FRS)

The STPMC1 supports single wire meter (SWM) operation. In this condition, since there is no voltage information, the current RMS values, instead of the energies, are accumulated in 20-bit dedicated registers located in ACR, ACS, ACT (20-bit accumulator of RMS I_X per hour [Ah]).

Each ACx register contains a 20-bit accumulator of the relative phase current I_X [Ah] and an 8-bit register carrying the information about phase delay between voltage channels.

The SWM mode is indicated by status bit *NAH* =0:

- Bit *NAH*=0 (SWM on) happens when *BFR*=1 and RMS value of current signal is $I_X > I_{Xmax}/4096 = 16$ ($I_{Xmax} = 2^{16}$). In this case frequency is out of limits and RMS current I_X is big enough, so it is accumulated in the corresponding ACx phase register.
- Bit *NAH*=1 (SWM off) happens if *BFR*=1 and RMS value of current signal is $I_X < I_{Xmax}/8192 = 8$, or *BFR*=0. In this case either voltage frequency is out of limits but RMS current I_X is too small to enter SWM mode, or voltage frequency is in the correct range.

When bit *BFR* is set, for a certain phase, its energy registers (active, reactive, fundamental) are blocked. Then, if RMS value of current signal is big enough, bit *NAH* is cleared (0) and a SWM operation is entered. In this case the RMS value of current signal is accumulated in ACx register and the value of voltage RMS U_X is set to zero.

Example 1: Single wire operation with SYS = 0

SYS = 0 (3-phase system) is set and in the R-phase the voltage signal is too low (status bits of phase R *BFR* = 1 and *LOW* = 1).

Because of the too low voltage signal the frequency can't be calculated and energy registers related to the R-phase are blocked.

If RMS value of current signal is big enough, the device enters SWM and clears *NAH* of R phase. The ACR register is incremented by adding I_R, the RMS value of current signal.

Example 2: Single wire operation with SYS = 0 and TCS = 1

SYS = 0 (3-phase system) and TCS = 1 (CT sensor selection) are set and in all phases (R, S and T) the voltage signal is too low (status bits *BFR* = 1 and *LOW* = 1 for all phases).

Because of the too low voltage signal the frequency could not be calculated and all energy registers are blocked.

Since when TCS = 1, a frequency value is needed to calculate the RMS value of the current signal, the default value of 50 Hz or 60 Hz (if bit FRS=1) is taken. If the RMS value of current signal is big enough, the device enters SWM and clears *NAH* of all phases and ACR, ACS and ACT registers is fed with the correspondent I_X.

The accumulators ACx can be read by means of SPI.

To retrieve energy information, RMS value of current signal accumulated in registers ACx can be multiplied by a constant representing the value of RMS voltage. This operation must be executed by a microcontroller.

Usually the supply voltage for the electronic meter is taken from the line voltage. In SWM, since the line voltage is not present anymore, some other power source must be used in order to provide the necessary supply to STPMC1 and the other electronic components of the meter.

9.8 Load monitoring (status bit *BIL*, configuration bit LTCH)

The STPMC1 includes in each phase a no-load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured voltage is below the set threshold, an internal signal *BIL* becomes high. The

information about this signal is also available in the status bit *BIL*, one per each phase (see *Table 32*).

The three phase status bit *BIL* is the AND of each phase status bit *BIL*.

The no-load condition occurs when the product between U_X and I_X register values is below a given value. This value can be set by the LTCH configuration bits. Four different no-load threshold values can be chosen according to the two LTCH bits as reported in *Table 14*.

When a no-load condition occurs (*BIL* = 1) the integration of power is suspended. The no-load condition flag *BIL* in standalone mode blocks generation of pulses for stepper and is brought out to the output selector forcing SCLNLC pin low. In peripheral mode, the *BIL* signal can be accessed through the SPI interface.

The minimum output frequency (at no-load threshold) is given as % of the full-scale (FS) output frequency, where FS internal AW frequency is 1370 Hz per phase.

Table 14. No-load detection thresholds

LTCH (2 bits)	NLC threshold
0	0,00125*FS
1	0,0025*FS
2	0,005*FS
3	0,010*FS

Example 3: No-load condition threshold calculation

An energy meter has a power constant of C = 64000 pulses/kWh on LED pin.

It is valid the following relation:

C = 3600000 * f / P

where 3600000 is the factor between kWh and Ws and f is the output frequency on the LED pin if P power is applied to the meter.

The minimum output frequency if LTCH [0] = LTCH [1] = 1 is:

f = 0,010 * 1370 Hz = 0,137 Hz

which gives a no-load condition power threshold equal to:

P = 3600000 * 0,137 Hz / 64000imp/kWh = 7,7 W

In this example, the no-load threshold is equivalent to 7,7 W of load or to a start-up current of 32 mA at 240 V.

In NLC function is also implemented an hysteresis. When the current is falling the threshold is half lower than that described above.

9.9 Error detection (status bits: *BCF*, *PIN*)

The STPMC1 has two error detection circuits that checks:

- the ΔΣ signals
- the state of output pins

The first error detection circuit checks if any of the ΔΣ signals from the analog part is stuck at 1 or 0 within the period of observation (250 µs). In case of detected error the corresponding ΔΣ signal is replaced with an idle ΔΣ signal, which represents a constant value 0. When this

error occurs the correspondent phase bit *BCF* is set. When the ΔΣ signal becomes correct again the *BCF* flag is cleared immediately.

The 3-ph status bit *BCF* is the OR of each phase bit BFC, but it takes into account also the connection of the neutral wire (DAN-I stream).

The other error condition occurs if the MOP, MON and LED pin outputs signals are different from the internal signals that drive them. This can occur if some of this pin is forced to GND or to some other imposed voltage value. In this case the internal status bit *PIN* is immediately activated providing the information that some hardware problem has been detected, for example the stepper motor has been mechanically blocked.

These two error condition don't influence energy accumulation.

9.10 Tamper detection module (status bits: *BCS*, *BSF*, *BIF*, configuration bit ENH)

The tamper detection module is used to prevent theft of energy through improper connection of the meter. The tamper indicator is activated when:

- sum of currents is above tamper threshold (status bit *BCS* = 1),
- phase sequence is wrong (status bit *BSF* = 1),
- phase active powers don't have the same sign (status bit *BIF* = 1),
- electromagnetic interference (EMI) is detected (only with ENH = 1).

In standalone application mode (APL [1] = 1) the SDATD pin is used to notify the tamper condition.

In 3-phase system (SYS = 0, 1, 2) this output is set if at least one of the internal status bits: *BCS*, *BSF*, *BIF* has been set or if EMI has been detected.

In other systems (SYS ≠ 0, 1, 2) it indicates only *BCS* or EMI.

Example 4: Tamper output on SDATD pin

SYS = 0, 1 or 2 and APL [1] = 1:

BCS = 0, *BSF* = 0, *BIF* = 0 → Tamper (SDATD pin) = 0

BCS = 0, *BSF* = 1, *BIF* = 1 → Tamper (SDATD pin) = 1

SYS = 0, 1 or 2, APL [1] = 1 and ENH = 1:

BCS = 0, *BSF* = 0, *BIF* = 0, EMI = 0 → Tamper (SDATD pin) = 0

BCS = 0, *BSF* = 0, *BIF* = 0, EMI = 1 → Tamper (SDATD pin) = 1

BCS = 1, *BSF* = 1, *BIF* = 1, EMI = 1 → Tamper (SDATD pin) = 1

In peripheral application mode these information can be read out by SPI interface checking the 3-ph status bits, or the status bits corresponding to each phase.

9.10.1 Sum of currents is above tamper threshold (status bit *BCS*)

Tamper detection through bit *BCS* is meaningful only for SYS = 0, 2, 5, 6 (systems with neutral wire). In other measurement systems it is not useful because there are not enough input current streams.

The STPMC1 check tamper detection only if

$$\sum I_X > \frac{I_{max}}{256}$$

Where:

$I_{max} = 2^{16}$

$\Sigma I_X = I_R + I_S + I_T + I_N$ for SYS = 0, 1, 2, 3, 4, 7

$\Sigma I_X = I_S + I_T$ for SYS = 5, 6

Bit *BCS* is set according to *Table 15*

Table 15. Tamper conditions

BCS	SYS = 0, 1, 2, 3, 4, 7	SYS = 5, 6
0	$\left(\sum i_X\right)_{RMS} < \frac{\sum I_X}{8}$	$\frac{7}{9}I_S < I_T < \frac{9}{7}I_S$ or $\frac{7}{9}I_T < I_S < \frac{9}{7}I_T$
1	$\left(\sum i_X\right)_{RMS} > \frac{\sum I_X}{8}$	$\frac{7}{9}I_S > I_T > \frac{9}{7}I_S$ or $\frac{7}{9}I_T > I_S > \frac{9}{7}I_T$

with $(\Sigma i_X)_{RMS} = (i_R + i_S + i_T + i_N)_{RMS}$

Example 5: 3-ph system - BCS = 0

Let us consider a three-phase, four wires system where the RMS values of the current applied are:

$I_R = 5$ A

$I_S = 5$ A

$I_T = 4.4$ A

$I_N = 0$ A

The sum of all instantaneous currents ($i_R + i_S + i_T + i_N$) should always be zero, unless there is a tamper condition.

The STPMC1 calculates this sum and put its RMS value divided by four (called sIRMS) into register DMN (see paragraph *9.17.2*).

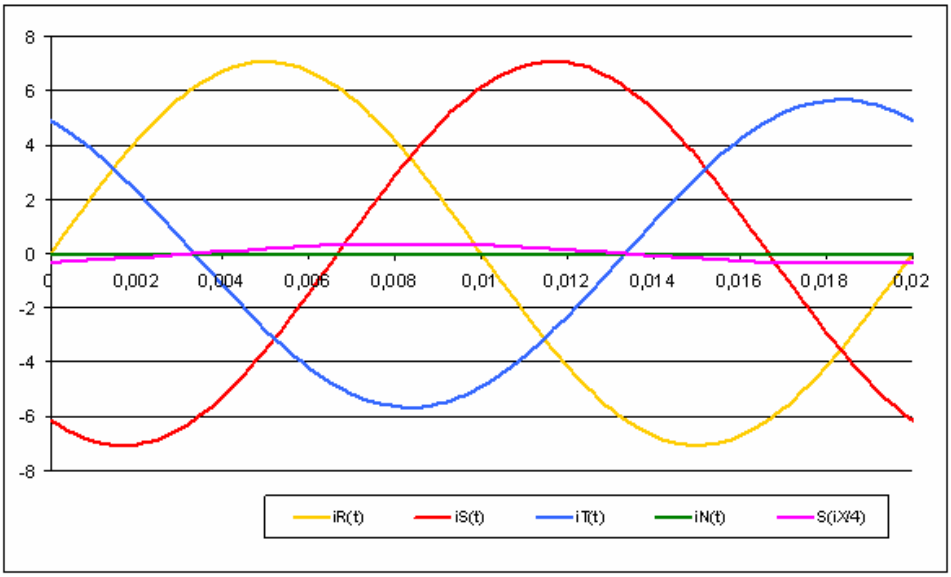
This value should always be zero (or very close).

In our case:

$$\text{sIRMS} = \left(\sum \frac{i_X}{4}\right)_{RMS} = 0.149967\,\text{A}$$

The currents are shown in *Figure 11* below.

Figure 11. Currents of the three phase system in example



The value I_{MAX} corresponds to the maximum current value hold by each RMS current register (internal value FFFF). It is a function of the sensor type, sensitivity and of the current channel gain. Let us suppose that

I_{MAX} = 180 A

The tamper condition is evaluated only if

$$\sum I_X = I_R + I_S + I_T + I_N > \frac{I_{MAX}}{256}$$

This means that the sum of the RMS value of currents is not negligible with respect to I_{MAX} (the threshold corresponds to about 0.4% of I_{MAX}).

In this case this is true since:

$I_R + I_S + I_T + I_N$ = 14.4 A > 0,703125 A = I_{MAX} / 256

The criterion for tamper detection is

$$\left(\sum i_X\right)_{RMS} > \frac{\sum I_X}{8}$$

This can also be expressed as

$$\text{sIRMS} = \left(\sum \frac{i_X}{4}\right)_{RMS} = \frac{\left(\sum i_X\right)_{RMS}}{4} > \frac{\sum I_X}{32}$$

which means the sIRMS value must not exceed 3.13% of ($I_R + I_S + I_T + I_N$).

In this example:

sIRMS = 0,149967 < 0.45 = ($I_R + I_S + I_T + I_N$) / 32

Then BCS = 0.

Example 6: 3-ph system - BCS = 1

Let us consider a three-phase, four wires system where:

I_R = 5 A

I_S = 5 A

I_T = 3.2 A

I_N = 0 A

The tamper is evaluated because

$I_R + I_S + I_T + I_N$ = 13.2 A > 0,703125 A = I_{MAX} / 256

In this case

sIRMS = 0,449901 A > 0,4125 A = $(I_R + I_S + I_T + I_N)$ / 32

Then BCS = 1.

Example 7: 1-ph system - BCS = 0

Let us consider a single phase systems with only S and T wires connected where

I_S= 5 A

I_T = 4 A

I_{MAX} = 180 A

In this case the criterion for tamper evaluation is verified since:

$(I_S + I_T)$ = 9 A > 0,703125 A = I_{MAX} / 256

But BCS = 0 because

7/9 I_T = 3.11 A < I_S = 5 A < 9/7 I_T = 5.14 A

and

7/9 I_S = 3.88 A < I_T = 4 A < 9/7 I_S = 6.43 A

Example 8: 1-ph system - BCS = 1

Let us consider the case in which:

I_S = 5 A

I_T = 3 A

I_{MAX} = 180 A

Also in this case the criterion for tamper evaluation is verified:

$(I_S + I_T)$ = 8 A > 0,703125 A = I_{MAX} / 256

Now BCS = 1 because

7/9 I_S = 3.88 A > I_T = 3 A

9.10.2 Phase sequence is wrong (status bit *BSF*)

One tamper condition is that phase sequence is not correct. A 3-ph phase status bit *BSF* checks the sequence of phases, which, in a three phase system is one of the following:

- R → S → T
- S → T → R
- T → R → S

In one of the above cases *BSF* is cleared, otherwise bit *BSF* is set.

Whatever the SYS bits setting (indicating phases presence and configuration), bit *BSF* is always calculated, but it is valid only in cases SYS is 0, 1, 2 and 3. In fact in this case all the three phase voltage signals (u_R, u_S, u_T) are available and can be checked, as shown in 0.

In cases SYS is 4, 5, 6, 7, only two or one voltage signal are available (u_S and/or u_T), so that the sequence cannot be checked. Bit *BSF* is always set in the status byte, but it must be ignored.

In standalone application for SYS = 0, 1 or 2 (3-phase systems) bit *BSF* is available as output on SDATD pin.

Table 16. Pin description versus SYS configuration (u_X and i_X represent the voltage and the current signals)

Pin	SYS							
	0	1	2	3	4	5	6	7
DAR	u_R	u_R	u_R	u_R	-	-	-	-
DAS	u_S	u_S	u_S	u_S	u_S	-	-	-
DAT	u_T	u_T	u_T	u_T	u_T	u_T	u_T	u_T
DAN	i_N	-	-	-	-	-	-	-
DAR	i_R	i_R	i_R	i_R	-	-	-	-
DAS	i_S	i_S	i_S	-	i_S	i_S	i_S	-
DAT	i_T	i_T	i_T	i_T	i_T	i_T	i_T	i_T

9.10.3 Phase active powers do not have the same sign (status bit *BIF*)

The 3-phase status bit *BIF* is produced from status bit *SIGN* of each phase. If bit *SIGN* is not equal in all three phases (R, S and T), then bit *BIF* is set.

In a standalone application for SYS = 0, 1 or 2 (3-phase system) bit *BIF* is available as output on SDATD pin.

Example 9: status bit *BIF*

$SIGN_R = 0$, $SIGN_S = 0$, $SIGN_T = 0 \rightarrow BIF = 0$
$SIGN_R = 1$, $SIGN_S = 1$, $SIGN_T = 1 \rightarrow BIF = 0$
$SIGN_R = 1$, $SIGN_S = 0$, $SIGN_T = 0 \rightarrow BIF = 1$
$SIGN_R = 0$, $SIGN_S = 1$, $SIGN_T = 0 \rightarrow BIF = 1$

9.10.4 EMI is detected

EMI tamper detection is enabled by configuring bits ENH = 1 and APL [1] = 1 (APL [1] sets standalone application mode).

The DAH signal is checked to verify that:

- its DC component does not exceed $DC_{MAX}/16$
- its RMS value does not exceed the maximum value $RMS_{MAX}/16$

where $DC_{MAX} = RMS_{MAX} = 2^{16}$ with hysteresis.

If these condition are not verified the EMI tamper is detected.

EMI tamper condition is not available as internal status signal, but it is available (in OR with other tamper conditions) on the SDATD pin of the device.

In peripheral application mode it is possible to detect EMI tamper comparing the value of the 16-bit DCuN and of the 12-bit RMSuN to the threshold through a microcontroller.

9.11 Energy to frequency conversion (configuration bits: APL, KMOT, LVS, FUND)

The STPMC1 provides energy to frequency conversion both for calibration and energy readout purposes.

The three hard-wired xDSP, implemented as four 2-channel $\Delta\Sigma$ signal processors perform all calculations and produce output data and signals. Inside them, each three stage decimation filter inputs a filtered $\Delta\Sigma$ signal and its integral as parallel bus or stream to the power and RMS computer. All three streams of power (active, reactive and active from the fundamental harmonic) are connected to the corresponding integrators.

Within the integrators, all three powers are accumulated into energies of 20-bit values according to configuration bit ABS and the results are converted into pulse train signals, the frequency of which is proportional to the accumulated energies. Each of these signals can be brought out to the LED pin.

Due to the innovative and proprietary power calculation algorithm the frequency signal is not affected by any ripple at twice the line frequency. This feature strongly reduces the calibration time of the meter.

Through calibration the meter is configured to provide a certain number of pulses per kWh (referred to as power meter constant **C**) on the LED pin. According to the APL, KMOT, LVS and FUND configuration bits, the frequency of LED signal can provide different information, as shown in paragraphs *9.12* and *9.13*.

Given **C**, the number of pulses per kWh provided, the relationship between the LSB value of the source energy registers and the number of pulses provided to LED pin is indicated in the table below:

Table 17. Energy registers LSB value

Register	SYS = 0, 1, 2, 4, 5, 6, 7	SYS = 3
3-ph active energy wide band (P)	$K_P = \frac{1000}{C \cdot 2^{10}}[Wh]$	$K_P = \frac{1000}{C \cdot 2^{10}}[Wh]$
3-ph reactive energy wide band (Q)	$K_Q = \frac{1000}{C \cdot 2^{10}}[Varh]$	$K_Q = \frac{1000}{C \cdot 2^{9}}[Varh]$
3-ph active energy fundamental (F)	$K_F = \frac{1000}{C \cdot 2^{10}}[Wh]$	$K_F = \frac{1000}{C \cdot 2^{9}}[Wh]$
3-ph reactive energy fundamental (R)	$K_R = \frac{1000}{C \cdot 2^{10}}[Varh]$	$K_R = \frac{1000}{C \cdot 2^{9}}[Varh]$

Example 10: energy registers LSB value for SYS = 0, 1, 2, 4, 5, 6, 7

C = 64000 pulses/kWh = 17.7 Hz*kW

$K_P = K_F$ = 15.258 *10-6 Wh

$K_Q = K_R$ = 15.258 *10-6 VArh

This means that the reading of 0x00001 in the active energy register represents 15.258 µWh, while 0xFFFFF represents 16 Wh.

Example 11: Energy registers LSB value for SYS = 3

C = 64000 pulses/kWh = 17.7 Hz*kW

K_P = 15.258 *10-6 Wh

K_F = 30.517 *10-6 Wh

$K_Q = K_R$ = 30.517 *10-6 VArh

From 3-phase active energy wide band signal the stepper driving signals *MA* and *MB* (output from MOP and MON pins) are generated. The frequency of these signals can be configured as shown in paragraph *9.13*.

9.12 Using STPMC1 in microcontroller based meter - peripheral operating mode (configuration bits: APL, KMOT, LVS, FUND)

The higher flexibility of the STPMC1 allows its use in microcontroller based energy meters. In this case the STPMC1 must be programmed to work in peripheral mode setting bit APL [1] = 0. All the SPI pins (SCS, SCLNCL, SDATD, SYN) are used only for communication purposes, allowing the microcontroller to write and read the internal STPMC1 registers.

The peripheral mode has two further different configuration modes according to the status of the APL configuration bit, which changes the function of MOP, MON and LED pins as described below.

APL = 0:

In the MOP pin, the *ZCR* signal is available (see paragraph *9.5* for details on *ZCR* signal);

The pin MON provides the WatchDOG signal. The DOG signal generates a 16 ms long positive pulse every 1.6 seconds. Generation of these pulses can be suspended if data are read in intervals shorter than 1.6 ms. The DOG signal is actually a watchdog reset signal that can be used to control an operation of an on-board microcontroller. It is set to high whenever the V_{CC} voltage is below 2.5 V, but after V_{CC} goes above 2.5 V this signal starts to run.

It is expected that an application microcontroller should access the data in the metering device on regular basis, at least 1/s (recommended is 32/s). Every latching of results in the metering device requested from the microcontroller also resets the watchdog. If latching requests does not follow each other within 1.6 second, an active high pulse on MON is produced, because device assumes that microcontroller does not operate properly. This signal can be either control the RESET pin of the microcontroller or it can be tied to some interrupt pin. The second chance is recommended for a battery backup application which can enter some sleep mode due to power down condition and should not be reset by metering device.

The LED pin can be configured through LVS, FUND and KMOT to output different energy signals, as shown in the table below.

Table 18. LED pin configuration for APL = 0

LVS (1 bit)	FUND (1 bit)	KMOT (2 bits)	LED energy output	Phase	Freq
0	0	0	Active energy wide band **P**	3-ph	C (1)
		1		R	
		2		S	
		3		T	
0	1	0	Active energy fundamental **F**	3-ph	C
		1		R	
		2		S	
		3		T	
1	0	0	Reactive energy wide band **Q**	3-ph	C
		1		R	
		2		S	
		3		T	
1	1	0	Reactive energy fundamental **R**	3-ph	C
		1		R	
		2		S	
		3		T	

1. C is the number of pulses per kWh set with calibration.

APL = 1:

MOP/MON provides stepper motor driving signals from 3-phase active energy wide band register with frequency CM related to C (number of pulses on LED pin, see par. *9.11*) according to *Table 20*.

LED pin provides 3-phase energy pulses according to *Table 19* with frequency C not related to KMOT.

Table 19. LED pin configuration for APL = 1

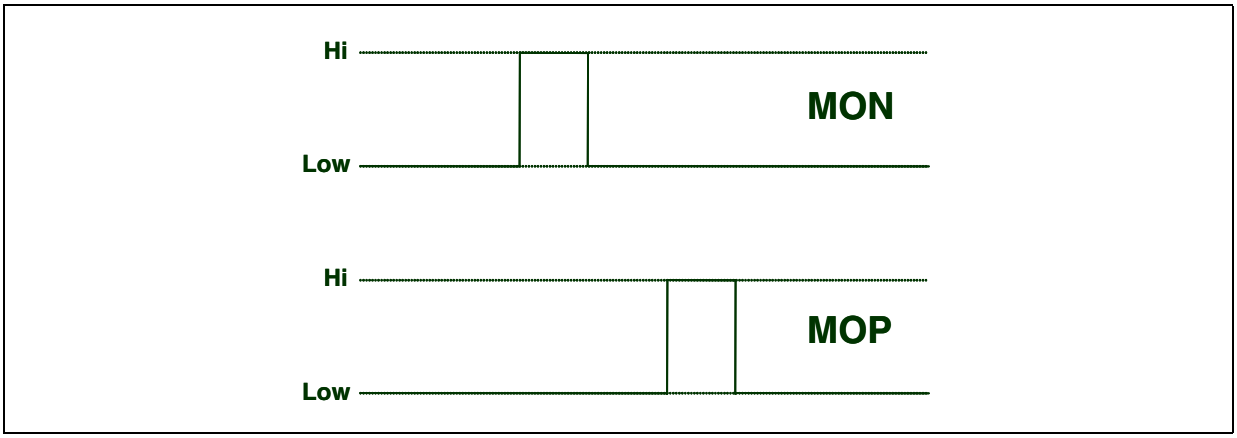
LVS (1 bit)	FUND (1 bit)	LED energy output	Phase	Freq
0	0	Active energy wide band **P**	3-ph	C
0	1	Active energy fundamental **F**		
1	0	Reactive energy wide band **Q**		
1	1	Reactive energy fundamental **R**		

9.13 Driving a stepper motor - standalone operating mode (configuration bits: APL, LVS, KMOT)

When used in standalone mode (APL[1] = 1), the STPMC1 is able to directly drive a stepper motor.

From signal P_{Σ} (3-ph active energy), stepper motor driving signals *MA* and *MB* (see *Figure 12*) are generated by means of internal divider, mono-flop and decoder and brought to MOP and MON pins.

Figure 12. Stepper driving signals



The numbers of pulses per kWh on MOP and MON outputs (CM) is related to the number of pulses on LED pin (C, see par. *9.11*) following the table below.

Table 20. Configuration of MOP and MON driving signals with APL = 1, 2, 3

LVS (1 bit)	KMOT (2 bits)	Pulses Length	Freq. CM
0	0	31.25 ms	C/64
	1		C/128
	2		C/32
	3		C/256
1	0	156.25 ms	C/640
	1		C/1280
	2		C/320
	3		C/2560

The mono-flop limits the length of the pulses according to the LVS bit value.

The decoder distributes the pulses to *MA* and *MB* alternatively, which means that each of them has only a half of selected frequency.

When a no-load condition is detected (*BIL*=1) MOP and MON are held low because integration of power is suspended.

The LED pin provides 3-phase active energy pulses according to the table below:

Table 21. LED pin configuration for APL = 2, 3

APL (2 bits)	KMOT (2 bits)	LED energy output	Phase	Freq
2	-	Active energy wide band **P**	3-ph	C
3	0	Active energy wide band **P**	3-ph	C/64
	1			C/128
	2			C/32
	3			C/256

9.14 Negative power accumulation (configuration bit ABS, status bit *SIGN*)

The ABS bits govern energy accumulation in case of negative power; they only affect active power P and fundamental active power F.

The 3-ph status bit *SIGN* depends upon 3-ph cumulative power direction while the phase status bits $SIGN_X$ depends upon phase X power direction.

Table 22 shows power calculation modes according to ABS

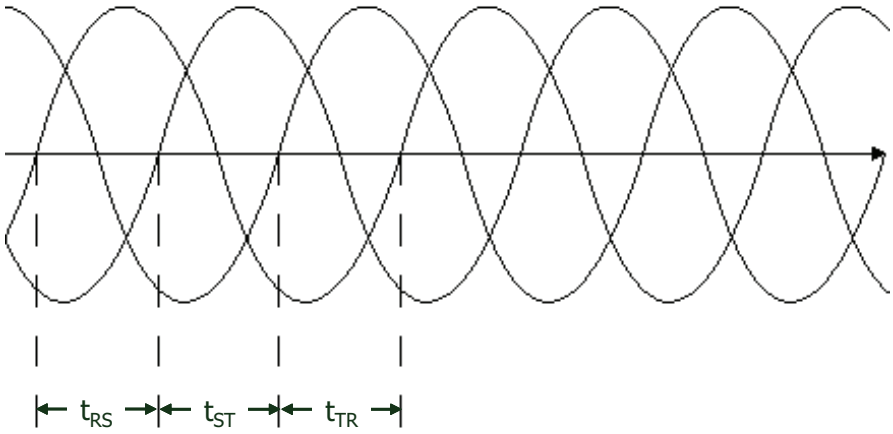
Table 22. Accumulation mode for negative power

ABS (2 bits)	Accumulation mode	Power calculation	3-ph *SIGN*	*MA - MB*
0	3-phase Ferraris mode	$P_\Sigma = P_R + P_S + P_T$	$P_\Sigma < 0 \rightarrow SIGN = 0$ $P_\Sigma \geq 0 \rightarrow SIGN = 1$	$P_\Sigma < 0 \rightarrow MA$ and MB low $P_\Sigma \geq 0 \rightarrow$ see *Figure 12*
1	Absolute accumulation per phase	$P_\Sigma = \lvert P_R \rvert + \lvert P_S \rvert + \lvert P_T \rvert$	$P_\Sigma \geq 0 \rightarrow SIGN = 1$	$P_\Sigma \geq 0 \rightarrow$ see *Figure 12*
2	Ferraris mode per phase	if $P_X < 0 \rightarrow P_X = 0$ $P_\Sigma = P_R + P_S + P_T$	$P_\Sigma \geq 0 \rightarrow SIGN = 1$	$P_\Sigma \geq 0 \rightarrow$ see *Figure 12*
3	Signed accumulation	$P_\Sigma = P_R + P_S + P_T$	$P_\Sigma < 0 \rightarrow SIGN = 0$ $P_\Sigma \geq 0 \rightarrow SIGN = 1$	$P_\Sigma < 0 \rightarrow$ see *Figure 12* $P_\Sigma \geq 0 \rightarrow$ see *Figure 12*

9.15 Phase delay calculation

The STPMC1 allows the calculation of the phase delays between voltages. If the line frequency f_{line} is 50 Hz, a 120° phase delay corresponds to 6.7 ms.

Figure 13. Phase delay



The ACR, ACS and ACT registers (bits [7:0], see paragraph 9.17.7) holds the information needed for this calculation.

Let us indicate t_{RS}, t_{ST}, t_{TR}, the delays between R, S and T phases. It is:

Equation 1

$t_{RS} + t_{ST} + t_{TR} = T = 1 / f$

Concatenating ACT[7:0], ACS[7:0], ACR[7:0] bytes, two 12 bits vectors defined as below are obtained:

ACT[7:0], ACS[7:0], ACR[7:0] = Asr[12, 10:0], Art[12, 10:0]

The delay times are calculated with the following formulas:

Equation 2

$$time_{Asr} = t_{ST} - t_{TR} = \left(Asr[10:0] - \left(2^{11}\right)^{Asr[12]} + 1 \right) \cdot \frac{8}{f_{MCLK}}$$

Equation 3

$$time_{Art} = t_{RS} - t_{ST} = \left(Art[10:0] - \left(2^{11}\right)^{Art[12]} + 1 \right) \cdot \frac{8}{f_{MCLK}}$$

From *Equation 1*, *Equation 2* and *Equation 3* it is possible to retrieve phase delays t_{RS}, t_{ST} and t_{TR}.

Example 12: Phase delay calculation

f_{XTAL1} = 4 MHz; MDIV = 0; FR1 = 0 $\rightarrow$ f_{MCLK} = 8 MHz
f_{LINE} = 50 Hz $\rightarrow$ T = 20 ms;
ACR[7:0] = 0101 1010
ACS[7:0] = 0010 0000
ACT[7:0] = 0000 0101
Asr[12] = 0
Asr[10:0] = 000 0101 0010_2 = 82
Art[12] = 0
Art[10:0] = 00001011010_2 = 90

$$time_{Asr} = \left(Asr[10:0] - \left(2^{11}\right)^{Asr[12]} + 1 \right) \cdot \frac{8}{MCLK} = \left(00001010010_2 - \left(2^{11}\right)^{0} + 1 \right) \cdot \frac{8}{8 \cdot 10^6} = +82\mu s$$

$$\Rightarrow \frac{82\mu s}{20ms} \cdot 360^\circ = +1{,}5^\circ$$

$$time_{Art} = \left(Art[10:0] - \left(2^{11}\right)^{Art[12]} + 1 \right) \cdot \frac{8}{MCLK} = \left(00001011010_2 - \left(2^{11}\right)^{0} + 1 \right) \cdot \frac{8}{8 \cdot 10^6} = +90\mu s$$

$$\Rightarrow \frac{90\mu s}{20ms} \cdot 360^\circ = +1{,}6^\circ$$

Example 13: Phase delay calculation

f_{XTAL1} = 4 MHz; MDIV = 0; FR1 = 0 $\rightarrow$ f_{MCLK} = 8 MHz
f_{LINE} = 50 Hz $\rightarrow$ T = 20 ms;
ACR[7:0] = 1011 0011
ACS[7:0] = 0011 1111
ACT[7:0] = 0000 0101
Asr[12] = 0
Asr[10:0] = 000 0101 0011_2 = 83
Art[12] = 1
Art[10:0] = 111 1011 0011_2 = 1971

$$time_{Asr} = \left(Asr[10:0] - \left(2^{11}\right)^{Asr[12]} + 1 \right) \cdot \frac{8}{MCLK} = \left(00001010011_2 - \left(2^{11}\right)^{0} + 1 \right) \cdot \frac{8}{8 \cdot 10^6} = +83\mu s$$

$$\Rightarrow \frac{83\mu s}{20ms} \cdot 360^\circ = +1{,}5^\circ$$

$$time_{Art} = \left(Art[10:0] - \left(2^{11}\right)^{Art[12]} + 1 \right) \cdot \frac{8}{MCLK} = \left(11110110011_2 - \left(2^{11}\right)^{1} + 1 \right) \cdot \frac{8}{8 \cdot 10^6} = -76\mu s$$

$$\Rightarrow \frac{-76\mu s}{20ms} \cdot 360^\circ = -1{,}4^\circ$$

9.16 Calibration (configuration bits: PM, TCS, CIX, CVX, CCA, CCB, CPX)

9.16.1 Voltage and current channels calibration

The 8-bit calibration values CVX and CIX (where X stands for N, R, S or T) are used as static data for the channel ΔΣ calibrators, multiplying their streams to the following factor:

$K_X = (4096 - 1024 + 4CXX)/4096$ (± 12.5 %)

When configuration bit PM is set, a 2-bit CvX or CiX is appended to each CVX or CIX respectively:

$K_X = (8192 - 1024 + 4CXX + CxX)/8192$ (± 6.25 %)

CvX bits are part of the CCA configuration byte while CiX are part of CCB configuration byte.

9.16.2 Phase compensation

The STPMC1 does not introduce any phase shift between voltage and current channel.

However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors.

The STPMC1 provides a means of digitally calibrating these small phase errors introducing some delay. The amount of phase compensation can be set per each phase using the 4 bits of the phase calibration configurators (CPR, CPS, CPT).

A vector method of phase shift compensation is implemented.

The compensating voltage vector, which is produced from a frequency compensated signal of integrated voltage vector multiplied by a given compensation constant per each phase and is almost perpendicular to the input voltage vector, is subtracted from the input voltage vector at the input of the decimation filter.

Those phase compensators are merged from a common coarse part CPC and from each phase 4-bit phase error compensator CPX:

CPC[1] = 0: $K_{PHC} = -(16\ CPC[0] + CPX)$

CPC[1] = 1: $K_{PHC} = (16 - CPX)$

When either PM or TCS are set, a 2-bit CpC is appended to CPC to produce the following factor:

CPC[1] = 0: $K_{PHC} = -(32\ CpC + 16\ CPC[0] + CPX)$

CPC[1] = 1: $K_{PHC} = [64 - (32\ CpC + 16\ CPC[0] + CPX)]$

CpC bits are part of the CCA configuration byte.

The equation for phase compensation in degree is:

Equation 4

$$\varphi_{phc} = K_{PHC} \frac{360° \cdot f_{line}}{f_{phc}}$$

φ_{phc} is the phase compensation in degree,

K_{PHC} is the calculated coefficient,

f_{line} is the frequency of voltage signal,

f_{phc} is the clock for phase compensation.

The clock for phase compensation f_{phc} can be derived as reported in *Table 23* and *Table 24*

Table 23. f_{phc} frequency settings

MDIV (1 bit)	PM (1 bit)	HSA (1 bit)	f_{CLK}
X	0	0	f_{XTAL1} / 8
X	0	1	f_{XTAL1} / 4
0	1	X	f_{XTAL1} / 2
1	1	X	f_{XTAL1} / 4

Table 24. f_{phc} frequency values

f_{XTAL1}	PM (1 bit)	HSA (1 bit)	f_{CLK}
4.194 MHz	0	0	524 kHz
4.195 MHz			614 kHz
8.192 MHz			1.024 MHz
9.830 MHz			1.229 MHz
4.194 MHz		1	1.049 MHz
4.195 MHz			1.229 MHz
8.192 MHz			2.048 MHz
9.830 MHz			2.458 MHz
4.194 MHz	1	X	2.097 MHz
4.195 MHz			2.458 MHz
8.192 MHz			2.048 MHz
9.830 MHz			2.458 MHz

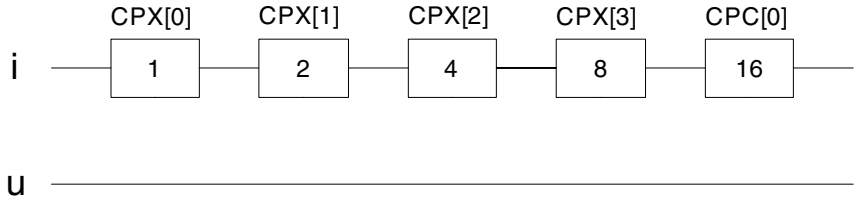
Table 25. f_{phc} frequency settings for PM = 1

f_{XTAL1}	f_{phc}
4.194 MHz	2.097 MHz
4.915 MHz	2.458 MHz
8.192 MHz	2.048 MHz
9.830 MHz	2.458 MHz

Example 14: Phase compensation for PM = 0, TCS = 0

Phase shift current for $-\varphi_{phc}$:

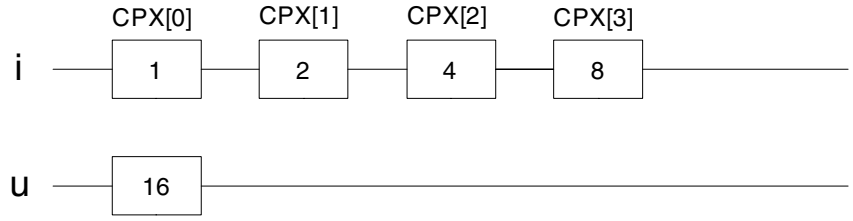
CPC[1] = 0



K_{phc} = - (16 CPC[0] + CPX[3:0])

Phase shift current for φ_{phc}:

CPC[1] = 1



K_{phc} = (16 - CPX[3:0])

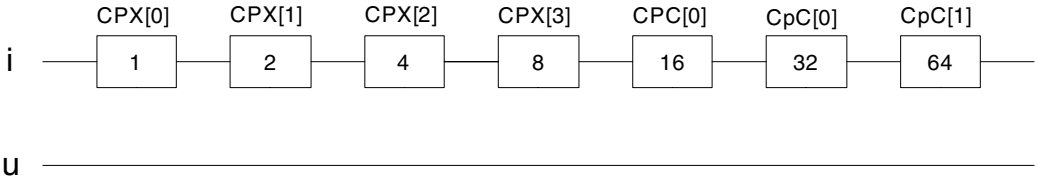
Table 26. Phase compensation for PM = 0, TCS = 0, f_{line} = 50 Hz

CLK	HSA	f_{phc}	φ_{phc}	$\Delta\varphi_{phc}$
4.194 MHz	0	524 kHz	+0.550°, -1.064°	0.034°
4.915 MHz		614 kHz	+0.469°, -0.908°	0.029°
8.192 MHz		1.024 MHz	+0.281°, -0.545°	0.018°
9.830 MHz		1.229 MHz	+0.234°, -0.454°	0.015°
4.194 MHz	1	1.049 MHz	+0.275°, -0.532°	0.017°
4.915 MHz		1.229 MHz	+0.234°, -0.454°	0.015°
8.192 MHz		2.048 MHz	+0.141°, -0.272°	0.009°
9.830 MHz		2.458 MHz	+0.117°, -0.227°	0.007°

Example 15: Phase compensation for PM = 0, TCS = 1

Phase shift current for $-\varphi_{phc}$:

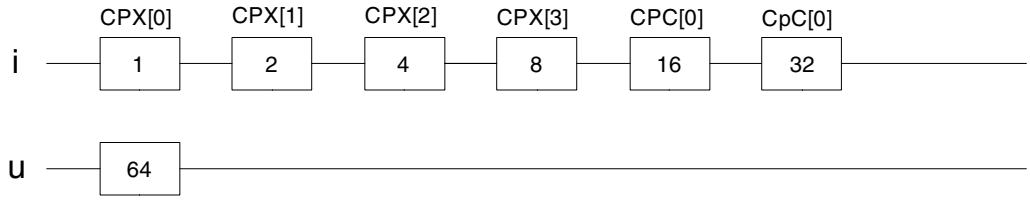
CPC[1] = 0



K_{phc} = - (32 CpC[1:0] + 16 CPC[0] + CPX[3:0])

Phase shift current for φ_{phc}:

CPC[1] = 1



K_{phc} = 64 - (32 CpC[0] + 16 CPC[0] + CPX[3:0])

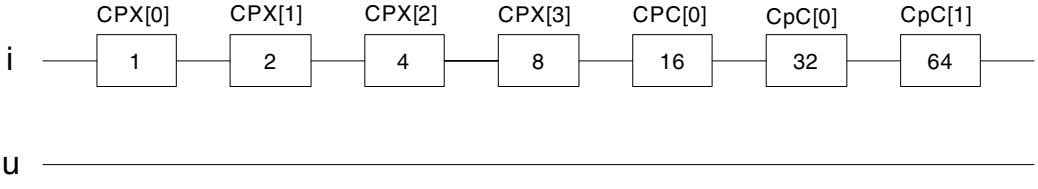
Table 27. Phase compensation for PM = 0, TCS = 1, f_{line} = 50 Hz

CLK	HSA	f_{phc}	φ_{phc}	$\Delta\varphi_{phc}$
4.194 MHz	0	524 kHz	+2.198°, -4.361°	0.034°
4.915 MHz		614 kHz	+1.876°, -3.721°	0.029°
8.192 MHz		1.024 MHz	+1.125°, -2.232°	0.018°
9.830 MHz		1.229 MHz	+0.937°, -1.860°	0.015°
4.194 MHz	1	1.049 MHz	+1.098°, -2.180°	0.017°
4.915 MHz		1.229 MHz	+0.937°, -1.860°	0.015°
8.192 MHz		2.048 MHz	+0.562°, -1.116°	0.009°
9.830 MHz		2.458 MHz	+0.469°, -0.930°	0.007°

Example 16: Phase compensation for PM = 1

Phase shift current for $-\varphi_{phc}$:

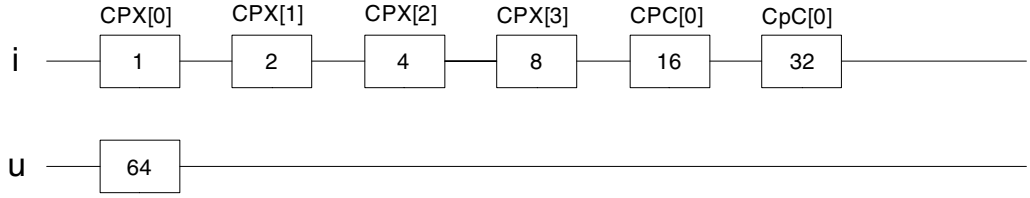
CPC[1] = 0



K_{phc} = - (32 CpC[1:0] + 16 CPC[0] + CPX[3:0])

Phase shift current for φ_{phc}:

CPC[1] = 1



K_{phc} = 64 - (32 CpC[0] + 16 CPC[0] + CPX[3:0])

Table 28. Phase compensation for PM = 1, f_{line} = 50 Hz

CLK	HSA	f_{phc}	φ_{phc}	$\Delta\varphi_{phc}$
4.194 MHz	X	2.097 MHz	+0.549°, -1.090°	0.009°
4.915 MHz		2.458 MHz	+0.469°, -0.930°	0.007°
8.192 MHz		2.048 MHz	+0.562°, -1.116°	0.009°
9.830 MHz		2.458 MHz	+0.469°, -0.930°	0.007°

9.16.3 Mutual current compensation

Mutual current compensation is available only when TCS is clear (Rogowski coil).

When PM is cleared, the CCA and CCB configuration bytes can be used for mutual current influence compensation according to SYS value.
For monophase systems (SYS > 3) the correction factors, α (alpha) and β (beta), are computed as follows:

Equation 5

$$\alpha = \frac{(-1)^{CCA[8]} \cdot CCA[7:0]}{8192} \qquad (\pm 3.1\ \%)$$

Equation 6

$$\beta = \frac{(-1)^{CCA[8]} \cdot CCB[7:0]}{8192} \qquad (\pm 3.1\ \%)$$

An asymmetrical compensation is implemented by multiplying the phase current with α and the neutral current with β and these values are subtracted from neutral and phase currents respectively, as shown below:

Table 29. Mutual current compensation matrix for single-phase systems (SYS > 3)

phase	S	T
S	-	β
T	α	-

$i_{CS} = \beta\, i_T$

$i_{CT} = \alpha\, i_S$

For other values of SYS, the values of CCA and CCB three correction factors, a 7-bit α, 6-bit β and 4-bit γ (gamma) are calculated as follows:

Equation 7

$$\alpha = \frac{(-1)^{CCA[8]} \cdot CCA[5:0]}{8192} \qquad (\pm 0.78\ \%)$$

Equation 8

$$\beta = \frac{(-1)^{CCA[7]} \cdot CCB[7:3]}{8192} \qquad (\pm 0.39\ \%)$$

Equation 9

$$\gamma = \frac{(-1)^{CCA[6]} \cdot CCB[2:0]}{8192} \qquad (\pm 0.09\ \%)$$

From these factors a 4 x 4 matrix, shown in *Table 30*, implements a symmetrical compensation multiplying each phase and neutral current with its row, adding the products together and subtracting them from the currents.

Table 30. Mutual current compensation matrix for three-phase systems (SYS < 4)

phase	R	S	T	N
R	-	α	β	γ
S	α	-	α	β
T	β	α	-	α
N	γ	β	α	-

$i_{CR} = \alpha\, i_S + \beta\, i_T + \gamma\, i_N$

$i_{CS} = \alpha\, i_R + \alpha\, i_T + \beta\, i_N$

$i_{CT} = \alpha\, i_N + \alpha\, i_S + \beta\, i_R$

$i_{CN} = \alpha\, i_T + \beta\, i_S + \gamma\, i_R$

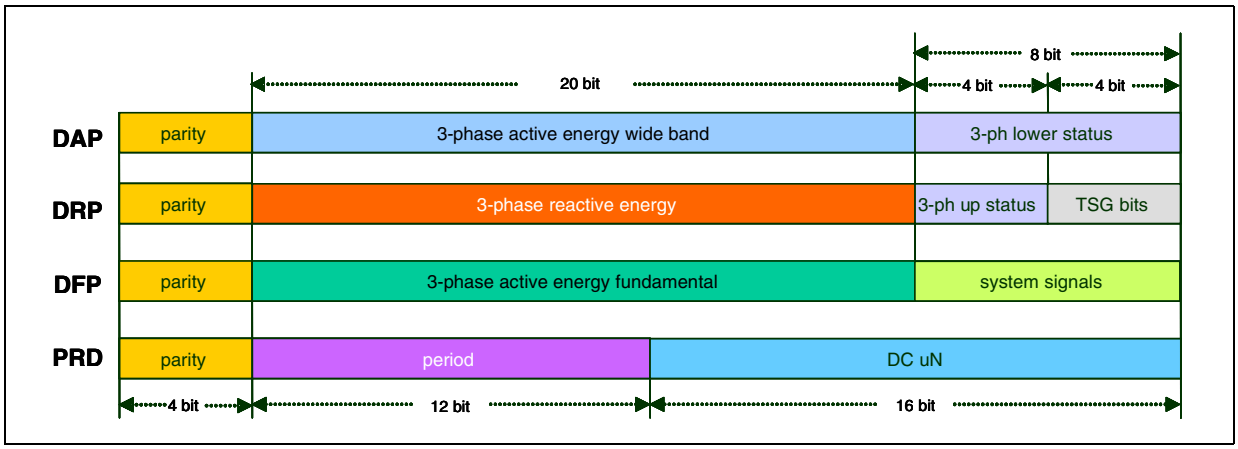
9.17 Data records map

There are seven groups of four data records available, each consisting of a parity nibble (see paragraph *9.17.8*) and 28-bit data field.

The data records have fixed position of reading. This means that no addressing of records is necessary. It is up to an application to decide how many records should read out from the device. If an application sends to device a precharge command (see paragraph *9.20*) before the reading of a group, the internal group pointer is incremented. This way, a faster access to later groups is possible. Below are shown all the groups, their position within the sequence of reading, and the name and assembly of data records.

9.17.1 Group 0 data records

Figure 14. Group 0 data records



0.1 DAP:

- 3- phase active energy wide band: 20-bit accumulator of 3-ph active energy wide band (see paragraph *9.11*)
- 3-ph lower status: bits [0:7] of 3-phase status (see *Table 31*)

0.2 DRP:

- 3- phase reactive energy: 20-bit accumulator of 3-ph reactive energy (see paragraph *9.11*)
- 3-ph up status: bits [8:11] of 3-phase status (see *Table 31*)
- TSG bits: 4 TSG mode signal (see paragraph *9.20*)

0.3 DFP:

- 3-phase active energy fundamental: 20-bit accumulator of 3-ph active energy from fundamental harmonic (see paragraph *9.11*)
- system signals: commands BANK-PUMP-TST0-TST1-TST2-RD-WE-precharge (see paragraph *9.20*)

0.4 PRD:

- period: 12-bit line period measurement (see paragraph *9.6*). By default it is calculated from R-phase signal, if it is missing from S-phase then from T-phase. The value of the period can be calculated from the decimal value of period as:

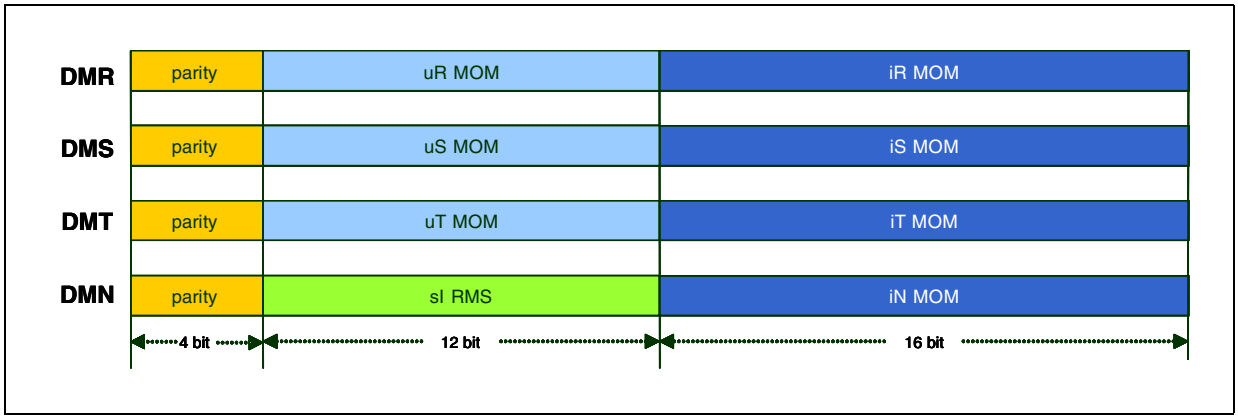
Equation 10

$$T = \frac{period \cdot 2^6}{f_{MCLK}}$$

- DC uN: 16-bit DC component of voltage channel of NDSP. It may be DAN-V or DAH according to the value of ENH bit. For example it is DC offset in sigma delta uN if ENH=0, or DC value of magnetic field if ENH is set and a magnetic sensor is connected via STPMSx on DAH input.

9.17.2 Group 1 data records

Figure 15. Group 1 data records



1.1 DMR:

- uR MOM: 12-bit momentary value of R phase voltage
- iR MOM: 16-bit momentary value of R phase current

1.2 DMS:

- uS MOM: 12-bit momentary value of S phase voltage
- iS MOM: 16-bit momentary value of S phase current

1.3 DMT:

- uT MOM: 12-bit momentary value of T phase voltage
- iT MOM: 16-bit momentary value of T phase current

1.4 DMN:

- sI RMS: 12-bit RMS value of the sum of all the instantaneous currents ($i_R + i_S + i_T + i_N$) divided by four:

Equation 11

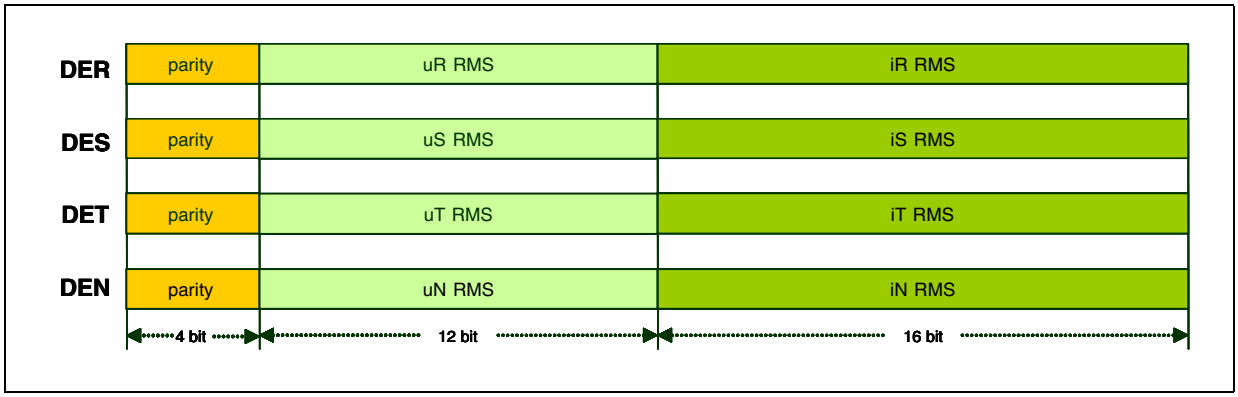
$$sIRMS = \left(\sum \frac{i_X}{4} \right)_{RMS}$$

- iN MOM: 16-bit momentary value of neutral current

Note: In systems 3-phase, no neutral, u_{ST}, u_{TR}, u_{RS} replace u_R, u_S, u_T respectively.

9.17.3 Group 2 data records

Figure 16. Group 2 data records



2.1 DER:

- uR RMS: 12-bit RMS value of R phase voltage
- iR RMS: 16-bit RMS value of R phase current

2.2 DES:

- uS RMS: 12-bit RMS value of S phase voltage
- iS RMS: 16-bit RMS value of S phase current

2.3 DET:

- uT RMS: 12-bit RMS value of T phase voltage
- iT RMS: 16-bit RMS value of T phase current

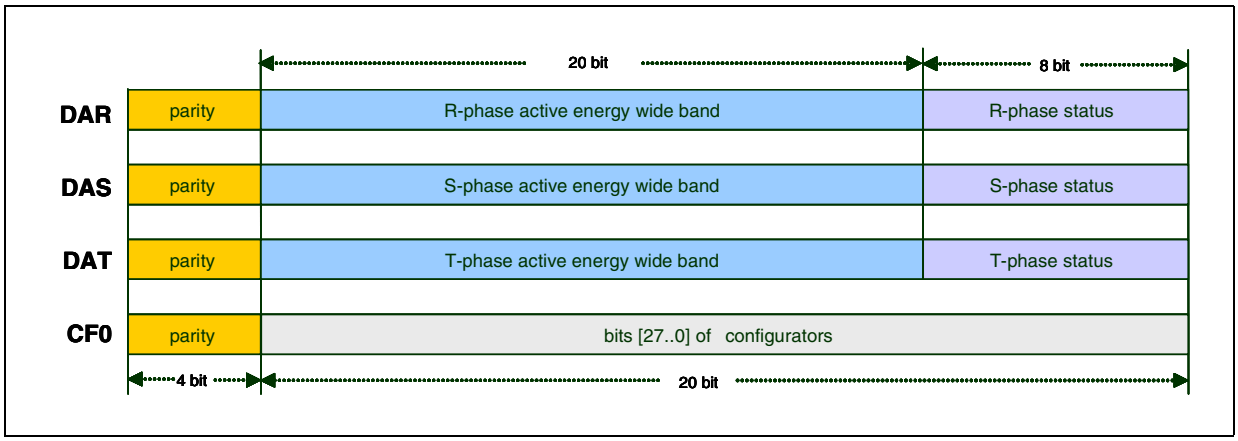
2.4 DEN:

- uN RMS: 12-bit RMS value of voltage channel of NDSP. It may be DAN-V or DAH according to the value of ENH bit.
- iN RMS: 16-bit RMS value of neutral current

Note: In systems 3-phase, no neutral, U_{ST}, U_{TR}, U_{RS} replace U_R, U_S, U_T respectively.

9.17.4 Group 3 data records

Figure 17. Group 3 data records



3.1 DAR:

- R-phase active energy wide band: 20-bit accumulator of R phase active energy wide band
- R-phase status: 8-bit R phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase R active energy wide band.

3.2 DAS:

- S-phase active energy wide band: 20-bit accumulator of S phase active energy wide band
- S-phase status: 8-bit S phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase S active energy wide band.

3.3 DAT:

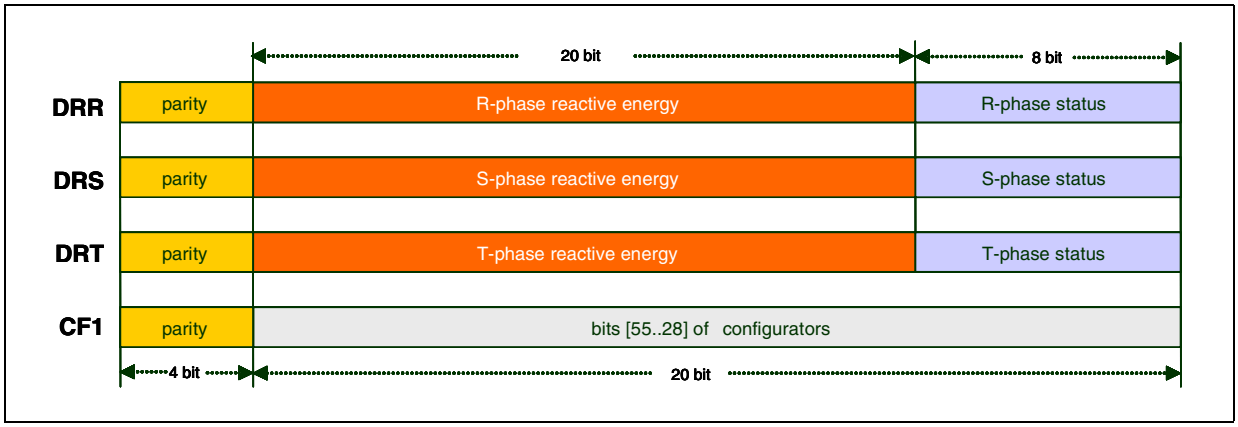
- phase active energy wide band: 20-bit accumulator of T phase active energy wide band
- T-phase status: 8-bit T phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase T active energy wide band.

3.4 CF0:

- bits [27..0] of configurators (see *Table 33*).

9.17.5 Group 4 data records

Figure 18. Group 4 data records



4.1 DRR:

- R-phase reactive energy: 20-bit accumulator of R phase reactive energy.
- R-phase status: 8-bit R phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase R reactive energy.

4.2 DRS:

- S-phase reactive energy wide band: 20-bit accumulator of S phase reactive energy
- S-phase status: 8-bit S phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase S reactive energy.

4.3 DRT:

- T-phase reactive energy wide band: 20-bit accumulator of T phase reactive energy
- T-phase status: 8-bit T phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase T reactive energy.

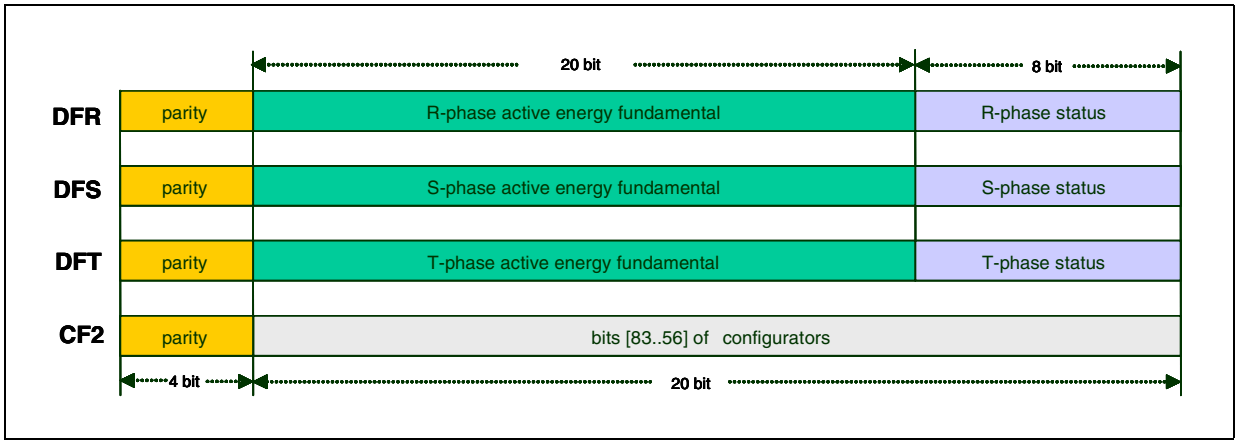
4.4 CF1:

- bits [55..28] of configurators (see *Table 33*)

Note: When the configuration bit FUND is set, fundamental reactive energy replaces full bandwidth reactive energy.

9.17.6 Group 5 data records

Figure 19. Group 5 data records



5.1 DFR:

- R-phase active energy fundamental: 20-bit accumulator of R phase active energy from fundamental harmonic
- R-phase status: 8-bit R phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase R active energy fundamental.

5.2 DFS:

- S-phase active energy fundamental: 20-bit accumulator of S phase active energy from fundamental harmonic
- S-phase status: 8-bit S phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase S active energy fundamental.

5.3 DFT:

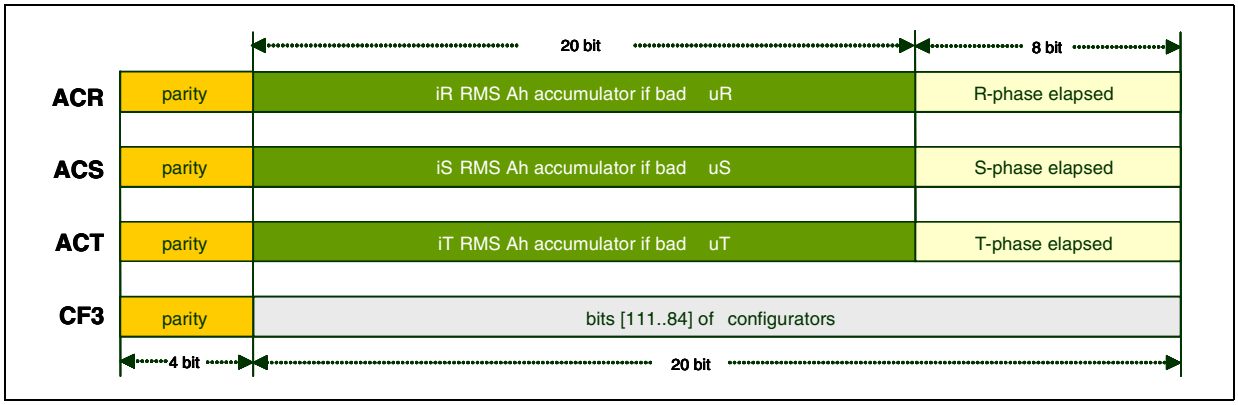
- T-phase active energy fundamental: 20-bit accumulator of T phase active energy from fundamental harmonic
- T-phase status: 8-bit T phase status (see *Table 32*). Bit [0] (*BIL*) represents no-load condition for phase T active energy fundamental.

5.4 CF2:

- bits [83..56] of configurators (see *Table 33*)

9.17.7 Group 6 data records

Figure 20. Group 6 data records



6.1 ACR:

- iR RMS SWM accumulator: 20-bit accumulator of R phase current in SWM mode (see paragraph *9.7*)
- R-phase elapsed: phase delay (see paragraph *9.15*)

6.2 ACS:

- iS RMS SWM accumulator: 20-bit accumulator of S phase current in SWM mode (see paragraph *9.7*)
- S-phase elapsed: phase delay (see paragraph *9.15*)

6.3 ACT:

- iT RMS SWM accumulator: 20-bit accumulator of T phase current in SWM mode (see paragraph *9.7*)
- T-phase elapsed: phase delay (see paragraph *9.15*)

6.4 CF3:

- bits [111..84] of configurators (see *Table 33*)

9.17.8 Parity calculation

Each bit of parity nibble is defined as odd parity of all seven corresponding bits of data nibbles. In order to check the data record integrity, the application might execute the following C code, given as an example:

```
int BadParity (unsigned char *bp)
{register unsigned char prty = grp;/* temp register set to group #
(0..6)*/
  prty ^= *bp;              /* xor it with 1st byte of data */
  prty ^= *(bp+1);          /* xor it with the 2nd byte */
  prty ^= *(bp+2);          /* and with the 3rd byte */
  prty ^= *(bp+3);          /* and last, with the 4th byte */
  prty ^= prty<<4;          /* combine */
  prty &= 0xF0;             /* remove the lower nibble */
  return (prty != 0xF0);    /* returns 1, if bad parity */}
```

Example 17: Parity calculation

Let us calculate parity of DMR, the first register of second group:

DMR: 02 80 00 C8

```
prty = grp = 1              /* prty set to 1 - group #*/
prty ^= *bp = 3             /* xor it with 1st byte of data 02 */
prty ^= *(bp+1) = 83        /* xor it with the 2nd byte 80 */
prty ^= *(bp+2) = 83        /* and with the 3rd byte 00 */
prty ^= *(bp+3) = 4B        /* and last, with the 4th byte C8 */
prty ^= prty<<4 = FB        /* and with B0 */
prty &= 0xF0 = F0           /* parity is ok */
```

9.18 Status bits map

The STPMC1 includes 12 status bits for 3-phase cumulative, and 3 8-bit status byte, one per each phase. All of them provide information about the current meter status.

Table 31. 3-phase status bits description

Bit	Name	0	1
0	*BIL*	No-load condition not detected in any phase	No-load condition detected in all phases
1	*BCF*	ΣΔ signals alive in all phases	ΣΔ signal stuck in at least one phase
2	*BFF*	*BFR* = 0 in all phases	*BFR* = 1 in at least one phase
3	SIGN	Three-phase active energy is negative	Three-phase active energy is positive
4	PHR	Phase $0 \le u_R < \pi$	Phase $\pi \le u_R < 2\pi$
5	PHS	Phase $0 \le u_S < \pi$	Phase $\pi \le u_S < 2\pi$
6	PHT	Phase $0 \le u_T < \pi$	Phase $\pi \le u_T < 2\pi$
7	*HLT*	Data records reading is valid	Data records are not valid. A reset occurred and a restart is in progress.
8	*PIN*	The output pins are consistent with the data	The output pins are different from the data, this means some output pin is forced to 1 or 0.
9	*BCS*	Sum of all phase currents is below threshold	Sum of all currents above threshold
10	*BSF*	Phase sequence is R -> S -> T	Phase sequence is not R -> S -> T
11	*BIF*	Phase energies have equal sign	Phase energies do not have equal sign

Table 32. X-phase status bits description

Bit	Name	0	1
0	*BIL*	No-load Condition not detected	No-load condition detected
1	*BCF*	ΣΔ signals alive	One or both ΣΔ signal stuck
2	*BFR*	Frequency of phase voltage is in range	Frequency of line voltage is out of range or voltage amplitude is below threshold (*LOW* = 1)
3	SIGN	Active energy is negative	Active energy is positive
4	*LIN*	Phase $0 \leq u < \pi$	Phase $\pi \leq u < 2\pi$
5	ZRC	After zero crossing	After max value crossing
6	*LOW*	$U_x > U_{Xmax} / 16$	$U_x < U_{Xmax} / 32$
7	*NAH*	Single Wire Meter mode $I_X > I_{Xmax}$ /4096 and *BFR*==1	Normal operation mode *BFR*==0 or $I_X < I_{Xmax}$ / 8192 and *BFR*==1

$U_{Xmax} = 2^{12}$

$I_{Xmax} = 2^{16}$

There is no differences between status register of x phase in DAx, DRx, DFx, except for first bit of status register [0] *BIL*. This bit indicates no-load condition.

In DAx status register bit *BIL* is represents NLC for phase X active energy.

In DRx status register bit *BIL* is represents NLC for phase X reactive energy.

In DFx status register bit *BIL* is represents NLC for phase X fundamental energy.

In standalone operating mode the 3-ph *BIL* signal is available on SCLNLC pin, 3-ph SIGN in the SYN pin and Tamper flag (is the OR of all tamper conditions - see paragraph *9.10*) in SDATD pin. All the other signals can be read only through SPI interface.

When STPMC1 is used in peripheral mode all these signals can be read through the SPI interface. See paragraph *9.18* for details on the Status bit location in the STPMC1 data records.

9.19 Configuration bits map

As indicated in the data records map (see paragraph *9.17*), the STPMC1 has 112 configuration bits (CFG data records). Each of them consists of paired elements, one is the latch (the OTP shadow), and the other is the OTP antifuse element. In this way all the configuration bits that control the operation of the device can be written in a temporary or permanent way.

In case of temporary writing the configuration bits values are written in the so-called shadow registers, which are simple latches that hold the configuration data. The shadow registers are cleared whenever a reset condition occurs (both POR and remote reset).

In case of permanent writing the configuration bits are stored in the OTP (one time programmable) cells that keep the information permanently even if the STPMC1 is without supply, but, once written, they cannot be changed anymore. That's why the CFG are used to keep critical informations like configuration and calibration values of device. When the STPMC1 is released all antifuses presents low logic state.

Each configuration bit can be written sending a byte command to STPMC1 through its SPI interface. See paragraph *9.21* for details on SPI operation.

A system signal WE (see paragraph *9.20*) is used in order to do the permanent write of some OTP bit. There is also a special high voltage input pad VOTP, which delivers the power level necessary for permanent write to OTP cell.

The STPMC1 can work either using the data stored in the OTP cells or the data from the shadow latches. This is done through the RD system signal (see paragraph *9.20*). If RD is set, the CFG bits originates from corresponding OTP shadow latches otherwise, if RD is cleared, the CFG bits originates from corresponding OTP antifuses. In this way it is possible to test temporary configurators and calibrators before writing permanently on the device, for example during meter production tests.

The very first CFG bit, called TSTD, disables any further OTP writing. After TSTD bit has been set, the only commands accepted are the mode signal precharge (see paragraph *9.20*) and the remote reset request (see paragraph *9.21.1*), this implies that the test mode is disabled and shadow latches cannot be used as source of configuration data anymore.

The following table represents a collection and function of all configuration bits in the device. For multibit configurations the most significant bit address is **bold**.

Table 33. Configuration bits map

Address		Name	N. of bits	Description IMPORTANT: The decimal value indicated in this column represents the value of the configuration bits with MSB in bold.
7-BIT Binary	DEC			
0000000	0	TSTD	1	Test mode and OTP write disable: - TSTD=0: enable test modes and system signals, - TSTD=1: normal operation and no more writes to OTP or test modes
0000001	1	MDIV	1	Selection of measurement clock option: - MDIV=0: $f_{MCLK} = f_{XTAL1} * 2$, - MDIV=1: $f_{MCLK} = f_{XTAL1}$
0000010	2	HSA	1	High speed analog clock selection: - HSA=0: $f_{CLK} = f_{XTAL1}/4$, - HSA=1: $f_{CLK} = f_{XTAL1}/2$
0000011 0000100	3 4	APL	2	Application type selection: - APL=0: peripheral MOP, MON=*ZCR*, WatchDOG, LED=pulses (X), - APL=1: peripheral MOP, MON=stepper(P), LED=pulses (X), - APL=2: standalone MOP, MON=stepper(P), LED=pulses(P), SCLNLC=no-load SDATD=tamper detected, SYN=neg act power - APL=3: standalone, MOP,MON=stepper(P) LED=pulses (P/64) SCLNLC=no-load, SDATD=tamper indicator, SYN=neg act power
0000101	5	TCS	1	Type of current sensor selection: - TCS=0: Rogowski coil, - TCS=1: Current transformer (CT)
0000110	6	FRS	1	Nominal base frequency: - FRS=0: 50Hz - FRS=1: 60Hz
0000111	7	FUND		Fundamental active and reactive energy: - FUND=0: full bandwidth active energy controls the stepper; full bandwidth reactive energy computation. - FUND=1: fundamental active energy controls the stepper; fundamental reactive energy computation

Table 33. Configuration bits map (continued)

Address		Name	N. of bits	Description IMPORTANT: The decimal value indicated in this column represents the value of the configuration bits with MSB in bold.
7-BIT Binary	DEC			
0001000	8	ART	1	Reactive energy computation algorithm: - ART=0: natural computation - ART=1: artificial computation – not allowed if FUND =1
0001001	9	MSBF	1	Bit sequence output during record data reading selection: - MSBF=0: msb first - MSBF=1: lsb first
0001010 0001011	10 **11**	ABS	2	Negative power accumulation type: - ABS=0: 3-phase Ferraris, - ABS=1: absolute accumulation per phase - ABS=2: Ferraris per phase, - ABS=3: signed accumulation
0001100 0001101	12 **13**	LTCH	2	No-load condition threshold: - LTCH=0: 0,00125 * FS, - LTCH=1: 0,0025 * FS - LTCH=2: 0,005 * FS - LTCH=3: 0,010 * FS
0001110 0001111	14 **15**	KMOT	2	If APL=0 output selection for LED pin: KMOT=0 KMOT=1 KMOT=2 KMOT=3 3-phase R phase S phase T phase If APL = 1, 2, 3 pulsed output divider: If LVS=0, KMOT=0 KMOT=1 KMOT=2 KMOT=3 P/64 P/128 P/32 P/256 The constants at LVS=0 is valid also for LED when APL=3 If LVS=1, KMOT=0 KMOT=1 KMOT=2 KMOT=3 P/640 P/1280 P/320 P/2560

0010000	16	LVS	1	if APL = 0, 1 Selection of pulses(X) for LED:
				- LVS=0: active power,
				- LVS=1: reactive power.
				if APL = 1, 2, 3 Type of stepper selection:
				- LVS=0: 10 poles, 30ms, 5V stepper,
				- LVS=1: 2 poles, 150ms, 3V stepper

0010001 0010010 0010011	17 18 **19**	SYS	3	Measurement system selection: - SYS=0: 3-phase, 4-wire RSTN, 4-systxem RSTN (tamper) - SYS=1: 3-phase, 4-wire RSTN, 3-system RST_ - SYS=2: 3-phase, 3-wire RST_, 3-system RST_ (tamper) - SYS=3: 3-phase, 3-wire RST_, 2-system R_T_ (Aron) - SYS=4: 2-phase, 3-wire _STN, 2-system _ST_ (America) - SYS=5: 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:coil) - SYS=6: 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:shunt) - SYS=7: 1-phase, 2-wire __TN, 1-system __T_
0010100	20	SCLP	1	Polarity of SCLNLC idle state selection: - SCLP=0: idle state SCLNLC=1, - SCLP=1: idle state SCLNLC=0

Table 33. Configuration bits map (continued)

Address		Name	N. of bits	Description **IMPORTANT: The decimal value indicated in this column represents the value of the configuration bits with MSB in bold.**
7-BIT Binary	**DEC**			
0010101	21	PM	1	Precision meter: - PM=0: Class 1, - PM=1: Class 0.1
0010110	22	FR1	1	Selection of measurement clock value: - FR1=0: f_{MCLK} =8.192 MHz, - FR1=1: f_{MCLK} =9.8304 MHz
0010111 0011000 0011001 0011010 0011011 0011100 0011101 0011110 0011111	23 24 25 26 27 28 29 30 **31**	CCA	9	- **PM=0**, **TCS=0:** Mutual current influence compensation data A SYS = 0, 1, 2, 3 SYS = 4, 5, 6, 7 CCA[8] = sign α CCA[8] = sign α CCA[7] = sign β CCA[7..0] = α CCA[6] = sign γ CCA[5..0] = α - **PM=1**: Calibration extenders for voltage and phase CCA[8..7] = CvT CCA[6..5] = CvS CCA[4..3] = CvR CCA[1..0] = CpC
0100000 0100001 0100010 0100011 0100100 0100101 0100110 0100111	32 33 34 35 36 37 38 **39**	CIN	8	Calibration data for current channel of neutral conductor
0101000 0101001 0101010 0101011 0101100 0101101 0101110 0101111	40 41 42 43 44 45 46 **47**	CIR	8	Calibration data for current channel of phase R
0110000 0110001 0110010 0110011 0110100 0110101 0110110 0110111	48 49 50 51 52 53 54 **55**	CIS	8	Calibration data for current channel of phase S
0111000 0111001 0111010 0111011 0111100 0111101 0111110 0111111	56 57 58 59 60 61 62 **63**	CIT	8	Calibration data for current channel of phase T

Table 33. Configuration bits map (continued)

Address		Name	N. of bits	Description IMPORTANT: The decimal value indicated in this column represents the value of the configuration bits with MSB in bold.
7-BIT Binary	DEC			
1000000 1000001 1000010 1000011 1000100 1000101 1000110 1000111	64 65 66 67 68 69 70 **71**	CVR	8	Calibration data for voltage channel of phase R
1001000 1001001 1001010 1001011 1001100 1001101 1001110 1001111	72 73 74 75 76 77 78 **79**	CVS	8	Calibration data for voltage channel of phase S
1010000 1010001 1010010 1010011 1010100 1010101 1010110 1010111	80 81 82 83 84 85 86 **87**	CVT	8	Calibration data for voltage channel of phase T
1011000 1011001 1011010 1011011	88 89 90 **91**	CPR	4	Compensation of phase error of phase R
1011100 1011101 1011110 1011111	92 93 94 **95**	CPS	4	Compensation of phase error of phase S
1100000 1100001 1100010 1100011	96 97 98 **99**	CPT	4	Compensation of phase error of phase T
1100100 1100101 1100110 1100111 1101000 1101001 1101010 1101011	100 101 102 103 104 105 106 **107**	CCB	8	- **PM=0**, **TCS=0:** Mutual current influence compensation data B SYS = 0, 1, 2, 3 SYS = 4, 5, 6, 7 CCB[7..3] = β CCB[7..0] = β CCB[2..0] = γ - **PM=1**: Calibration extenders for current CCB[7..6] = CiT CCB[5..4] = CiS CCB[3..2] = CiR CCB[1..0] = CiN
1101100 1101101	108 **109**	CPC	2	Common sign and coarse phase error compensation

Table 33. Configuration bits map (continued)

Address		Name	N. of bits	Description IMPORTANT: The decimal value indicated in this column represents the value of the configuration bits with MSB in bold.
7-BIT Binary	DEC			
1101110	110	ENH	1	Fifth data input enable: - ENH=0: Voltage#0=DAN, - ENH=1: Voltage#0=DAH
1101111	111	CHK	1	Reserved – Must be always set to 1

9.20 Mode signals

The STPMC1 includes 12 Mode signals located in the DRP and DFP registers, some are used for internal testing purposes while others are useful to change some of the operation of the STPMC1. The mode signals are not retained when the STPMC1 supply is not available and then they are cleared when a POR occurs, while they are not cleared when a remote reset command (RRR) is sent through SPI.

The mode signal bit can be written using the normal writing procedure of the SPI interface (see SPI section).

In the table below the commands to change mode signals are given.

Table 34. Mode signals description

Bit pos. 76543210	REGISTER	Functional description of commands for changing system signals (X, D, A = {0, 1})	
D1110000	DRP	TSG0=D,	Controls the transmission latches when APL>1
D1110001	DRP	TSG1=D	Reserved
D1110010	DRP	TSG2=D	Reserved
D1110011	DRP	TSG3=D	Reserved
D1111000	DFP	BANK=D	Reserved
D1111001	DFP	PUMP=D	Charge pump mode of **MOP**:**MON** switch ON/OFF signal
D1111010	DFP	TST0=D	Reserved
D1111011	DFP	TST1=D	Reserved
D1111100	DFP	TST2=D	Reserved
D1111101	DFP	RD=D	Read disable of OTP block, CFG = (RD == 0)? OTP: shadow
D1111110	DFP	WE=D	Write enable, WE = 1 execute permanent write to OTP cell
X1111111	DFP	Precharge	Increments group data record pointer

RD mode signal has been already described in paragraph *9.19* but there is another implied function of the signal RD. When it is set, each sense amplifier is disconnected from corresponding antifuse element and this way, its 3 V NMOS gate is protected from the high voltage of VOTP during permanent write operation. This means that as long as the VOTP voltage reads more than 3 V, the signal RD should be set.

PUMP: when set, the PUMP mode signal transform the MOP and MON pins to act as driving signals to implement a charge-pump DC-DC converter. This feature is useful in order

to boost the V_{CC} supply voltage of the STPMC1 to generate the VOTP voltage (14 V to 20 V) needed to program the OTP antifuse elements.

WE (write Enable): This mode signal is used to permanently write to the OTP antifuse element. When this bit is not set, any write to the configuration bit is recorded in the shadow latches. When this bit is set the writing is recorded both in the shadow latch and in the OTP antifuse element.

Precharge: this command increments the index register while reading. After reading a 32-bit data record it is possible to access next group data records by sending this command. This way, a faster access to later groups is possible.

TSG0: In standalone mode it is possible to produce a data latching request by a pulse on test signal TSG0. In fact in such configuration is not possible to latch internal data into transmission latches because the **SYN** is an output pin as long as **SCS** is in idle state and it is under control of an indicator signal of negative power.

After TSTD configuration bit is set, only the precharge and TSGx commands can be executed.

9.21 SPI interface (configuration bit SCLP)

The SPI interface supports a simple serial protocol, which is implemented in order to enable a communication between some master system (microcontroller or PC) and the device. Three tasks can be performed with this interface:

- remotely resetting the device,
- reading data records,
- writing the mode bits and the configuration bits (temporarily or permanently);

Four pins of the device are dedicated to this purpose: SCS, SYN, SCLNCN, SDATD. SCS, SYN and SCLNLC are all input pins while SDATD can be input or output according if the SPI is in write or read mode. A high level signal for these pins means a voltage level higher than 0.75 x V_{CC}, while a low level signal means a voltage value lower than 0.25 x V_{CC}.

The STPMC1 internal registers are not directly accessible, rather a 32-bit of transmission latches are used to pre-load the data before being read or written to the internal registers.

The condition in which SCS, SYN and SCLNLC inputs are set to high level determines the idle state of the SPI interface and no data transfer occurs.

As previously described in the document, when the STPMC1 is in standalone mode, SYN, SCLNLC and SDATD can provide information on the meter status (see programmable pin functions) and are not used for SPI communication. In this section, the SYN, SCLNLC and SDATD operation as part of the SPI interface is described.

SCS: when low, SCS pin enables SPI communication, both in standalone and in peripheral operating mode. This means that the master can abort any task in any phase by deactivation of SCS. In standalone mode SCS high enables SYN, SCLNLC and SDATD to output meter status.

SYN: this pin operates different functions according to the status of SCS pin. When SCS is low the SYN pin status select if the SPI is in read (SYN = 1) or write mode (SYN = 0). When SCS is high and SYN is also high the results of the input or output data are transferred to the transmission latches.

SCLNLC: it is basically the clock pin of the SPI interface. Configuration bit SCLP controls the polarity of the clock (see configuration bits map). This pin function is also controlled by

the SCS status. If SCS is low, SCLNCL is the input of serial bit synchronization clock signal. When SCS is high, SCLNLC determines idle state of the SPI.

SDATD: is the data pin. If SCS is low, the operation of SDATD is dependent on the status of SYN pin. If SYN is high SDATD is the output of serial bit data (read mode) if SYN is low SDATD is the input of serial bit data signal (write mode). If SCS is high SDATD is input of idle signal.

Any of the pins above has an internal weak pull-up device of a nominal 15 A. This means that when a pin is not forced by external signals, the state of the pin is logic high. A high state of any of the input pins above is considered in an idle (not active) state.

For the SPI to operate correctly the STPMC1 must be correctly supplied as described in the power supply section. Idle state of SPI module is recognized when the signals of pins SYN, SCS, SCLNLC and SDATD are in a logic high state. Any SPI operations should start from such an idle state. The exception to this rule is when the STPMC1 has been put into standalone application mode. In this mode it is possible that the states of the pins SCLNLC, SDATD and SYN are not high due to the states of the corresponding internal status bits.

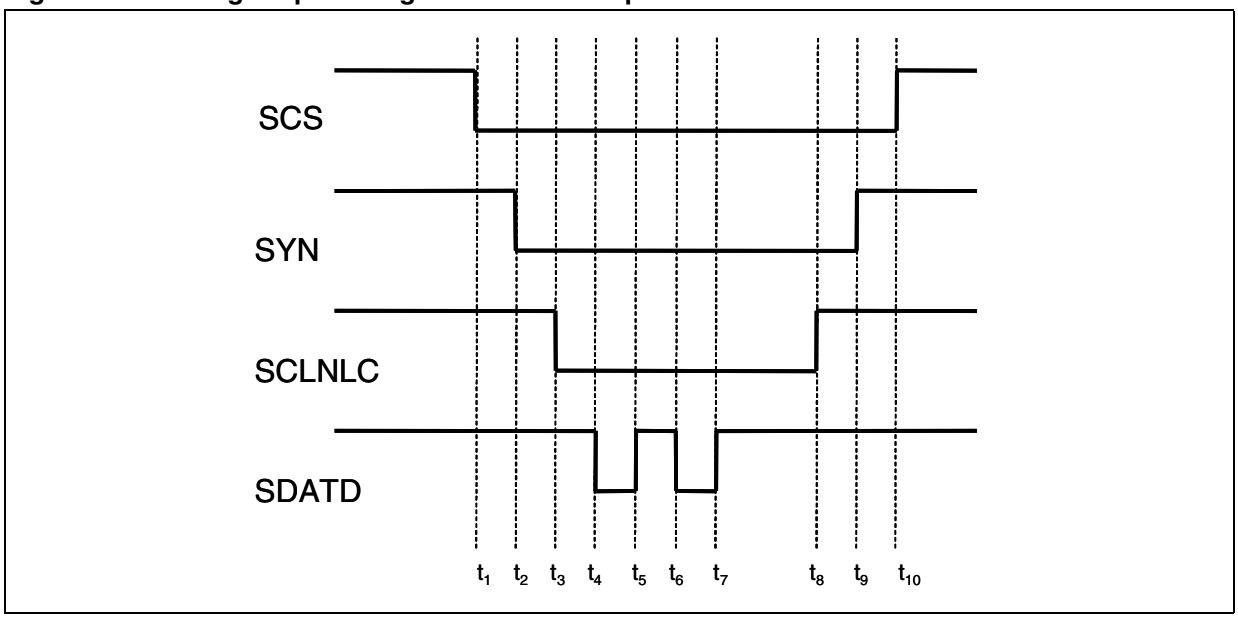
When SCS is active (low), signal SDATD should change its state at the trailing edge of the signal SCLNLC and signal SDATD should be stable at the next leading edge of signal SCLNLC. The first valid bit of SDATD is always started with activation of signal SCLNLC.

9.21.1 Remote reset

The timing diagram of the operation is shown in remote reset request timing. The time step can be as short as 30 ns.

The internal reset signal is called RRR. Unlike the POR, the RRR signal does not cause the 125 ms delayed restart of the digital module. This signal does not clear the mode signals.

Figure 21. Timing for providing remote reset request



Note: All the time intervals must be longer than 30 ns.
t_7 -> t_8 is the reset time, this interval must be longer than 30 ns as well.

9.21.2 Reading data records

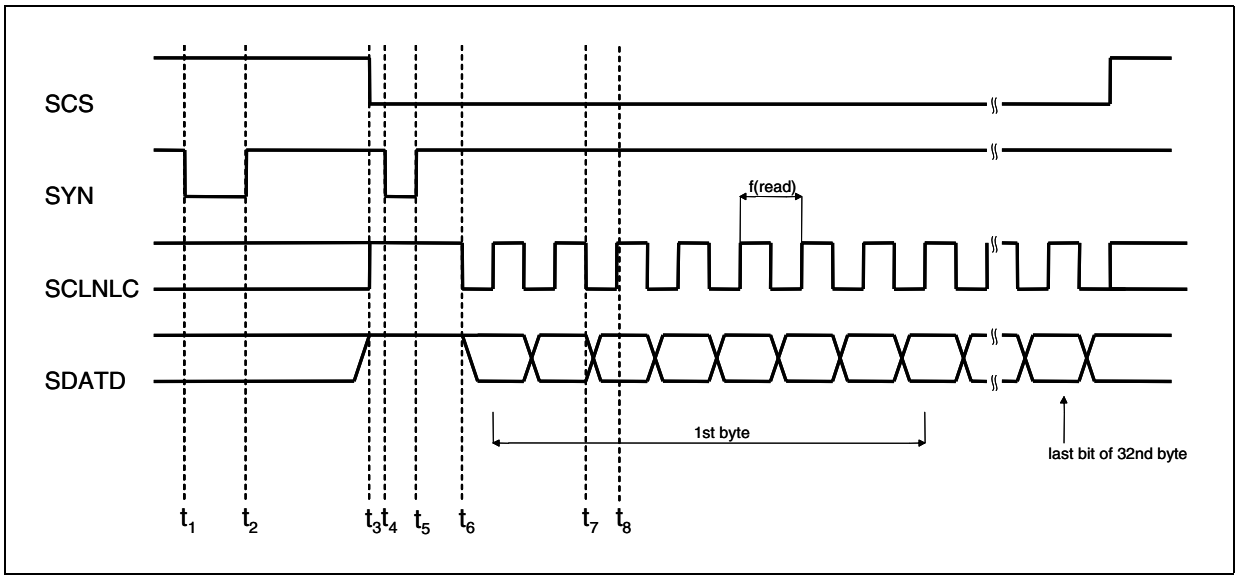
Data record reading takes place most often when there is an on-board microcontroller in an application. This microcontroller is capable of reading all measurement results and all system signals (configuration, calibration, status, mode). Again, the time step can be as short as 30 ns. There are two phases of reading, called **latching** and **shifting**.

Latching is used to sample results into transmission latches. The transmission latches are the flip-flops that hold the data in the SPI interface. This is done with the active pulse on **SYN** when **SCS** is idle. The length of pulse on **SYN** must be longer than 2 periods of measurement clock, i.e. more than 500 ns at 4 MHz.

The shifting starts when **SCS** become active. In the beginning of this phase another, but much shorter, pulse (30 ns) on **SYN** should be applied in order to ensure that an internal transmission serial clock counter is reset to zero. An alternative way is to extend the pulse on SYN into the second phase of reading. After that reset is done, a 32 serial clocks per data record should be applied. Up to 8 data records can be read this way. This procedure can be aborted at any time by deactivation of **SCS**.

The timing diagram of the reading operation is shown in timing for data records reading. One can see the latching and beginning of shifting phase of the first byte of the first data record and end of reading.

Figure 22. Timing for data records reading



t_1 –> t_2: Latching Phase. Interval value > $2/f_{CLK}$

t_2 –> t_3: Data latched, SPI idle. Interval value > 30 ns.

t_3 –> t_4: Enable SPI for read operation. Interval value > 30 ns.

t_4 –> t_5: Serial clock counter is reset. Interval value > 30 ns.

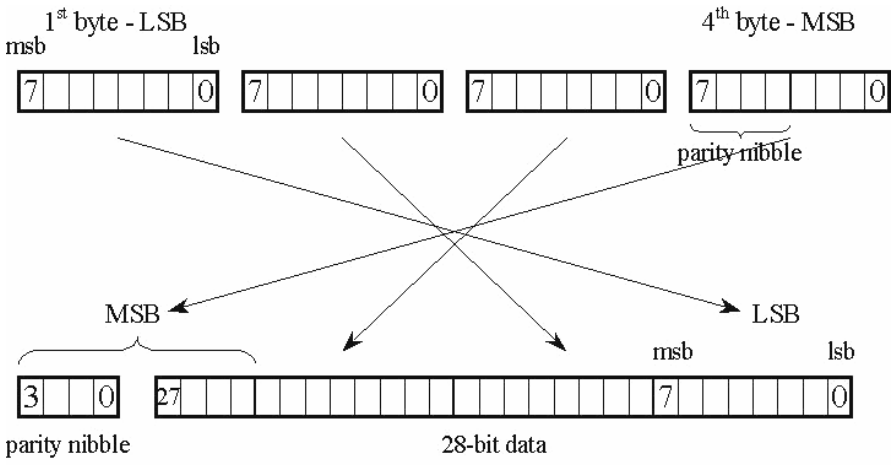
t_5 –> t_6: SPI reset and enabled for read operation. Interval value > 30 ns

t_7: Internal data transferred to SDATD

t_8: SDATD data is stable and can be read

The first read out byte of the data record is the least significant byte (LSB) of the data value and of course, the fourth byte is the most significant byte (MSB) of the data value. Each byte can be further divided into a pair of 4-bit nibbles, most and least significant nibble (msn, lsn). This division makes sense with the MSB of the data value because the msn holds the parity code.

Figure 23. Data records reconstruction



The sequence of the data record during the reading operation is fixed. However, an application may apply a precharge command (see mode signal description) prior to the reading phase. This command increases the group pointer forcing the device to respond with the next group data records sequence.

The system that reads the data record from the STPMC1 should check the integrity of each data record, as indicated in paragraph *9.17.8*. If the check fails, the reading should be repeated, but this time only the shifting should be applied; otherwise new data would be latched into transmission latches, thus losing the previous reading.
Normally, each byte is read out as the most significant bit (msb) first. But this can be changed by setting the MSBF configuration bit in the STPMC1 CFL data record. If this is done, each byte is read out as the least significant bit (lsb) first.

9.21.3 Writing procedure

Each writable bit (configuration and mode bits) has its own 7-bit absolute address. For the configuration bits, the 7-bit address value corresponds to its decimal value, while for the mode bits the addresses are those indicated in the mode signal paragraph.

In order to change the state of a latch one must send to the STPMC1 a byte of data which is the normal way to send data via SPI. This byte consists of 1-bit data to be latched (msb), followed by 7-bit address of destination latch, which makes total 8 bits of command byte, as summarized in the table below.

Table 35. Functional description of commands

Bit pos. 76543210	Command (X, D, A = {0, 1})
D0000000	CFG000=D, (shadow of first configurator, TSTD)
DAAAAAAA	CFGa=D, (shadow of any configurator, a = $AAAAAA_2$ < 1110000_2)
D1101111	CFG111=D, (shadow of last configurator, CHK)

Example 18: Setting a configuration bit

To set the configuration bit 47 (part of the R-phase current channel calibrator) to 0, we must convert the decimal 47 to its 7-bit binary value: 0101111. The byte command is then composed like this:

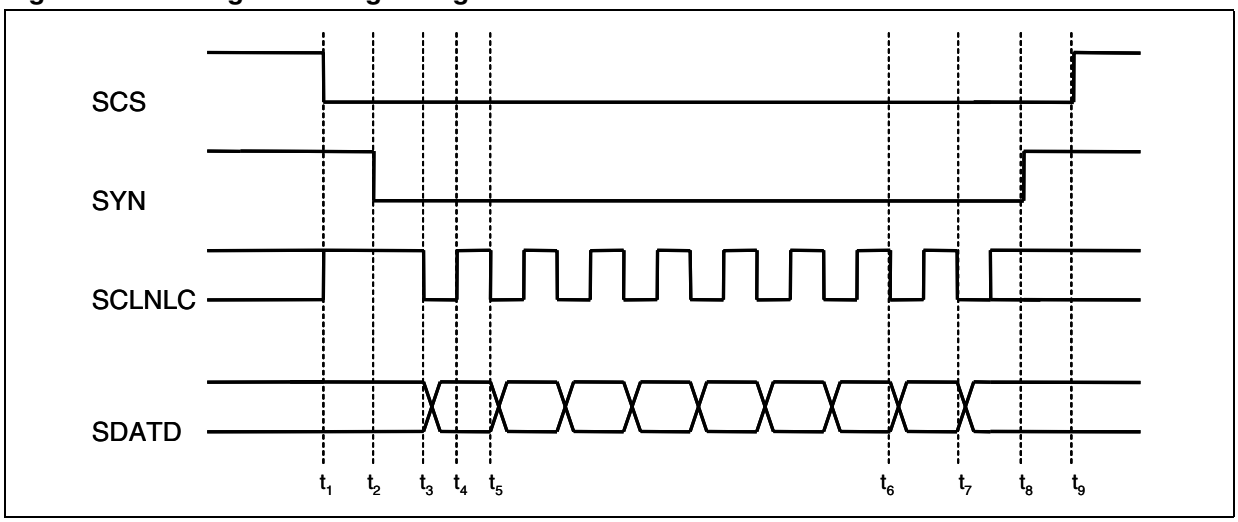
1 bit DATA value+7-bits address = 10101111 (0xAF)

The same procedure should be applied for the mode signals, but in this case the 7-bits address must be taken from the relative *Table 34*.

The lsb of command is also called EXE bit because instead of a data bit value, the corresponding serial clock pulse is used to generate the necessary latching signal. This way the writing mechanism does not need the measurement clock in order to operate, which makes the operation of SPI module of STPMC1 completely independent from the rest of device logic except from the signal POR.

Commands for changing system signals should be sent during active signals SCS and SYN as it is shown in *Figure 24*. The SYN must be put low in order to disable SDATD output driver of STPMC1 and make the SDATD as an input pin. A string of commands can be send within one period of active signals SCS and SYN or command can be followed by reading the data record but, in this case, the SYN should be deactivated in order to enable SDATD output driver and a SYN pulse should be applied before activation of SCS in order to latch the data.

Figure 24. Timing for writing configuration and mode bits



t_1 –> t_2 (> 30 ns): SPI out of idle state

t_2 –> t_3 (> 30 ns): SPI enabled for write operation

t_3: data value is placed in SDA

t_4: SDA value is stable and shifted into the device

t_3 –> t_5 (> 10 µs): writing clock period

t_3 –> t_5: 1 bit data value

t_5 –> t_6: 6 bits address of the destination latch

t_6 –> t_7: 1 bit EXE command

t_8: end of SPI writing

t_9: SPI enters idle state

9.21.4 Interfacing the standard 3-wire SPI with STPMC1 SPI

Due to the fact that a 2-wire SPI is implemented in the STPMC1, it is clear that sending any command from a standard 3-wire SPI would require 3-wire to 2-wire interface, which should produce a proper signal on SDATD from host signals SDI, SDO and SYN. A single gate 3-state buffer could be omitted by an emulation of SPI just to send some command. On a microcontroller this would be done by the following steps:

1. disable the SPI module
2. set SDI pin which is connected to SDATD to be output
3. activate SYN first and then SCS
4. apply new bit value to SDI and activate SCL
5. deactivate SCL
6. repeat the last two steps seven times to complete one byte transfer
7. repeat the last three steps for any remaining byte transfer
8. set SDI pin to be input
9. deactivate SCS and the SYN
10. enable the SPI module

In case of precharge command (0xFF), emulation above is not necessary. Due to the pull up device on the SDATD pin of the STPMC1 the processor needs to perform the following steps:

1. activate SYN first in order to latch the result;
2. after at least 1 s activate SCS
3. write one byte to the transmitter of SPI (this produces 8 pulses on SCL with SDI = 1)
4. deactivate SYN
5. optionally read the data records (the sequence of reading is altered
6. deactivate SCS

9.21.5 Permanent writing of the CFG bits

In order to make a permanent set of some CFG bits, the following procedure should

be conducted:

1. collect all addresses of CFG bits to be permanently set into some list
2. clear all OTP shadow latches
3. set the system signal RD
4. connect a current source of at least +14 V, 1 mA to 3 mA to VOTP
5. wait for VOTP voltage is stable
6. set one OTP shadow latch from the list
7. set the system signal WE
8. wait for 300 µs
9. clear the system signal WE
10. clear the OTP shadow latch which was set in step 6
11. until all wanted CFG bits are permanently set, repeat steps 5 to 11
12. disconnect the current source
13. wait for VOTP voltage is less than 3V
14. clear the system signal RD
15. read all data records, in the last two of them there is read back of CFG bits
16. if verification of CFG bits fails and there is still chance to pass, repeat steps 1 to 16

For set or clear steps, apply the timing shown in timing for data records reading with proper signal on the SDATD. For step 15, apply the timing shown in timing for writing configuration and mode bits.

For permanent set of the TSTD bit, which causes no more writing to the configuration bits, the procedure above must be conducted in such way that steps 6 to 13 are performed in series during single period of active SCS because the idle state of SCS would make the signal TSTD immediately effective which in turn, would abort the procedure and possibly destroy the device due to clearing of system signal RD and so, connecting all gates of 3 V NMOS sense amplifiers of already permanently set CFG bits to the VOTP source.

10 Energy calculation algorithm

For the purpose of simplicity the energy computation shown below is relative to only one phase.

Given line voltage and current as:

Equation 12

$u = U \sin(\omega t)$ $i = I \sin(\omega t + \varphi)$

The voltage divider, AD converter and calibrator produce the value:

Equation 13

$v_u = u\,(R_2/(R_1+R_2))\,(A_U/V_{REF})\,k_U = u\,k_D = A \sin(\omega t)$

The Rogowski coil preamplifier, AD converter and calibrator produce the value:

Equation 14

$v_i = -L\,(di/dt)\,(A_I/V_{REF})\,k_I = -I\,k_L\,\omega \cos(\omega t + \varphi) = -B\,\omega \cos(\omega t + \varphi)$

The 2nd stage internal integrations produce the values:

Equation 15

$v_{ui} = \int v_u dt = -(A / \omega) \cos(\omega t)\,k_{INT}$

Equation 16

$vii = \int v_i dt = -B \sin(\omega t + \varphi)\,k_{INT}$

From signs of v_u and v_{ui} the base frequency of line can be produced:

Equation 17

$\omega / k_{INT} = k / T$

This result is used to compensate Eq. 41, Eq. 44, Eq. 45 and Eq. 54.

The frequency compensated values are:

Equation 18

$v_{uic} = \omega / k_{INT}\,v_{ui} = -A \cos(\omega t)$

Equation 19

$v_{iic} = \omega / k_{INT}\,v_{ii} = -B\,\omega \sin(\omega t + \varphi)$

The 3rd stage internal integrations and DC cancellations produce the values:

Equation 20

$v_{uiic} = \int v_{uic} dt = -(A / \omega) \sin(\omega t)\,k_{INT}$

Equation 21

$v_{iiic} = \int v_{iic} dt = B \cos(\omega t + \varphi)\,k_{INT}$

In case of shunt sensor (TCS = 1), an additional stage of internal digital differentiated produces the value:

Equation 22

$v_d = dv_u/dt = A\ \omega \cos(\omega t)\ k_{DIF}$

The shunt preamplifier, AD converter and calibrator produce the value:

Equation 23

$vs = i\ R_S\ (A_I/V_{REF})\ k_I = i\ k_S = C \sin(\omega t + \varphi)$

The 2nd stage internal integrations produce the values:

Equation 24

$v_{di} = \int v_d dt = A \sin(\omega t)\ k_{DIF}\ k_{INT} = A \sin(\omega t)$

Equation 25

$v_{si} = \int v_s dt = -(C / \omega) \cos(\omega t + \varphi)\ k_{INT}$

The frequency compensated values are:

Equation 26

$V_{dic} = \omega / k_{INT}\ v_{di} = A\ \omega \sin(\omega t) / k_{INT}$

Equation 27

$v_{sic} = \omega / k_{INT}\ v_{si} = -C \cos(\omega t + \varphi)$

The 3rd stage internal integrations and DC cancellations produce the values:

Equation 28

$v_{diic} = \int v_{dic} dt = A \cos(\omega t)\ k_{DIF}\ k_{INT} = A \cos(\omega t)$

Equation 29

$v_{siic} = \int v_{sic} dt = -(C / \omega) \sin(\omega t + \varphi)\ k_{INT}$

10.1 Active energy calculation

The active power is computed as follows.

First, the voltage stream from the 1st stage (*Equation 13* or *Equation 22*) is multiplied to the 16-bit current from the 2nd stage (*Equation 16* or *Equation 25*) and current stream from the 1st stage (*Equation 14* or *Equation 23*) is multiplied to 16-bit voltage from the 2nd stage of filter (*Equation 15* or *Equation 24*), yielding:

Equation 30

$P_1 = v_u\ v_{ii} = -ABk_{INT} \sin(\omega t) \sin(\omega t + \varphi) = -ABk_{INT}[\cos\varphi - \cos(2\omega t + \varphi)] / 2$

Equation 31

$P_2 = v_{ui}\ v_i = ABk_{INT} \cos(\omega t) \cos(\omega t + \varphi) = ABk_{INT}[\cos\varphi + \cos(2\omega t + \varphi)] / 2$

In case of a non Rogowski sensor, the corresponding products are:

Equation 32

$$P_1 = v_d\, v_{si} = -\,AC\, k_{DIF} k_{INT} \cos(\omega t) \cos(\omega t + \varphi) = -\,AC\, [\cos\varphi + \cos(2\omega t + \varphi)] / 2$$

Equation 33

$$P_2 = v_{di}\, v_s = AC\, k_{DIF} k_{INT} \sin(\omega t) \sin(\omega t + \varphi) = AC\, [\cos\varphi - \cos(2\omega t + \varphi)] / 2$$

Then a subtraction of P_1 from P_2 is performed:

Equation 34

$$P = (P_2 - P_1) / 2 = (AB \cos\varphi)\, k_{INT} / 2 = (Uk_D Ik_L \cos\varphi)\, k_{INT} / 2 = U_{RMS}\, I_{RMS} \cos\varphi\, k_P$$

where:

Equation 35

$$k_P = k_D\, k_L\, k_{INT}$$

This gives the same result for P in case of non Rogowski sensor, substituting B and $k_L\, k_{INT}$ with C and k_S:

Equation 36

$$P = (P_2 - P_1) / 2 = (AC \cos\varphi) / 2 = (Uk_D Ik_S \cos\varphi) / 2 = U_{RMS}\, I_{RMS} \cos\varphi\, k_P$$

where:

Equation 37

$$k_P = k_D\, k_S$$

The result in *Equation 35* and *Equation 36* is proportional to the DC part of active power of line. The division by 2 is a feature of ΔΣ subtractor. The absence of harmonic components eliminates the spread of results due to asynchronism with the line. This fact enables fast a calibration procedure which is used to set the target constant of meter k_P.

A sensitivity analysis of k_P yields:

Equation 38

$$\Delta k_P/k_P = \Delta L/L + R_1 / (R_1+R_2)(\Delta R_2/R_2 - \Delta R_1/R_1) + \Delta A_U/A_U + \Delta A_I/A_I - 2\,\Delta V_{REF}/V_{REF}$$

Equation 39

$$\Delta k_P/k_P = \Delta R_S / R_S + R_1 / (R_1+R_2)(\Delta R_2/R_2 - \Delta R_1/R_1) + \Delta A_U/A_U + \Delta A_I/A_I - 2\,\Delta V_{REF}/V_{REF}$$

It is clear that the device is responsible for A_U, A_I and V_{REF} parts. The parts k_U, k_I and k_{INT} are omitted, because they are not subject to aging or temperature variations due to digital implementation.

10.2 Reactive energy calculation

The natural reactive power (ART = 0) of the line is computed as follows.

First, 16-bit voltage from the 3rd stage (*Equation 20* or *Equation 28*) is multiplied by the current stream from the 1st stage (*Equation 14* or *Equation 23*) and the frequency

compensated stream of 16-bit voltage from the 2nd stage of filter (*Equation 18* or *Equation 26*) is multiplied by the 16-bit current stream from the 2nd stage (*Equation 16* or *Equation 25*) yielding:

Equation 40

$$Q_1 = v_{uiic}\, v_i = ABk_{INT} \sin(\omega t) \cos(\omega t + \varphi) = - ABk_{INT} [\sin\varphi - \sin(2\omega t + \varphi)] / 2$$

Equation 41

$$Q_2 = \omega / k_{INT}\, v_{ui}\, v_{ii} = ABk_{INT} \cos(\omega t) \sin(\omega t + \varphi) = ABk_{INT} [\sin\varphi + \sin(2\omega t + \varphi)] / 2$$

In case of non Rogowski sensor, the corresponding products are:

Equation 42

$$Q_1 = v_{diic}\, v_s = ACk_{DIF}k_{INT} \cos(\omega t) \sin(\omega t + \varphi) = AC [\sin\varphi + \sin(2\omega t + \varphi)] / 2$$

Equation 43

$$Q_2 = \omega / k_{INT}\, v_{di}\, v_{si} = - ACk_{DIF}k_{INT} \sin(\omega t) \cos(\omega t + \varphi) = - AC [\sin\varphi - \sin(2\omega t + \varphi)] / 2$$

Then a subtraction of Q_1 from Q_2 is performed:

Equation 44

$$Q = (Q_2 - Q_1) / 2 = (AB \sin\varphi)\, k_{INT} / 2 = (Uk_DIk_L \sin\varphi)\, k_{INT} / 2 = U_{RMS}\, I_{RMS} \sin\varphi\, k_P$$

This gives the same result for Q in case of non Rogowski sensor, substituting B and k_Lk_{INT} with C and k_S:

Equation 45

$$Q = (Q_2 - Q_1) / 2 = (AC \sin\varphi) = (Uk_DIk_S \sin\varphi) / 2 = U_{RMS}\, I_{RMS} \sin\varphi\, k_P$$

The artificial reactive power (ART = 1) of line is computed as follows.

The inter-phase voltage sigma-delta stream is computed from voltage stream from the 1st stage as follows:

Equation 46

$$\Delta v_{uR} = (v_{uS} - v_{uT}) / 2$$

$$\Delta v_{uS} = (v_{uT} - v_{uR}) / 2$$

$$\Delta v_{uT} = (v_{uR} - v_{uS}) / 2$$

The inter-phase voltage sigma-delta stream (*Equation 46*), the 16-bit current from the 2nd stage (*Equation 16* or *Equation 25*) and the value of $1 / \sqrt{3}$ are multiplied yielding:

Equation 47

$$Q = \Delta v_u\, v_{ii}\, 1 / \sqrt{3} = AB\, k_{INT} [\sin\varphi + \sin(2\omega t + \varphi)] / 2$$

or in case of non Rogowski sensor, the corresponding products are:

Equation 48

$$Q = \Delta v_d\, v_{si}\, 1 / \sqrt{30} = AC [\sin\varphi + \sin(2\omega t + \varphi)] / 2$$

10.3 Voltage and current RMS values calculation

The I_{RMS} value is produced from 16-bit value of *Equation 16*:

Equation 49

$$I_{RMS}k_L k_{INT} = \sqrt{\frac{1}{T}\int_0^T V_{ii}^2 dt} = B\sqrt{\frac{1}{2}}$$

The Ui_{RMS} is produced from stream and 16-bit value of *Equation 15*:

Equation 50

$$Ui_{RMS}k_D = \sqrt{\frac{1}{T}\int_0^T V_{ui}^2 dt} = Ak_{INT}/\omega\sqrt{\frac{1}{2}}$$

In case of non Rogowski sensor, the same dedicated RMS blocks produce some other values, because input values for the blocks are changed.

Therefore, another RMS value, named Ii_{RMS} is produced from 16-bit value of *Equation 25*:

Equation 51

$$Ii_{RMS}k_S k_{INT} = \sqrt{\frac{1}{T}\int_0^T V_{si}^2 dt} = C/\omega\sqrt{\frac{1}{2}}$$

The U_{RMS} is produced from stream and 16-bit value of *Equation 24*:

Equation 52

$$U_{RMS}k_D = \sqrt{\frac{1}{T}\int_0^T V_{di}^2 dt} = A\sqrt{\frac{1}{2}}$$

10.4 Energy integration

The internal hard-wired DSP unit performs all the computations above in real time for a power line in parallel by means of arithmetic blocks. Due to implementation of an integrator, up/down counter or deviator, part of which is also an integrator in a feedback, additional factors are introduced into computations. If we declare f_{MCLK} as the measurement clock frequency and M as number of possible values of some integrator, the following constant factors can be defined:

Equation 53

$k_{INT} = 2\ f_{MCLK} / M_{INT} = 2^8$

$k_{UD} = 2\ f_{MCLK} / M_{UD} = 2^{11}$

$k_{DIF} = M_{DIF} / 2\ f_{MCLK} = 2^{-8}$

The DSP performs also an integration of powers (P, Q) into energies:

Equation 54

$AW = U_{RMS} I_{RMS} \cos \varphi k_P k_{UD}$

Equation 55

$AW = U_{RMS} I_{RMS} \sin \varphi k_P k_{UD}$

These integrators are implemented as up/down counters and they can roll over. 20-bit output buses of the counters are assigned as the most significant part of the energy data records. It is a responsibility of the application to read the counters at least every second so as not to miss any rollover. The integration of power can be suspended due to detected error on the source signals or due to no load condition. From AW, stepper output signals are generated.

10.5 Fundamental power calculation

The fact that integration suppresses all but fundamental components of signals is used to compute the fundamental active power, which is in case of Rogowski coil:

Equation 56

$F_1 = v_{uic} v_{iiic} = - ABk_{INT} \cos (\omega t) \cos (\omega t + \varphi) = - ABk_{INT} [\cos \varphi + \cos (2 \omega t + \varphi)] / 2$

Equation 57

$F_2 = v_{iic} v_{uiic} = - ABk_{INT} \sin (\omega t) \sin (\omega t + \varphi) = ABk_{INT} [\cos \varphi - \cos (2 \omega t + \varphi)] / 2$

Equation 58

$F = (F_2 - F_1) / 2 = (AB \cos \varphi) k_{INT} / 2 = (Uk_D Ik_L \cos \varphi) k_{INT} / 2 = U_{RMS} I_{RMS} \cos \varphi k_P$

Similar result are found in case of non Rogowski sensor:

Equation 59

$F_1 = v_{dic} v_{siic} = - AC \sin (\omega t) \sin (\omega t + \varphi) = - AC [\cos \varphi - \cos (2 \omega t + \varphi)] / 2$

Equation 60

$F_2 = v_{sic} v_{diic} = - ACk_{DIF} k_{INT} \cos (\omega t) \cos (\omega t + \varphi) = - AC [\cos \varphi + \cos (2 \omega t + \varphi)] / 2$

Equation 61

$F = (F_2 - F_1) / 2 = - AC \cos (2 \omega t + \varphi) = Uk_D Ik_s \cos (2 \omega t + \varphi) / 2 = U_{RMS} I_{RMS} \cos (2 \omega t + \varphi) k_P$

The **fundamental reactive power** in case of a Rogowski coil is:

Equation 62

$Q = v_{uiic} v_{iiic} \omega / k_{INT} = - ABk_{INT} \cos (\omega t) \sin (\omega t + \varphi) = ABk_{INT} [\sin \varphi - \sin (2 \omega t + \varphi)] / 2$

Similar results are found in cases of non Rogowski sensors:

Equation 63

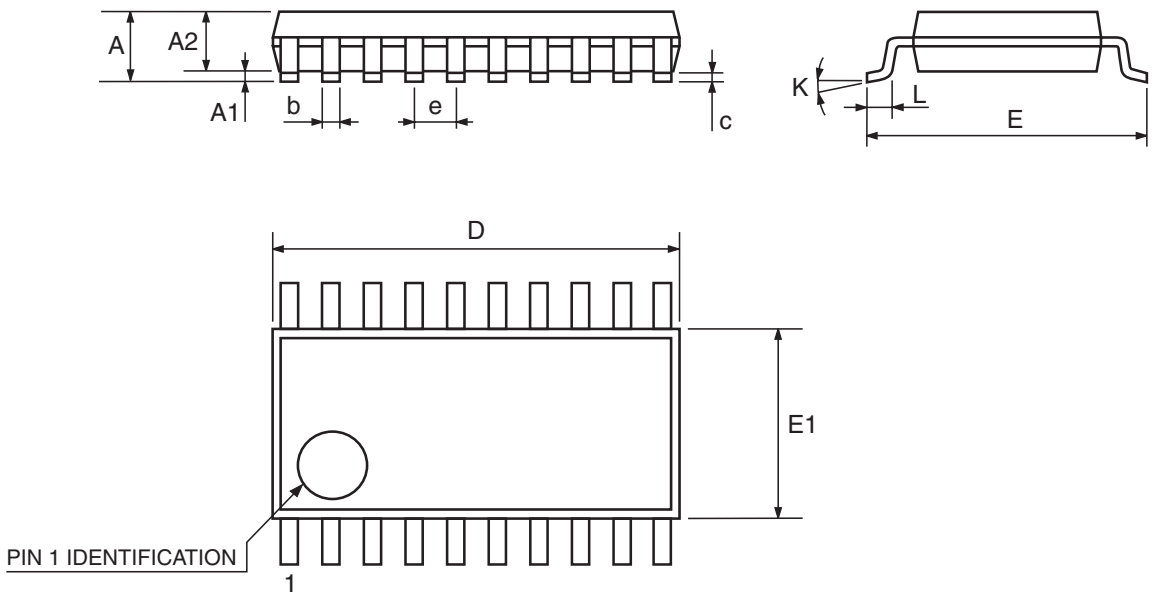
$Q = v_{diic} v_{siic} \omega / k_{INT} = - AC \cos (\omega t) \sin (\omega t + \varphi) = AC [\sin \varphi - \sin (2 \omega t + \varphi)] / 2.$

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

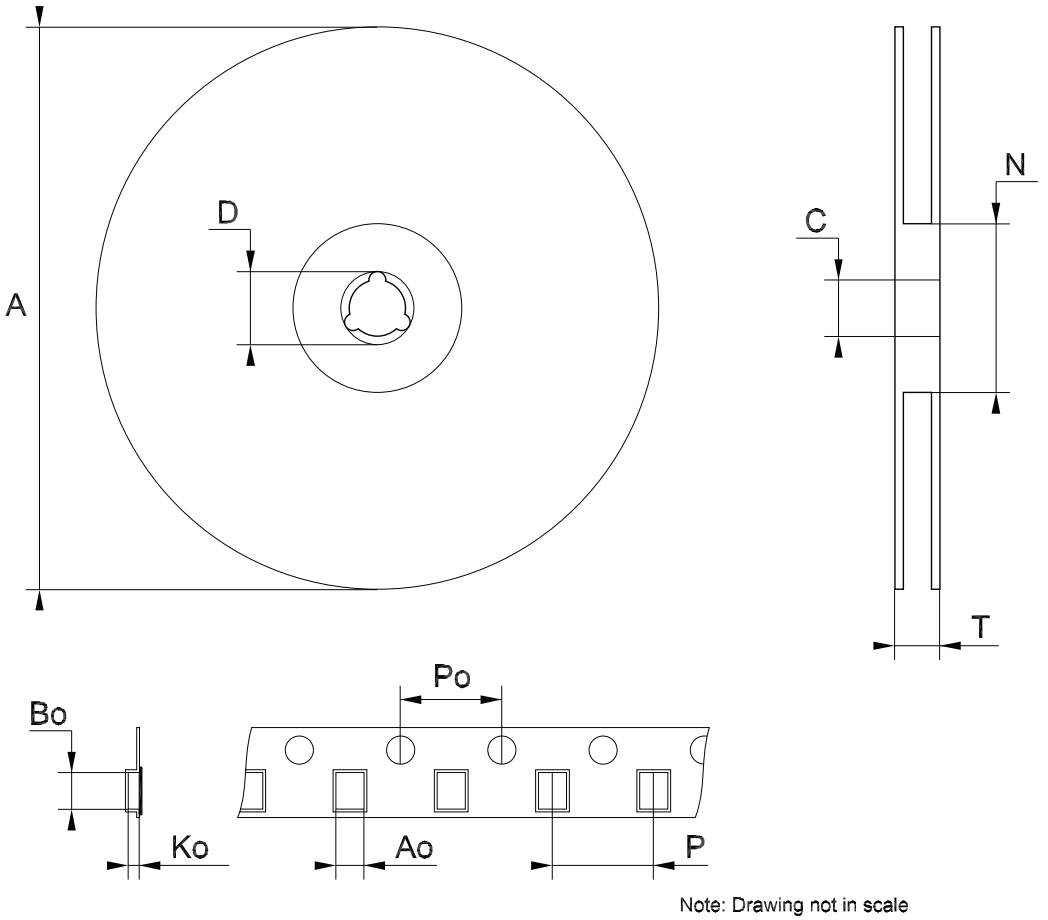
TSSOP20 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & reel TSSOP20 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

12 Revision history

Table 36. Document revision history

Date	Revision	Changes
22-May-2009	1	Initial release.
03-Jul-2009	2	Updated: paragraphs *9.4*, *9.16* and *9.17.8*.
28-Jul-2009	3	Updated: paragraph *9.16.2*.
19-May-2010	4	Added: *Example 5: 3-ph system - BCS = 0 on page 29*, *Example 6: 3-ph system - BCS = 1 on page 31*, *Example 7: 1-ph system - BCS = 0 on page 31*, *Example 8: 1-ph system - BCS = 1 on page 31* and *Equation 11: on page 48*. Modified: paragraph *9.17.2 on page 47*.
11-Oct-2011	5	Updated: V_{IH} and V_{IL} values *Table 7 on page 13*.
24-Apr-2012	6	Modified: Supports IEC 62052-11 / 62053-21 / 62053-23 standards *Features on page 1*, *Table 11 on page 23* and *Table 23 on page 41*. Added: *Table 12 on page 23*.
14-Nov-2012	7	Modified *Figure 8 on page 22*.

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