



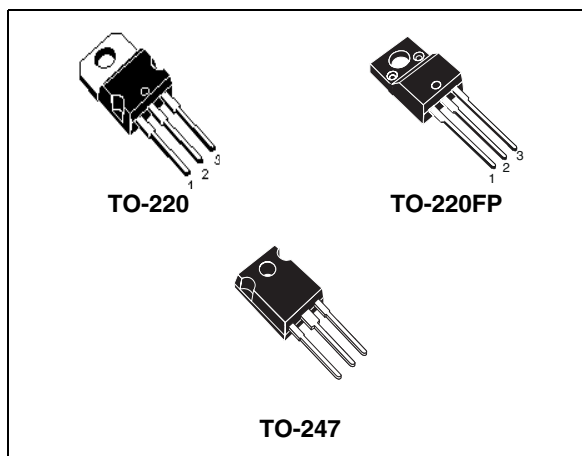
STP8NK80Z - STP8NK80ZFP STW8NK80Z

N-channel 800V - 1.3Ω - 6.2A - TO-220 /TO-220FP/TO-247
Zener-protected SuperMESH™ Power MOSFET

Features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|-------------|------------------|---------------------|----------------|
| STP8NK80Z | 800 V | < 1.5 Ω | 6.2 A |
| STP8NK80ZFP | 800 V | < 1.5 Ω | 6.2 A |
| STW8NK80Z | 800 V | < 1.5 Ω | 6.2 A |

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Application

- Switching applications

Figure 1. Internal schematic diagram

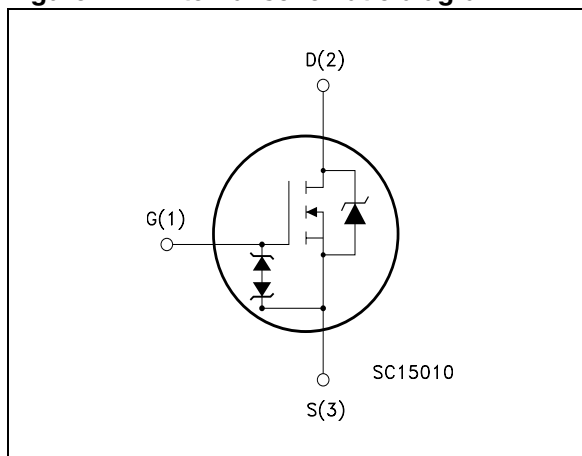


Table 1. Device summary

| Order codes | Marking | Package | Packaging |
|-------------|-----------|----------|-----------|
| STP8NK80Z | P8NK80Z | TO-220 | Tube |
| STP8NK80ZFP | P8NK80ZFP | TO-220FP | Tube |
| STW8NK80Z | W8NK80Z | TO-247 | Tube |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | | Unit |
|--------------------|---|-----------------|---------------------|---------------------|
| | | TO-220 - TO-247 | TO-220FP | |
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 800 | | V |
| V_{GS} | Gate- source voltage | ± 30 | | V |
| I_D | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 6.2 | 6.2 ⁽¹⁾ | A |
| I_D | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 3.9 | 3.9 ⁽¹⁾ | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 24.8 | 24.8 ⁽¹⁾ | A |
| P_{TOT} | Total dissipation at $T_C = 25^\circ\text{C}$ | 140 | 30 | W |
| | Derating factor | 1.12 | 0.24 | W/ $^\circ\text{C}$ |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=1.5K Ω) | 4000 | | V |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 4.5 | | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; $T_C = 25^\circ\text{C}$) | - | 2500 | V |
| T_j T_{stg} | Max operating Junction temperature Storage temperature | -55 to 150 | | $^\circ\text{C}$ |

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 6.2$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

| Symbol | Parameter | Value | | | Unit |
|----------------|--|--------|----------|--------|---------------------------|
| | | TO-220 | TO-220FP | TO-247 | |
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.89 | 4.2 | 0.89 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient max | 62.5 | | 50 | $^\circ\text{C}/\text{W}$ |
| T_l | Maximum lead temperature for soldering purpose | 300 | | | $^\circ\text{C}$ |

Table 4. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|---|-------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max) | 6.2 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_d = I_{AR}$, $V_{dd} = 50\text{V}$) | 300 | mJ |

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|---|---|------|------|----------|--------------------|
| $V_{(BR)DSS}$ | Drain-source Breakdown voltage | $I_D = 1mA, V_{GS} = 0$ | 800 | | | V |
| I_{DSS} | Zero gate voltage Drain current ($V_{GS} = 0$) | $V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, @125^{\circ}C$ | | | 1 50 | μA μA |
| I_{GSS} | Gate-body leakage Current ($V_{DS} = 0$) | $V_{GS} = \pm 20 V$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 100 \mu A$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10 V, I_D = 3.1 A$ | | 1.3 | 1.5 | Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|----------------------------------|---|------|------|------|------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DS} = 15V, I_D = 3.1 A$ | | 5.2 | | S |
| C_{iss} | Input capacitance | $V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$ | | 1320 | | pF |
| C_{oss} | Output capacitance | | | 143 | | pF |
| C_{rSS} | Reverse transfer capacitance | | | 27 | | pF |
| $C_{oss \text{ eq.}}^{(2)}$ | Equivalent output capacitance | $V_{DS} = 0V, V_{DS} = 0V \text{ to } 640V$ | | 58 | | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400 V, I_D = 3.1 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 21) | | 17 | | ns |
| t_r | Rise time | | | 30 | | ns |
| $t_{r(off)}$ | Turn-off delay time | | | 48 | | ns |
| t_f | Fall time | | | 28 | | ns |
| Q_g | Total gate charge | $V_{DD} = 640 V, I_D = 6.2 A,$ $V_{GS} = 10 V$ | | 46 | | nC |
| Q_{gs} | Gate-source charge | | | 8.5 | | nC |
| Q_{gd} | Gate-drain charge | | | 25 | | nC |
| $t_{r(Voff)}$ | Off-voltage rise time | $V_{DD} = 640 V, I_D = 6.2 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 23) | | 9 | | ns |
| t_f | Fall time | | | 9 | | ns |
| t_c | Cross-over time | | | 18 | | ns |

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | | | 6.2 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 24.8 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 6.2 \text{ A}, V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 6.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ | | 460 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 50 \text{ V}, T_j = 150^\circ\text{C}$ | | 2990 | | nC |
| I_{RRM} | Reverse recovery current | (see Figure 23) | | 13 | | A |

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------|--|------|------|------|------|
| $BV_{GSO}^{(1)}$ | Gate-source breakdown voltage | $I_{gs} = \pm 1 \text{ mA}$ (Open Drain) | 30 | | | V |

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

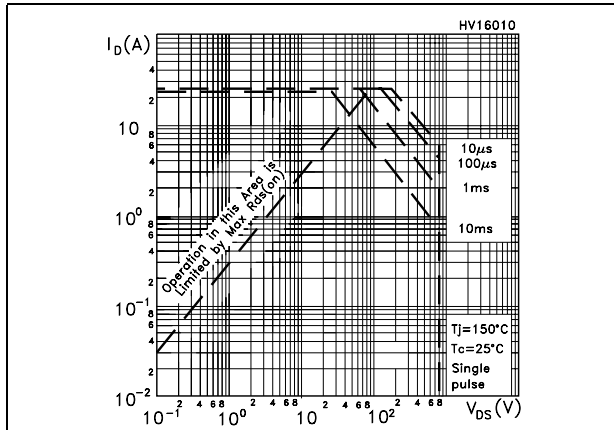


Figure 3. Thermal impedance for TO-220

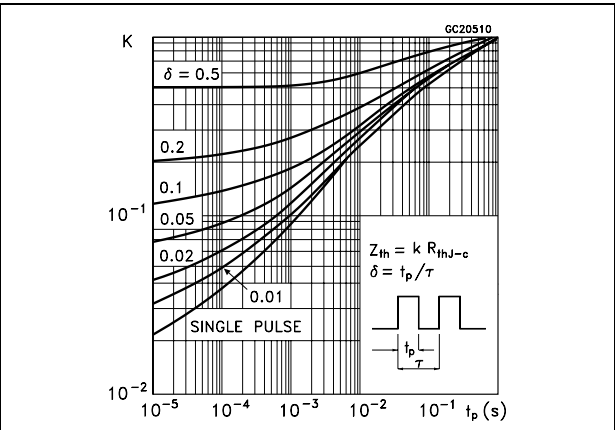


Figure 4. Safe operating area for TO-220FP

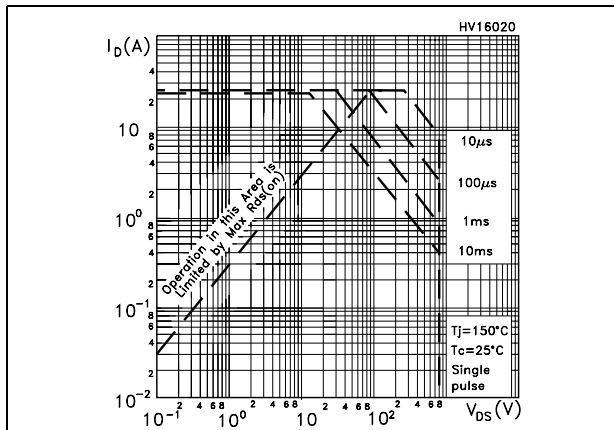


Figure 5. Thermal impedance for TO-220FP

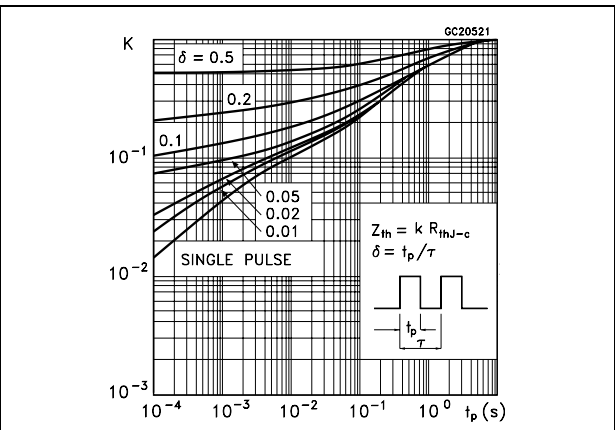


Figure 6. Safe operating area for TO-247

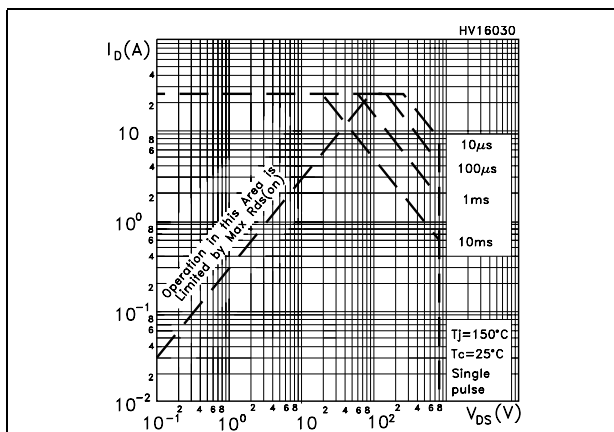


Figure 7. Thermal impedance for TO-247

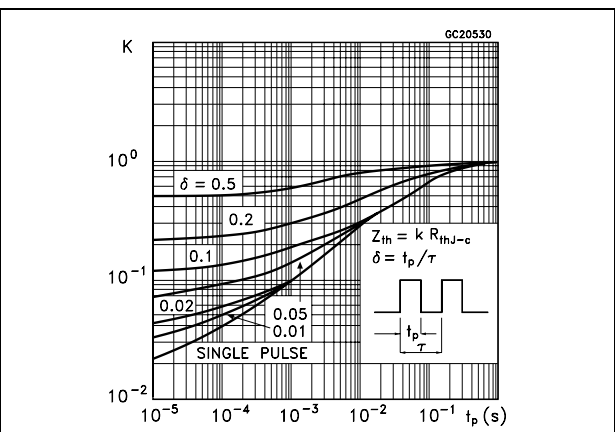


Figure 8. Output characteristics

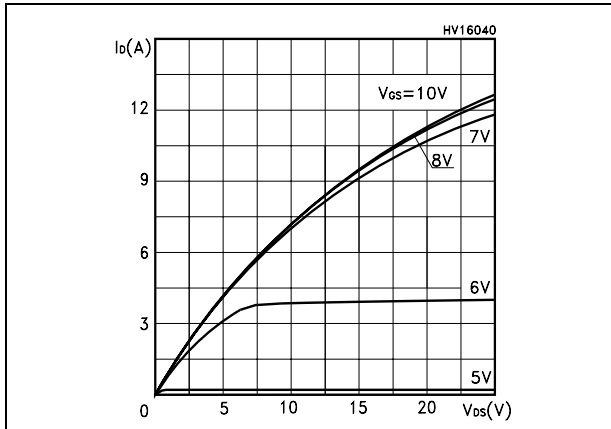


Figure 9. Transfer characteristics

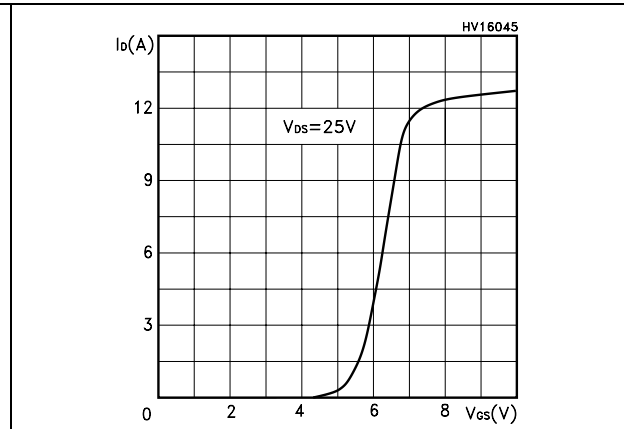


Figure 10. Transconductance

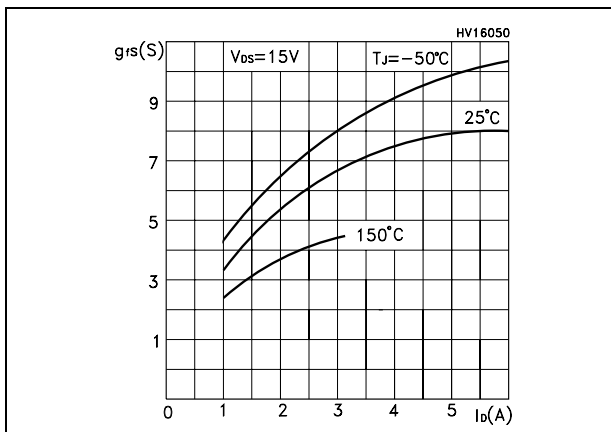


Figure 11. Static drain-source on resistance

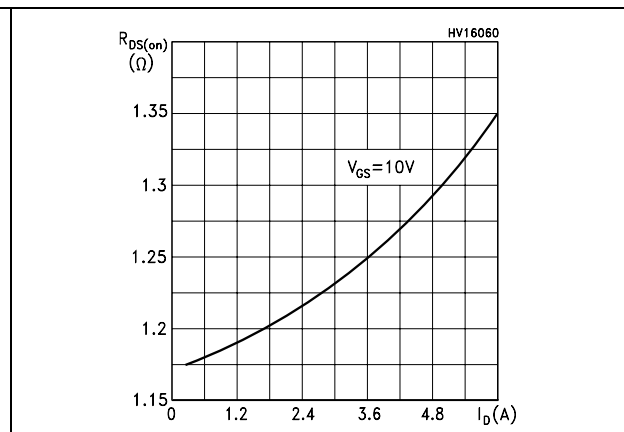


Figure 12. Gate charge vs gate-source voltage

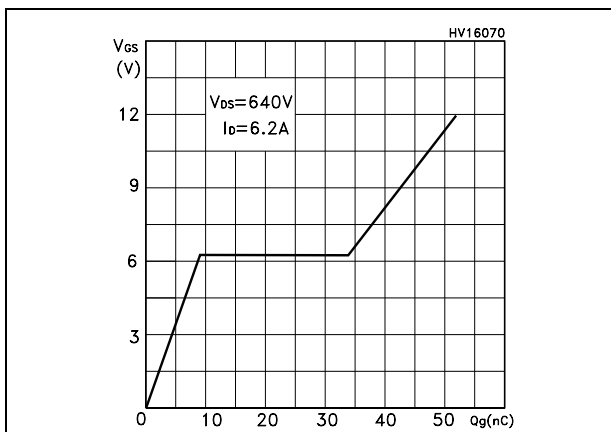


Figure 13. Capacitance variations

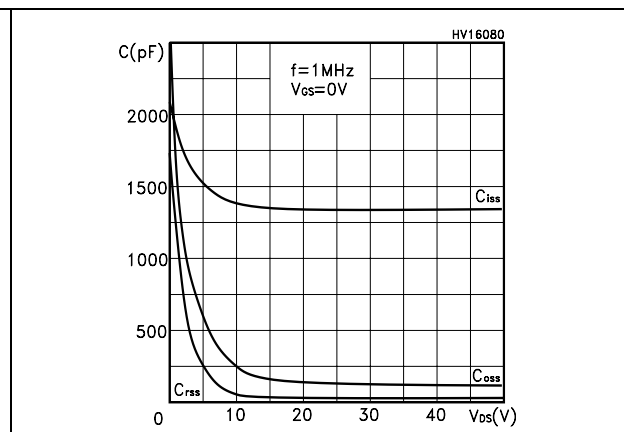


Figure 14. Normalized gate threshold voltage vs temperature

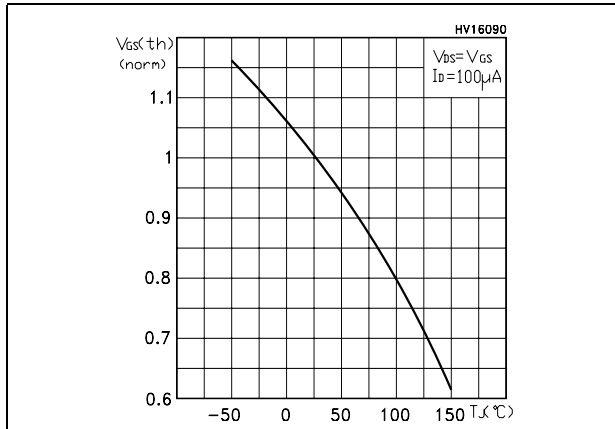


Figure 15. Normalized on resistance vs temperature

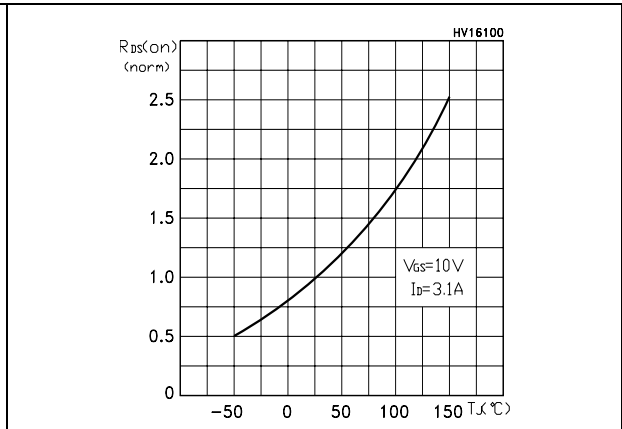


Figure 16. Source-drain diode forward characteristic

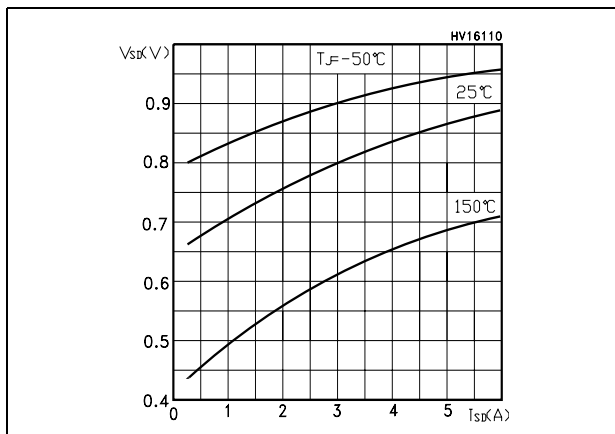


Figure 17. Normalized BV_{DSS} vs temperature

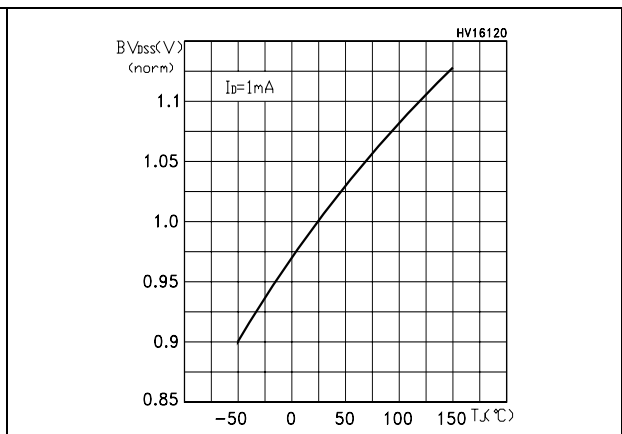
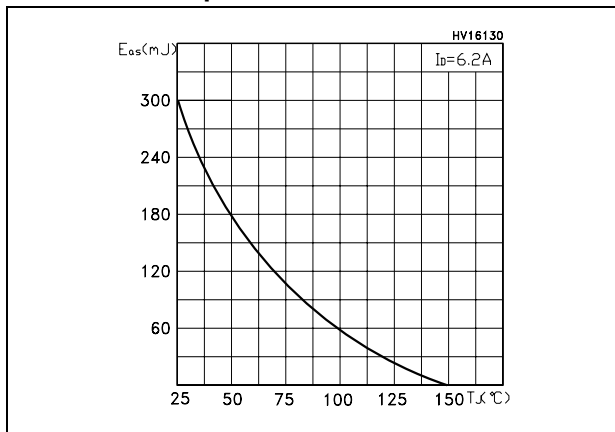


Figure 18. Maximum avalanche energy vs temperature



3 Test circuit

Figure 19. Unclamped inductive load test circuit

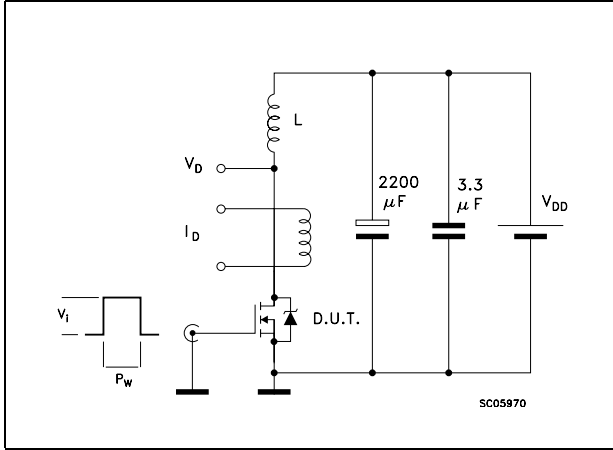


Figure 20. Unclamped inductive waveform

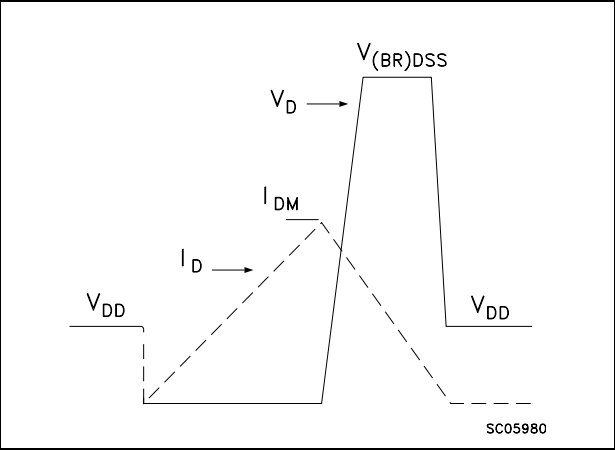


Figure 21. Switching times test circuit for resistive load

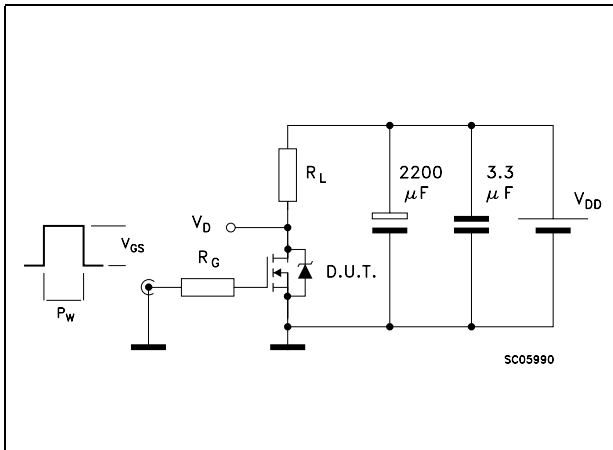


Figure 22. Gate charge test circuit

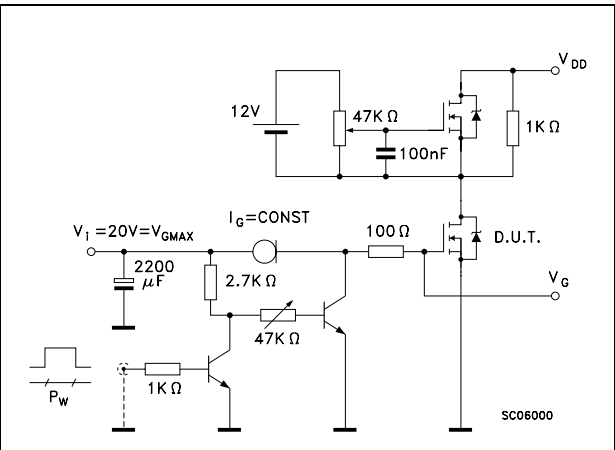
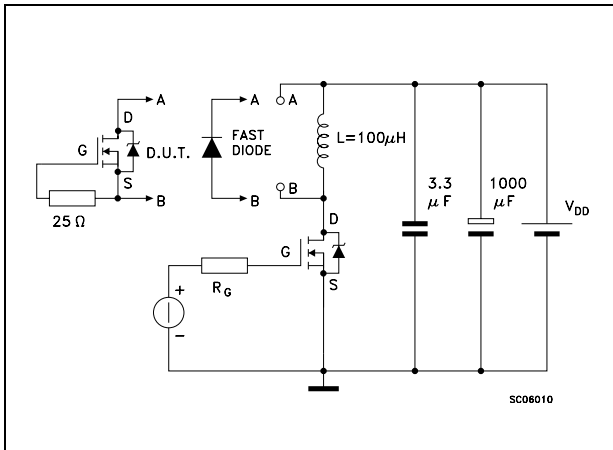


Figure 23. Test circuit for inductive load switching and diode recovery times

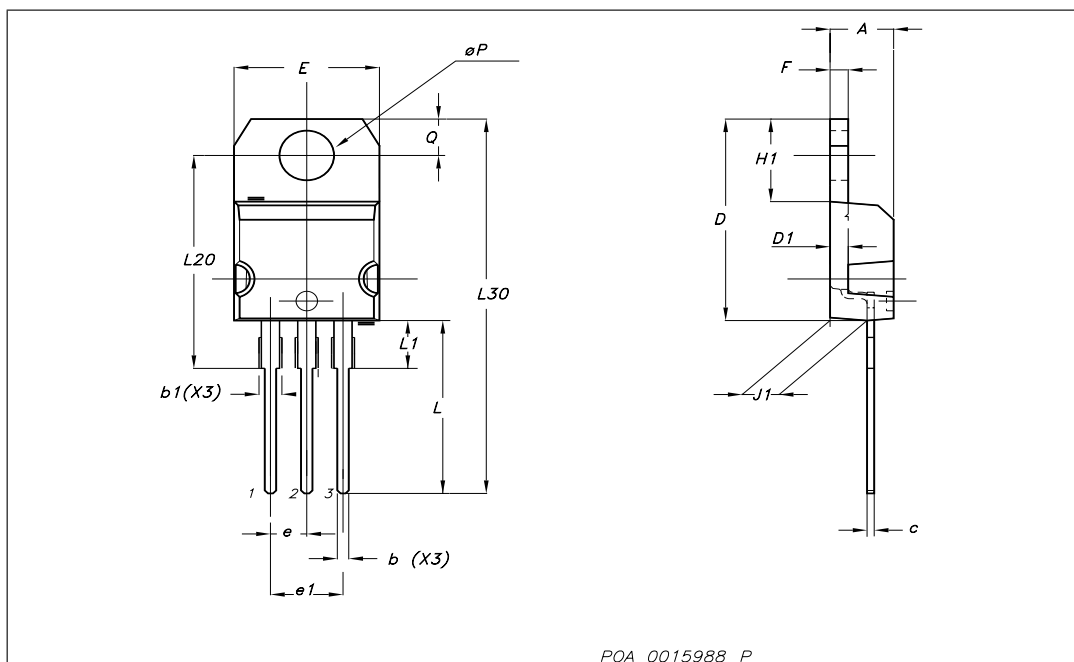


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

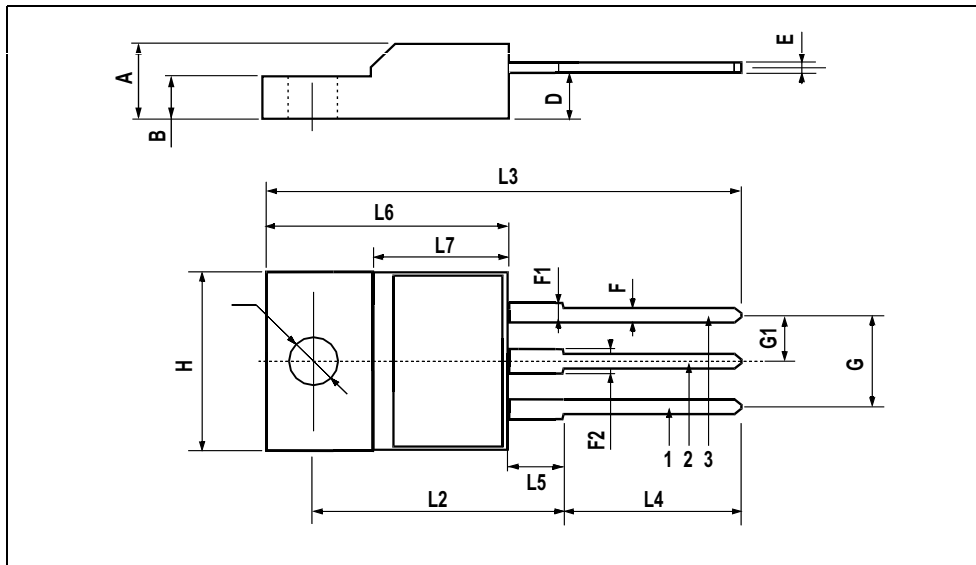
TO-220 mechanical data

| Dim | mm | | | inch | | |
|-----|-------|-------|-------|-------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 4.40 | | 4.60 | 0.173 | | 0.181 |
| b | 0.61 | | 0.88 | 0.024 | | 0.034 |
| b1 | 1.14 | | 1.70 | 0.044 | | 0.066 |
| c | 0.49 | | 0.70 | 0.019 | | 0.027 |
| D | 15.25 | | 15.75 | 0.6 | | 0.62 |
| D1 | | 1.27 | | | 0.050 | |
| E | 10 | | 10.40 | 0.393 | | 0.409 |
| e | 2.40 | | 2.70 | 0.094 | | 0.106 |
| e1 | 4.95 | | 5.15 | 0.194 | | 0.202 |
| F | 1.23 | | 1.32 | 0.048 | | 0.051 |
| H1 | 6.20 | | 6.60 | 0.244 | | 0.256 |
| J1 | 2.40 | | 2.72 | 0.094 | | 0.107 |
| L | 13 | | 14 | 0.511 | | 0.551 |
| L1 | 3.50 | | 3.93 | 0.137 | | 0.154 |
| L20 | | 16.40 | | | 0.645 | |
| L30 | | 28.90 | | | 1.137 | |
| ∅P | 3.75 | | 3.85 | 0.147 | | 0.151 |
| Q | 2.65 | | 2.95 | 0.104 | | 0.116 |



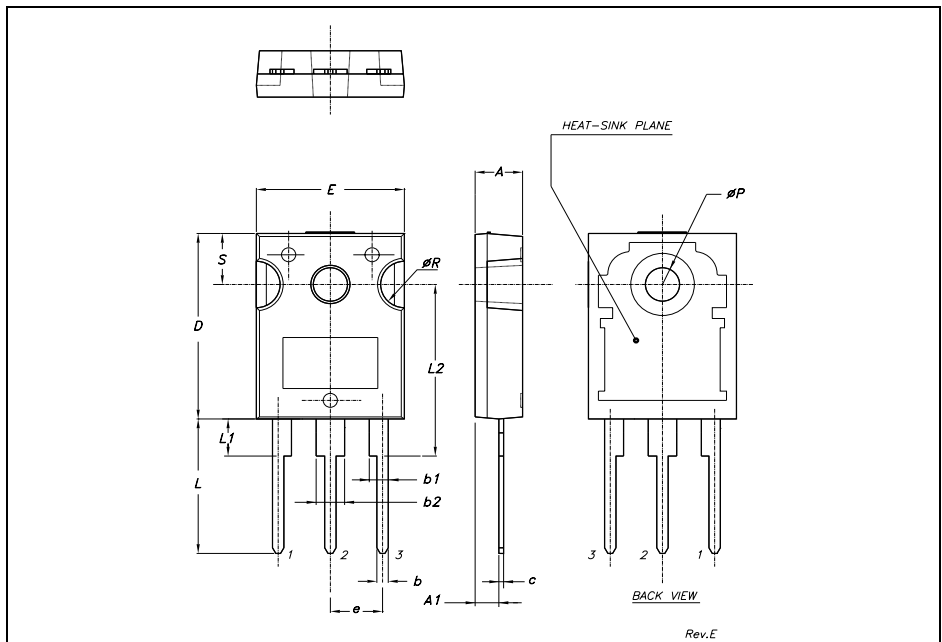
TO-220FP MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| B | 2.5 | | 2.7 | 0.098 | | 0.106 |
| D | 2.5 | | 2.75 | 0.098 | | 0.108 |
| E | 0.45 | | 0.7 | 0.017 | | 0.027 |
| F | 0.75 | | 1 | 0.030 | | 0.039 |
| F1 | 1.15 | | 1.7 | 0.045 | | 0.067 |
| F2 | 1.15 | | 1.7 | 0.045 | | 0.067 |
| G | 4.95 | | 5.2 | 0.195 | | 0.204 |
| G1 | 2.4 | | 2.7 | 0.094 | | 0.106 |
| H | 10 | | 10.4 | 0.393 | | 0.409 |
| L2 | | 16 | | | 0.630 | |
| L3 | 28.6 | | 30.6 | 1.126 | | 1.204 |
| L4 | 9.8 | | 10.6 | .0385 | | 0.417 |
| L5 | 2.9 | | 3.6 | 0.114 | | 0.141 |
| L6 | 15.9 | | 16.4 | 0.626 | | 0.645 |
| L7 | 9 | | 9.3 | 0.354 | | 0.366 |
| Ø | 3 | | 3.2 | 0.118 | | 0.126 |



TO-247 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.85 | | 5.15 | 0.19 | | 0.20 |
| A1 | 2.20 | | 2.60 | 0.086 | | 0.102 |
| b | 1.0 | | 1.40 | 0.039 | | 0.055 |
| b1 | 2.0 | | 2.40 | 0.079 | | 0.094 |
| b2 | 3.0 | | 3.40 | 0.118 | | 0.134 |
| c | 0.40 | | 0.80 | 0.015 | | 0.03 |
| D | 19.85 | | 20.15 | 0.781 | | 0.793 |
| E | 15.45 | | 15.75 | 0.608 | | 0.620 |
| e | | 5.45 | | | 0.214 | |
| L | 14.20 | | 14.80 | 0.560 | | 0.582 |
| L1 | 3.70 | | 4.30 | 0.14 | | 0.17 |
| L2 | | 18.50 | | | 0.728 | |
| øP | 3.55 | | 3.65 | 0.140 | | 0.143 |
| øR | 4.50 | | 5.50 | 0.177 | | 0.216 |
| S | | 5.50 | | | 0.216 | |



5 Revision history

Table 9. Revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 09-Sep-2004 | 2 | Complete version |
| 17-Aug-2006 | 3 | New template, no content change |
| 20-Apr-2007 | 4 | Typo errors on Table 6 |
| 02-Jul-2007 | 5 | Table 2 has been updated |

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