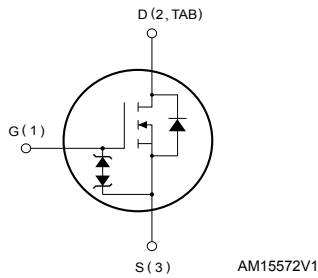
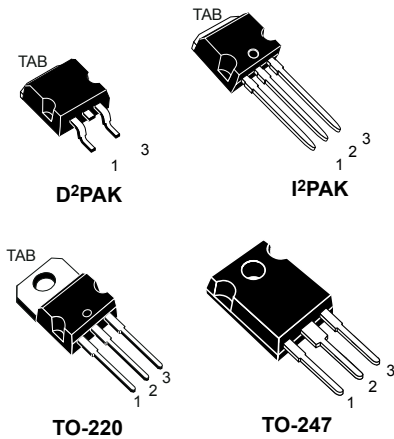


N-channel 600 V, 0.255 Ω typ., 13 A MDmesh M2 Power MOSFETs in D²PAK, I²PAK, TO-220 and TO-247 packages



Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max.}$	I_D	Package
STB18N60M2	650 V	0.280 Ω	13 A	D ² PAK
STI18N60M2				I ² PAK
STP18N60M2				TO-220
STW18N60M2				TO-247

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Application

- Switching applications
- LLC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using the MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.

Product status link

[STB18N60M2](#)

[STI18N60M2](#)

[STP18N60M2](#)

[STW18N60M2](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	52	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 13\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	I ² PAK TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case	1.14			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	50	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30			$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	135	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$		0.255	0.280	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	791	-	μF
C_{oss}	Output capacitance		-	40	-	μF
C_{riss}	Reverse transfer capacitance		-	1.3	-	μF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$	-	164.5	-	μF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ V}$	-	5.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 13\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	21.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	11.3	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 6.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	12	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	47	-	ns
t_f	Fall time		-	10.6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	305		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	3.3		μC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	417		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	4.6		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	22		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

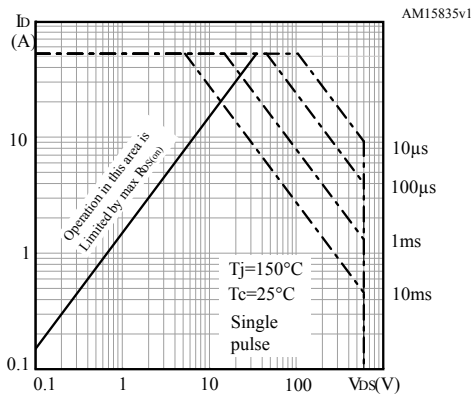
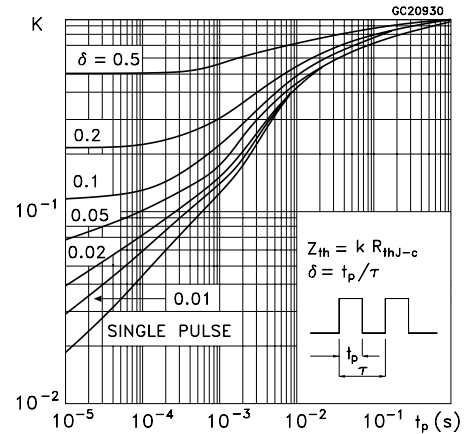
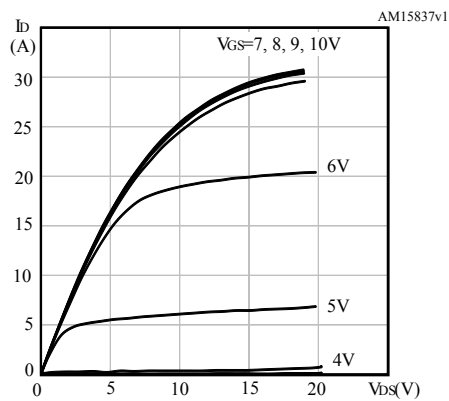
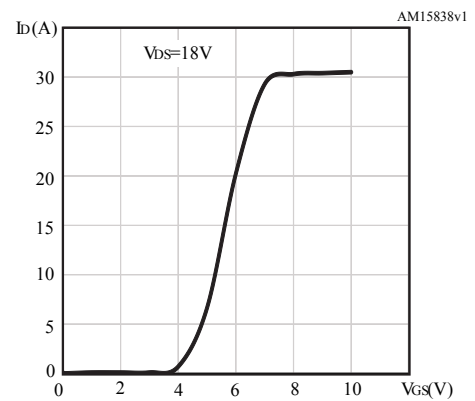
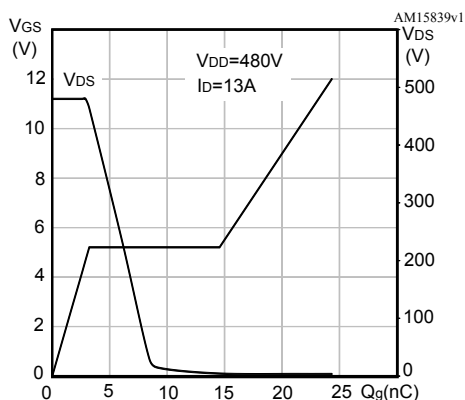
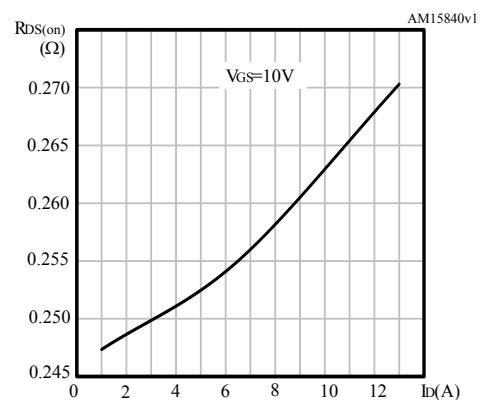
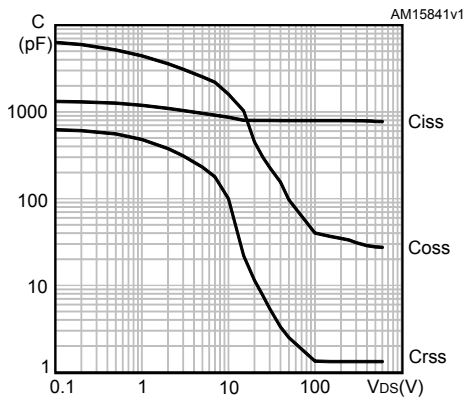
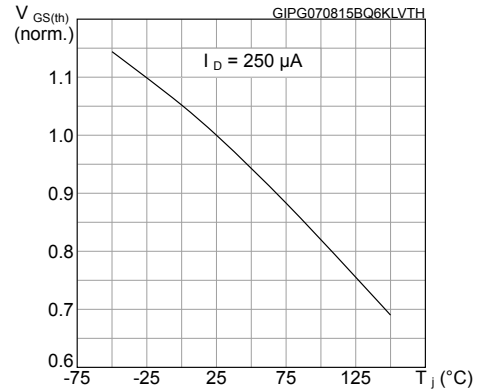
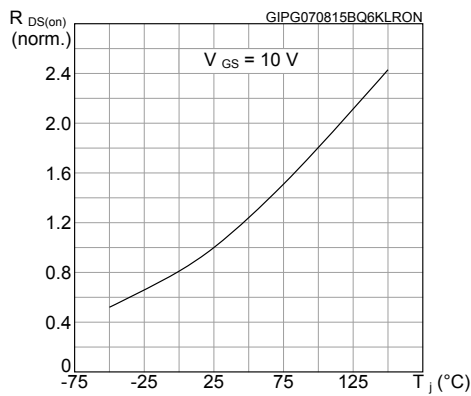
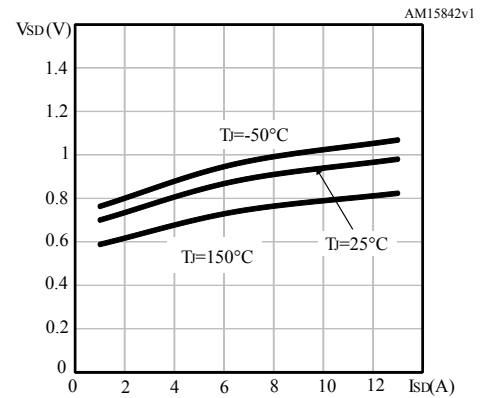
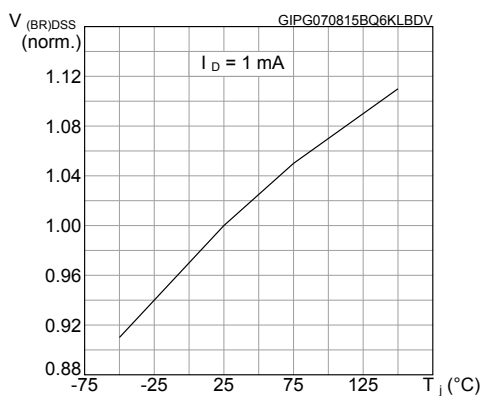
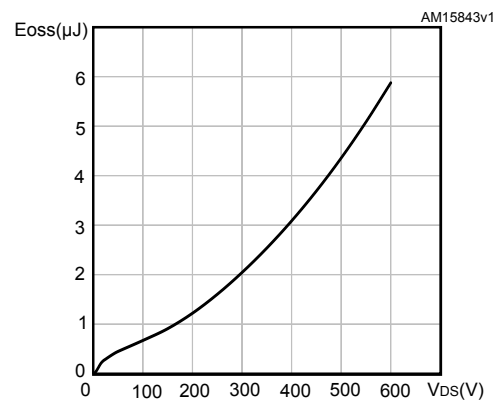
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Source-drain diode forward characteristics

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Output capacitance stored energy


3 Test circuits

Figure 13. Test circuit for resistive load switching times



AM01468v1

Figure 14. Test circuit for gate charge behavior



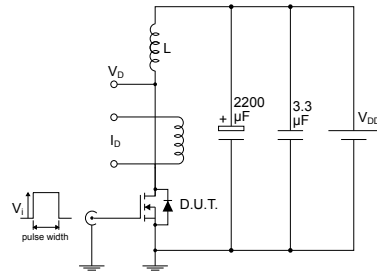
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Figure 15. Test circuit for inductive load switching and diode recovery times



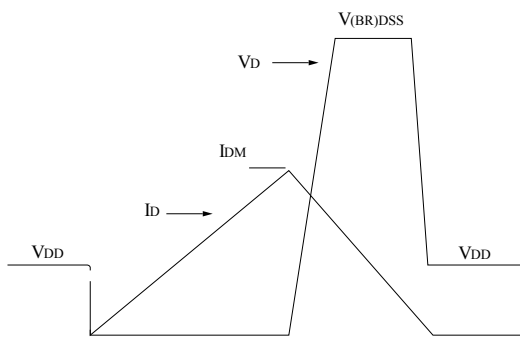
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Figure 16. Unclamped inductive load test circuit



AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

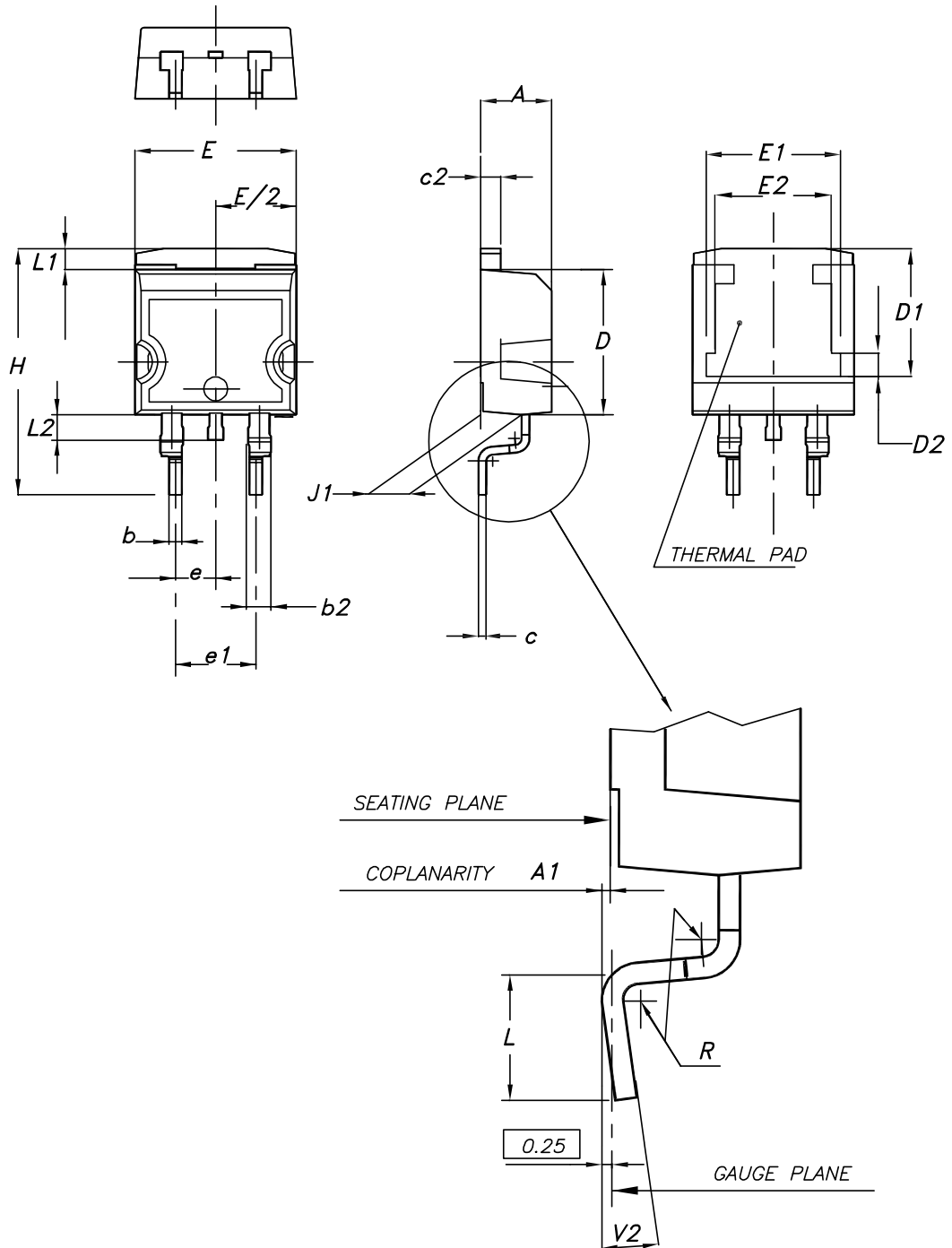


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) package information

Figure 19. D²PAK (TO-263) type A package outline

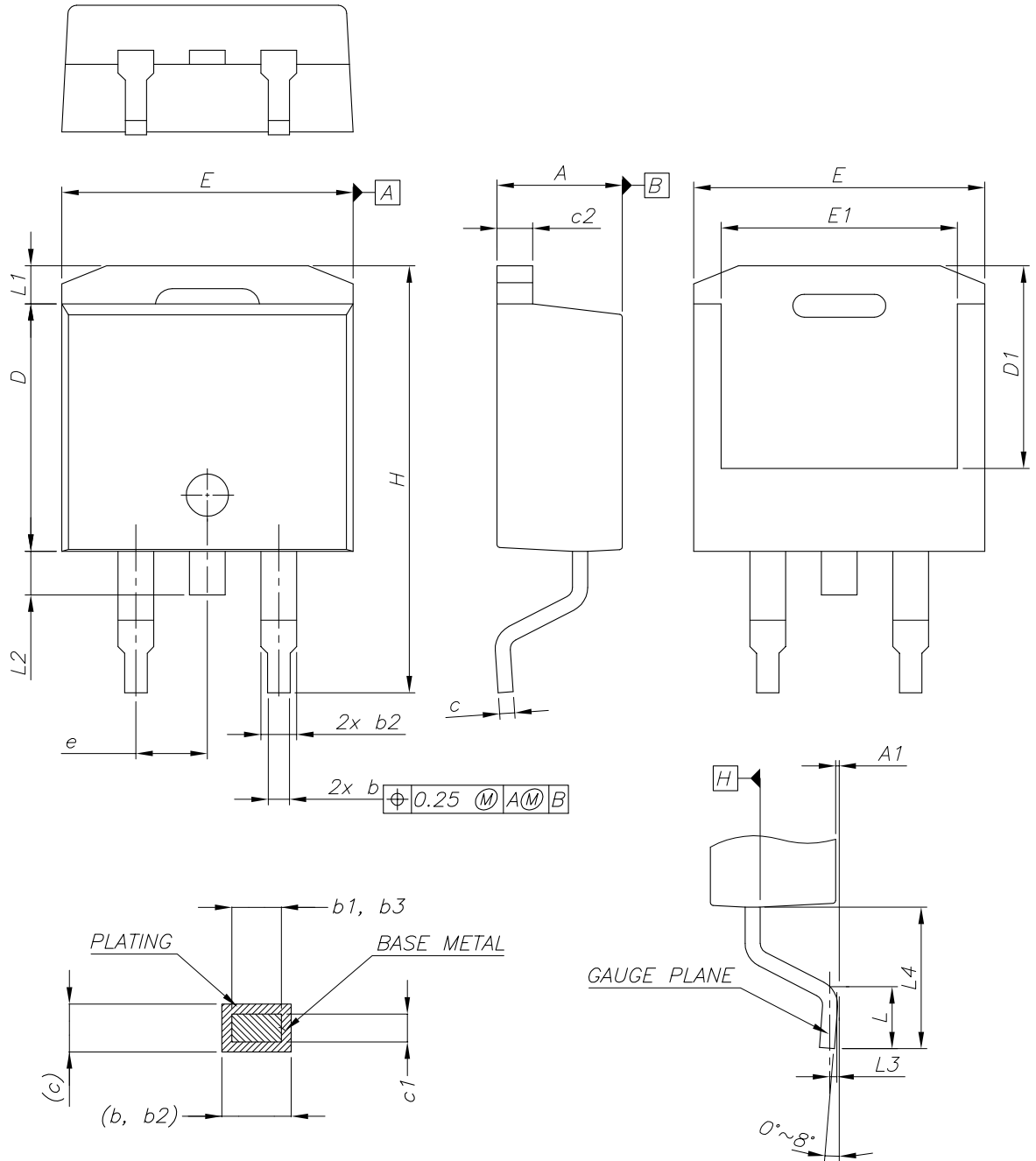


0079457_25

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20. D²PAK (TO-263) type B package outline

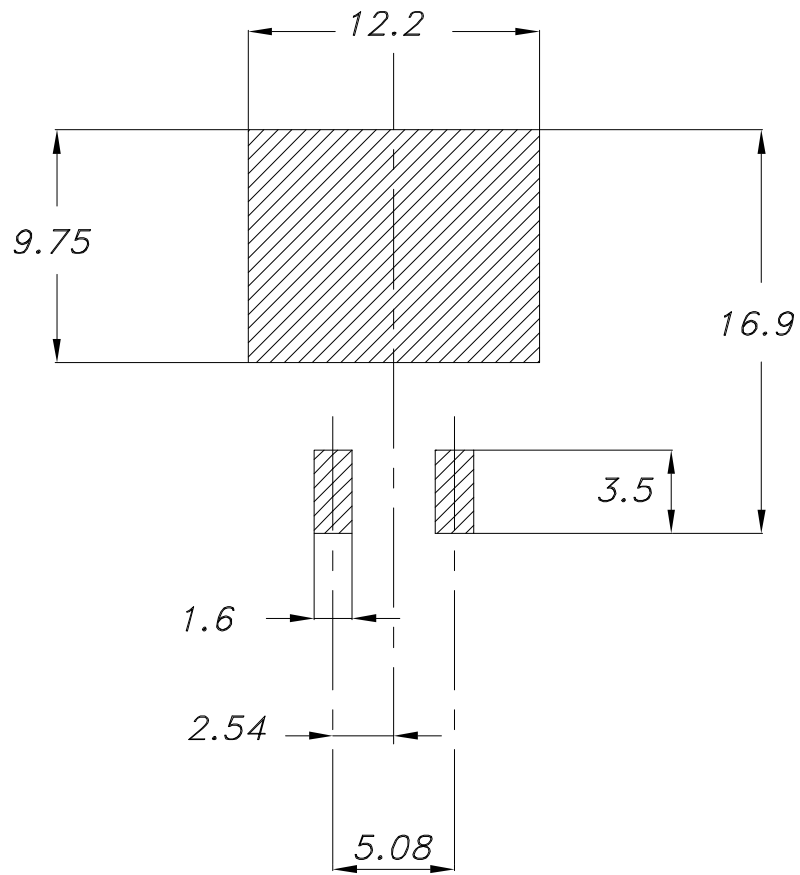


0079457_25_B

Table 9. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

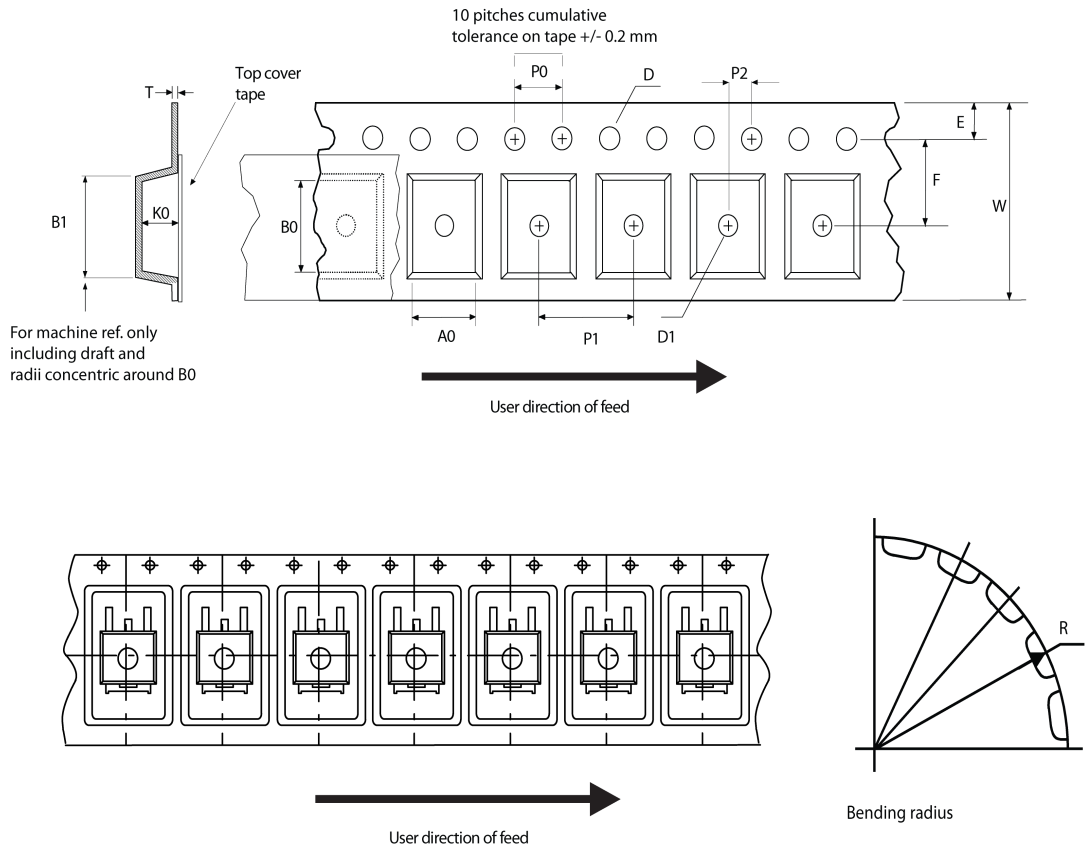
Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)



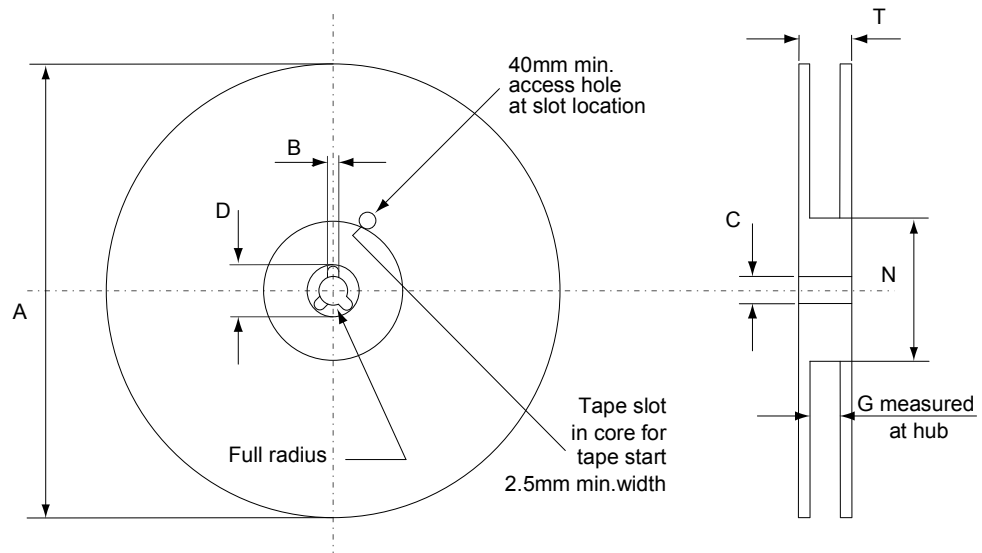
Footprint

4.2 D²PAK packing information

Figure 22. D²PAK tape outline



AM08852v1

Figure 23. D²PAK reel outline


AM06038v1

Table 10. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1	Base quantity		
P1	11.9	12.1			
P2	1.9	2.1	Bulk quantity		
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 D²PAK type B packing information

Figure 24. D²PAK type B tape outline

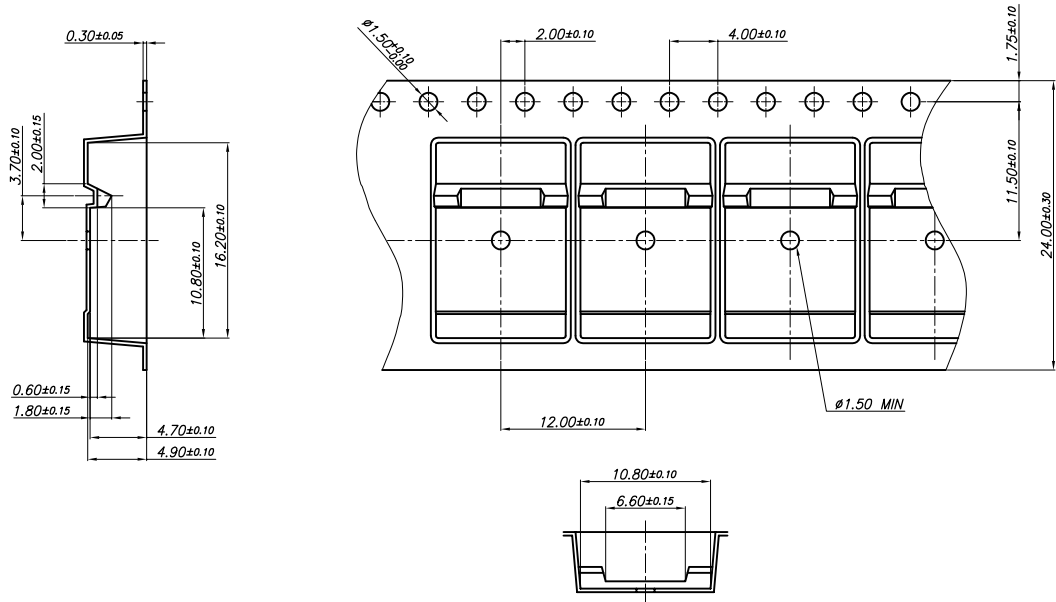
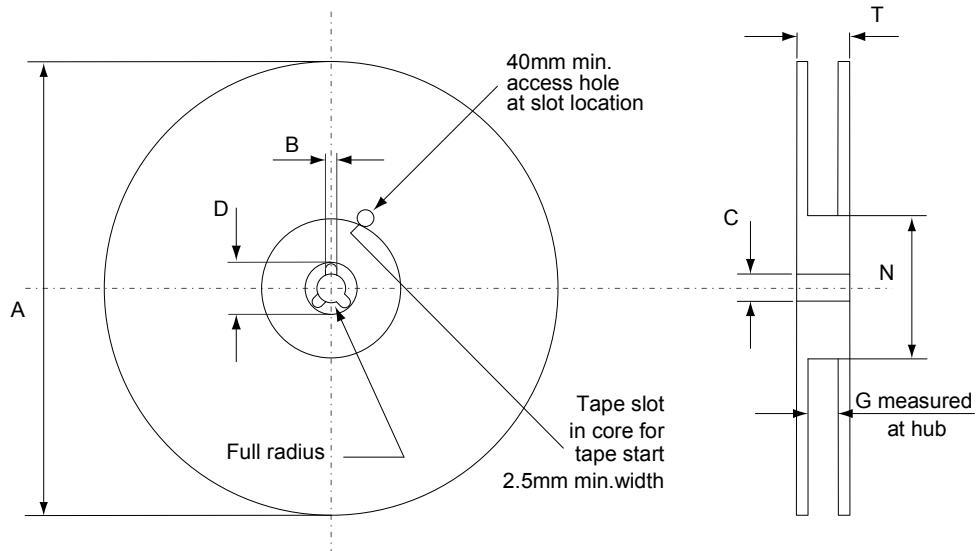


Figure 25. D²PAK type B reel outline



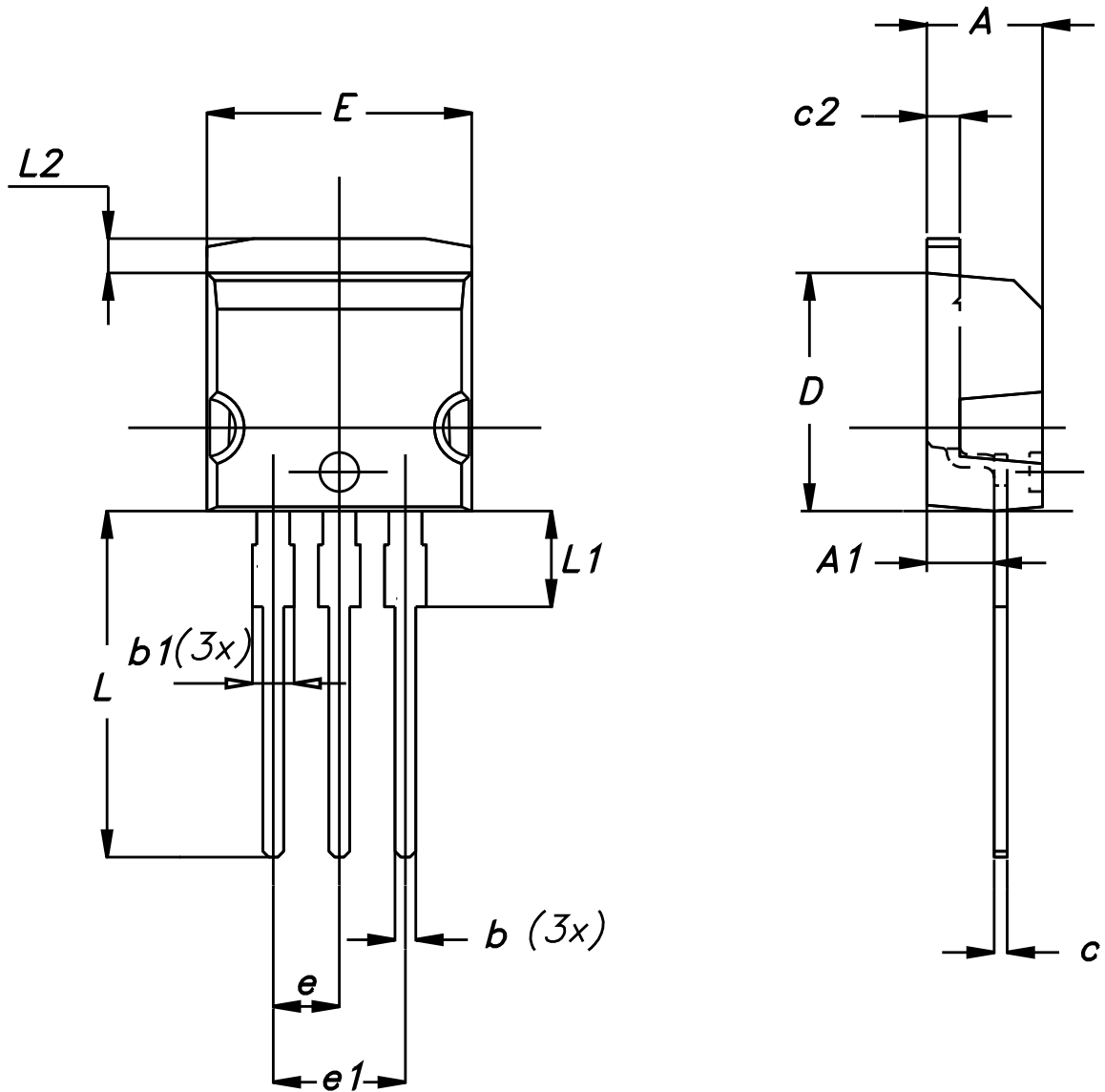
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Table 11. D²PAK type B reel mechanical data

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

4.4 I²PAK package information

Figure 26. I²PAK package outline



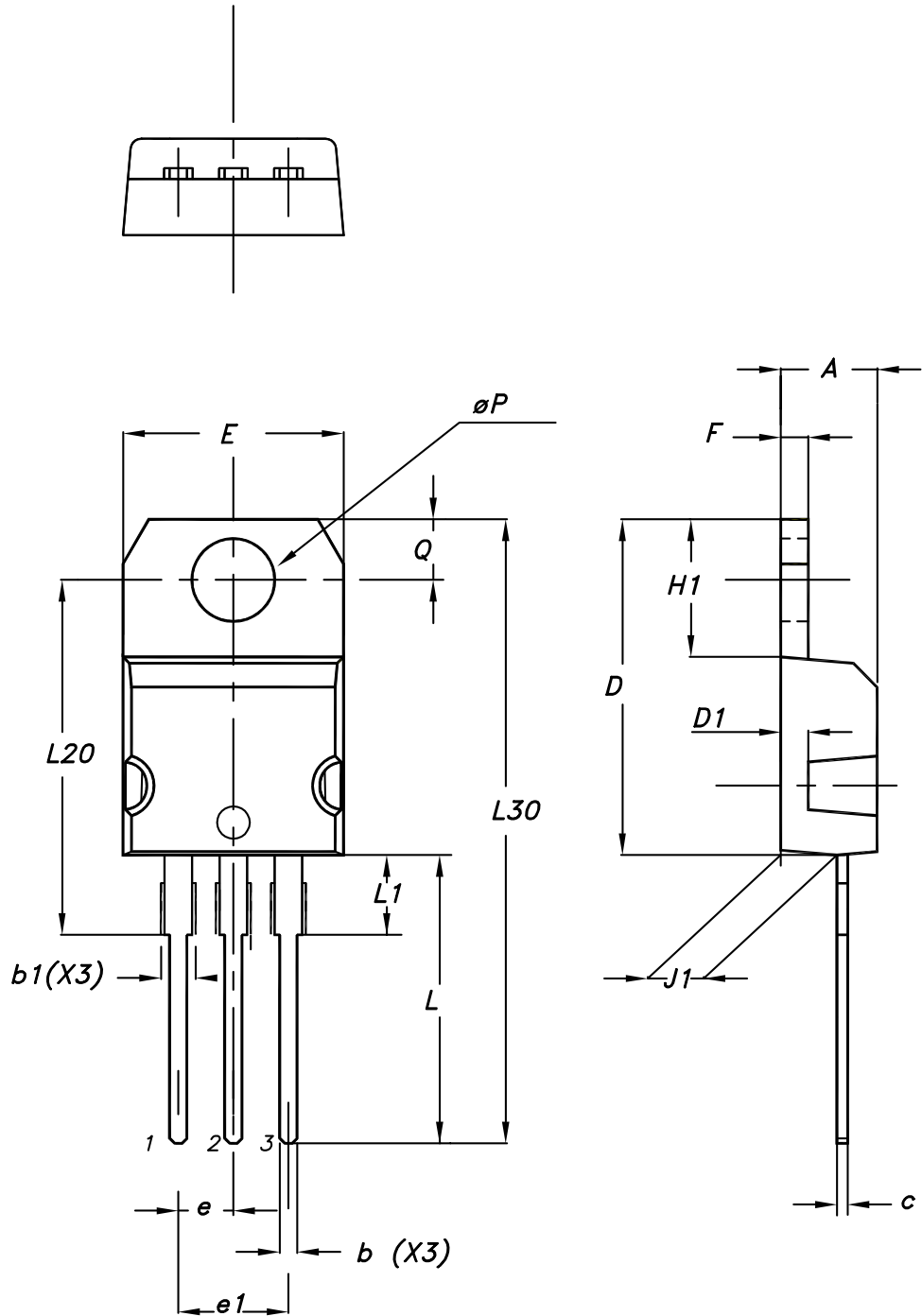
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Table 12. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.5 TO-220 type A package information

Figure 27. TO-220 type A package outline



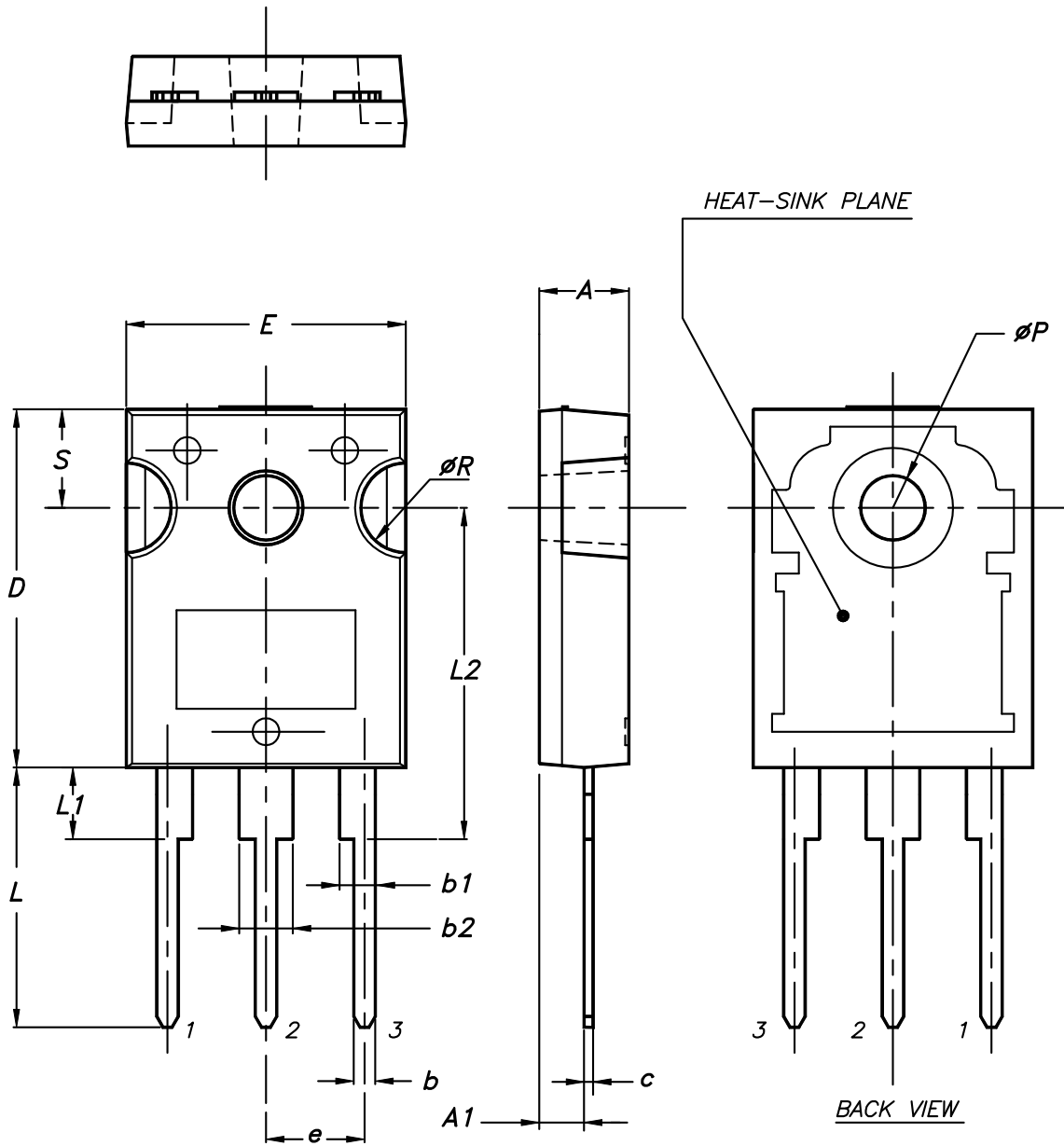
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Table 13. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 TO-247 package information

Figure 28. TO-247 package outline



0075325_9

Table 14. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Ordering information

Table 15. Order codes

Order code	Marking	Package	Packing
STB18N60M2	18N60M2	D ² PAK	Tape and reel
STI18N60M2		I ² PAK	Tube
STP18N60M2		TO-220	
STW18N60M2		TO-247	

Revision history

Table 16. Document revision history

Date	Version	Changes
05-Jun-2013	1	First release.
28-Feb-2014	2	<ul style="list-style-type: none"> – Modified: note 1 in Table 2 – Rthj-case value in Table 3 – Minor text changes
16-Apr-2018	3	<p>Removed maturity status indication from cover page. The document status is production data.</p> <p>Modified the title and the description in cover page.</p> <p>Updated Section 4 Package information.</p> <p>Minor text changes.</p>
06-Nov-2018	4	<p>Added part number STI18N60M2 in I²PAK, document updated accordingly.</p> <p>Updated Section 2.1 Electrical characteristics curves and Section 4 Package information.</p> <p>Minor text changes.</p>

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