

STN1110

Multiprotocol OBD to UART Interpreter Datasheet

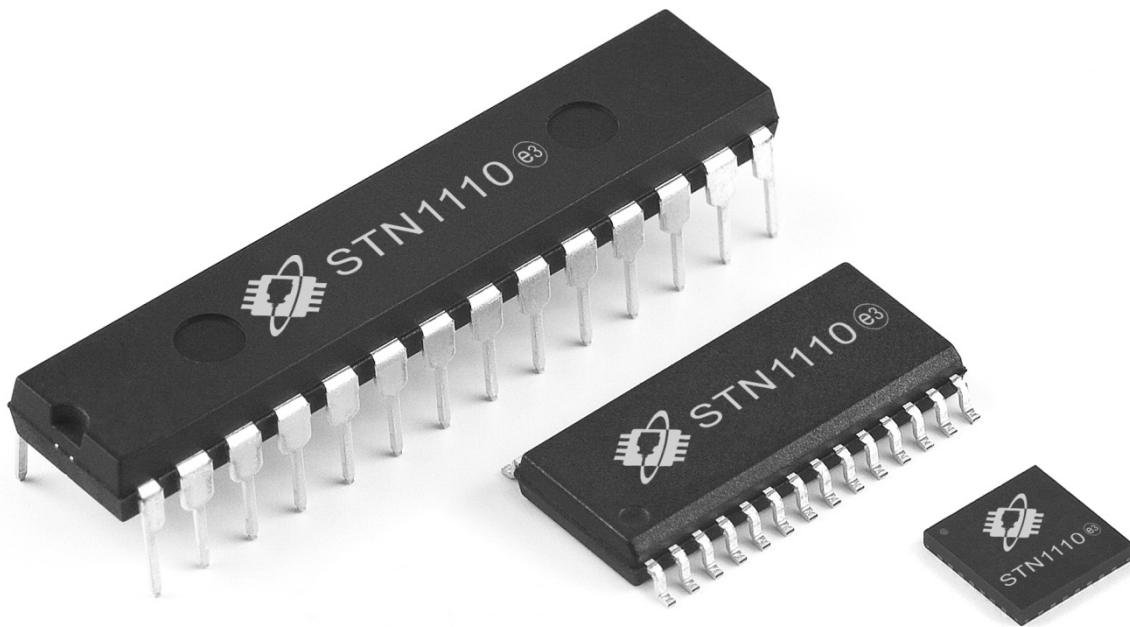


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1.0 Overview

This datasheet summarizes the features of the STN1110 device. It is not intended as a comprehensive reference source. To complement the information in this datasheet refer to the “**STN1100 Family Reference and Programming Manual**”. Please see the OBD Solutions website (www.obdsol.com) for the latest version of the STN1100 Family Reference Manual.

The STN1110 is an OBD to UART interpreter IC designed to provide bi-directional half-duplex communication with the vehicle's On-Board Diagnostic System (OBD-II). It supports all legislated OBD-II protocols

A wealth of information can be obtained by tapping into the OBD bus, including the status of the malfunction indicator light (MIL), diagnostic trouble

codes (DTCs), inspection and maintenance (I/M) information, freeze frames, VIN, hundreds of real-time parameters, and more.

The STN1110 is fully compatible with the *de facto* industry standard ELM327 command set. Based on a 16-bit processor core, the STN1110 offers more features and better performance than any other ELM327 compatible IC.

2.0 Feature Highlights

- **Stable, field-tested firmware**
- Fully **compatible with the ELM327** AT command set
- **Extended ST command set**
- **UART interface** (baud rates from 38 bps to 10 Mbps¹)
- Secure **bootloader** for easy firmware updates
- Support for **all legislated OBD-II protocols**:
 - ISO 15765-4 (CAN)
 - ISO 14230-4 (Keyword Protocol 2000)
 - ISO 9141-2 (Asian, European, Chrysler vehicles)
 - SAE J1850 VPW (GM vehicles)
 - SAE J1850 PWM (Ford vehicles)
- Support for **non-legislated OBD protocols**:
 - ISO 15765
 - ISO 11898 (raw CAN)
- Support for the heavy-duty **SAE J1939 OBD protocol**
- Superior **automatic protocol detection** algorithm
- **Large memory buffer**
- Sophisticated **PowerSave Sleep/Wakeup Triggers**
- Available in **SPDIP, SOIC** and **QFN-S** packages
- **RoHS** compliant

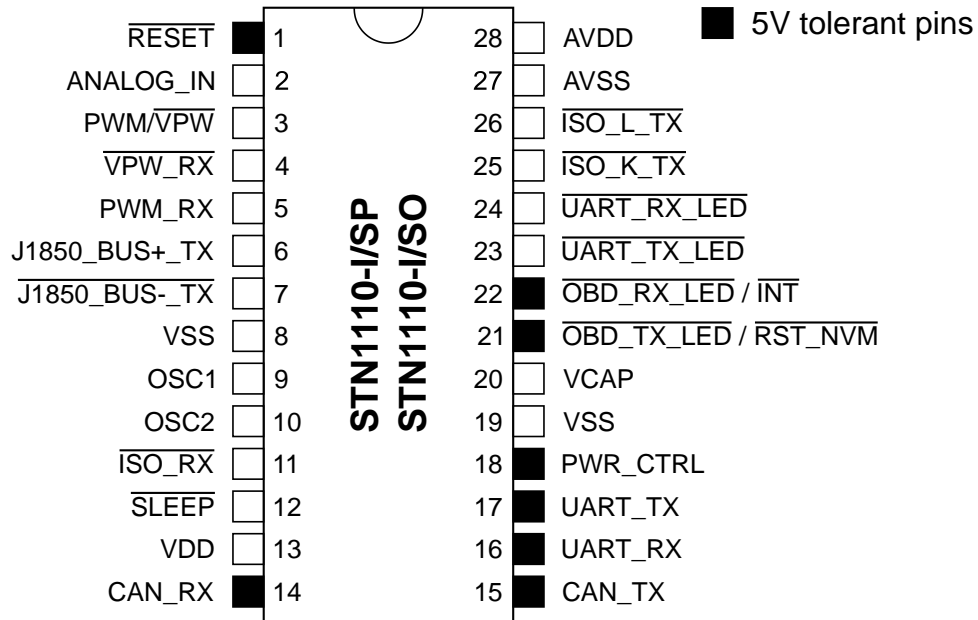
Note 1: Maximum theoretical baud rate. Actual maximum baud rate is application dependent and may be limited by driver hardware.

3.0 Typical Applications

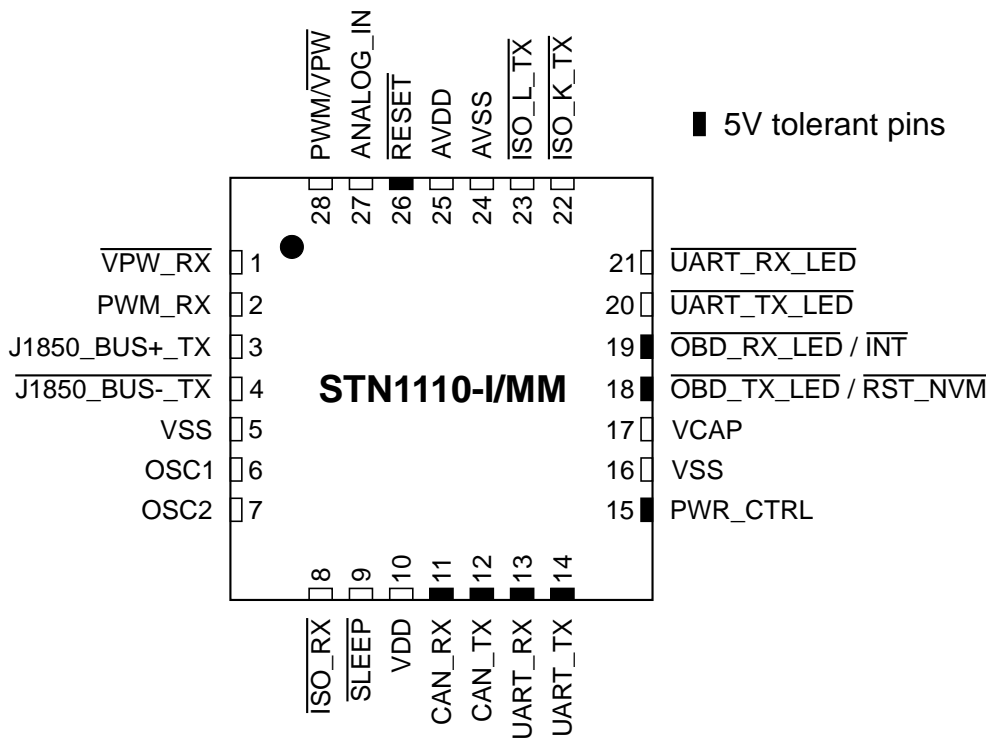
- Vehicle telematics
- Fleet management and tracking applications
- Usage-based insurance (UBI)
- OBD data loggers
- Automotive diagnostic scan tools and code readers
- Digital dashboards

4.0 Pinout

28-Pin SPDIP, SOIC



28-Pin QFN-S⁽¹⁾



Note 1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4.1 Pinout Summary

Table 1: Pinout Summary

| Pin Number | | Pin Name | Pin Type | Pin Description |
|------------|-------|----------------------|--------------|--|
| SOIC SPDIP | QFN-S | | | |
| 1 | 26 | RESET | I, 5V | Active low device reset input |
| 2 | 27 | ANALOG_IN | A | Analog voltage measurement input |
| 3 | 28 | PWM/VPW | O, 4x | SAE J1850 PWM/VPW Bus+ voltage select output |
| 4 | 1 | VPW_RX | I | Active low J1850 VPW receive input |
| 5 | 2 | PWM_RX | I | SAE J1850 PWM receive input |
| 6 | 3 | J1850_BUS+_TX | O, 4x | SAE J1850 Bus+ transmit output |
| 7 | 4 | J1850_BUS-_TX | O, 4x | Active low SAE J1850 Bus- transmit output |
| 8 | 5 | VSS | P | Ground reference for logic and I/O pins |
| 9 | 6 | OSC1 | I | 16.000 MHz oscillator crystal input |
| 10 | 7 | OSC2 | O | 16.000 MHz oscillator crystal output |
| 11 | 8 | ISO_RX | I | Active low ISO 9141/ISO 14230 K-line input |
| 12 | 9 | SLEEP | I | External sleep control input |
| 13 | 10 | VDD | P | Positive supply for logic and I/O pins |
| 14 | 11 | CAN_RX | I, 5V | CAN receive input |
| 15 | 12 | CAN_TX | OD, 5V, 4x | CAN transmit output |
| 16 | 13 | UART_RX | I, 5V | UART receive input |
| 17 | 14 | UART_TX | OD, 5V, 4x | UART transmit output |
| 18 | 15 | PWR_CTRL | OD, 5V, 4x | External power control output |
| 19 | 16 | VSS | P | Ground reference for logic and I/O pins |
| 20 | 17 | VCAP | P | CPU logic filter capacitor connection |
| 21 | 18 | OBD_TX_LED / RST_NVM | OD/I, 5V, 2x | Active low OBD transmit activity LED output <i>and</i> active low input to reset non-volatile settings to factory defaults |
| 22 | 19 | OBD_RX_LED / INT | OD, 5V, 2x | Active low OBD receive activity LED <i>or</i> interrupt output |
| 23 | 20 | UART_TX_LED | O, 4x | Active low UART transmit activity LED output |
| 24 | 21 | UART_RX_LED | O, 4x | Active low UART receive activity LED output |
| 25 | 22 | ISO_K_TX | O, 4x | Active low ISO 9141/ISO 14230 K-line output |
| 26 | 23 | ISO_L_TX | O, 4x | Active low ISO 9141/ISO 14230 L-line output |
| 27 | 24 | AVSS | P | Analog ground reference |
| 28 | 25 | AVDD | P | Analog positive supply |
| — | PAD | | — | Thermal pad |

Legend:

| | | | | | |
|---|--|----|-----------------------|----|-------------------------|
| I | – Schmitt trigger input with CMOS levels | O | – digital output | 2x | – 2x source/sink driver |
| A | – analog input | OD | – open drain output | 4x | – 4x source/sink driver |
| P | – power pin | 5V | – 5 volt tolerant pin | | |

4.2 Detailed Pin Descriptions

RESET

Device reset input. A logic low pulse (min 2 μ s) on this pin will reset the device. Apply a continuous logic low to hold the device in reset. If your circuit does not use this functionality, connect this pin to VDD.

ANALOG_IN

Analog voltage measurement input (AVDD max). By default, this input is calibrated for an external 62 k Ω /10 k Ω voltage divider connected to battery positive. Connect to AVSS if unused.

PWM / VPW

The firmware uses this pin to control the voltage level of the SAE J1850 PWM/VPW Bus+ supply. When the PWM protocol is selected, it outputs a logic high to switch the supply voltage to a nominal 5V. When the VPW protocol is selected, it outputs a logic low to switch the supply voltage to a nominal 8V. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

VPW_RX

Active low SAE J1850 VPW receive input. When the SAE J1850 Bus+ is in the recessive (low) state, this pin should be at a logic high level. When the SAE J1850 Bus+ is in the dominant (high) state, this pin should be at a logic low level. Pull up to VDD if unused.

PWM_RX

SAE J1850 PWM receive input. When the SAE J1850 bus is in the recessive state (Bus+ is low, Bus- is high), this pin should be at a logic low level. When the SAE J1850 bus is in the dominant (Bus+ is high) state, this pin should be at a logic high level. Connect to VSS if unused.

J1850_BUS+_TX

SAE J1850 Bus+ transmit output. When the pin is high, Bus+ should be high (dominant). This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

J1850_BUS-_TX

Active low SAE J1850 Bus- transmit output. When the pin is high, Bus- should be low (dominant). This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

VSS

Ground reference for logic and I/O pins.

OSC1, OSC2

16.000 MHz oscillator crystal connection.

ISO_RX

Active low ISO 9141/ISO 14230 K-line receive input. When K-line is high (recessive), this pin should be at a logic low level. Connect to VSS if unused.

SLEEP

External sleep control input. When enabled in firmware, puts the device into low-power sleep mode. Polarity of this pin can be configured in firmware; default configuration is active low. Internal pull-up to VDD is enabled by default, but can be disabled in firmware. Leave unconnected if unused.

VDD

Positive 3.0 – 3.6V supply for logic and I/O pins.

CAN_RX

CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

CAN_TX

CAN transmit output. Open drain – requires a pull-up to VDD or 5V. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull-up value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 k Ω . Pull up to VDD via 100 k Ω resistor if unused.

UART_RX

UART receive input. Compatible with 3.3V and 5V logic.

UART_TX

UART transmit output. Open drain – requires a pull-up to VDD or 5V. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull-up value depends on UART baud rate and the trace length (higher resistor values can be used with lower baud rates and shorter traces); typical value is 1 k Ω .

PWR_CTRL

External power control output. Used to switch external circuitry into low-power (sleep) state. Polarity can be configured in firmware; default configuration is active high (logic low = sleep mode). Open drain – requires a pull-up to VDD or 5V; be mindful of the fact that the pull-up will draw current in low-power state. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Pull down to VSS via 100 k Ω resistor if unused.

VCAP

CPU logic filter capacitor connection. Connect to a low-ESR (< 5 Ω) tantalum or ceramic capacitor. Minimum value is 4.7 μ F; typical value is 10 μ F.

OBD_TX_LED / RST_NVM

Active low OBD transmit activity LED output *and* active low input to reset NVM to factory defaults. Open drain – requires a pull-up to VDD or 5V. This pin has a 2x current rating (see Table 6 “Output Pin DC Specifications”). Pull up to VDD via 100 k Ω resistor if unused.

OBD_RX_LED / INT

Active low OBD receive activity LED *or* interrupt output. Open drain – requires a pull-up to VDD or 5V when configured as interrupt. This pin has a 2x current rating (see Table 6 “Output Pin DC Specifications”). Pull up to VDD if unused.

UART_TX_LED

Active low UART transmit activity LED output. Voltage on the anode of the LED must not exceed VDD + 0.3V.

This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

UART_RX_LED

Active low UART transmit activity LED output. Voltage on the anode of the LED must not exceed VDD + 0.3V. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

ISO_K_TX

Active low ISO 9141/ISO 14230 K-line output. When the pin is logic high, K-line should be low. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

ISO_L_TX

Active low ISO 9141/ISO 14230 L-line output. When the pin is logic high, L-line should be low. This pin has a 4x current rating (see Table 6 “Output Pin DC Specifications”). Leave unconnected if unused.

AVSS

Analog ground reference. Must be connected to analog “clean” ground (between VSS - 0.3V and VSS + 0.3V) or VSS.

AVDD

Analog positive supply. Must be connected to VDD or an external voltage reference (between VDD - 0.3V or 3.0V, whichever is greater and VDD + 0.3V or 3.6V, whichever is less). AVDD may be decoupled from digital supply by connecting it to VDD via a 10 Ω resistor or a small (10 μ H – 47 μ H) inductor.

PAD

The metal plane at the bottom of the device (QFN package only). It is not connected to any pins internally. Connect to VSS externally.

5.0 Guidelines for Getting Started with STN1110

5.1 Basic Connection Requirements

Getting started with the STN1110 IC requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- **VDD and both Vss** pins (see Section 5.2 “Decoupling Capacitors”)
- **AVDD and AVSS** pins (see Section 5.2 “Decoupling Capacitors” and Section 5.3 “AVDD and AVSS Pins”)
- **VCAP** (see Section 5.4 “Internal Voltage Regulator Filter Capacitor”)
- **RESET** pin (see Section 5.5 “Device Reset Pin”)
- **OSC1 and OSC2** pins (see Section 5.6 “Oscillator Pins”)
- **RST_NVM** pin (see Section 5.7 “NVM Reset Input”)
- **Open Drain Output Pull-ups** (see Section 5.8 “Open Drain Outputs”)

5.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, Vss and AVDD, AVSS is required. Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 1 μF , 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within $\frac{1}{4}$ ” (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and

return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

5.2.1 Tank Capacitors

On boards with power traces running longer than six inches in length, use a tank capacitor for integrated circuits, including STN1110, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

5.3 AVDD and AVSS Pins

As a minimum, AVDD must be connected directly to VDD and AVSS must be connected directly to VSS. It is recommended that AVDD be connected to VDD via a 10 Ω resistor or a small (10 μH – 47 μH) inductor.

AVSS should be connected to the electrically cleanest ground net (plane). For best results, analog circuitry should have a separate ground plane with a point connection to VSS ground plane as close as possible to the AVSS pin.

5.4 Internal Voltage Regulator Filter Capacitor

A low-ESR ($< 5 \Omega$) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 μF and 10 μF , 16V connected to ground. The type can be ceramic or tantalum. Refer to Section 7.2 “Electrical Characteristics” for additional information. The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceed $\frac{1}{4}$ ” (6 mm).

5.5 Device Reset Pin

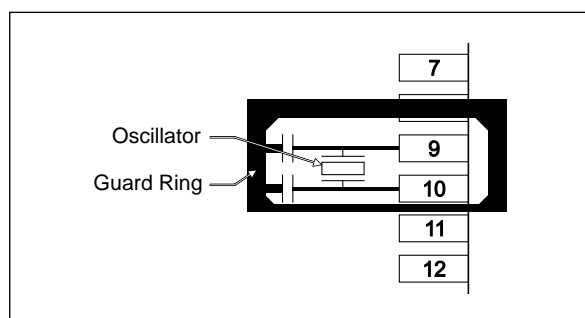
RESET pin must be logic high for STN1110 to run. If this pin is not controlled by the host controller, it must be connected to VDD.

It is recommended to pull up RESET pin to VDD via a 10 k Ω resistor.

5.6 Oscillator Pins

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the STN1110 ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 1.

Figure 1 – Suggested Placement of the Oscillator Circuit



5.7 NVM Reset Input

RST_NVM pin must be pulled up to VDD via a 100 kΩ resistor for proper device operation.

5.8 Open Drain Outputs

All open drain outputs (as specified in section 4.1) that are in use must be pulled up to VDD or 5V. Specifically, UART_TX pin must be pulled up in order to be able to communicate with the device. See section 4.2 “Detailed Pin Descriptions” for more information.

5.9 Unused Inputs and Unused Open Drain Outputs

None of the unused inputs or unused open drain outputs (as specified in section 4.1) should be left unconnected. The STN1110 is a CMOS integrated

circuit. Leaving any of its inputs or open drain outputs floating may result in IC damage.

Unused open drain outputs can only be terminated with a resistor connected to VDD or 5V. Unused inputs can be terminated via a resistor or direct connection to VSS or VDD.

Unused inputs and open drain outputs should be connected as shown in Table 2. See section 4.2 “Detailed Pin Descriptions” and section 6.1 “Recommended Minimum Connection” for more information.

Table 2 – Recommended Unused Input and Open Drain Output Connections

| Pin Number | | Pin Name | Level |
|------------|-------|----------------------|------------------|
| SOIC SPDIP | QFN-S | | |
| 1 | 26 | RESET | H |
| 2 | 27 | ANALOG_IN | L ⁽¹⁾ |
| 4 | 1 | VPW_RX | H ⁽¹⁾ |
| 5 | 2 | PWM_RX | L ⁽¹⁾ |
| 11 | 8 | ISO_RX | L ⁽¹⁾ |
| 12 | 9 | SLEEP | — ⁽²⁾ |
| 14 | 11 | CAN_RX | H |
| 15 | 12 | CAN_TX | H ⁽³⁾ |
| 16 | 13 | UART_RX | H |
| 17 | 14 | UART_TX | H ⁽³⁾ |
| 18 | 15 | PWR_CTRL | L ⁽⁴⁾ |
| 21 | 18 | OBD_TX_LED / RST_NVM | H ⁽³⁾ |
| 22 | 19 | OBD_RX_LED / INT | H ⁽³⁾ |

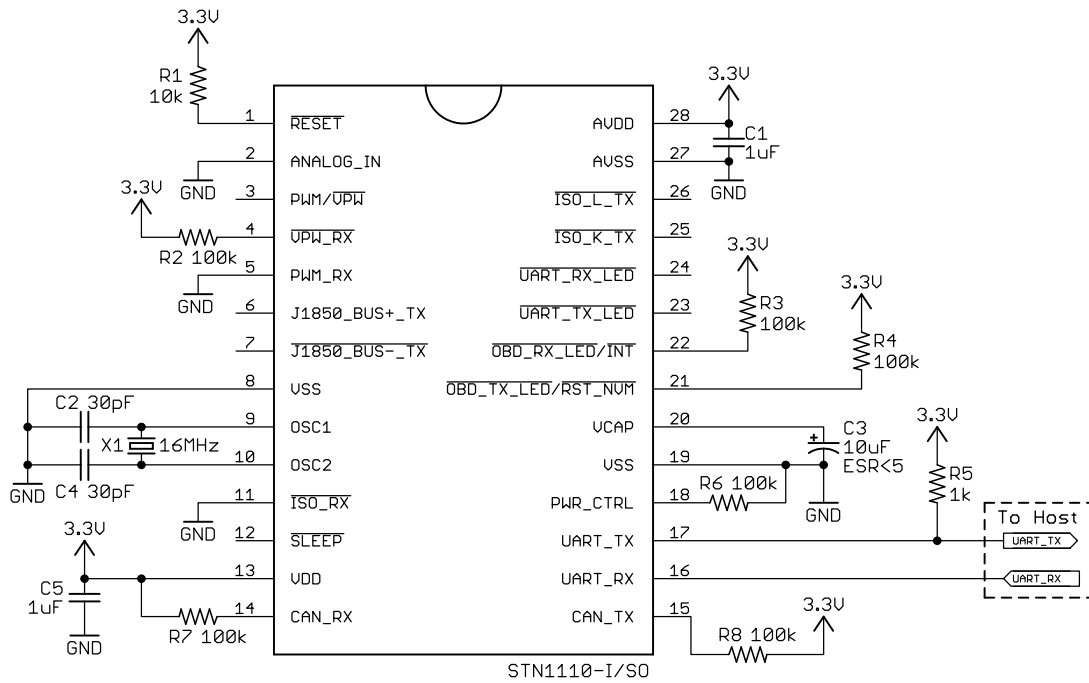
- Note**
1. These inputs may be connected to either VDD or VSS. However, the preferred level is shown.
 2. SLEEP input has internal pull-up to VDD enabled by default. Therefore, it can be left unconnected.
 3. These open drain outputs cannot be connected to VDD directly. They can only be connected to VDD or 5V via a resistor.
 4. This open drain output should not be connected to VSS directly. For reduced current consumption during sleep, when unused, this output should be connected to VSS via a resistor.

6.0 Reference Schematics

6.1 Recommended Minimum Connection

Figure 2 shows the recommended minimum of components necessary to get the STN1110 to operate reliably, while minimizing power consumption. It is not a practical circuit; it is intended as a reference to show what to do with unused pins. Refer to the detailed pin descriptions (section 4.2) for more information.

Figure 2 – Recommended Minimum Connection



6.2 Typical Configuration

This section contains schematics showing the typical configuration for the various circuit blocks. Pay special attention when choosing substitutes for components with specific part numbers, to make sure they have the same or better characteristics. Components without specific part numbers are generic. Use good engineering practices and common sense to make sure the specific parts you choose are appropriate for your application.

Figure 3 – STN1110 IC

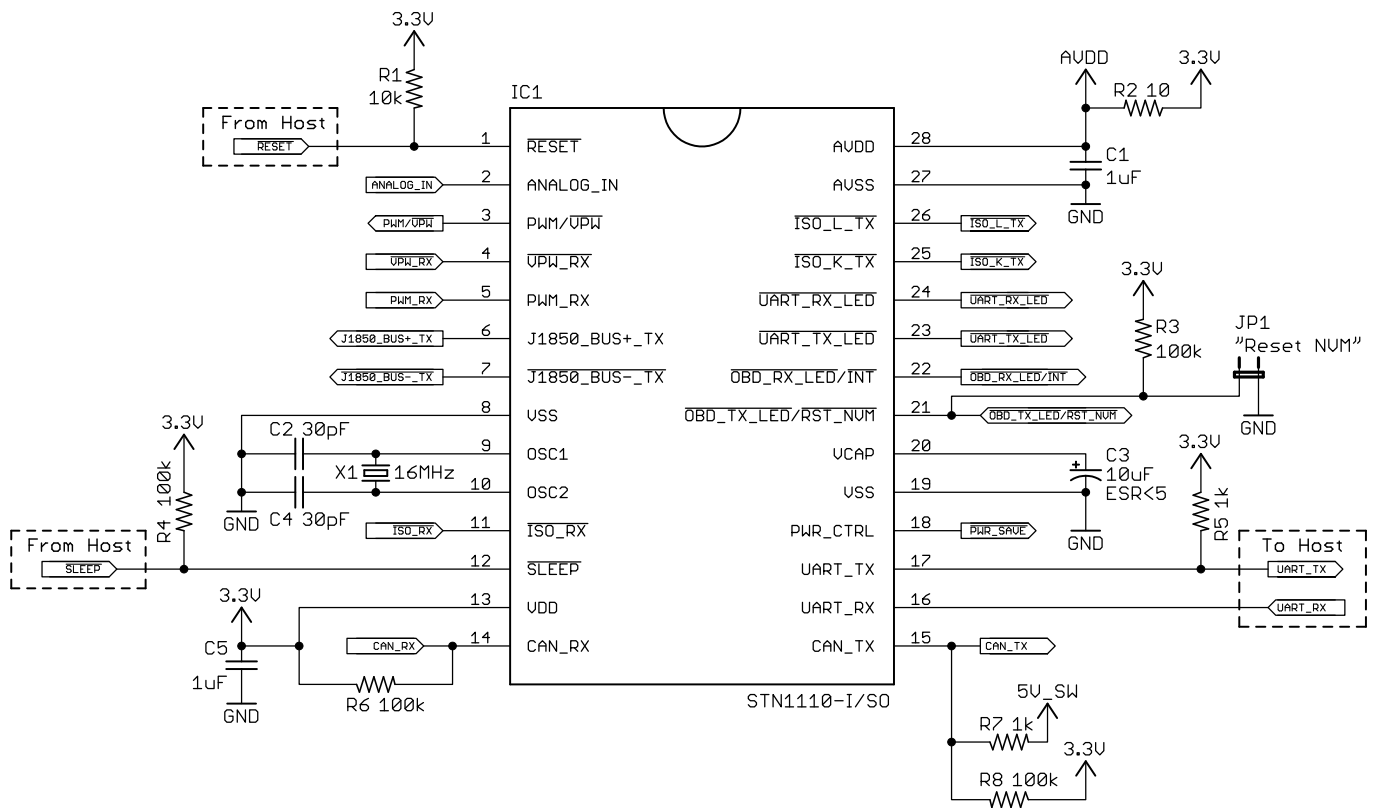


Figure 4 – LEDs

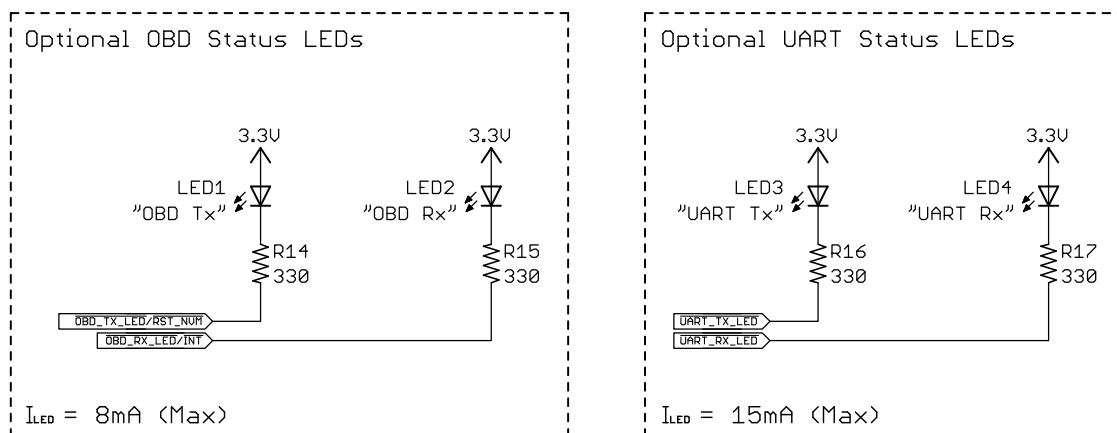


Figure 5 – Voltage Sense

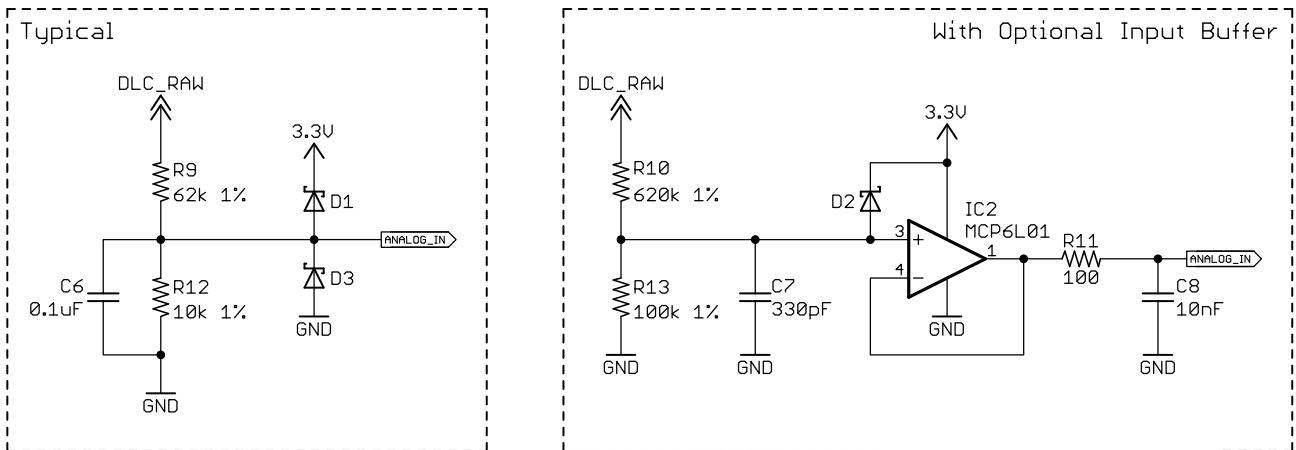


Figure 6 – Power Supplies

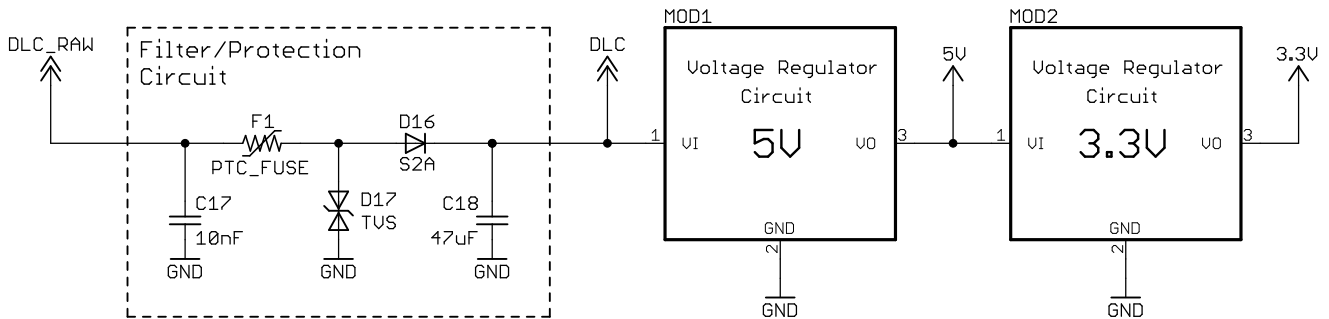


Figure 7 – Switched Power Control

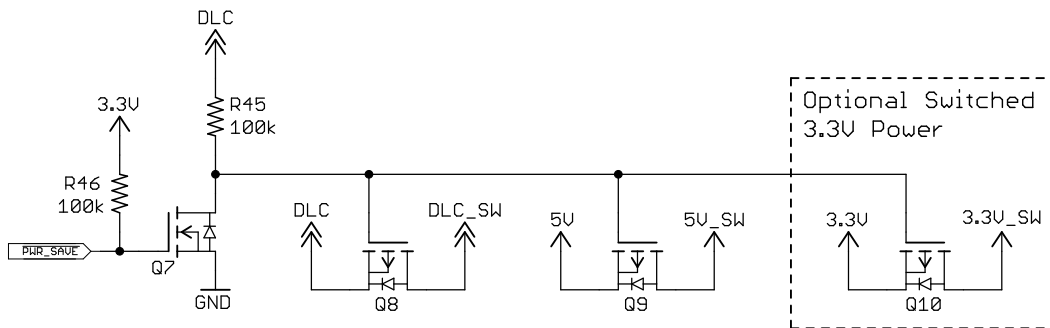


Figure 8 – OBD Port Connector

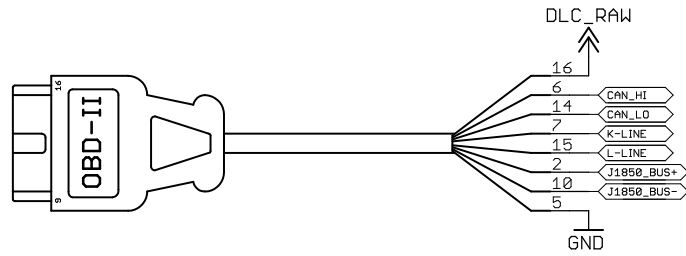


Figure 9 – ISO Transceiver

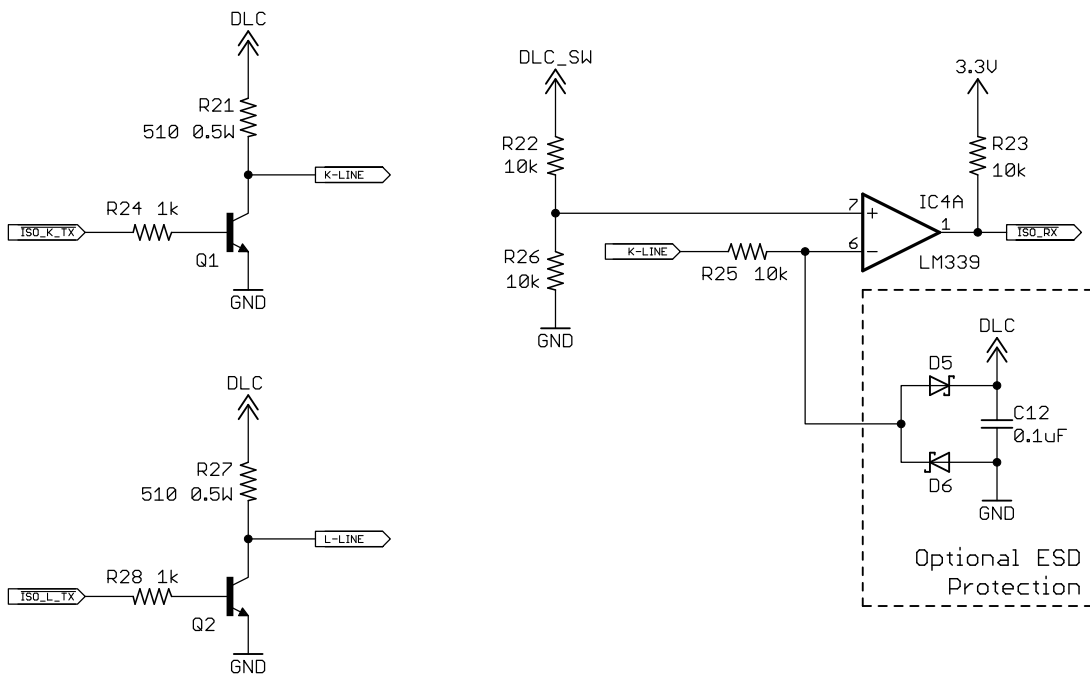
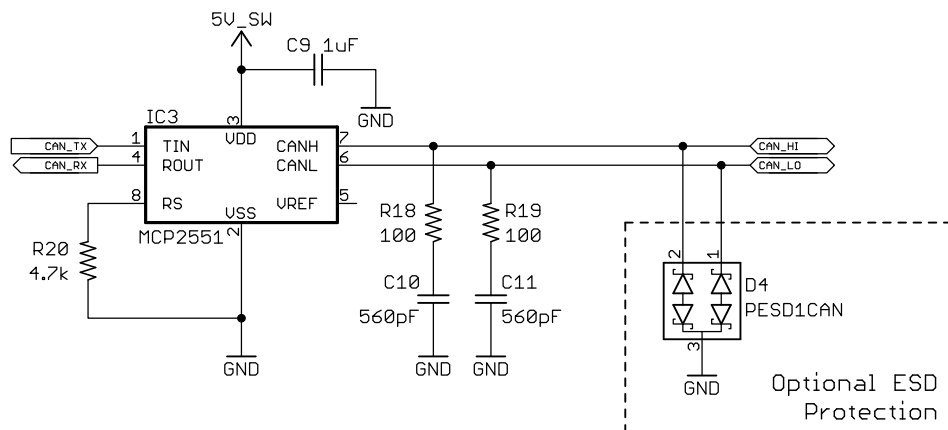


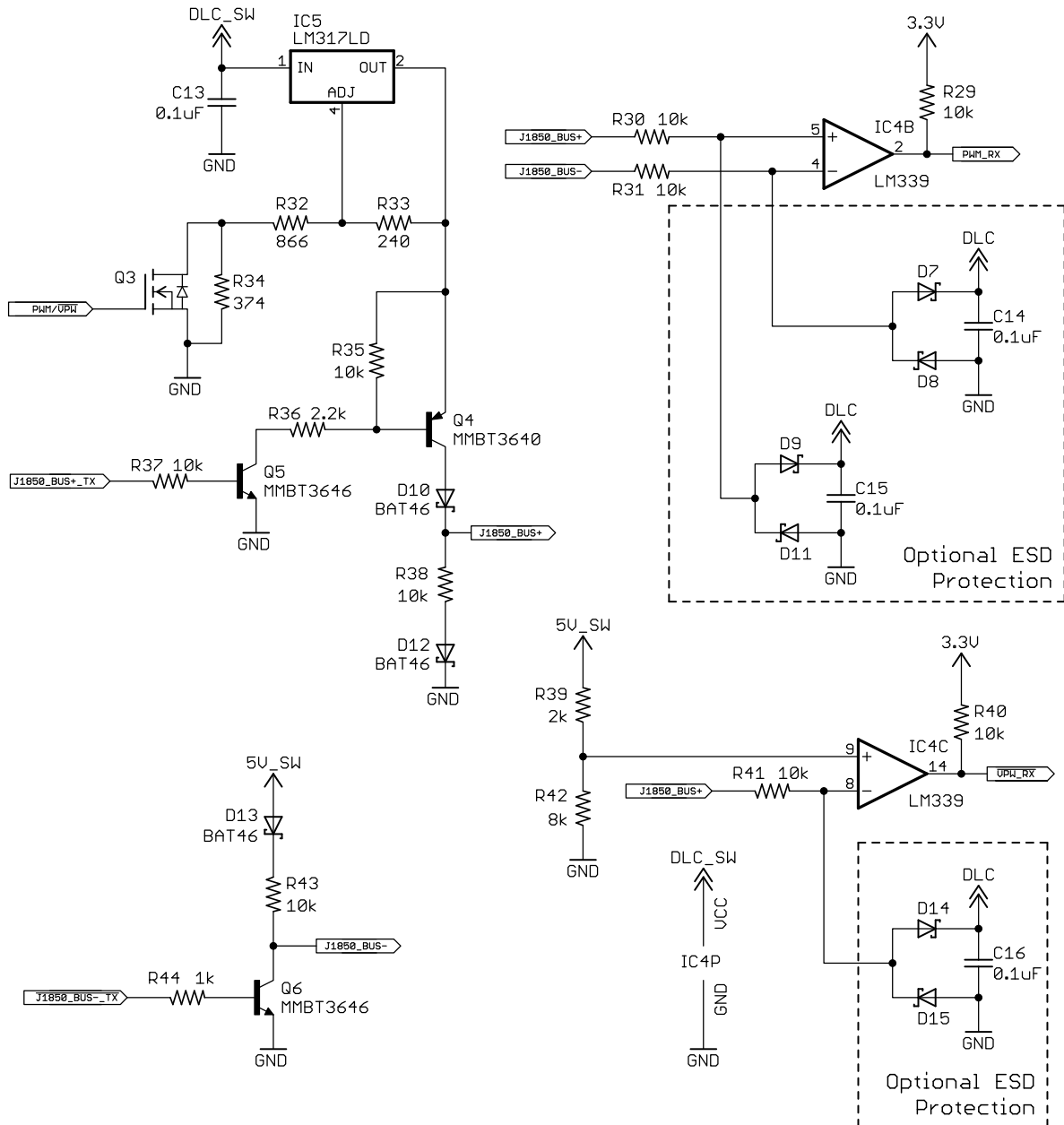
Figure 10 – CAN Transceiver



STN1110

Important: Q4, Q5, and Q6 can only be substituted with transistors that have the same or better switching characteristics. OK to substitute fast-switching silicon diodes (e.g., 1N4148) for D10, D12 and D13. Also, note that the comparator IC4 is powered from DLC_SW.

Figure 11 – J1850 Transceiver



7.0 Electrical Characteristics

This section provides an overview of STN1110 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

The STN1110 is based on the PIC24HJ128GP502 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at <http://www.microchip.com>.

7.1 Absolute Maximum Ratings ⁽¹⁾

| | |
|---|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +160°C |
| Voltage on VDD with respect to VSS | -0.3V to +4.0V |
| Voltage on any pin that is not 5V tolerant with respect to VSS ⁽²⁾ | -0.3V to (VDD + 0.3V) |
| Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽²⁾ | -0.3V to +5.6V |
| Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽²⁾ | -0.3V to 3.6V |
| Maximum current sourced/sunk by any 2x output ⁽³⁾ | 8 mA |
| Maximum current sourced/sunk by any 4x output ⁽³⁾ | 15 mA |

- Note**
1. Stresses beyond those listed here can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 2. See section 4.0 "Pinout" for the list of 5V tolerant pins.
 3. See section 4.1 "Pinout Summary" to determine current rating of individual pins.

7.2 Electrical Characteristics

Table 3: Thermal Operating Conditions

| Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|-----|--------------------------------|-----|-----|------|-------|------------|
| TJ | Operating Junction Temperature | -40 | — | +125 | °C | |
| TA | Operating Ambient Temperature | -40 | — | +85 | °C | |

Table 4: Power Specifications

| Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
|------|---|-----------------------------------|--------------------|----------------------------------|-------|----------------|
| VDD | Supply Voltage | 3.0 | — | 3.6 | V | |
| VPOR | VDD Start Voltage to ensure internal power-on reset (POR) signal | — | — | VSS | V | |
| SVDD | VDD Rise Rate ⁽²⁾ to ensure internal power-on reset (POR) signal | 0.03 | — | — | V/ms | 0–3.0V in 0.1s |
| AVDD | Analog Supply Voltage | Greater of VDD – 0.3 or 3.0 | — | Lesser of VDD + 0.3 or 3.6 | V | |
| AVSS | Analog Ground Reference | VSS – 0.3 | — | VSS + 0.3 | V | |

STN1110

| Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
|------|---|------|--------------------|--------------------|-------|------------------------|
| VBOR | Brown-out Reset Voltage⁽³⁾ on VDD transition high-to-low | 2.40 | — | 2.55 | V | |
| IDD | Operating Current⁽⁴⁾ | — | 68 | 82 ⁽⁵⁾ | mA | |
| IPD | Average Sleep Current^(4,6) | — | 98 | 210 ⁽⁵⁾ | μA | T _A = +25°C |
| | | — | 300 ⁽⁵⁾ | 710 ⁽⁵⁾ | μA | T _A = +85°C |
| CEFC | External Filter Capacitor⁽⁷⁾ connected to VCAP pin | 4.7 | 10 | — | μF | ESR < 5 Ω |

- Note**
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
 2. This spec must be met in order to ensure that a correct internal power-on reset (POR) occurs. It is easily achieved using most common types of supplies, but may be violated if a supply with slowly varying voltage is used, as may be obtained through direct connection to solar cells or some charge pump circuits.
 3. This parameter is for design guidance only and is not tested in manufacturing.
 4. STN1110 device current only. Does not include any load currents.
 5. Values are characterized, but not tested.
 6. All wakeup triggers are on and wakeup trigger inputs are in their inactive states.
 7. Typical VCAP voltage = 2.5V when VDD ≥ VDDMIN.

Table 5: Input Pin DC Specifications

| Sym | Characteristic | Min | Typ ⁽¹⁾ | Max | Units | Conditions |
|-------------------|---|---------|--------------------|-----------------------|-------|--|
| VIL | Input Low Voltage | | | | | |
| | MS_CAN_RX pin | VSS | — | 0.3 VDD | V | |
| | all other inputs | VSS | — | 0.2 VDD | V | |
| VIH | Input High Voltage | | | | | |
| | non-5V tolerant pins ⁽²⁾ | 0.7 VDD | — | VDD | V | |
| | 5V tolerant pins ⁽²⁾ | 0.7 VDD | — | 5.5 | V | |
| VIN | ANALOG_IN Input Voltage | AVSS | — | AVDD | V | |
| RIN | Recommended ANALOG_IN Voltage Source Impedance | — | — | 200 | Ω | |
| I _{PU} | Internal Pull-up Current | 50 | 250 | 400 | μA | VDD = 3.3V, V _{PIN} = VSS |
| I _{ICL} | Input Low Injection Current | 0 | — | -5 ^(4,7) | mA | All pins, except VDD, VSS, AVDD, AVSS, RESET, VCAP, SLEEP, ISO_RX and ISO_K_TX |
| I _{ICH} | Input High Injection Current | 0 | — | +5 ^(5,6,7) | mA | All pins, except VDD, VSS, AVDD, AVSS, RESET, VCAP, SLEEP, ISO_RX, ISO_K_TX, and 5V tolerant designated pins |
| ΣI _{ICT} | Total Input Injection Current sum of all I/O and control pins | 0 | — | 20 ⁽⁸⁾ | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins (I _{ICL} + I _{ICH}) ≤ ΣI _{ICT} |

- Note**
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
 2. See section 4.0 “Pinout” for the list of 5V tolerant pins.

3. Negative current is defined as current sourced by the pin.
4. V_{IL} source < ($V_{SS} - 0.3$). Characterized, but not tested.
5. Non-5V tolerant pins: V_{IH} source > ($V_{DD} + 0.3$), 5V tolerant pins: V_{IH} source > 5.5V. Characterized, but not tested.
6. 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
7. Injection currents > 0 can affect the ADC results by approximately 4-6 counts.
8. Any number and/or combination of inputs listed under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins does not exceed the specified limit. Characterized, but not tested.

Table 6: Output Pin DC Specifications

| Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|------|---|-----|-----|-----|--|---|
| VOL | Output Low Voltage ⁽¹⁾ | | | | | |
| | 2x Sink Driver Pins ⁽²⁾ | — | — | 0.4 | V | $I_{OL} \leq 3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | 4x Sink Driver Pins ⁽²⁾ | — | — | 0.4 | V | $I_{OL} \leq 6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| VOH | Output High Voltage ⁽¹⁾ | | | | | |
| | 2x Source Driver Pins ⁽²⁾ | 2.4 | — | — | V | $I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | 4x Source Driver Pins ⁽²⁾ | 2.4 | — | — | V | $I_{OH} \geq -6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| VOH1 | Output High Voltage ⁽¹⁾ | | | | | |
| | 2x Source Driver Pins ⁽²⁾ | 1.5 | — | — | V | $I_{OH} \geq -6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | | 2.0 | — | — | V | $I_{OH} \geq -5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | | 3.0 | — | — | V | $I_{OH} \geq -2 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | 4x Source Driver Pins ⁽²⁾ | 1.5 | — | — | V | $I_{OH} \geq -12 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| | | 2.0 | — | — | V | $I_{OH} \geq -11 \text{ mA}$, $V_{DD} = 3.3\text{V}$ |
| 3.0 | | — | — | V | $I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ | |

- Note**
1. Parameters are characterized, but not tested.
 2. See section 4.1 "Pinout Summary" for the output driver current rating designations.

Table 7: I/O Pin Timing Requirements

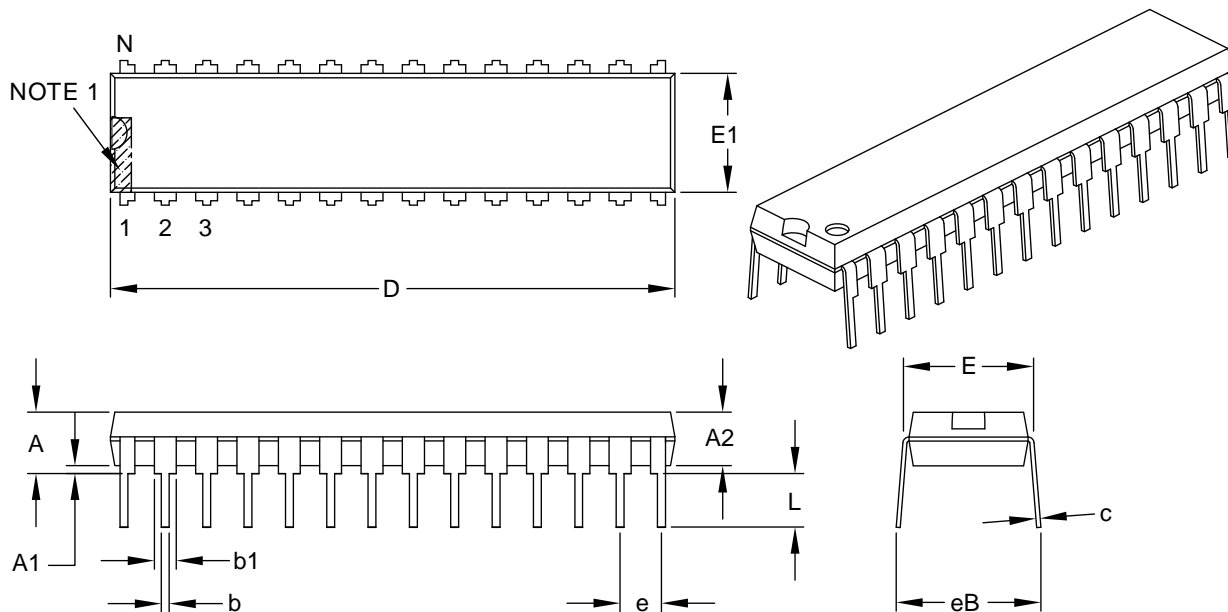
| Sym | Characteristic | Min | Typ | Max | Units | Conditions |
|------|---|-----|-----|--------|---------------|------------------------|
| TRST | RESET Pulse Width (low) | 2 | — | — | μs | |
| TUWM | Minimum UART Rx Pulse Width required for wakeup (user settable) | — | 20 | — | ns | user setting < 15 |
| | | 15 | — | 65,534 | μs | user setting ≥ 15 |
| TSTM | Minimum SLEEP Input Time to stay high before wakeup (user settable) | — | 15 | — | μs | user setting = 0 |
| | | 1 | — | 65,534 | ms | user setting > 0 |

8.0 Packaging Diagrams and Parameters

8.1 SPDIP (SP) Package

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|-------|-------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | — | — | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | — | — |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | — | — | .430 |

Notes:

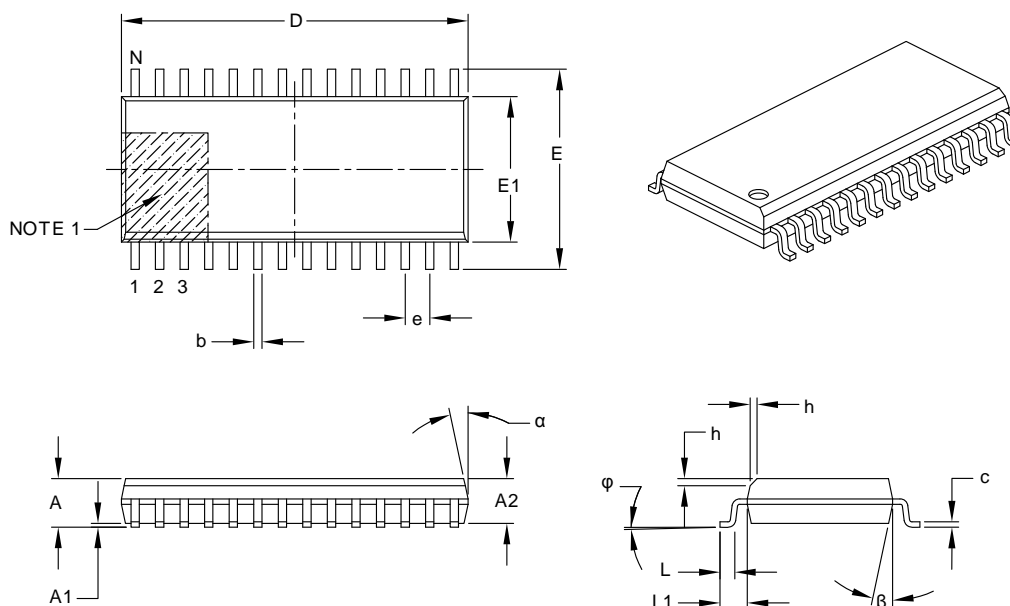
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

8.2 SOIC 300mil (SO) Package

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



| | | Units | MILLIMETERS | | |
|--------------------------|----------|-------|-------------|-----|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | | |
| Pitch | e | | 1.27 BSC | | |
| Overall Height | A | — | — | — | 2.65 |
| Molded Package Thickness | A2 | | 2.05 | — | — |
| Standoff § | A1 | | 0.10 | — | 0.30 |
| Overall Width | E | | 10.30 BSC | | |
| Molded Package Width | E1 | | 7.50 BSC | | |
| Overall Length | D | | 17.90 BSC | | |
| Chamfer (optional) | h | | 0.25 | — | 0.75 |
| Foot Length | L | | 0.40 | — | 1.27 |
| Footprint | L1 | | 1.40 REF | | |
| Foot Angle Top | ϕ | | 0° | — | 8° |
| Lead Thickness | c | | 0.18 | — | 0.33 |
| Lead Width | b | | 0.31 | — | 0.51 |
| Mold Draft Angle Top | α | | 5° | — | 15° |
| Mold Draft Angle Bottom | β | | 5° | — | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

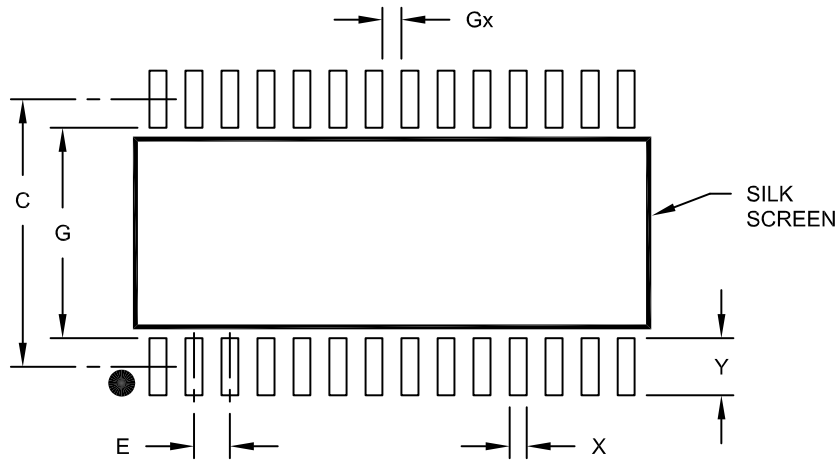
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

8.3 SOIC 300mil (SO) Land Pattern

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



RECOMMENDED LAND PATTERN

| | | Units | MILLIMETERS | | |
|--------------------------|----|----------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | | |
| Contact Pad Spacing | C | | | 9.40 | |
| Contact Pad Width (x28) | X | | | | 0.60 |
| Contact Pad Length (x28) | Y | | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | | |
| Distance Between Pads | G | 7.40 | | | |

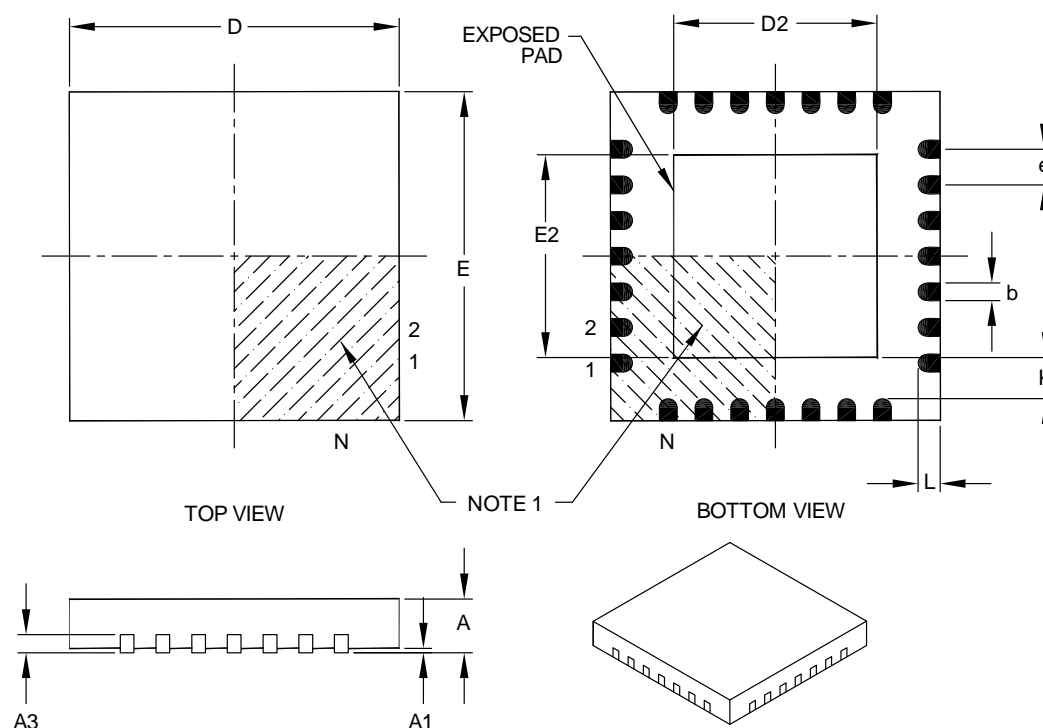
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

8.4 QFN-S (MM) Package

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



| | | Units | MILLIMETERS | | |
|------------------------|----|-------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | | |
| Pitch | e | | 0.65 BSC | | |
| Overall Height | A | | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | | |
| Overall Width | E | | 6.00 BSC | | |
| Exposed Pad Width | E2 | | 3.65 | 3.70 | 4.70 |
| Overall Length | D | | 6.00 BSC | | |
| Exposed Pad Length | D2 | | 3.65 | 3.70 | 4.70 |
| Contact Width | b | | 0.23 | 0.38 | 0.43 |
| Contact Length | L | | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | | 0.20 | — | — |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

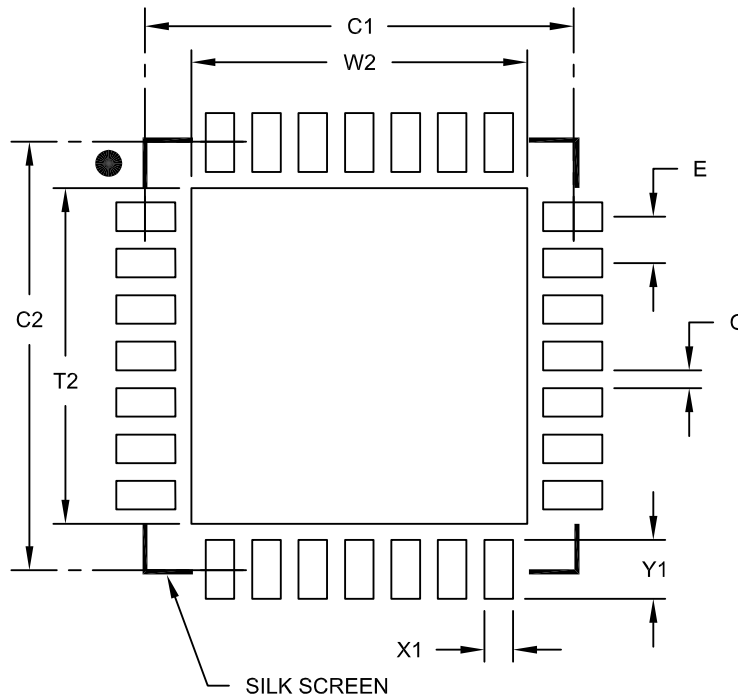
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

8.5 QFN-S (MM) Land Pattern

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 4.70 |
| Optional Center Pad Length | T2 | | | 4.70 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (x28) | X1 | | | 0.40 |
| Contact Pad Length (x28) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

9.0 Ordering Information

| TA | Package | | Part Number | SKU |
|----------------|------------|------|--------------|--------|
| -40°C to +85°C | SPDIP (SP) | Tube | STN1110-I/SP | 365101 |
| | SOIC (SO) | Tube | STN1110-I/SO | 365111 |
| | QFN-S (MM) | Tube | STN1110-I/MM | 365121 |

Appendix A: Revision History

Revision A (October 22, 2010)

Initial release of this document.

Revision B (July 13, 2012)

Revised the “Overview”, “Feature Highlights”, and “Typical Applications” sections. Added current capability ratings to the “Pinout Summary” table and relevant pin descriptions. Changed recommended connections for unused pins. Deleted last sentence of NVM Reset Input description (RST_NVM needs a pullup whether an LED is connected or not). Added “Recommended ANALOG_IN Voltage Source Impedance” (RIN) specification to “Input Pin Specifications” table. Updated schematics, and added short descriptions to the “Recommended Minimum Connection” and “Typical Configuration” sections. Minor typographical and formatting changes.

Appendix B: Contact Information

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