STL40N10F7

N-channel 100 V, 0.02 Ω typ., 10 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

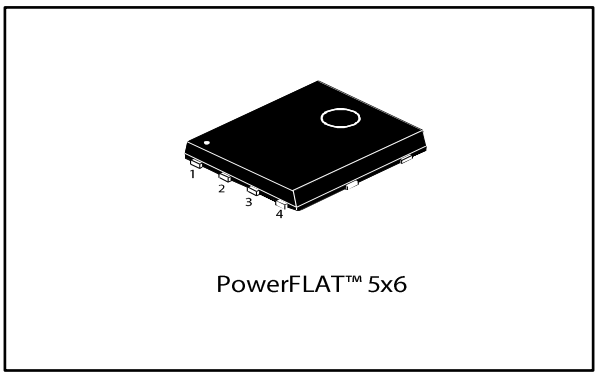
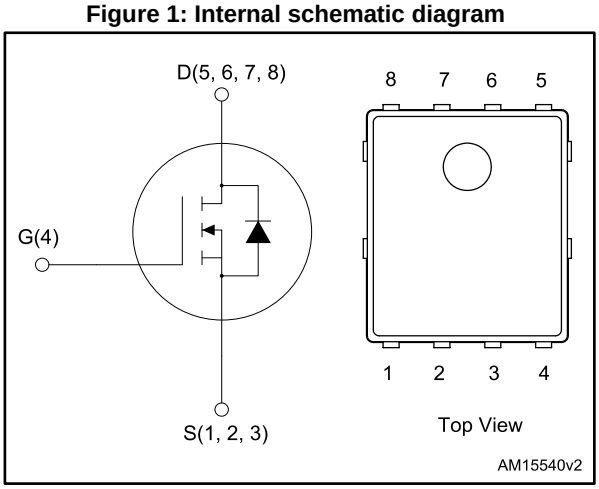


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL40N10F7	100 V	0.024Ω	10 A	5 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL40N10F7	40N10F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	40	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	28	A
I_D (2)	Drain current (continuous) at T_C = 25 °C	10	A
I_D (2)	Drain current (continuous) at T_C = 100 °C	7	A
I_{DM} (2)(3)	Drain current (pulsed)	40	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	70	W
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	5	W
T_j	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		

Notes:

(1)This value is rated according to $R_{thj\text{-}c}$

(2)This value is rated according to $R_{thj\text{-}pcb}$

(3)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	2.08	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max.	31	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V_{DS} = 100 V			10	µA
		V_{GS} = 0 , V_{DS} = 100 V, T_C = 125° C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS}= +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 10 A		0.02	0.024	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1270	-	pF
C_{oss}	Output capacitance		-	290	-	pF
C_{rss}	Reverse transfer capacitance		-	24	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 32 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	119	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 16 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	12	-	ns
t_r	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	5.6	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain curren	I_{SD} = 32 A, V_{GS} = 0 V	-		32	A
I_{SDM} (1)	Source-drain current (pulsed)				128	A
V_{SD} (2)	Forward on voltage				1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 32 A, di/dt = 100 A/µs V_{DD} = 80 V. T_J = 150° C	-	41		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.3		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

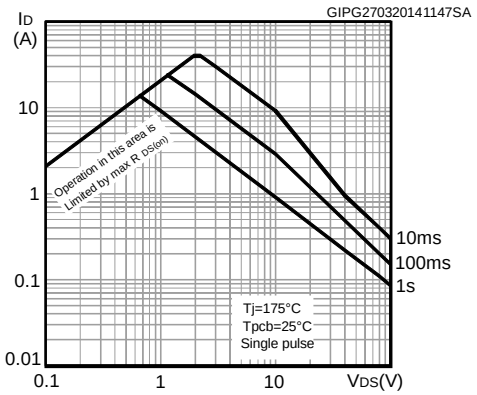


Figure 3: Thermal impedance

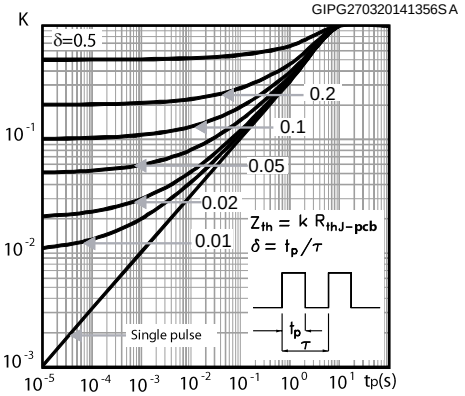


Figure 4: Output characteristics

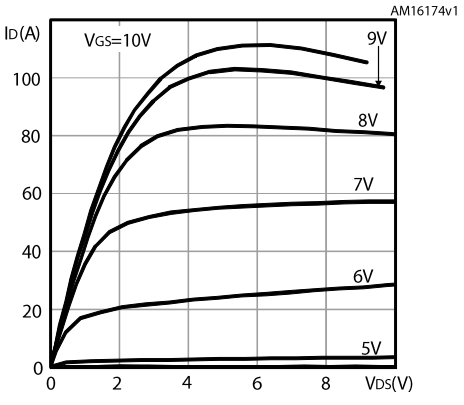


Figure 5: Transfer characteristics

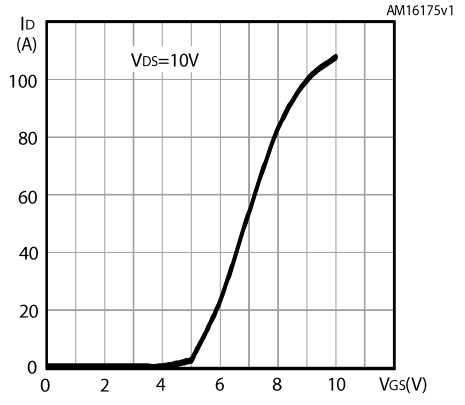


Figure 6: Gate charge vs gate-source voltage

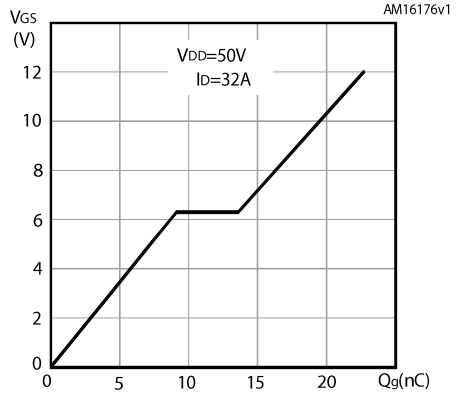


Figure 7: Static drain-source on-resistance

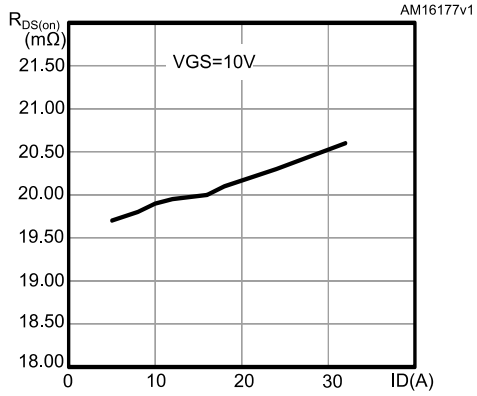


Figure 8: Capacitance variations

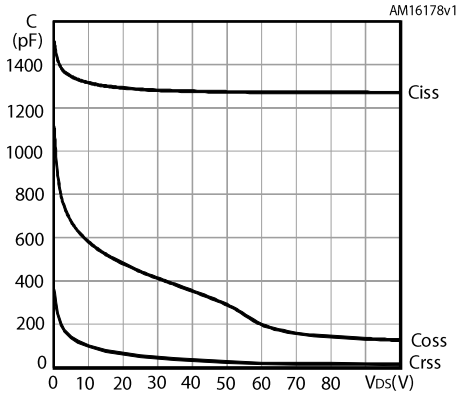


Figure 9: Normalized gate threshold voltage vs temperature

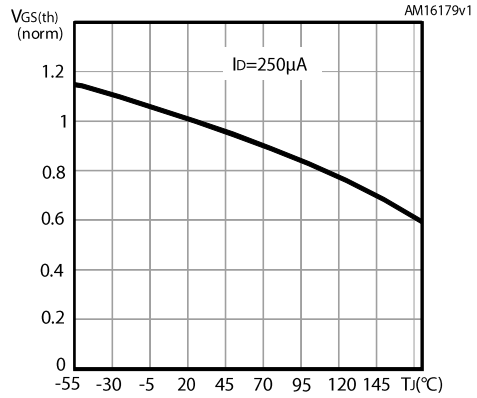


Figure 10: Normalized on-resistance vs temperature

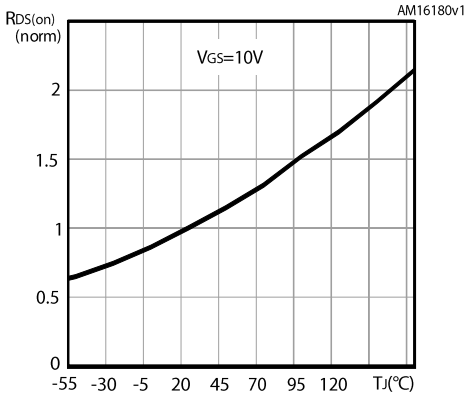


Figure 11: Normalized V(BR)DSS vs temperature

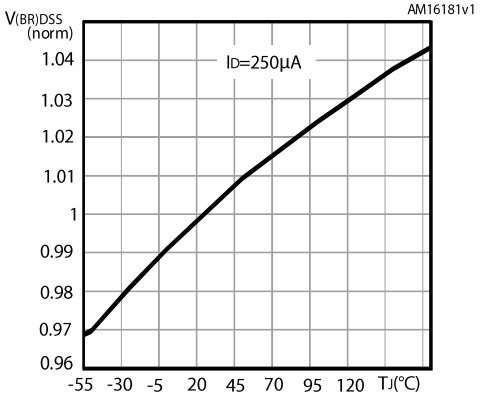
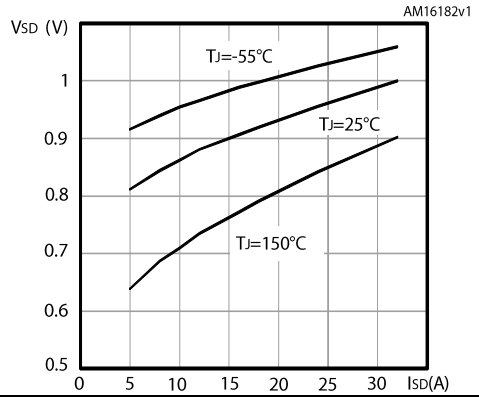


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

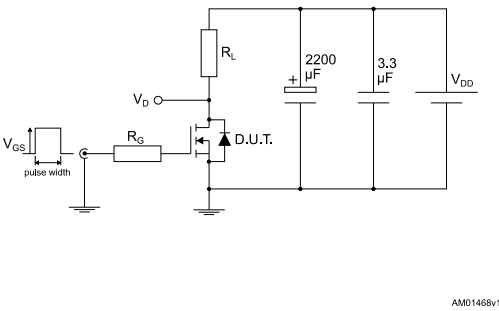


Figure 14: Test circuit for gate charge behavior

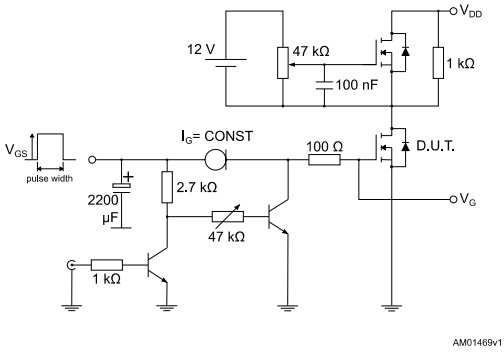


Figure 15: Test circuit for inductive load switching and diode recovery times

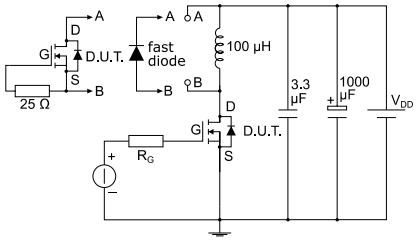


Figure 16: Unclamped inductive load test circuit

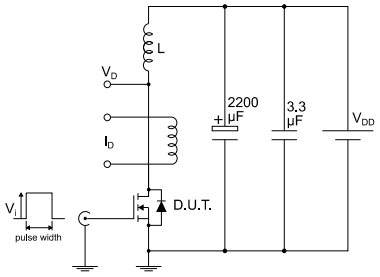


Figure 17: Unclamped inductive waveform

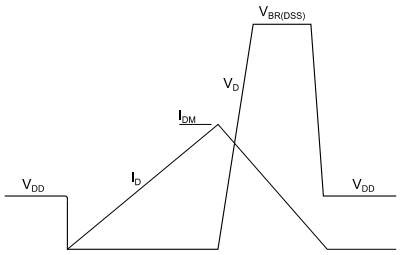
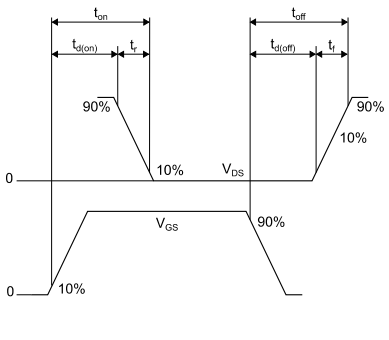


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 19: PowerFLAT™ 5x6 type R package outline

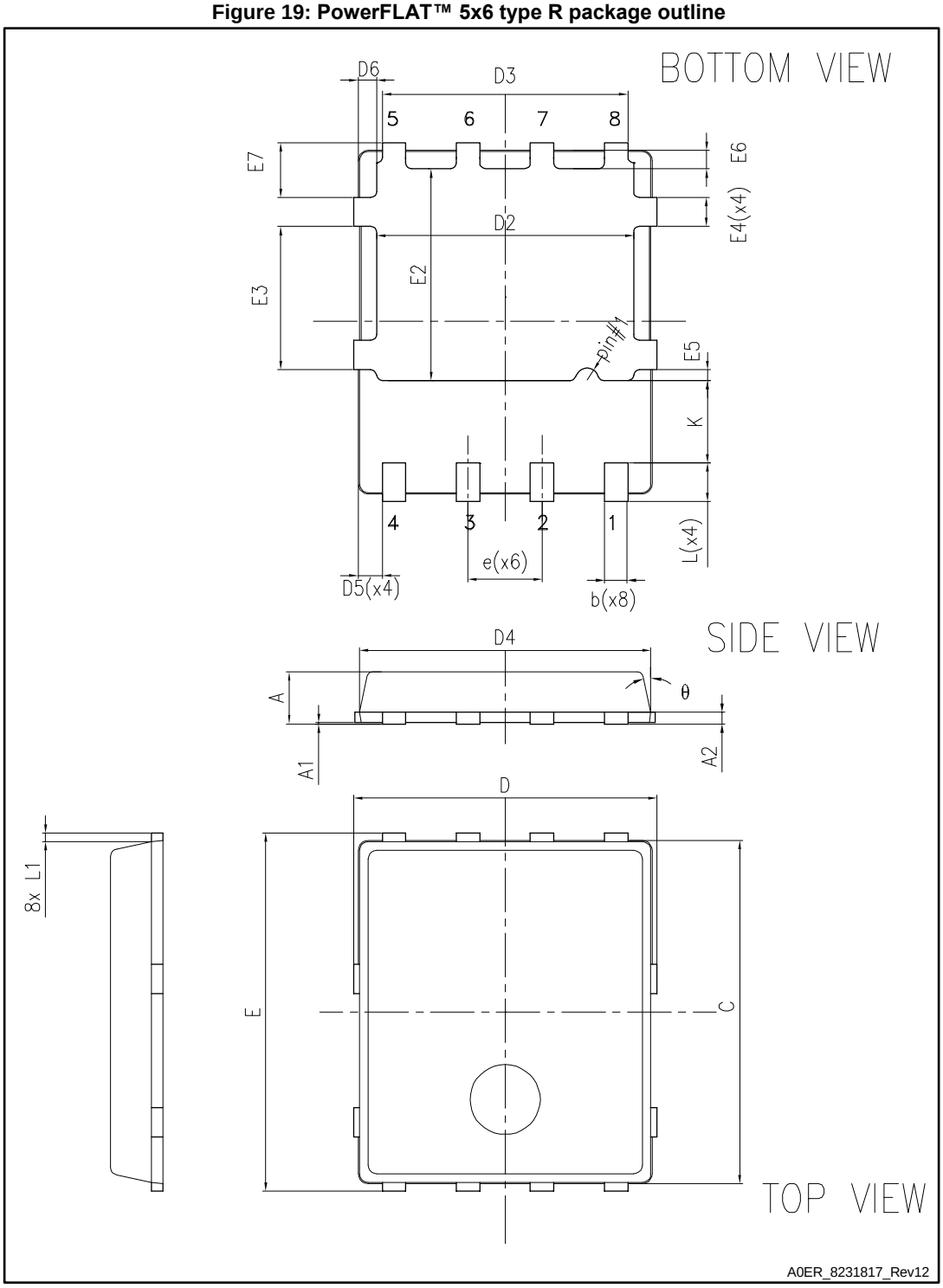
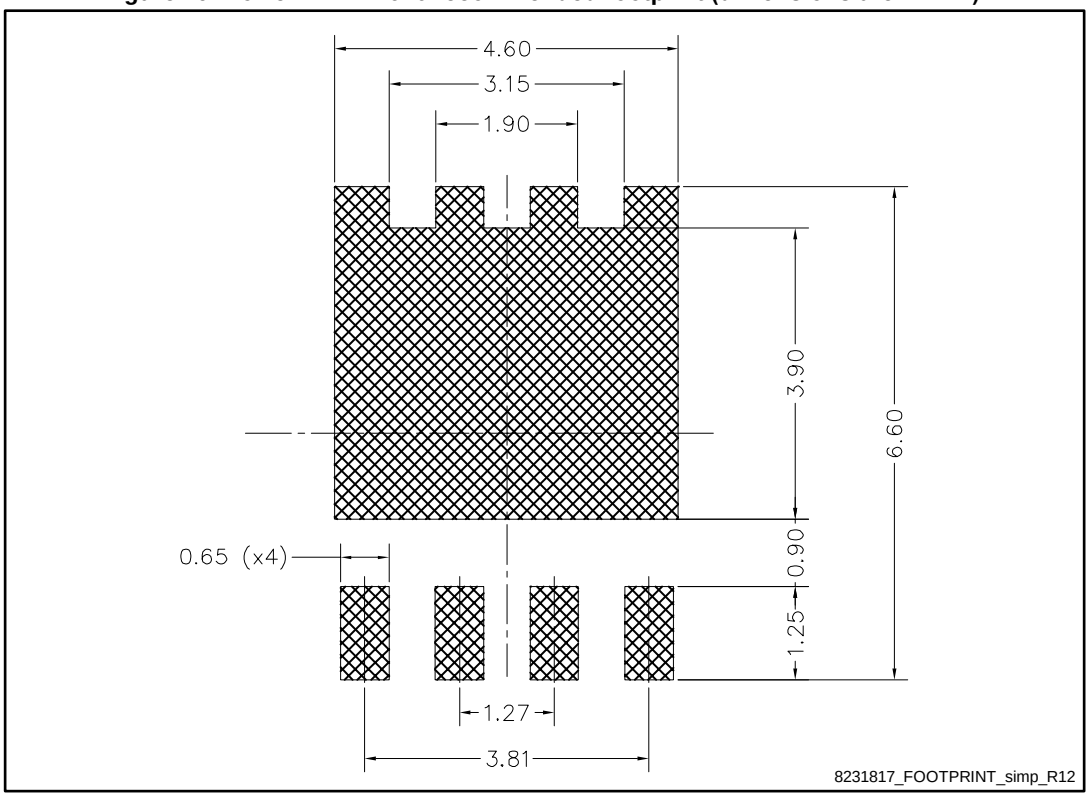


Table 8: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.75	0.90	1.25
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

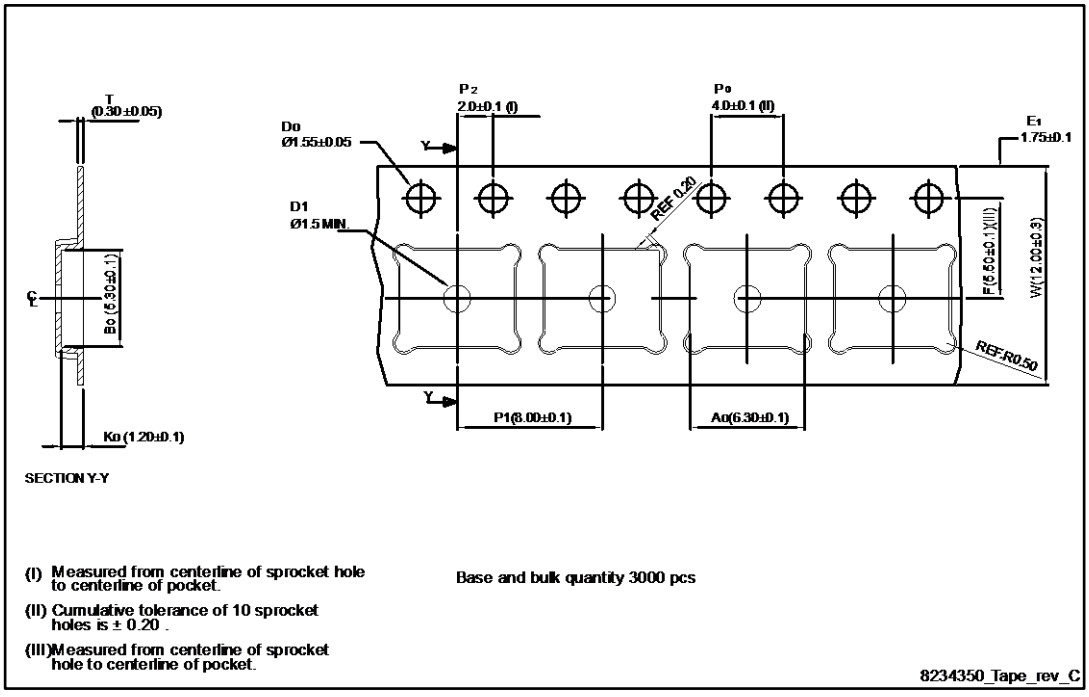


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

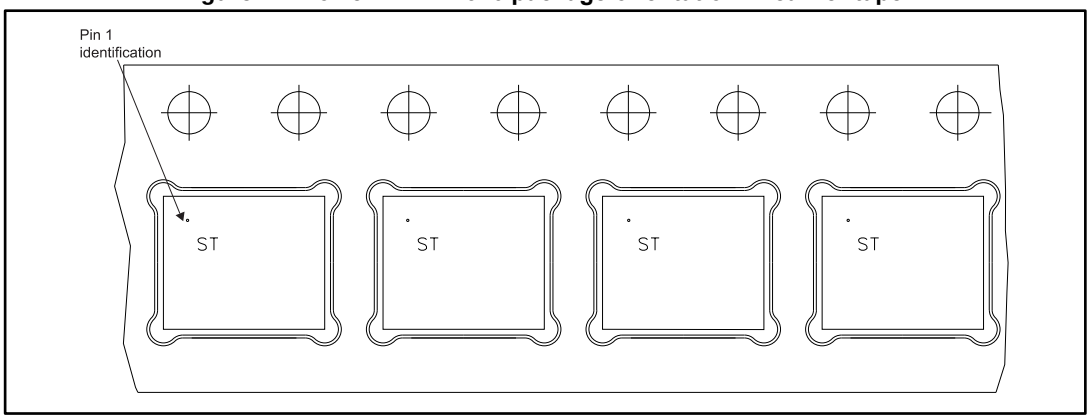
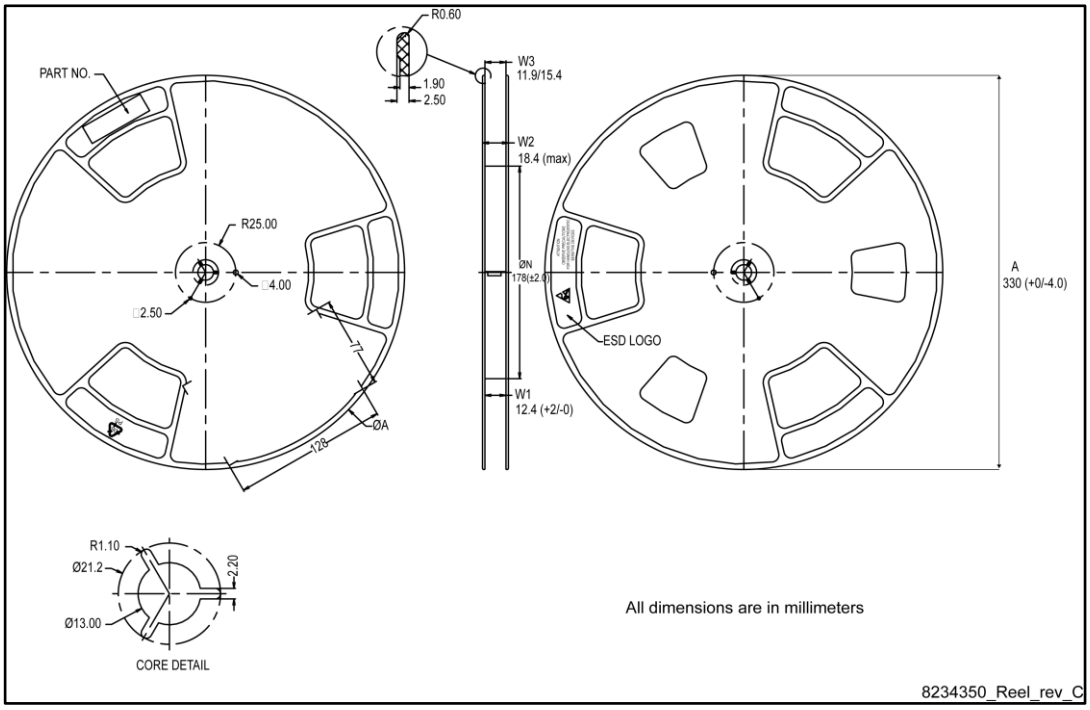


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-May-2015	1	First release.
02-Nov-2015	2	Document status promoted from preliminary to production data. Modified: $V_{GS(th)}$ values in tab 4. Updated the entire typical values in tab 5, tab 6 and tab7 Added Electrical characteristics (curves) Updated Figure 13, 14, 15 and 16 Minor text changes.
18-Dec-2015	3	Updated title, features and description. Updated *Table 2: "Absolute maximum ratings"*and *Table 4: "On/Off states".* Minor text changes.

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