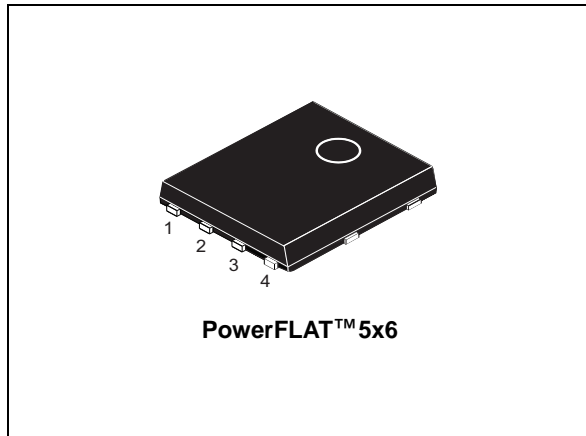


## N-channel 30 V, 0.00081 $\Omega$ typ., 50 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL220N3LLH7	30 V	0.0011 $\Omega$	50 A

- Very low on-resistance
- Very low Q<sub>g</sub>
- High avalanche ruggedness

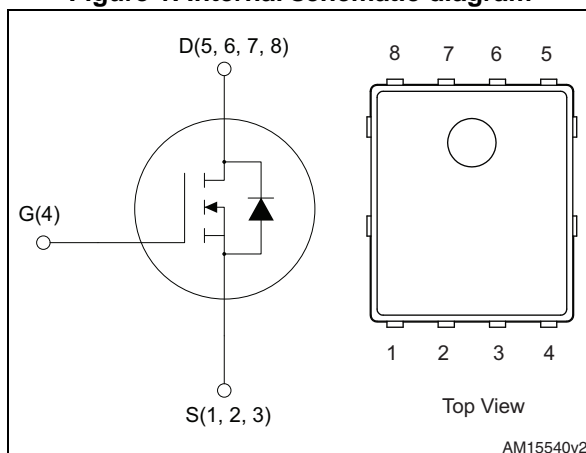
### Applications

- Switching applications

### Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL220N3LLH7	220N3LL7	PowerFLAT™ 5x6	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	220	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	160	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	880	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	50	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	32	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	200	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	113	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	W
$T_j$	Max. operating junction temperature	-55 to 150	$^\circ\text{C}$

1. This value is rated according to  $R_{thj-c}$
2. Pulse width limited by safe operating area.
3. This value is rated according to  $R_{thj-pcb}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max	1.1	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}$			1	$\mu A$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	1.2		2.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		0.00081	0.0011	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		0.00115	0.0015	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	8650	-	pF
$C_{oss}$	Output capacitance		-	2400	-	pF
$C_{rss}$	Reverse transfer capacitance		-	72	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 14</a> )	-	46	-	nC
$Q_{gs}$	Gate-source charge		-	26	-	nC
$Q_{gd}$	Gate-drain charge		-	10	-	nC
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$	-	0.61	1.8	$\Omega$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}, I_D = 25\text{ A},$ $R_G = 4.7\ \Omega, V_{GS} = 4.5\text{ V}$	-	55	-	ns
$t_r$	Rise time		-	115	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
$t_f$	Fall time		-	51	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		50	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		200	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 50 \text{ A}$ , $V_{GS} = 0$	-		1	V
$t_{rr}$	Reverse recovery time	$I_D = 50 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 24 \text{ V}$	-	66		ns
$Q_{rr}$	Reverse recovery charge		-	101		nC
$I_{RRM}$	Reverse recovery current		-	3.1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

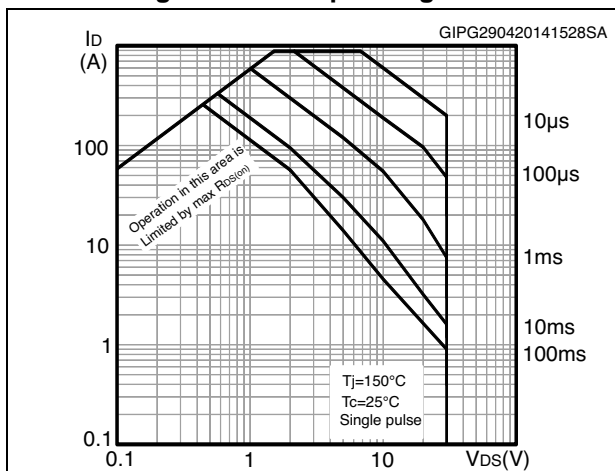


Figure 3. Thermal impedance

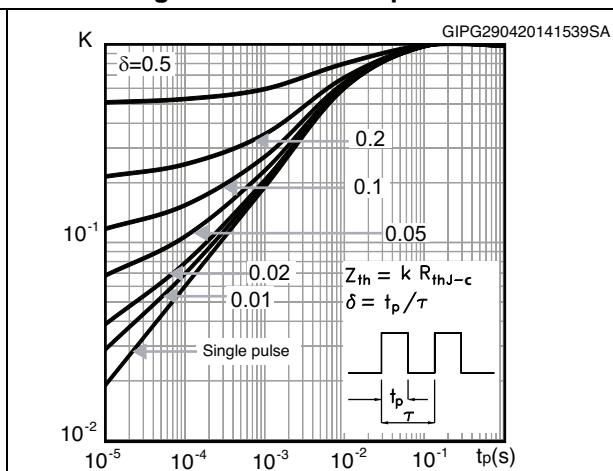


Figure 4. Output characteristics

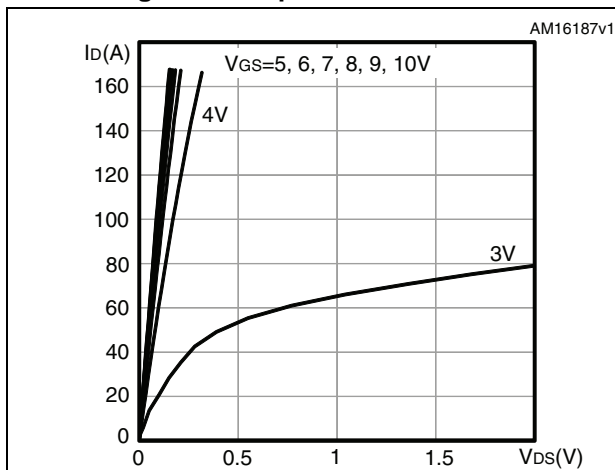


Figure 5. Transfer characteristics

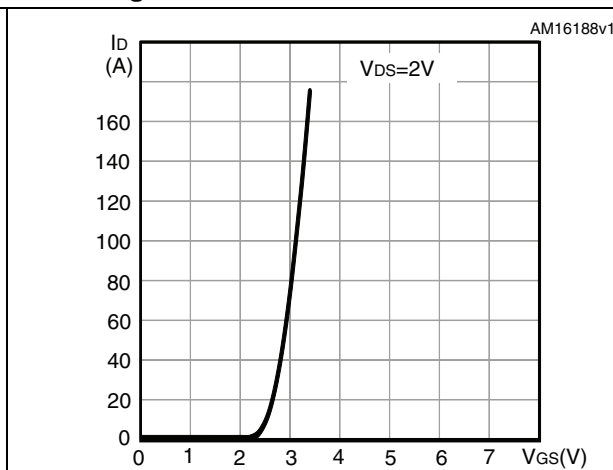


Figure 6. Gate charge vs gate-source voltage

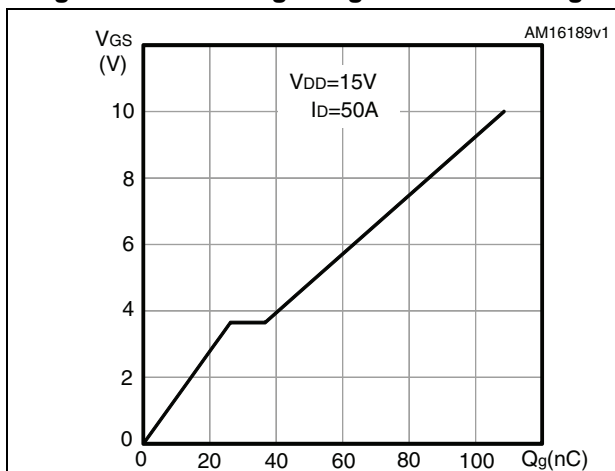


Figure 7. Static drain-source on-resistance

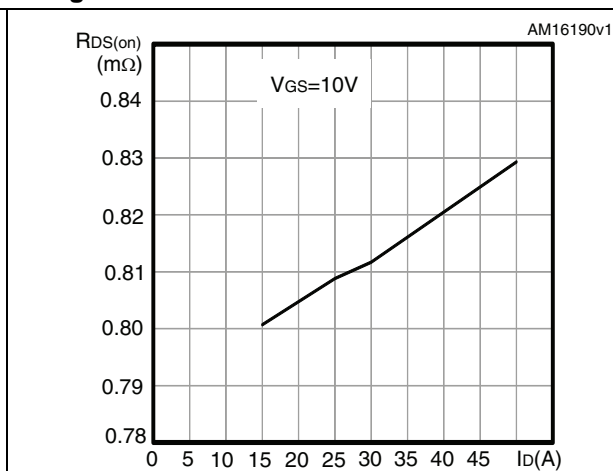


Figure 8. Capacitance variations

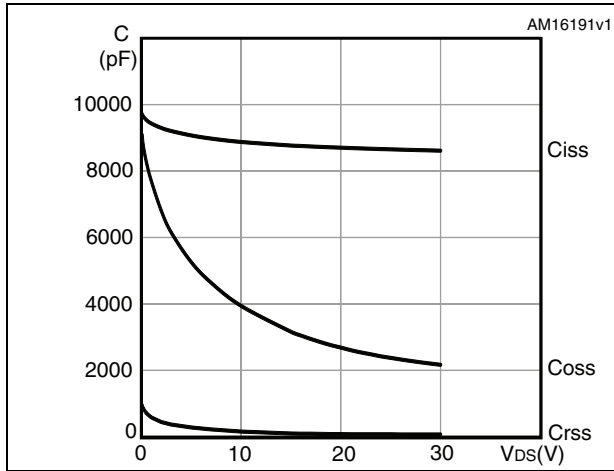


Figure 9. Normalized gate threshold voltage vs temperature

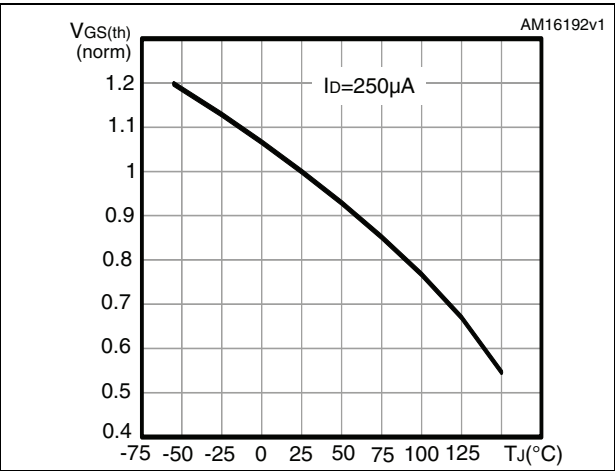


Figure 10. Normalized on-resistance vs temperature

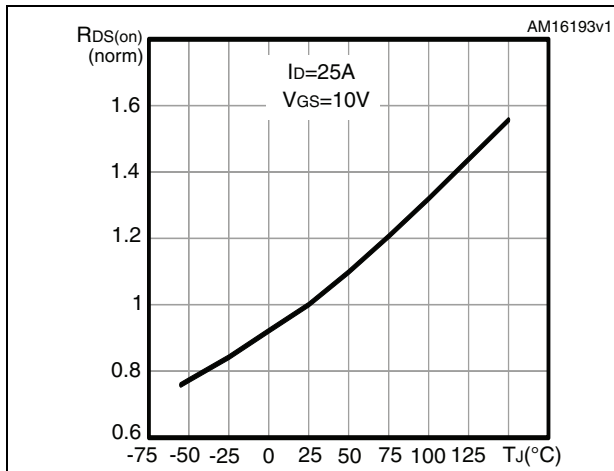


Figure 11. Normalized V(BR)DSS vs temperature

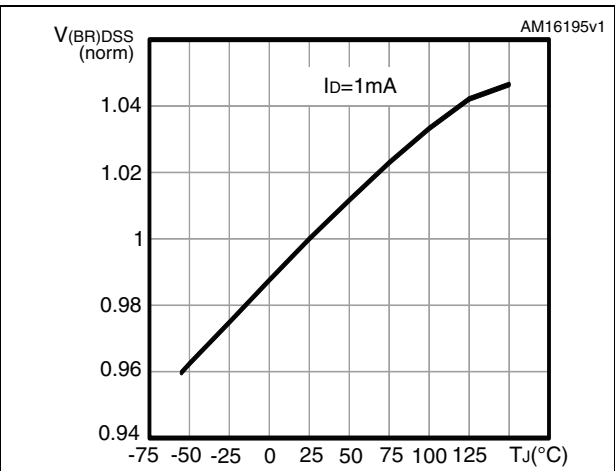
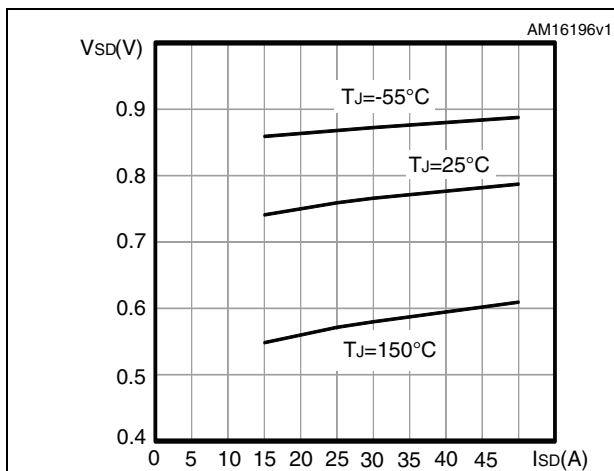


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**

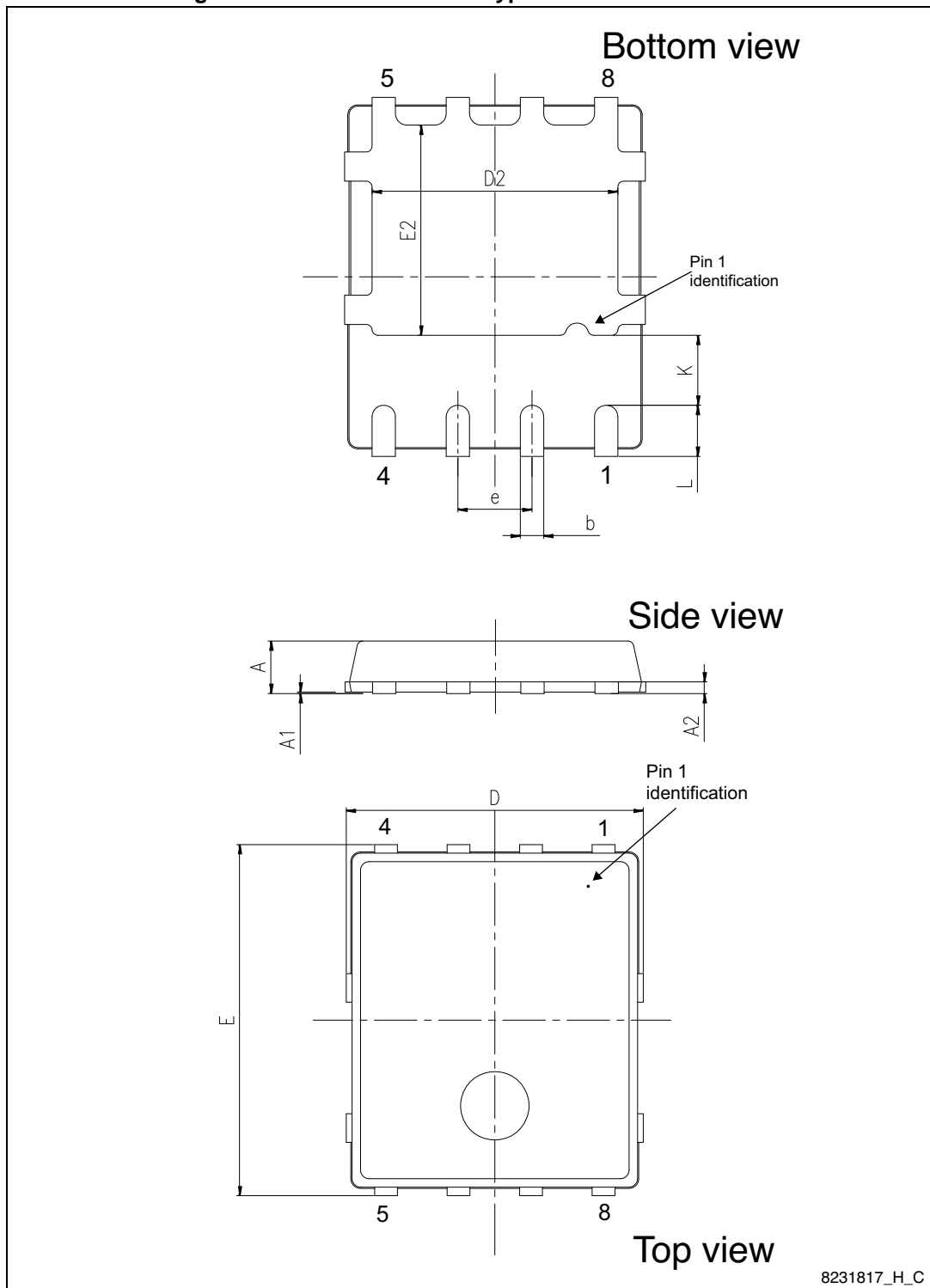




## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

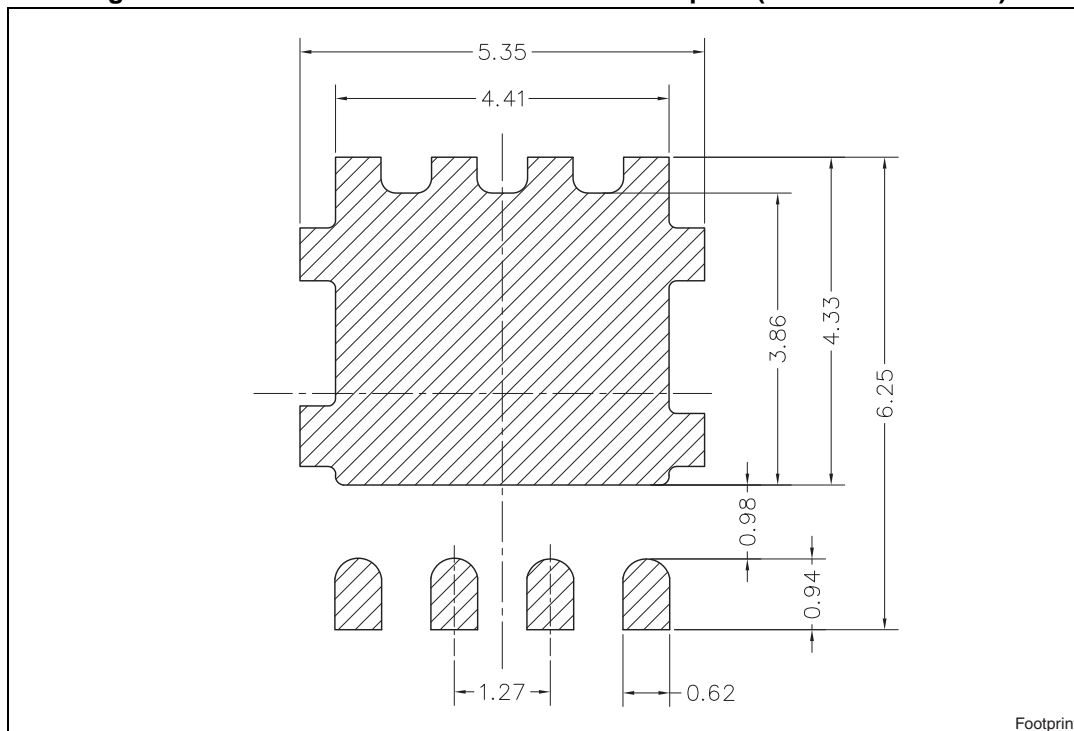


8231817\_H\_C

Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



# 5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape<sup>(a)</sup>

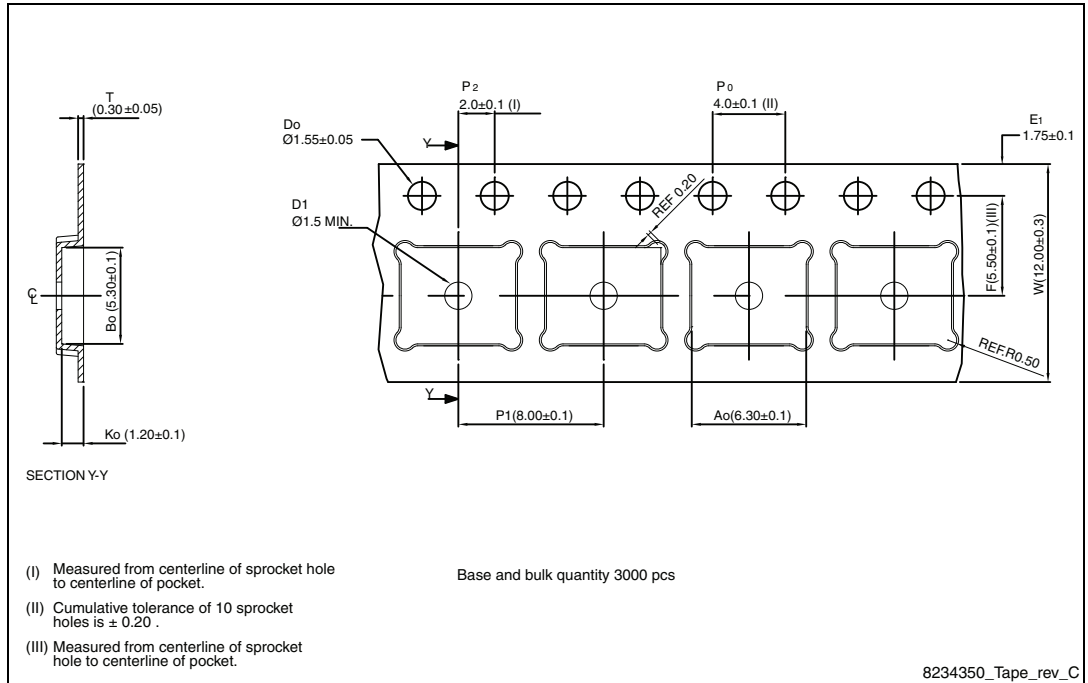
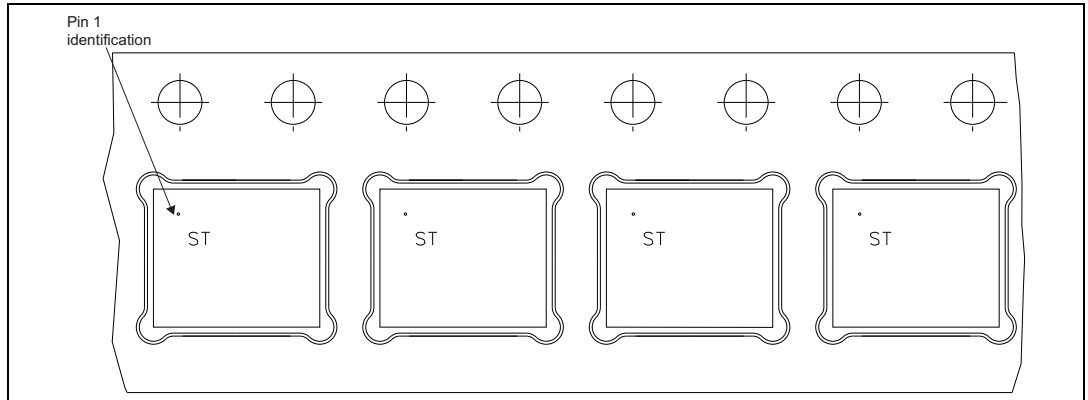
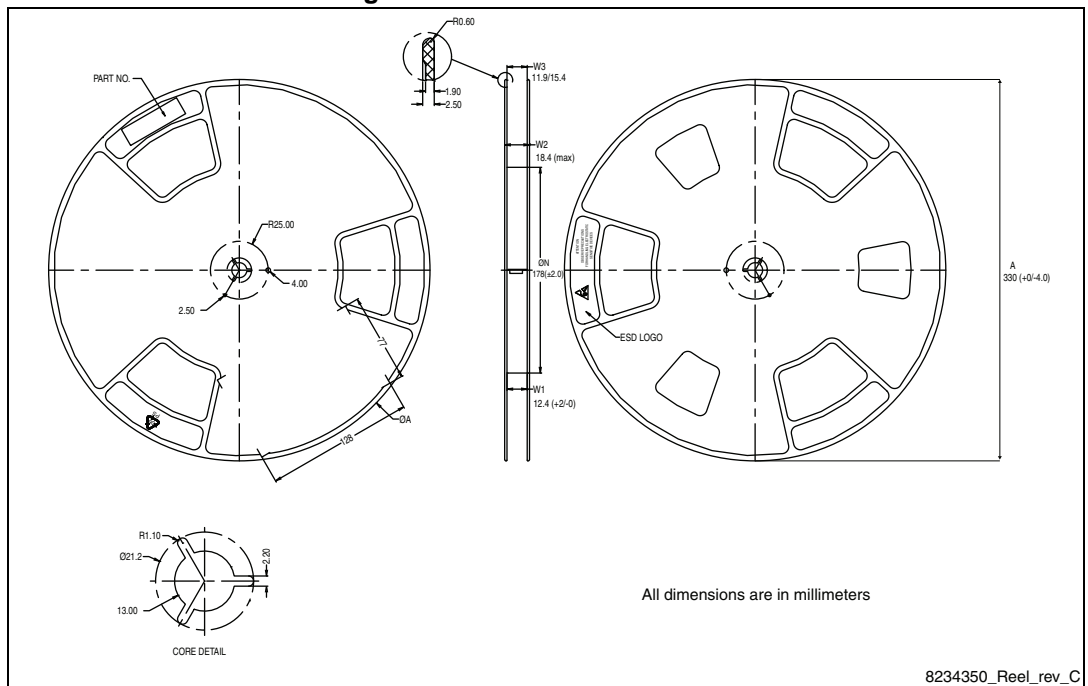


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
04-Jun-2013	1	First release.
11-Jun-2013	2	<ul style="list-style-type: none"> <li>– Changed: <i>Description</i></li> <li>– Minor text changes</li> </ul>
08-Nov-2013	3	<ul style="list-style-type: none"> <li>– Modified: title, <math>I_D</math> (Drain current (continuous) at <math>T_{pcb} = 100\text{ °C}</math>), <math>P_{TOT}</math> (Total dissipation at <math>T_C</math> and <math>T_{pcb} = 25\text{ °C}</math>) and <math>T_J</math> values in <a href="#">Table 2</a>, <math>R_{thj-case}</math> value in <a href="#">Table 3</a>, <math>V_{(BR)DSS}</math> and <math>V_{GS(th)}</math> test conditions, <math>R_{DS(on)}</math> typical values, the entire typical values in <a href="#">Table 5, 6</a>, <math>R_G</math> value in <a href="#">Table 6</a>, <math>V_{dd}</math> and typical values in <a href="#">Table 7</a></li> <li>– Updated: <a href="#">Section 4: Package mechanical data</a> and <a href="#">Section 5: Packaging mechanical data</a></li> </ul>
08-May-2014	4	<ul style="list-style-type: none"> <li>– Inserted: <math>R_g</math> parameter in <a href="#">Table 5</a></li> <li>– Minor text changes</li> </ul>

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