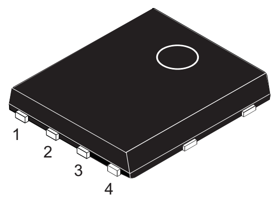
STL18N60M2

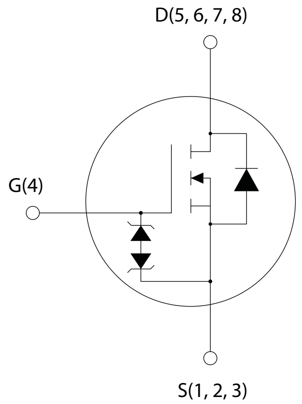
N-channel 600 V, 0.278 Ω typ., 9 A MDmesh II Plus™ low Qg Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



PowerFLAT™ 5x6 HV

Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL18N60M2	650 V	0.308 Ω	9 A

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Qg. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL18N60M2	18N60M2	PowerFLAT™ 5x6 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	9	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	5.5	A
I_{DM} (2)	Drain current (pulsed)	22	A
P_{TOT}(2)	Total dissipation at T_C = 25 °C	57	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	135	mJ
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj-case}$ and limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 9$ A, di/dt ≤ 400 A/μs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 400 V
4. $V_{DS} \leq 480$ V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.2	°C/W
$R_{thj-amb}$(1)	Thermal resistance junction-amb max	59	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C= 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.278	0.308	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 100 V, f = 1 MHz,	-	791	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	1.3	-	pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	164.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 13 A, V_{GS} = 10 V (see *Figure 15*)	-	21.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	11.3	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19*)	-	12	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-on delay time		-	47	-	ns
t_f	Fall time		-	10.6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM} (1)	Source-drain current (pulsed)		-		36	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0, I_{SD} = 13 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/μs V_{DD} = 60 V (see *Figure 16*)	-	305		ns
Q_{rr}	Reverse recovery charge		-	3.3		μC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	V_{DD} = 60 V di/dt = 100 A/μs, I_{SD} = 13 A T_j=150 °C (see *Figure 16*)	-	417		ns
Q_{rr}	Reverse recovery charge		-	4.6		μC
I_{RRM}	Reverse recovery current		-	22.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

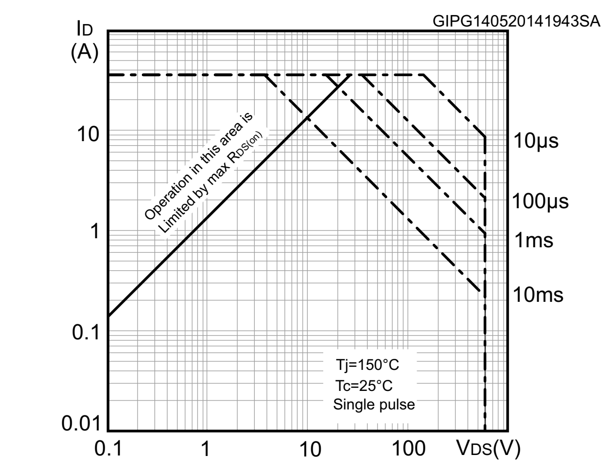


Figure 3. Thermal impedance

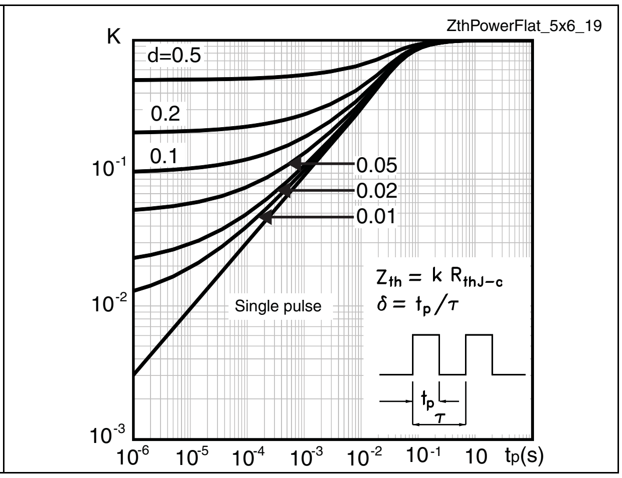


Figure 4. Output characteristics

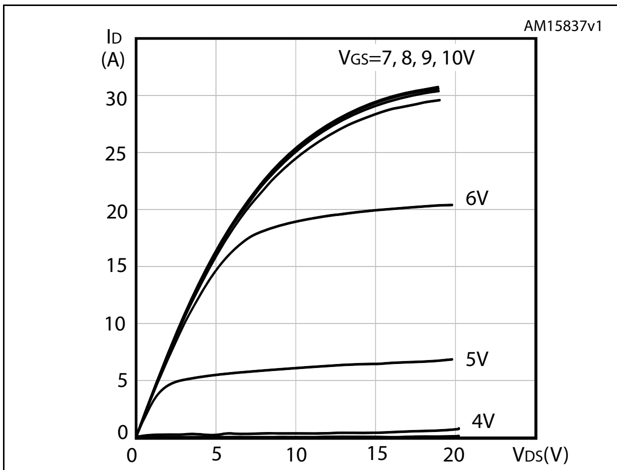


Figure 5. Transfer characteristics

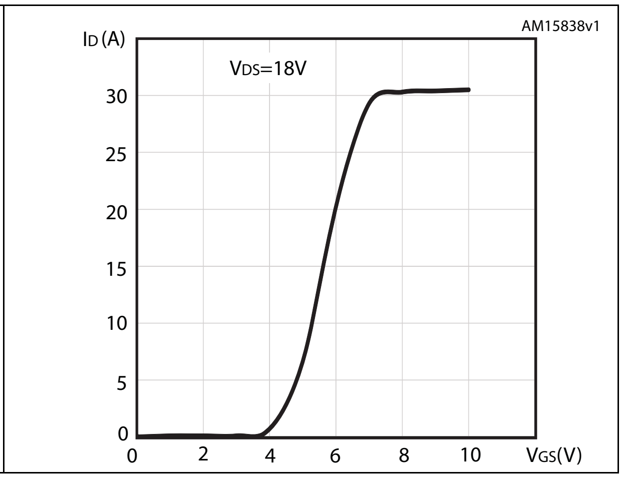


Figure 6. Gate charge vs gate-source voltage

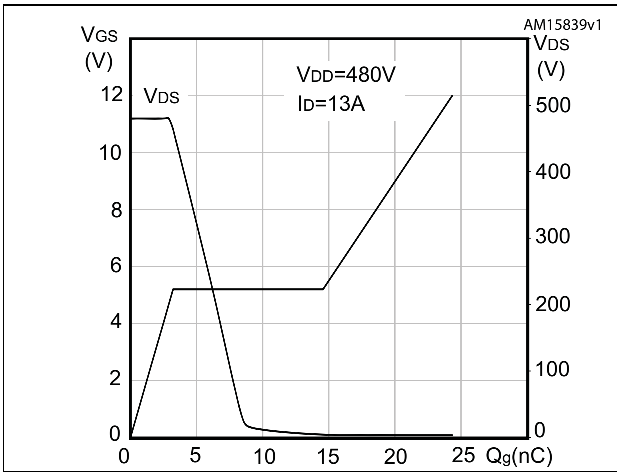


Figure 7. Static drain-source on-resistance

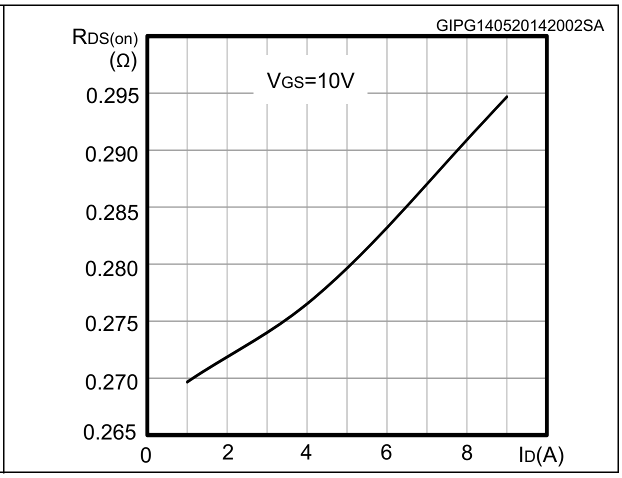


Figure 8. Capacitance variations

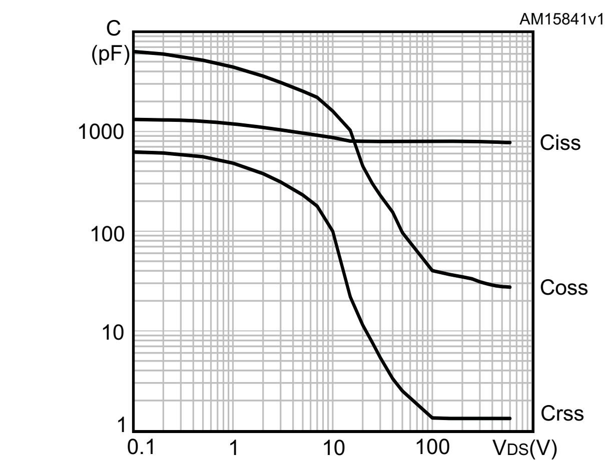


Figure 9. Output capacitance stored energy

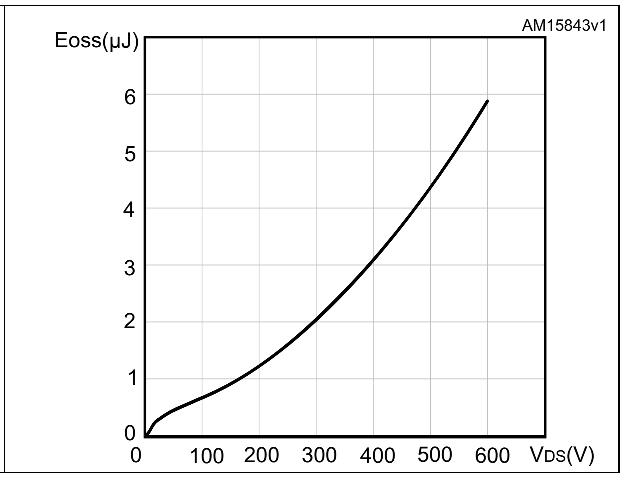


Figure 10. Normalized gate threshold voltage vs temperature

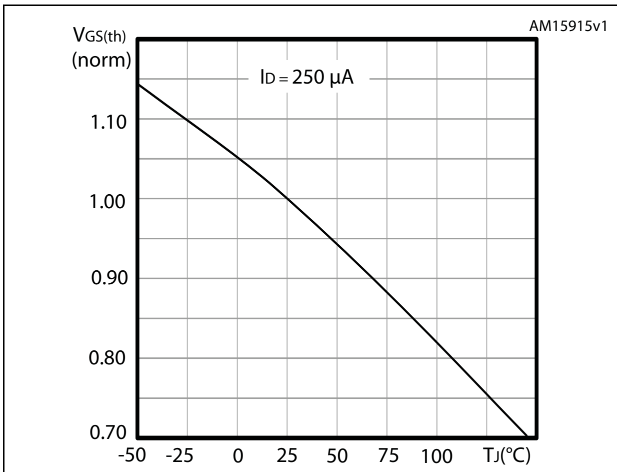


Figure 11. Normalized on-resistance vs temperature

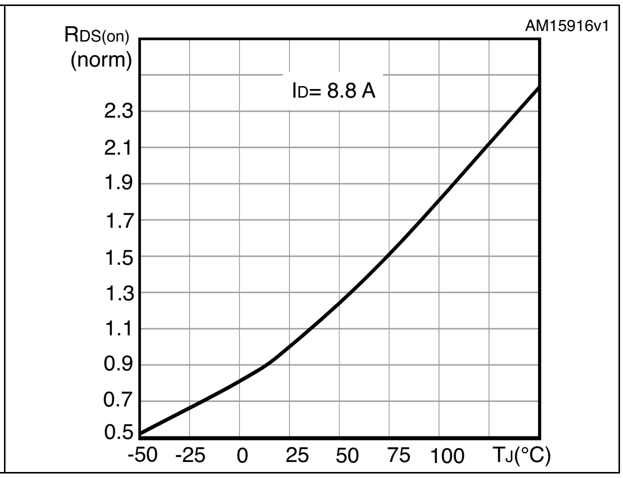


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

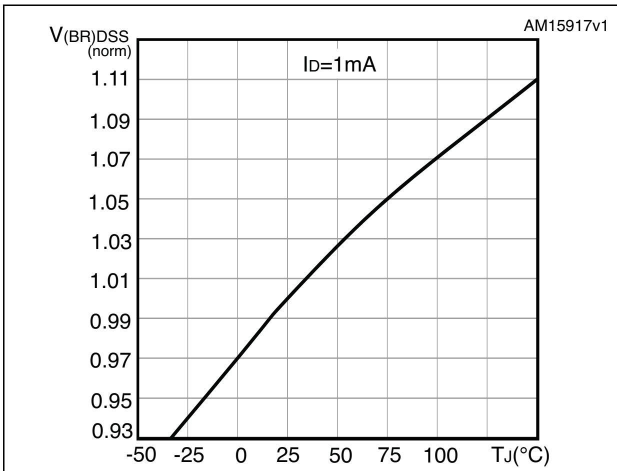
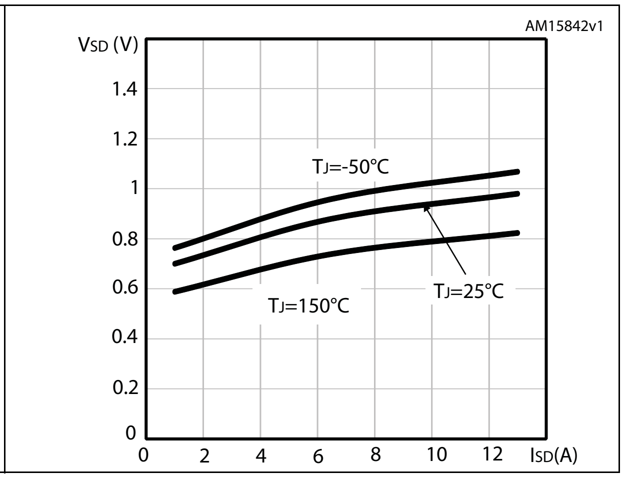


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

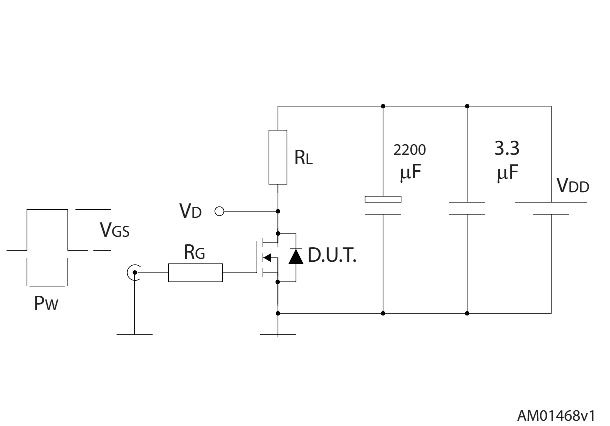


Figure 15. Gate charge test circuit

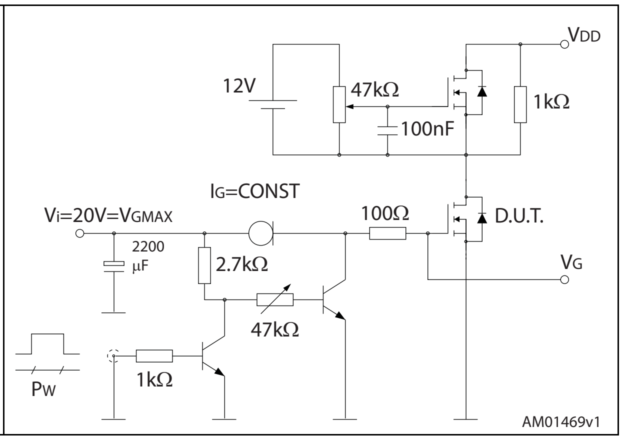


Figure 16. Test circuit for inductive load switching and diode recovery times

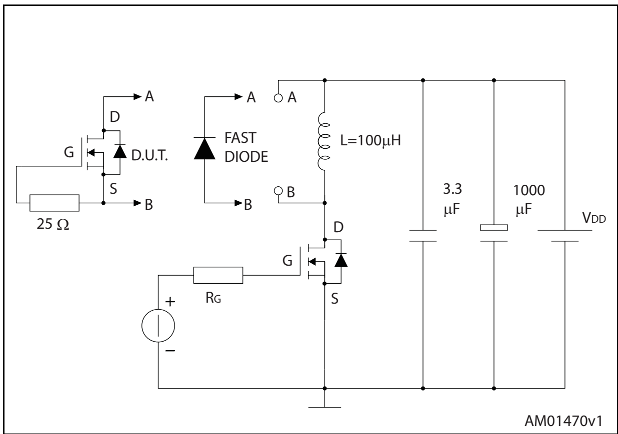


Figure 17. Unclamped inductive load test circuit

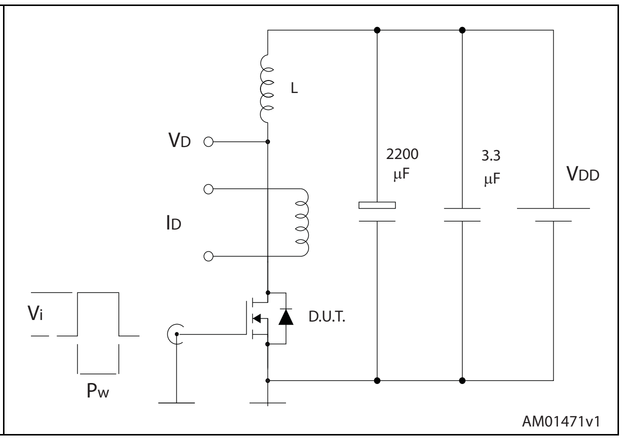


Figure 18. Unclamped inductive waveform

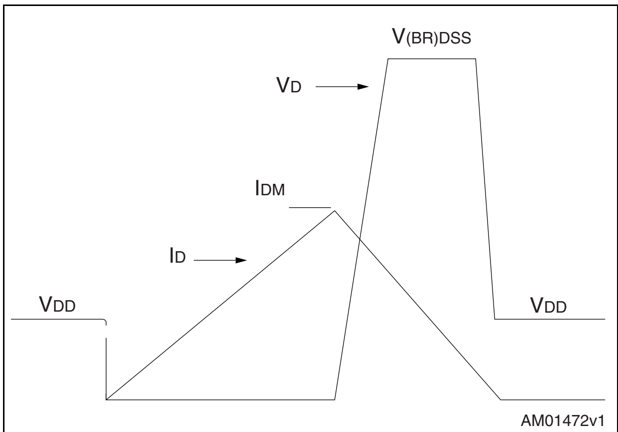
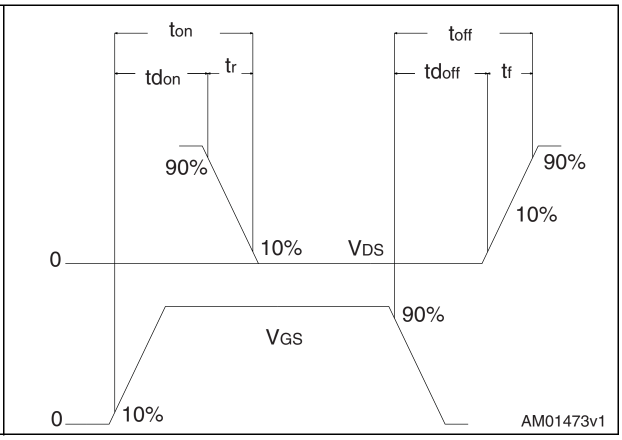


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. PowerFLAT™ 5x6 HV drawing

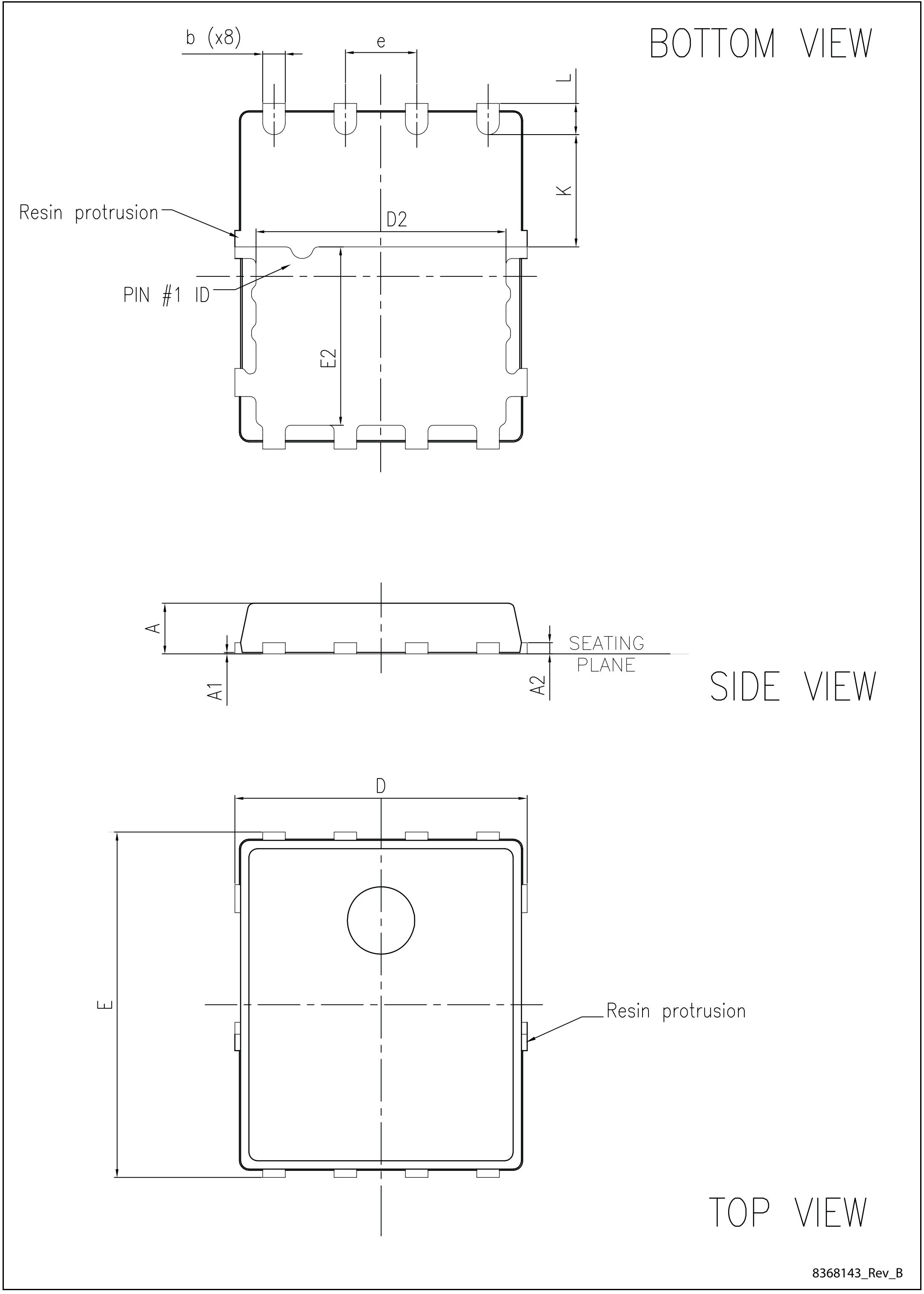


Figure 21. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)

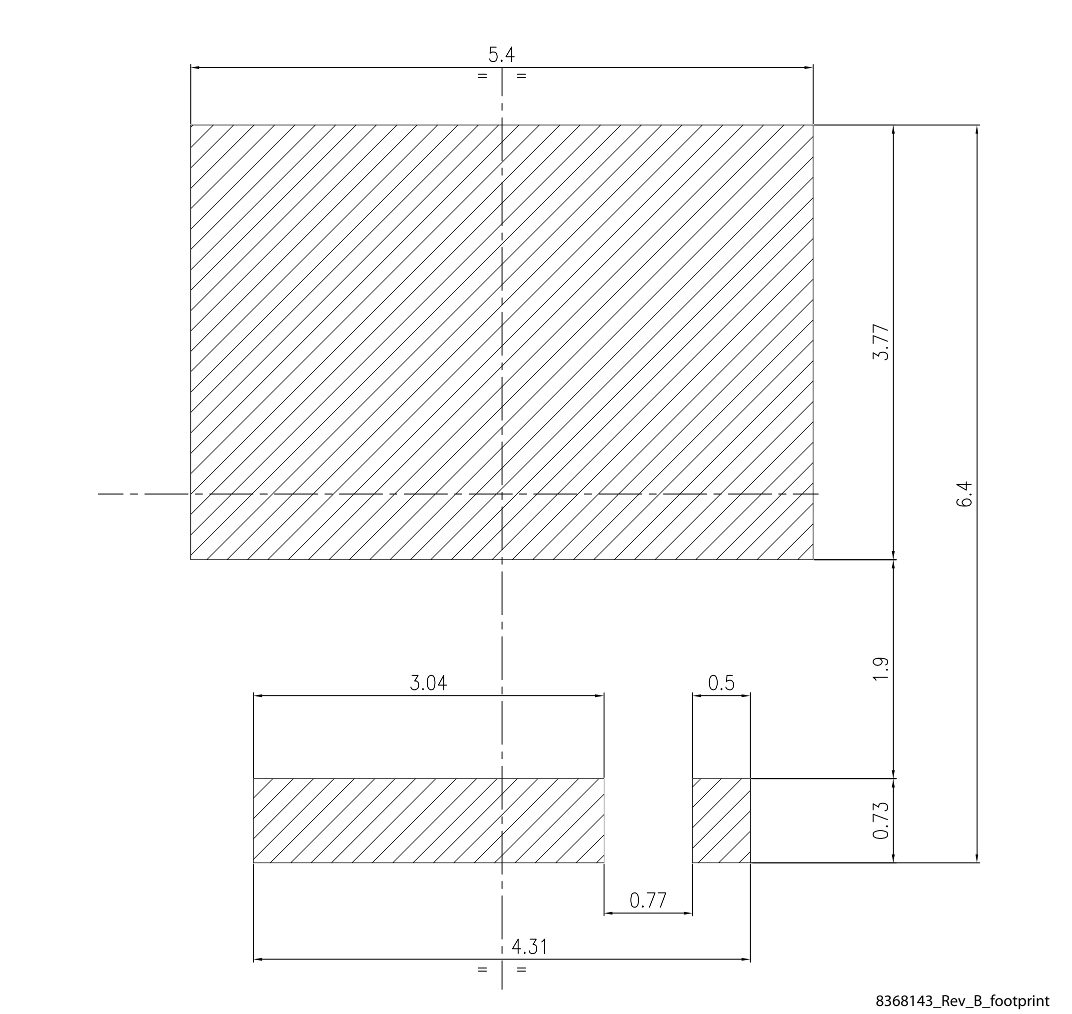


Table 8. PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

5 Packaging mechanical data

Figure 22. PowerFLAT™ 5x6 tape[(a)]

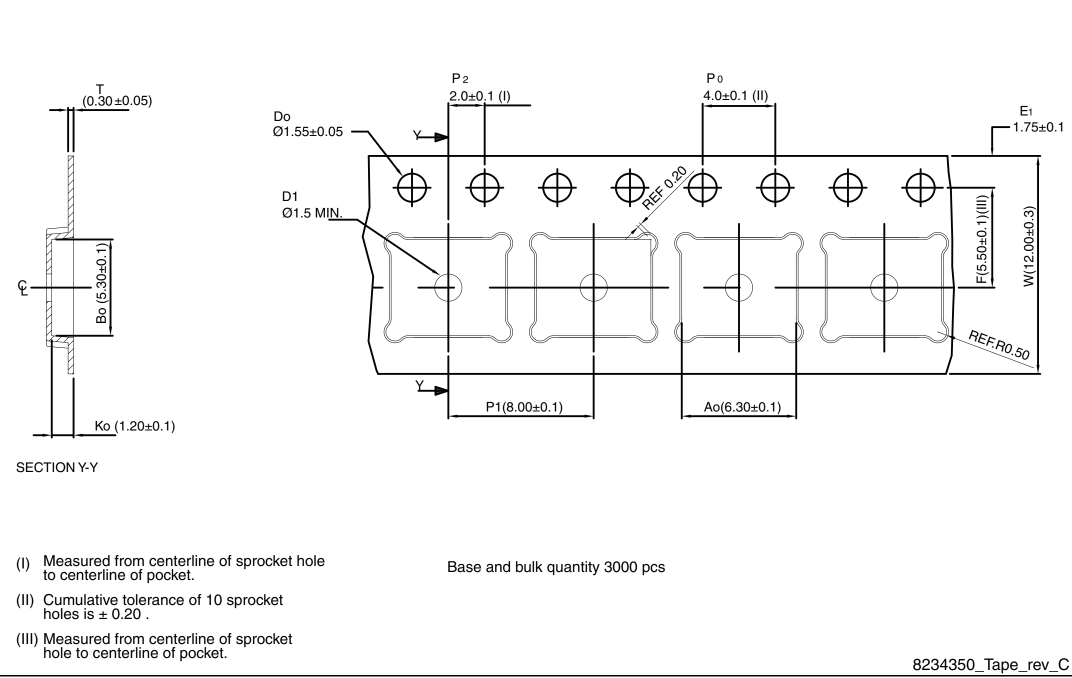
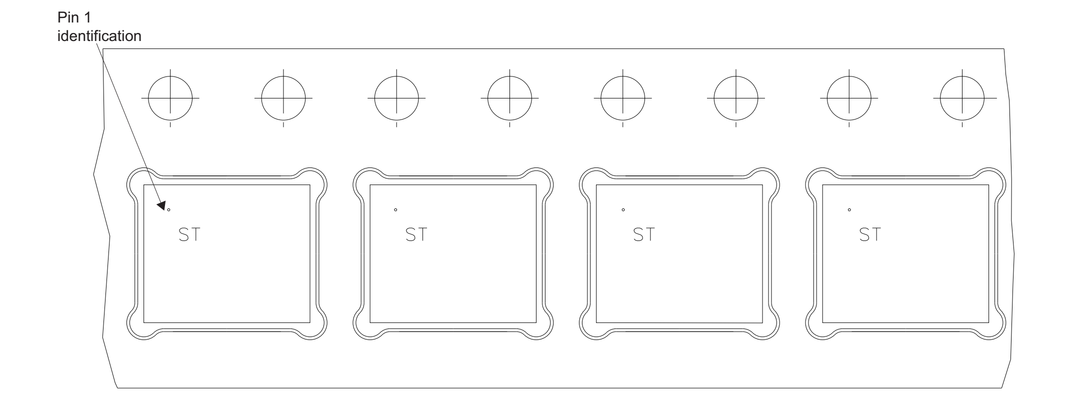
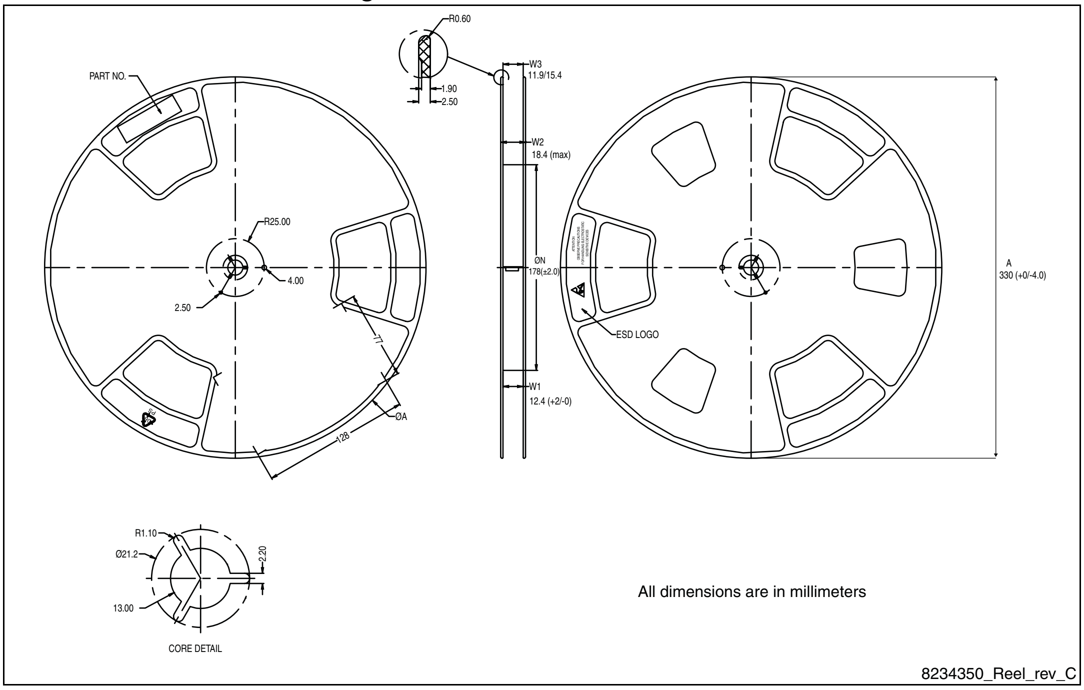


Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 24. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jun-2014	1	First release.

Please Read Carefully: